TECHNICAL NOTE

## Reversible Motor Driver ICs for Brush Motors

## Reversible Motor Drivers

for Output 2.0A or
more (1 Motor)

## BA6219BFP-Y,BA6222

## -Description

The BA6219BFP-Y and BA6222 are reversible motor driver ICs suitable for brush motors. Two logic inputs allow four output modes: forward, reverse, idling, and braking. Two revolution speeds can be set by controlling the voltage applied to the motor.

## -Features

1) Large output current (lo=2.2A max)
2) Built-in thermal shutdown circuit
3) Output voltage-setting pins
4) Small standby current.
-Applications
VCRs
-Absolute Maximum Ratings ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Limits |  | Unit |
| :--- | :---: | :---: | :---: | :---: |
|  |  | BA6219BFP-Y | BA6222 |  |
| Supply voltage | VCC1, VCC2 | 24 | 24 | V |
| Power dissipation | Pd | $1450^{*}$ | $2000^{* *}$ | mW |
| Operating temperature | Topr | $-25 \sim+75$ | $-25 \sim+75$ | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg | $-55 \sim+150$ | $-55 \sim+125$ | ${ }^{\circ} \mathrm{C}$ |
| Output current | Iomax | $2200^{* * *}$ | $2200^{* * *}$ | mA |
| Junction temperature | Tjmax | 150 |  | ${ }^{\circ} \mathrm{C}$ |

* Derated at $11.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$
(when mounted on a $90 \mathrm{~mm} \times 50 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy substrate)
** Derated at $20.0 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$
*** Do not allow current to exceed Pd and SOA.
$500 \mu \mathrm{~s}$ pulse with a duty cycle of $1 \%$

Recommended Operating Conditions ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )
BA6219BFP-Y, BA6222

| Parameter | Symbol | Range | Unit |
| :---: | :---: | :---: | :---: |
| Supply voltage | VCC1, VCC2 | $8 \sim 18$ | V |

- Electrical Characteristics

BA6219BFP-Y (Unless otherwise specified, $\quad \mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VCC} 1=12 \mathrm{~V}, \mathrm{VCC} 2=12 \mathrm{~V}$ )

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| Supply current 1 | ICC1 | - | 1.2 | 2.5 | mA | Standby mode |
| Supply current 2 | ICC2 | - | 16 | 35 | mA | FWD/REV mode |
| Supply current 3 | ICC3 | - | 25 | 60 | mA | Brake mode |
| Input threshold voltage " ${ }^{\text {" }}$ | VIH | 3.0 | - | VCC | V |  |
| Input threshold voltage "L" | VIL | 0 | - | 1.0 | V |  |
| VR bias current | IVREF | 0.6 | 1.2 | 2.4 | mA | $\mathrm{RL}=60 \Omega$, VR=6.8V |
| CD1 current | ICD1 | 0.7 | 1.5 | 3.0 | mA | $(\mathrm{IN} 1, \mathrm{IN} 2)=(\mathrm{H}, \mathrm{L}) \mathrm{CD} 1 \rightarrow$ GND |
| CD2 current | ICD2 | 0.7 | 1.5 | 3.0 | mA | $(\mathrm{IN} 1, \mathrm{IN} 2)=(\mathrm{H}, \mathrm{L}) \mathrm{CD} 2 \rightarrow \mathrm{GND}$ |
| Output leak current | IOL | - | - | 1 | mA | (IN1, IN2)=(L, L) VCC2 current |
| FOUT output voltage H | VHF | 6.5 | - | - | V | $\mathrm{RL}=60 \Omega$, VR=6.8V |
| FOUT output voltage L | VLF | - | - | 1.2 | V | $\mathrm{RL}=60 \Omega$, VR=6.8V |
| ROUT output voltage H | VHR | 6.5 | - | - | V | $\mathrm{RL}=60 \Omega$, VR=6.8V |
| ROUT output voltage L | VLR |  | - | 1.2 | V | $\mathrm{RL}=60 \Omega, \mathrm{VR}=6.8 \mathrm{~V}$ |

BA6222 (Unless otherwise specified, $\quad \mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VCC} 1=12 \mathrm{~V}, \mathrm{VCC} 2=12 \mathrm{~V}$ )

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| Supply current 1 | ICC1 | - | 1.2 | 2.5 | mA | Standby mode |
| Supply current 2 | ICC2 | - | 16 | 35 | mA | FWD/REV mode |
| Supply current 3 | ICC3 | - | 25 | 60 | mA | Brake mode |
| Input threshold voltage "H" | VIH | 3.0 | - | VCC | V |  |
| Input threshold voltage "L" | VIL | 0 | - | 1.0 | V |  |
| VR bias current | IVREF | - | 1.2 | 5.0 | mA | $\mathrm{VR}=1.0 \mathrm{~V}$ |
| VR-output gain | GV | 10.35 | 11.35 | 12.35 | dB | VR,OUT1,OUT2 (Note) IN1 or IN2="H" lo=100mA |
| CD1 current | ICD1 | 0.7 | 1.5 | 3.0 | mA | $(\mathrm{IN} 1, \mathrm{IN} 2)=(\mathrm{H}, \mathrm{L}) \mathrm{CD} 11 \rightarrow \mathrm{GND}$ |
| CD2 current | ICD2 | 0.7 | 1.5 | 3.0 | mA | $(\mathrm{IN} 1, \mathrm{IN} 2)=(\mathrm{H}, \mathrm{L}) \mathrm{CD} 2 \rightarrow \mathrm{GND}$ |
| Output leak current | IOL | - | - | 1 | mA | (IN1, IN2)=(L, L) VCC2 current |
| FOUT output voltage H | VHF | 9.5 | - | - | V | $\mathrm{l}_{\text {Out }}=0.1 \mathrm{~A}$ VREF $=5 \mathrm{~V}$ |
| FOUT output voltage L | VLF | - | - | 0.5 | V | $\mathrm{l}_{\text {lout }}=0.1 \mathrm{~A}$ VREF $=5 \mathrm{~V}$ |
| ROUT output voltage H | VHR | 9.5 | - | - | V | $\mathrm{I}_{\text {OUT }}=0.1 \mathrm{~A}$ VREF $=5 \mathrm{~V}$ |
| ROUT output voltage L | VLR |  | - | 0.5 | V | $\mathrm{l}_{\text {Out }}=0.1 \mathrm{~A}$ VREF $=5 \mathrm{~V}$ |

Note: Vout1 denotes the difference between output High voltage and output Low voltage when VR=1V, while Vout2 denotes the difference when $\mathrm{VR}=2 \mathrm{~V}$. Both values are defined when the output is stabilized without the use of a heat-radiating board.

OInput / Output Table
BA6219BFP-Y, BA6222

| Input |  | Output |  | Mode |
| :---: | :---: | :---: | :---: | :---: |
| IN1 | IN2 | OUT1 | OUT2 |  |
| L | L | OPEN | OPEN | Idle |
| H | L | H | L | Forward |
| L | H | L | H | Reverse |
| H | H | L | L | Brake |



Fig. 1 Supply Current 1(IDLE) (BA6219BFP-Y)


Fig. 4 Supply Current 1(IDLE)
(BA6222)


Fig. 7 Output Saturation Voltage H (BA6219BFP-Y)


Fig. 10 Output Saturation Voltage L (BA6222)


Fig. 2 Supply Current 2(REV) (BA6219BFP-Y)


Fig. 5 Supply Current 2(REV)
(BA6222)


Fig. 8 Output Saturation Voltage H (BA6222)


Fig. 3 Supply Current 3(BRK) (BA6219BFP-Y)


Fig. 6 Supply Current 3(BRK)
(BA6222)


Fig. 9 Output Saturation Voltage L (BA6219BFP-Y)


Note: Pins $1,3,5,9,12,14,16,17,18,21,22,23$, and 25 are N.C

## -Application Notes

[1] Capacitor preventing both output transistors from being turned on at the same time: The transistors are prevented from simultaneously turning on by delaying the potential build-up at the Base during the High output mode. Use capacitances between 0.01 to $1 \mu \mathrm{~F}$ and make sure throughcurrent caused when the transistors are on at the same time does not flow when output mode is switched.
[2] Capacitor for preventing parasitic oscillation: Noise or oscillation is generated at the output terminals due to various factors. Use a capacitance between 0.01 to 0.1 uF .
[3] Current-limiting resistor:
Current limiting resistors are used to reduce Collector loss and for protection should the output be short-circuited. Use resistances between $5-10 \Omega$ depending on the power supply voltage and taking into account the voltage drop caused by inrush current that flows when the motor is started.
[4] Zener diode for setting output voltage:
Used when the output High voltage VR (VREF) is set. It is possible to set to Zener voltage $\fallingdotseq$ output H voltage

BA6222

## Operations

1) Input Terminals (IN1, IN2) and I/O Mode

When IN1 is " H " and $\operatorname{IN} 2$ is " L ," normal mode is achieved and current flows from OUT1 to OUT2. When IN1 is " L " and $\operatorname{IN} 2$ is "H," reverse mode is set and current flows from OUT2 to OUT1. When both $\operatorname{IN} 1$ and $\operatorname{IN} 2$ are " H ", the system is in brake mode. The operation mechanism is described as follows: the upper-side output transistor turns OFF to stop driving the motor while the lower-side output transistor turns ON to absorb the electromotive force and brake the motor. When both IN1 and IN2 are "L," OUT1 and OUT2 become open (all output transistors are OFF) and the motor stops.
2) Output High Voltage Setting Function

This function sets the output voltage by the Output H Voltage setting terminal (VR) and controls the motor rotation speed. However, when the output H voltage is set to a low level, current consumption increases. Please take this into account when calculating the power dissipation (Pd).
Regarding BA6222 (See Fig. 15)
The relationship between the output High voltage setting (VR) voltage and output High voltage VOH is expressed by:
$\mathrm{VOH}=4 \times \mathrm{V} 4$ (VR voltage) +Vofs
The output voltage can be set to around four times the VR voltage. In such an event, there is a tolerance Vofs, which varies depending on output current and chip temperature.


Fig. 15

Regarding BA6219BFP-Y (See Fig. 16)
The circuit diagram associated with the output High voltage setting VR terminal is shown on the right.
The maximum output voltage Vomax is expressed by:
Vomax=VCC1-Vsat(Q1)-VF(Q2)-VF(Q3)-VF(Q4)
In addition, the relation of the VR voltage to the output voltage at Vomax or lower is expressed by:
$\mathrm{Vo}=\mathrm{VR}+\{\mathrm{VF}(\mathrm{Q} 5)+\mathrm{VF}(\mathrm{Q} 6)+\mathrm{VF}(\mathrm{Q} 7)-\mathrm{VF}(\mathrm{Q} 2)-\mathrm{VF}(\mathrm{Q} 3)-\mathrm{VF}(\mathrm{Q} 4)\}$
$=\mathrm{VR}+\triangle \mathrm{VF} \fallingdotseq \mathrm{VR}$
$\Delta \mathrm{VF}$ depends on the output current but is nearly $\mathrm{Vo}=\mathrm{VR}$.
Reference values: Vsat=0.1V, VF=0.75V
Set VCC1 and VCC2 to the following values.

| Pin | Voltage | Unit |
| :---: | :---: | :---: |
| VCC1 | $8 \sim 18$ | $V$ |
| VCC2 | $8 \sim 18$ | $V$ |

Power supply voltage range of VR

1) When the output voltage control terminal (VR) is used:

$$
\begin{aligned}
\mathrm{VR} & <\mathrm{VCC1} 1-\{\mathrm{Vsat}(\mathrm{Q} 1)+\mathrm{VF}(\mathrm{Q} 5)+\mathrm{VF}(\mathrm{Q} 6)+\mathrm{VF}(\mathrm{Q} 7)\} \\
& \fallingdotseq \mathrm{VCC1} 1-2.5 \mathrm{~V} \\
\mathrm{VR} & <\mathrm{VCC2}-\{\mathrm{Vsat}(\mathrm{Q} 3)-\mathrm{VF}(\mathrm{Q} 3)-\mathrm{VF}(\mathrm{Q} 2)\}+\{\mathrm{VF}(\mathrm{Q} 5)+\mathrm{VF}(\mathrm{Q} 6)+\mathrm{VF}(\mathrm{Q} 7)\} \\
& \fallingdotseq \mathrm{VCC2}-1 \mathrm{~V}
\end{aligned}
$$



Fig. 16


Fig. 17

The output voltage control function does not operate in regions outside this range.
In addition, when the VR terminal is not used, short VR to VCC1.
2) Normal/reverse rotation switching

Before switching, bring the motor to either the brake or idle condition.
When brake is applied : The longer the braking time the better
(Braking time is defined as the time required for the output $L$ terminal to achieve a potential below GND once the brake is activated)
When idle is applied: A time longer than 1 msec is recommended..

## -Thermal Derating Curves



## BA6222



Derated at $11.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$, (mounted on a $90 \mathrm{~mm} \times 50 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy substrate).

## - Input / Output Equivalent Circuits

- BA6219BFP-Y, BA6222


Fig. 20

- BA6219BFP-Y


Fig. 21

- BA6222


Fig. 22

## Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

## 3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.
4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

## 9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

|  | TSD on temperature [ $\left.{ }^{\circ} \mathrm{C}\right]$ (typ.) | Hysteresis temperature [ $\left.{ }^{\circ} \mathrm{C}\right]$ (typ.) |
| :--- | :---: | :---: |
| BA6219BFP-Y | 175 | 15 |
| BA6222 | 150 | 15 |

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
11. Regarding input pin of the IC

This monolithic IC contains $P+$ isolation and $P$ substrate layers between adjacent elements in order to keep them isolated.
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.


Fig. 23 Example of IC structure

## 12. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

- Part Number Explanation


ROHM part number


Package
None = HSIP10


Package specification
E2 = Embossed taping
FP-Y = HSOP25

## HSIP10


<Packing Information>

| Container | Tube |
| :--- | :--- |
| Quantity | 500pcs |
| Direction <br> of feed | Direction of products is fixed in a container tube. |



HSOP25


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