DDR2 SDRAM SOCDIMM

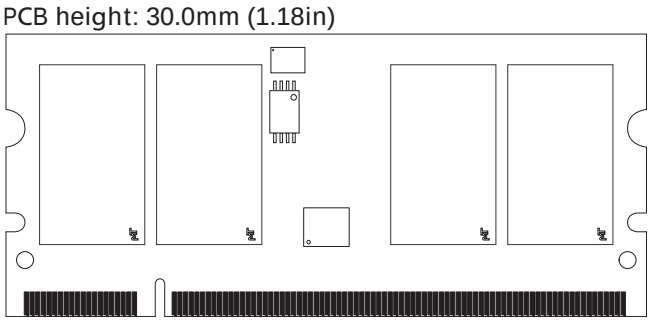
MT9HTF6472CH – 512MB
MT9HTF12872CH – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline clocked dual in-line memory module (SOCDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 72) and 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Phase-lock loop (PLL) to reduce system clock line loading
- Gold edge contacts
- Single rank
- I^2C temperature sensor

Figure 1: 200-Pin SOCDIMM (MO-224 R/C B)



Options — Marking

- Operating temperature[1]
  - Commercial ($0°C \le T_A \le +70°C$) — None
  - Industrial ($–40°C \le T_A \le +85°C$) — I
- Package
  - 200-pin DIMM (Pb-free) — Y
- Frequency/CAS latency
  - 2.5ns @ CL = 5 (DDR2-800)[2] — -80E
  - 2.5ns @ CL = 6 (DDR2-800)[2] — -800
  - 3.0ns @ CL = 5 (DDR2-667) — -667
  - 3.75ns @ CL = 4 (DDR2-533)[3] — -53E

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Contact Micron for product availability.
3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55

Table 2: Address Table

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	8 (BA0–BA2)
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M8,[1] 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF6472CHY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472CHY-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472CHY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472CHY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF12872CHY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872CHY-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872CHY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872CHY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
   Example: MT9HTF12872CHY-667E1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SOCDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQ18	101	VDD	151	VSS
3	DQ0	53	DQ19	103	A5	153	DQS5#
5	VSS	55	VSS	105	A3	155	DQS5
7	DQ1	57	DQ24	107	A2	157	VSS
9	DQS0#	59	DQ25	109	VDD	159	DQ42
11	DQS0	61	VSS	111	A10	161	DQ43
13	VSS	63	DQS3#	113	BA0	163	VSS
15	DQ2	65	DQS3	115	RAS#	165	DQ48
17	DQ3	67	VSS	117	VDD	167	DQ49
19	VSS	69	DQ26	119	CAS#	169	VSS
21	DQ8	71	DQ27	121	NC	171	DQS6#
23	DQ9	73	VSS	123	VDD	173	DQS6
25	VSS	75	CB0	125	NC	175	VSS
27	DQS1#	77	CB1	127	NC	177	DQ50
29	DQS1	79	VSS	129	DQ32	179	DQ51
31	VSS	81	DQS8#	131	VSS	181	VSS
33	DQ10	83	DQS8	133	DQ33	183	DQ56
35	DQ11	85	VSS	135	DQS4#	185	DQ57
37	VSS	87	CKE0	137	DQS4	187	VSS
39	DQ16	89	NC	139	VSS	189	DQS7#
41	DQ17	91	EVENT#	141	DQ34	191	DQS7
43	VSS	93	VDD	143	DQ35	193	DQ58
45	DQS2#	95	A12	145	VSS	195	VSS
47	DQS2	97	A9	147	DQ40	197	DQ59
49	VSS	99	A7	149	DQ41	199	VDDSPD

200-Pin SOCDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VSS	52	VSS	102	A6	152	VSS
4	DQ4	54	DQ28	104	A4	154	DM5
6	DQ5	56	DQ29	106	VDD	156	VSS
8	VSS	58	VSS	108	A1	158	DQ46
10	DM0	60	DM3	110	A0	160	DQ47
12	VSS	62	VSS	112	BA1	162	VSS
14	DQ6	64	DQ30	114	VDD	164	DQ52
16	DQ7	66	DQ31	116	WE#	166	DQ53
18	VSS	68	VSS	118	S0#	168	VSS
20	DQ12	70	CB4	120	ODT0	170	DM6
22	DQ13	72	CB5	122	A13	172	VSS
24	VSS	74	VSS	124	VDD	174	DQ54
26	DM1	76	DM8	126	CK0	176	DQ55
28	VSS	78	VSS	128	CK0#	178	VSS
30	DQ14	80	CB6	130	VSS	180	DQ60
32	DQ15	82	CB7	132	DQ36	182	DQ61
34	VSS	84	VSS	134	DQ37	184	VSS
36	DQ20	86	CB2	136	VSS	186	DM7
38	DQ21	88	CB3	138	DM4	188	DQ62
40	VSS	90	VSS	140	VSS	190	VSS
42	RESET#	92[1]	NC/BA2	142	DQ38	192	DQ63
44	DM2	94	NC	144	DQ39	194	SDA
46	VSS	96	A11	146	VSS	196	SCL
48	DQ22	98	VDD	148	DQ44	198	SA1
50	DQ23	100	A8	150	DQ45	200	SA0

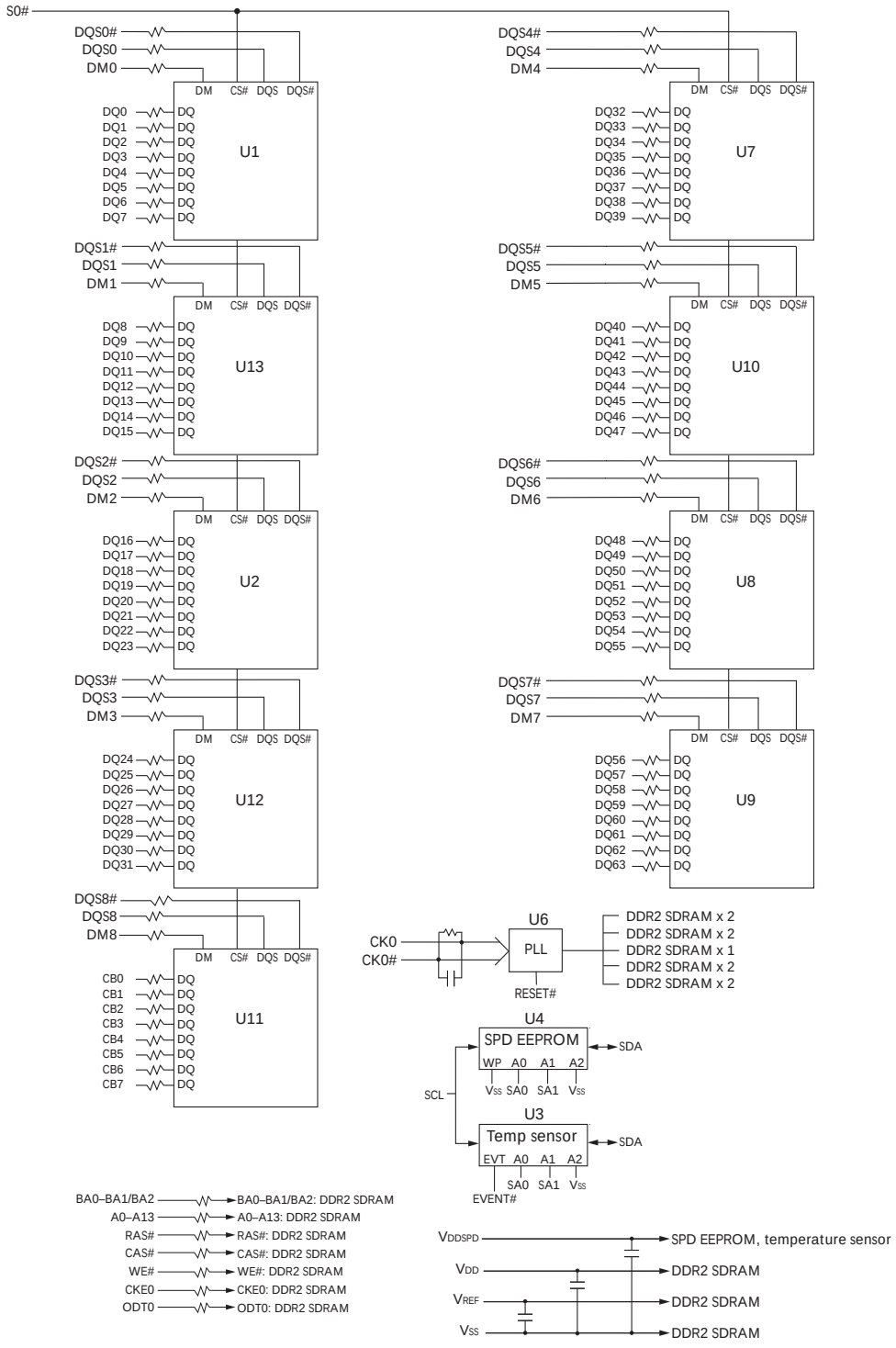
Notes: 1. Pin 92 is NC for 512MB and BA2 for 1GB.

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A13	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0, BA1 (512MB) and BA0–BA2 (1GB).
CK0, CK0#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
DM0–DM8	Input (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is enabled, RDQS0#–RDQS8# are used only during the READ command.
ODT0	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA1	Input (SSTL_18)	**Presence-detect address inputs:** These pins are used to configure the presence-detect and temperature sensor devices.
SCL	Input (SSTL_18)	**Serial clock:** SCL is used to synchronize the presence-detect and temperature sensor data transfer to and from the module.
RESET#	Input (LVCMOS)	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
CB0–CB7	I/O (SSTL_18)	Check bits.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS0–DQS8 (DQS0#–DQS8#)	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O (SSTL_18)	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
EVENT#	Output	**Temperature sensor alarm output:** The event pin is used to flag critical module temperatures.
V_{DD}	Supply	**Power supply:** +1.8V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM and temperature sensor positive power supply:** +3.0V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT9HTF6472CH and MT9HTF12872CH DDR2 SDRAM modules are high-speed, CMOS, dynamic random access 512MB and 1GB memory modules, organized in a x72 configuration. These modules use a 512Mb DDR2 SDRAM device with four internal banks or a 1Gb DDR2 SDRAM device with eight internal banks.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL Operation

A PLL chip on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The PLL minimizes system clock line loading. PLL clock timing is defined by JEDEC specifications and is ensured by the use of a JEDEC clock reference board.

Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. An EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, ODT, BA, S#, CKE	–45	+45	µA
		CK0, CK0#	–250	+250	
		DM	–5	+5	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ $V_{DD}Q$; DQ and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–18	+18	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. Refresh rate is required to double when 85°C < T_C ≤ 95°C.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades as shown in Table 8.

Table 8: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E

IDD Specifications

Table 9: DDR2 IDD Specifications and Conditions – 512MB

Values are shown for the MT9HTF6472 DDR2 SDRAM only and are computed from the values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	900	810	720	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,035	945	855	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	405	360	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	495	450	405	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3Pf	360	315	270	mA
	Slow PDN exit MR[12] = 1	IDD3Ps	108	108	108	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	630	585	495	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP= ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,755	1,530	1,260	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,845	1,620	1,305	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,070	1,620	1,530	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		IDD7	2,700	2,160	2,025	mA

Table 10: DDR2 IDD Specifications and Conditions – 1GB

Values are shown for the MT9HTF12872 DDR2 SDRAM only and are computed from the values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	765	630	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	990	900	855	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	360	360	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	450	360	270	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3Pf	360	270	270	mA
	Slow PDN exit MR[2] = 1	IDD3Ps	90	90	90	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	540	495	405	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,440	1,215	1,125	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,440	1,215	1,125	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,115	1,935	1,890	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		IDD7	3,015	2,520	2,430	mA

PLL Specifications

Table 11: PLL Device Specifications
CUA845 device or JESD82-21 equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	OE, OS, CK, CK#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	OE, OS, CK, CK#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	–	–	–0.3	V_{DDQ} + 0.3	V
DC high-level input voltage	V_{IH}	–	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	–	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	–	Differential input	(V_{DDQ}/2) - 0.15	(V_{DDQ}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	–	Differential input	0.3	V_{DDQ} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	–	Differential input	0.6	V_{DDQ} + 0.4	V
Input current	I_I	OE, OS, FBIN, FBIN#	V_I = V_{DDQ} or V_{SSQ}	–10	+10	µA
		CK, CK#	V_I = V_{DDQ} or V_{SSQ}	–250	+250	µA
Output disabled current	I_{ODL}	–	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}	–	CK = CK# = LOW	–	+500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 410 MHz, all outputs open (not connected to PCB)	–	+300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DDQ} or V_{SSQ}	+2.0	+3.0	pF

Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	6	µs
Input clock slew rate	slr(i)	1	4	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used.

Temperature Sensor

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD. This sensor complies with the "Mobile Platform Memory Module Thermal Sensor Component Specification," which is found in JEDEC standard JESD21-C.

Table 13: Temperature Sensor Specifications

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	+3.0	+3.6	V
Average operating supply current	–	–	+500	µA
Input high voltage: Logic 1; All inputs	V_{IH}	+2.1	–	V
Input low voltage: Logic 0; All inputs	V_{IL}	–	+0.8	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	+0.4	V
Logic input current	I_{IH}	–5	+5	µA
	I_{IL}	–5	+5	µA
Temperature sensing range	–	–40	+125	°C

Table 14: Temperature Sensor AC Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t_{BUF}	4.7	–	µs
Clock/data fall time	t_F	–	300	ns
Clock/data rise time	t_R	–	1,000	ns
Data hold time	$t_{HD:DAT}$	300	–	ns
Start condition hold time	$t_{HD:STA}$	4.0	–	µs
Clock HIGH period	t_{HIGH}	4.0	50	µs
Clock LOW period	t_{LOW}	4.7	–	µs
SCL clock frequency	f_{SCL}	–	400	kHz
Data setup time	$t_{SU:DAT}$	250	–	ns
Start condition setup time	$t_{SU:STA}$	4.7	–	µs
Stop condition setup time	$t_{SU:STO}$	4.0	–	µs
Clock frequency	t_{CK}	10	100	kHz

Serial Presence-Detect

Table 15: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage with temperature sensor option	V_{DDSPD}	3.0	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	2.1	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	0.8	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
SPD input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3.0	µA
SPD output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
SPD standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CC_R}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CC_W}	2.0	3.0	mA
Average temperature sensor current	–	–	500	µA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
Clock/data fall time	^tF	–	300	ns	2
Clock/data rise time	^tR	–	3,000	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

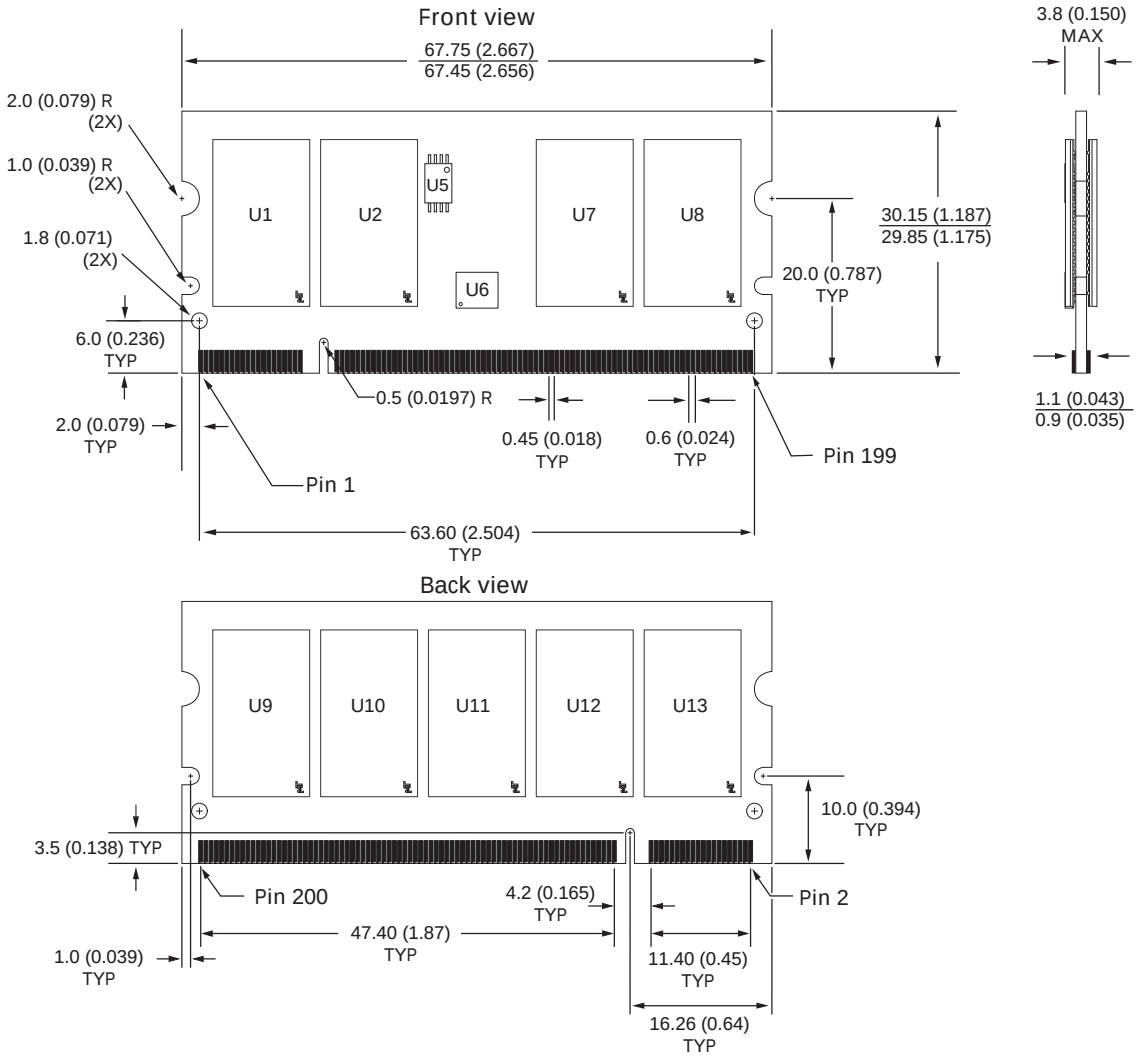
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 200-Pin DDR2 SOCDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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