DDR3 SDRAM RDIMM

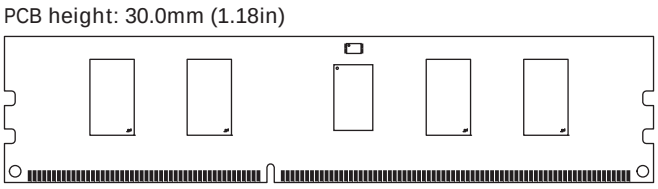
MT9JSF12872PY – 1GB
MT9JSF25672PY – 2GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- DDR3 functionality and operations supported as per component data sheet
- 240-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC3-10600, PC3-8500, or PC3-6400
- 1GB (128 Meg x 72), 2GB (256 Meg x 72)
- $V_{DD} = V_{DD}Q = 1.5V \pm 0.075V$
- $V_{DDSPD} = +3V$ to $+3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- Eight internal device banks for concurrent operation
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 via the mode register set
- Adjustable data-output drive strength
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- I^2C temperature sensor
- Pb-free
- Fly-by topology
- Terminated command, address, and control bus

Figure 1: 240-Pin RDIMM (MO-269 R/C A)



Options	Marking
• Operating temperature[1]	
– Commercial ($0°C \le T_A \le +70°C$)	None
– Industrial ($–40°C \le T_A \le +85°C$)	I
• Frequency/CAS latency	
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.5ns @ CL = 10 (DDR3-1333)	-1G3
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1
– 1.87ns @ CL = 8 (DDR3-1066)	-1G0
– 2.5ns @ CL = 5 (DDR3-800)	-80C
– 2.5ns @ CL = 6 (DDR3-800)	-80B

Notes: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)						t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G4	PC3-10600	–	1333	1066	800	–	–	13.5	13.5	49.5
-1G3	PC3-10600	1333	1066	800	–	–	–	15	15	51
-1G1	PC3-8500	–	–	–	1066	800	–	13.125	13.125	50.625
-1G0	PC3-8500	–	–	1066	800	–	–	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	800	–	15	15	52.5

Table 2: Addressing

Parameter	1GB	2GB
Refresh count	8K	8K
Row address	16K (A0–A13)	32K (A0–A14)
Device bank address	8 (BA0–BA2)	8 (BA0–BA2)
Device page size per bank	1KB	1KB
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9JSF12872P(I)Y-1G4__	1GB	128 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT9JSF12872P(I)Y-1G3__	1GB	128 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	10-10-10
MT9JSF12872P(I)Y-1G1__	1GB	128 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT9JSF12872P(I)Y-1G0__	1GB	128 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT9JSF12872P(I)Y-80C__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9JSF12872P(I)Y-80B__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9JSF25672P(I)Y-1G4__	2GB	256 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT9JSF25672P(I)Y-1G3__	2GB	256 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	10-10-10
MT9JSF25672P(I)Y-1G1__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT9JSF25672P(I)Y-1G0__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT9JSF25672P(I)Y-80C__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9JSF25672P(I)Y-80B__	2GB	256 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9JSF12872PY-1G1B1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

240-Pin RDIMM Front								240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3/ DQS12	182	VDD	212	DM5/ DQS14
3	DQ0	33	DQS3#	63	NC	93	DQS5#	123	DQ5	153	DQS12#	183	VDD	213	DQS14#
4	DQ1	34	DQS3	64	NC	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0/ DQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	DQS9#	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	PAR_IN	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DM8/ DQS17	191	VDD	221	DM6/ DQS15
12	DQ8	42	DQS8#	72	VDD	102	DQS6#	132	DQ13	162	DQS17#	192	RAS#	222	DQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	VSS	163	VSS	193	S0#	223	VSS
14	VSS	44	VSS	74	CAS#	104	VSS	134	DM1/ DQS10	164	CB6	194	VDD	224	DQ54
15	DQS1#	45	CB2	75	VDD	105	DQ50	135	DQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	VTT	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	VTT	79	NC	109	DQ57	139	VSS	169	NC	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7/ DQS16
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	DQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	ERR_OUT#	83	VSS	113	VSS	143	DM2/ DQS11	173	VDD	203	DM4/ DQS13	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	DQS11#	174	A12	204	DQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23#	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

Table 6: Pin Descriptions

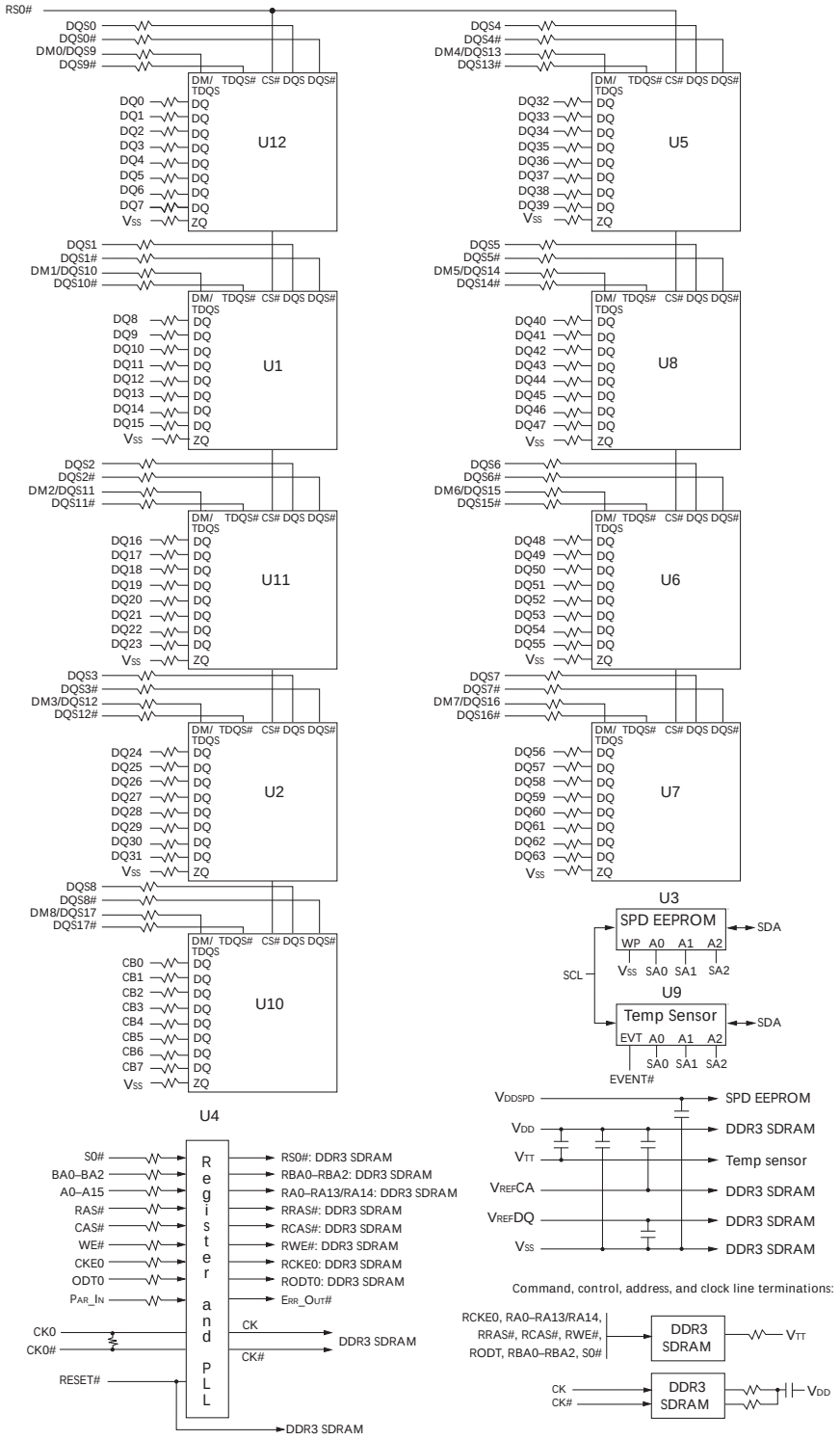
Symbol	Type	Description
A0–A15	Input	**Address inputs:** Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC = 4/BL = 8 identification as "BL on the fly" during CAS commands. The address inputs also provide the op-code during mode register command set. A0–A13 (1GB), A0–A14 (2GB), and A15 is used as part of the parity calculation.
BA0–BA2	Input	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0–BA1 are used as part of the parity calculation.
CK0, CK0#	Input	**Clock:** CK0 and CK0# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM0–DM8 (DQS9–DQS17)	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
PAR_IN	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** An active LOW CMOS input referenced to V_{SS} and not referenced to $V_{REF}CA$ or $V_{REF}DQ$. The reset pin input receiver is a CMOS input and is defined as a rail-to-rail signal with a DC HIGH $\geq 0.8 \times V_{DD}Q$ and DC LOW $\leq 0.2 \times V_{DD}Q$ (1.20V for HIGH and 0.30V for LOW). RESET# assertion and desertion are asynchronous. System applications will most likely be unterminated, heavily loaded, and have very slow slew rates. A slow slew rate receiver design is recommended along with implementing on-chip noise filtering to prevent false triggering (RESET# assertion minimum pulse width is 100ns).
SA0–SA2	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range.
S0#, S1#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. With both inputs HIGH, all outputs of the register(s) are disabled except for CKE and ODT.
SCL	Input	**Serial clock for presence-detect and temperature sensor:** SCL is used to synchronize the communication to and from the EEPROM temperature sensor.
DQ0–DQ63	I/O	**Data input/output:** Bidirectional data bus.
CB0–CB7	I/O	**Check bits:** Data used for ECC.
DQS0–DQS8, DQS0#–DQS8#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. DQS0–DQS8/DQS0#–DQS8# are inputs only when TDQS is disabled on x8 modules.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
EVENT#	Output	**Temperature event:** The optional event pin is used to flag critical module temperatures when used in conjunction with a temperature senor.

Table 6: Pin Descriptions (continued)

Symbol	Type	Description
ERR_OUT	Output (open drain)	**Parity error output:** Parity error found on the command, address, and control bus.
VDD	Supply	**Power supply:** 1.5V ±0.075V.
VSS	Supply	**Ground.**
VTT	Supply	**Termination voltage:** Used for address, command, and control. VDD/2.
VDDSPD	Supply	**Serial EEPROM and temperature sensor power supply:** +3V to +3.6V.
VREFDQ	Supply	**Reference voltage:** DQ, DM. VDD/2.
VREFCA	Supply	**Reference voltage:** Command, address, and control. VDD/2.
NC	–	**No connect:** These pins should be left unconnected.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. Used for the calibration of the component's on-die termination and output driver.

General Description

The MT9JSF12872PY and MT9JSF25672PY DDR3 SDRAM modules are high-speed, CMOS, dynamic random-access 1GB and 2GB memory modules organized in a x72 configuration. These DDR3 SDRAM modules use internally configured 8-bank 1Gb and 2Gb DDR3 SDRAM devices.

DDR3 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. To ensure the best possible signal quality, the clock and command/address busses have been routed in a fly-by topology, where each clock and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write leveling feature of DDR3.

Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver IC consisting of a register and a phase-lock loop (PLL). The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller.

Serial Presence-Detect Operation

DDR3 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.4	+1.975	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	–TBD	+TBD	µA
		CK, CK#	–5	+150	
		DM	–1	+1	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–1	+1	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–18	+18	µA

Table 8: Operating Conditions

Symbol	Parameter		Min	Max	Units
I_{VTT}	Termination reference current from V_{TT}		–600	+600	mA
V_{TT}[1]	Termination reference voltage – command address bus		–0.483 × V_{DD}	+0.517 × V_{DD}	V
T_A[2, 3]	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[2, 3]	DDR3 SDRAM component case operating temperature[4]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. V_{TT} termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. The T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site.
4. Refresh rate is required to double when 85°C < T_C ≤ 95°C.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9 on page 9.

Table 9: Module and Component Speed Grades

DDR3 components must be able to meet or exceed the listed module speed grade

Module Speed Grade	Component Speed Grade
-1G4	-15E
-1G3	-15
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

IDD Specifications

Table 10: DDR3 IDD Specifications and Conditions – 1GB
Values shown for each data rate are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	1,125	1,035	855	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	1,350	1,170	990	mA
Precharge power-down current: Slow exit	IDD2P	90	90	90	mA
Precharge power-down current: Fast exit	IDD2P	225	225	225	mA
Precharge quiet standby current	IDD2Q	630	540	450	mA
Precharge standby current	IDD2N	675	585	495	mA
Active power-down current	IDD3P	495	405	360	mA
Active standby current	IDD3N	810	675	540	mA
Burst read operating current	IDD4R	2,250	1,980	1,710	mA
Burst write operating current	IDD4W	2,475	2,160	1,845	mA
Refresh current	IDD5B	2,610	2,295	1,935	mA
Self refresh temperature current: MAX T_C = 85°C	IDD6ET	81	81	81	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	IDD6	54	54	54	mA
All bank interleaved read current	IDD7	4,860	4,230	3,960	mA

Table 11: DDR3 IDD Specifications and Conditions – 2GB
Values shown for each data rate are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	1,170	1,080	900	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	1,395	1,215	1,035	mA
Precharge power-down current: Slow exit	IDD2P	90	90	90	mA
Precharge power-down current: Fast exit	IDD2P	225	225	225	mA
Precharge quiet standby current	IDD2Q	630	540	450	mA
Precharge standby current	IDD2N	630	540	450	mA
Active power-down current	IDD3P	540	450	405	mA
Active standby current	IDD3N	855	720	585	mA
Burst read operating current	IDD4R	2,025	2,025	1,755	mA
Burst write operating current	IDD4W	2,700	2,385	2,070	mA
Refresh current	IDD5B	2,880	2,565	2,205	mA
Self refresh temperature current: MAX T_C = 85°C	IDD6ET	108	108	108	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	IDD6	72	72	72	mA
All bank interleaved read current	IDD7	4,140	3,870	3,600	mA

Registering Clock Driver Specifications

Table 12: Registering Clock Driver Electrical Characteristics
SSTE32882 devices or equivalent

Symbol	Parameter	Pins	Min	Nom	Max	Units
V_{DD}	DC supply voltage	–	1.425	1.5	1.575	V
V_{REF}	DC reference voltage	–	0.49 × V_{DD}	0.5 × V_{DD}	0.051 × V_{DD}	V
V_{TT}	DC termination voltage	–	V_{REF} - 40mV	V_{REF}	V_{REF} + 40mV	V
$V_{IH(AC)}$	AC high-level input voltage	Address, control, command	V_{REF} + 175mV	–	V_{DD} + 400mV	V
$V_{IL(AC)}$	AC low-level input voltage	Address, control, command	–0.4	–	V_{REF} - 175mV	V
$V_{IH(DC)}$	DC high-level input voltage	Address, control, command	V_{REF} + 100mV	–	V_{DD} + 0.4	V
$V_{IL(DC)}$	DC low-level input voltage	Address, control, command	–0.4	–	V_{REF} - 100mV	V
V_{IH} (CMOS)	High-level input voltage	RESET#, MIRROR	0.65 × V_{DD}	–	V_{DD}	V
V_{IL} (CMOS)	Low-level input voltage	RESET#, MIRROR	0	–	0.35 × V_{DD}	V
$V_{IX(AC)}$	Differential input cross point voltage range	CK, CK#, FBIN, FBIN#	0.5 × V_{DD} - 175mV	0.5 × V_{DD}	0.5 × V_{DD} + 175mV	V
$V_{ID(AC)}$	Differential input voltage	CK, CK#	350	–	V_{DD} + TBD	mV
I_{OH}	High-level output current	All outputs except ERR_OUT#	–	–	TBD	mA
I_{OL}	Low-level output current	All outputs except ERR_OUT#	–	–	TBD	mA
I_{OL}	Low-level output current (ERR_OUT#)	ERR_OUT	TBD	–	TBD	mA
V_{OD}	Differential redriven clock swing	Y*n*, Y*n*#	500	–	V_{DD}	mV
V_{OX}	Differential output crosspoint voltage	Y*n*, Y*n*#	0.5 × V_{DD} - 100mV	–	0.5 × V_{DD} + 100mV	V

Note: Timing and switching specifications for the register listed above are critical for proper operation of the DDR3 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

Temperature Sensor

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD. This sensor complies with the JEDEC standard JESD21-C, page 4.7-1.

Table 13: Temperature Sensor Specifications
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DD}	+3	+3.6	V
Average operating supply current	–	–	+500	µA
Input high voltage: Logic 1; All inputs	V_{IH}	+2.1	–	V
Input low voltage: Logic 0; All inputs	V_{IL}	–	+0.8	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	+0.4	V
Logic input current	I_{IH}	–5	+5	µA
	I_{IL}	–5	+5	µA
Temperature sensing range	–	–40	+125	°C

Table 14: Temperature Sensor AC Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t_{BUF}	4.7	–	µs
SDA and SCL fall time	t_F	–	300	ns
Data hold time	$t_{HD:DAT}$	300	–	ns
Start condition hold time	$t_{HD:STA}$	4	–	µs
Clock HIGH period	t_{HIGH}	4	50	µs
Clock LOW period	t_{LOW}	4.7	–	µs
SDA and SCL rise time	t_R	–	1	µs
SCL clock frequency	f_{SCL}	10	100	kHz
Data setup time	$t_{SU:DAT}$	250	–	ns
Start condition setup time	$t_{SU:STA}$	4.7	–	µs
Stop condition setup time	$t_{SU:STO}$	4	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin. Not used by the SPD, the EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated in Figure 3 on page 13. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode and the critical EVENT# cannot be cleared through software.

SM Bus Slave Subaddress Decoding

The temperature sensor's physical address differs from the module's SPD device physical addresses: 0011 for A0, A1, A2, and RW# in binary where A2, A1, and A0 are the three slave subaddress pins and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the SPD and temperature sensor, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Figure 3: EVENT# Pin Functionality

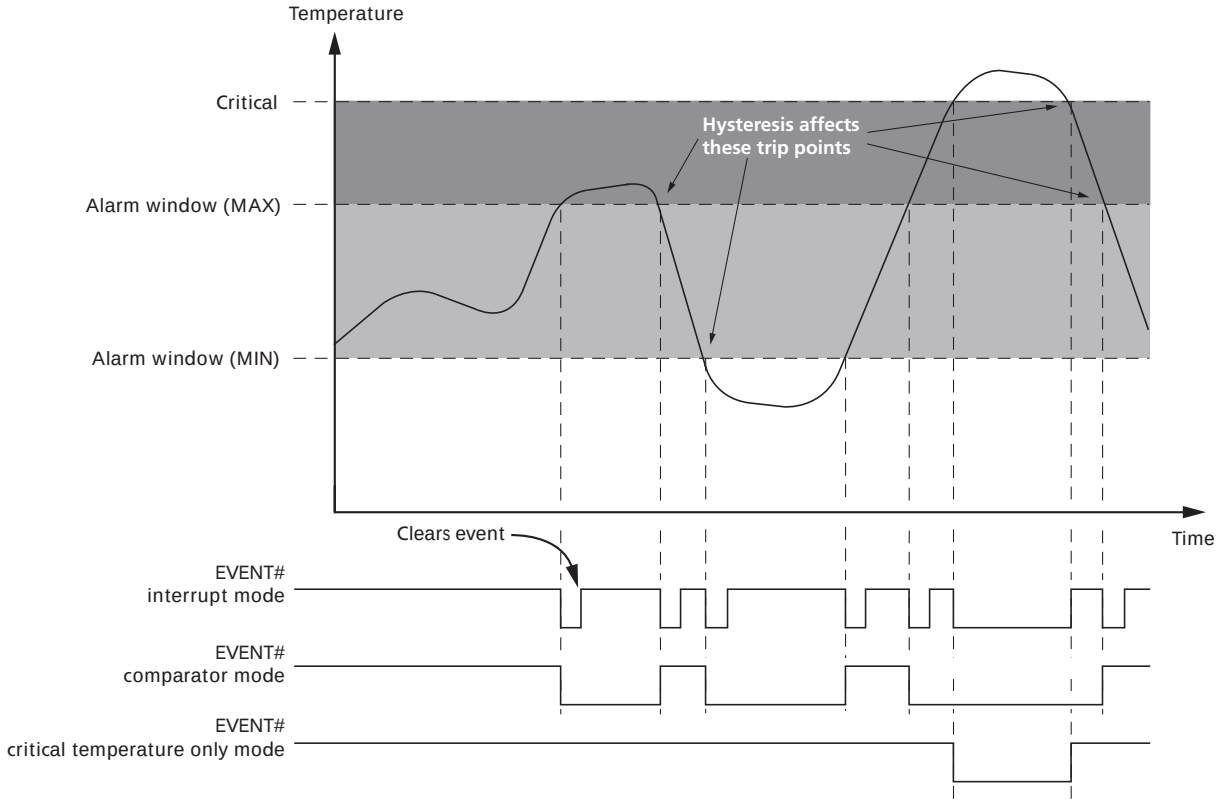


Table 15: Temperature Sensor Registers

Name	Address	Power-On Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

Table 16: Pointer Register Bits 0–7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	Register select	Register select	Register select	Register select

Table 17: Pointer Register Bits 0–2 Descriptions

Bit 2	Bit 1	Bit 0	Register
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 18: Capability Register Bits 0–15

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RFU	RFU	RFU	TRES1	TRES0	Wider range	Precision	Has alarm and critical temperature

Table 19: Capability Register Bits 0–15 Descriptions

Bit	Description
0	Basic capability 1: Has alarm and critical trip point capabilities
1	Accuracy 0: ±2°C over the active range and ±3°C over the monitor range 1: ±1°C over the active range and ±2°C over the monitor range
2	Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

Configuration Register

Table 20: Configuration Register Bits 0–15

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

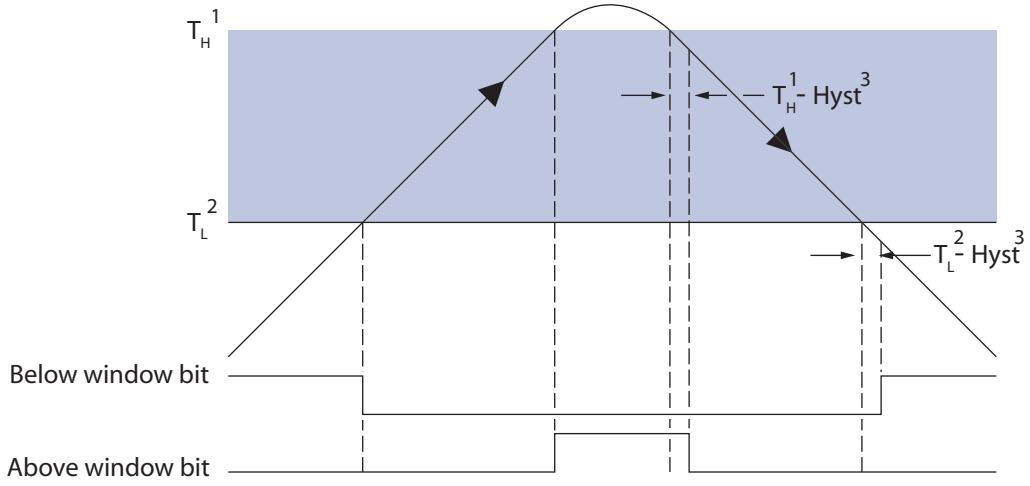
Table 21: Configuration Register Bits 0–10 Descriptions

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Cannot be changed if either of the lock bits is set
1	EVENT# polarity 0: Active LOW 1: Active HIGH	Cannot be changed if either of the lock bits is set
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register; the event causing the event can be determined from the read temperature register
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	

Table 21: Configuration Register Bits 0–10 Descriptions (continued)

Bit	Description	Notes
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	This is a write-only field in the register and is self-clearing
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	When enabled, a hysteresis is applied to temperature movement around the trip points. As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C The hysteresis is applied both to the above alarm window and the below alarm window bits found in the read-only temperature register. EVENT# is also affected by this register

Figure 4: Hysteresis



Notes:
1. T_H is the value set in the alarm temperature upper boundary trip register.
2. T_L is the value set in the alarm temperature lower boundary trip register.
3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 22: Hysteresis

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature gradient	Critical temperature	Temperature gradient	Critical temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

Temperature Format

The temperature trip point registers and temperature readout register use a "2's complement" format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C depending on which register is referenced. As an example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal –24.75°C

Upper Boundary Temperature Register

The upper boundary temperature register is used to set the maximum value of the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 23: Upper Boundary Temperature Register Bits 0–15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window upper boundary temperature												

Lower Boundary Temperature Register

The lower boundary temperature register is used to set the minimum value of the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 24: Lower Boundary Temperature Register Bits 0–15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window lower boundary temperature												

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 25: Critical Temperature Register Bits 0–15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Critical temperature trip point												

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.

Table 26: Temperature Register Bits 0–15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above critical trip	Above alarm window	Below alarm window	MSB												LSB
			Temperature												

Table 27: Temperature Register Bits 13–15 Descriptions

Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

Serial Presence-Detect

Table 28: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	ICC_W	2	3	mA

Table 29: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 30: Serial Presence-Detect Matrix

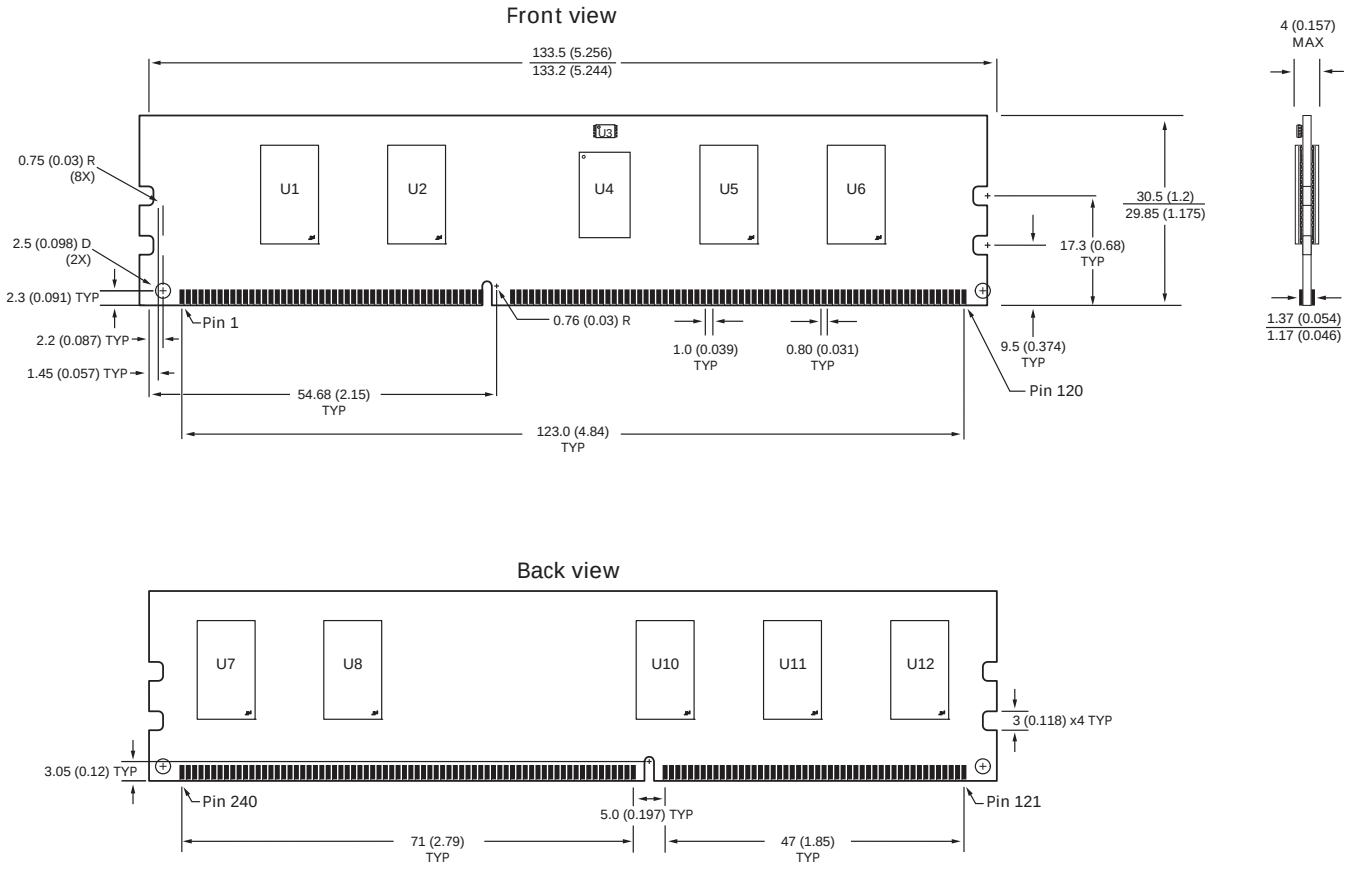
Byte	Description	Entry (Version)	1GB	2GB
0	Cyclic redundancy check (CRC) coverage EEPROM device size Number of SPD bytes written	Bytes 0–116 256 bytes 176 bytes	92	92
1	SPD revision	Rev 1.0	10	10
2	DRAM device type (technology)	DDR3 SDRAM	0B	0B
3	Module type (form factor)	RDIMM	01	01
4	SDRAM device density and internal banks	1Gb/8 banks 2Gb/8 banks	02 –	– 03
5	SDRAM device addressing (row and column counts)	(14, 10) (15, 10)	11 –	– 19
6	Reserved	0	00	00
7	Module organization (module ranks, SDRAM device width)	1 rank, x8 I/O	01	01
8	Module memory bus width	ECC and parity, 72-bit	0B	0B
9	Fine time base (FTB) dividend/divisor	5/2	52	52
10	Medium time base (MTB) dividend	1	01	01
11	Medium time base (MTB) divisor	8	08	08
12	SDRAM device minimum cycle time (^{t}CK [MIN])	-1G4/-1G3/-1G1/-1G0 -80C/-80B	0F 14	0F 14
13	Reserved	0	00	00
14	CAS latencies supported, low byte	-1G4 -1G3 -1G1 -1G0 -80C -80B	34 54 1C 14 06 04	34 54 1C 14 06 04
15	CAS latencies supported, high byte	0	00	00
16	MIN CAS latency time (^{t}AA [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	6C 78 69 78 64 78
17	MIN write recovery time (^{t}WR [MIN])	–	78	78
18	MIN RAS#-to-CAS# delay time (^{t}RCD [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	6C 78 69 78 64 78
19	MIN row active-to-row active delay time (^{t}RRD [MIN])	-1G4/-1G3/-1G1/-1G0 -80C/-80B	30 50	30 50
20	MIN row precharge delay time (^{t}RP [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78	6C 78 69 78 64 78
21	Upper nibble for ^{t}RAS and ^{t}RC	–	11	11

Table 30: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	1GB	2GB
22	MIN active-to-precharge delay time (^{t}RAS [MIN]), LSB	-1G4/-1G3 -1G1/-1G0/-80C/-80B	20 2C	20 2C
23	MIN active-to-active/refresh (^{t}RC [MIN]), LSB	-1G4 -1G3 -1G1 -1G0 -80C -80B	8C 98 95 A4 90 A4	8C 98 95 A4 90 A4
24	MIN refresh recovery delay time (^{t}RFC [MIN]), LSB	1Gb 2Gb	70 –	– 00
25	MIN refresh recovery delay time (^{t}RFC [MIN]), MSB	1Gb 2Gb	03 –	– 05
26	MIN internal WRITE-to-READ command delay time (^{t}WTR [MIN])	–	3C	3C
27	MIN internal READ-to-PRECHARGE command delay time (^{t}RTP [MIN])	–	3C	3C
28	MIN for activate window delay time (^{t}FAW [MIN]), upper nibble	-1G4/-1G3 -1G1/-1G0/-80C/-80B	00 01	00 01
29	MIN for activate window delay time (^{t}FAW [MIN]), LSB	-1G4/-1G3 -1G1/-1G0 -80C/-80B	F0 2C 40	F0 2C 40
30	SDRAM device output drivers supported	–	82	82
31	SDRAM device thermal refresh options	–	05	05
32–59	Reserved, general section	–	00	00
60	Module NOM height	30mm	0F	0F
61	Module MAX thickness	Single rank, 4mm	11	11
62	Reference raw card used	RDIMM R/C A	00	00
63	Reserved (for RDIMM)	–	00	00
64–116	Reserved	0	00	00
117	Module manufacturer ID (continuation code)	–	80	80
118	Module manufacturer ID (manufacturer's ID code)	–	2C	2C
119	Module manufacturing location	1–12	01–0C	01–0C
120–121	Module manufacturing date	–	Variable data	Variable data
122–125	Module serial number	–	Variable data	Variable data
126, 127	CRC	-1G4 -1G3 -1G1 -1G0 -80C -80B	8E28 685B 502C 380A CC1A 443C	EA90 098F BADC D2FA 26EA AECC
128–145	Module part number (ASCII)	–	Variable data	Variable data
146	Module revision code, SDRAM device die revision	–	Variable data	Variable data
147	Module revision code, PCB revision	–	Variable data	Variable data
148	DRAM device manufacturer ID (continuation code)	–	80	80
149	DRAM device manufacturer ID (manufacturer's ID code)	–	2C	2C
150–175	Reserved for manufacturer-specific data	–	00	00
176–255	Reserved for customer-specific data	–	FF	FF

Module Dimensions

Figure 5: 240-Pin DDR3 RDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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