

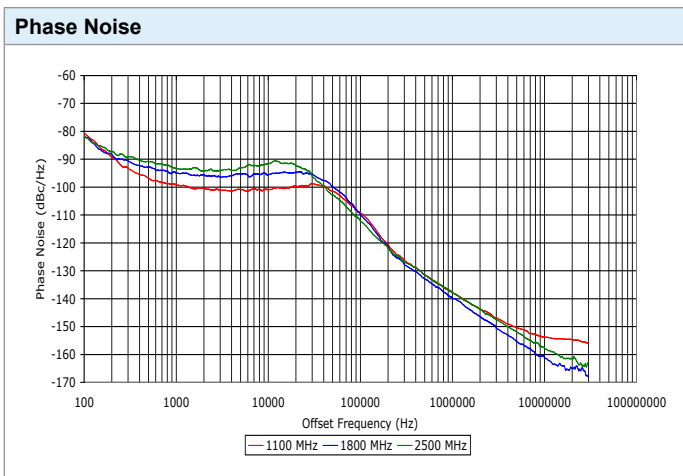
# INTELLIGENT INTERACTIVE SYNTHESIZER SURFACE MOUNT MODEL: MTS2500-110250-10

WIDE BANDWIDTH

1100 - 2500 MHz

## FEATURES:

- ▶ Over an octave bandwidth tuning
- ▶ Small step size resolution
- ▶ Outstanding spectral purity
- ▶ High spurious rejection
- ▶ Fast lock settling time
- ▶ Easy programmable format
- ▶ Patent Pending Rel-Pro Technology
- ▶ RoHS Compliant



## SPECIFICATIONS (Rev. A 06/17/08)

|                          |                          |
|--------------------------|--------------------------|
| Output Frequency         | 1100 - 2500 MHz          |
| Bandwidth                | 1400 MHz                 |
| External Reference *     | 10 MHz                   |
| External Reference Input | 1 V p-p to 3.3 V p-p     |
| Step Size                | Programmable to 1 Hz     |
| <b>Bias Voltage</b>      |                          |
| VCC1 (VCO)               | +5 VDC @ 70 mA (Max.)    |
| VCC2 (Analog)            | +3.3 VDC @ 140 mA (Max.) |
| VCC3 (Digital)           | +3.3 VDC @ 50 mA (Max.)  |
| VCC4 (Converter)         | +5 VDC @ 45 mA (Max.)    |
| VCC5 (Converter Output)  | +25 VDC                  |
| VCC6 (PLL)               | +5 VDC @ 2 mA (Max.)     |
| VCC7 (PLL)               | +3.3 VDC @ 20 mA (Max.)  |
| VCC8 (Vtune) **          | +25 VDC @ 5 mA (Max.)    |
| Output Power             | +9 dBm (Min.)            |
| Spurious Suppression     | 60 dB (Typ.)             |
| Harmonic Suppression     | 15 dB (Typ.)             |

|                                        |                              |                |
|----------------------------------------|------------------------------|----------------|
| <b>Typical Phase Noise</b>             | <b>Offset</b>                | <b>dBc/Hz.</b> |
|                                        | 1 kHz                        | -93            |
|                                        | 10 kHz                       | -95            |
| <b>Settling Time***</b>                | Within 1 kHz                 | <22 mSec       |
|                                        | Within 10 Hz                 | <36 mSec       |
|                                        | <b>Output Impedance</b>      | 50 Ohms (Nom.) |
| <b>Operating Temperature Range</b>     | -20 to +70 °C                |                |
| <b>Non-Operating Temperature Range</b> | -40 to +85 °C                |                |
| <b>Programming</b>                     | See Application Note: AN7400 |                |
| <b>Programming Bus****</b>             | Specify SPI or RS-232        |                |

## Absolute Maximum Ratings

|                                     |                |
|-------------------------------------|----------------|
| <b>Storage Temp. Range</b>          | -55 to +125 °C |
| <b>Bias Voltage (+3.3 V)</b>        | +3.6 V         |
| <b>Bias Voltage (+5 V)</b>          | +5.5 V         |
| <b>DC Voltage Applied to RF Out</b> | ± 25 V         |

\* Reference input frequency can be factory programmed for requested common reference frequencies from 10 - 25 MHz. Unless otherwise specified, the reference frequency is factory programmed for 10 MHz.

\*\* If supply voltage from converter output is not used.

\*\*\* Time between latch enable (LE) high (after user command) and final output frequency.

\*\*\*\* Default bus (if unspecified) is SPI.

This product is manufactured under one or more of the following patents: Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113  
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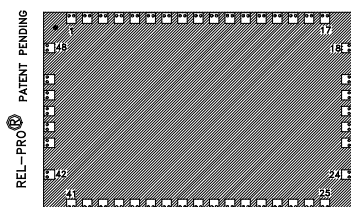
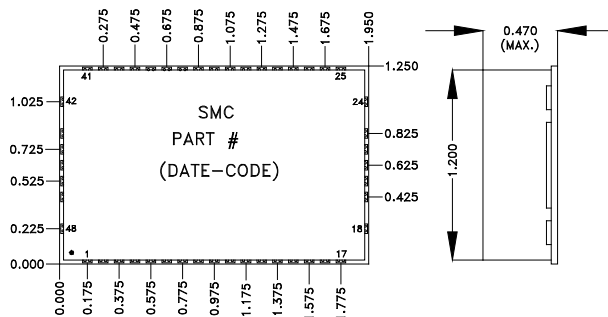


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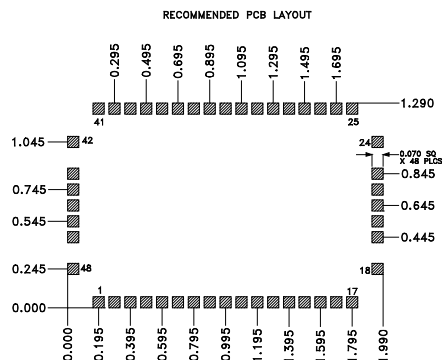
WIDE BANDWIDTH

1100 - 2500 MHz

Package # 344



PACKAGE MOUNTING: SEE APPLICATION NOTE AN7200  
TOLERANCES ON THREE  
DECIMAL PLACES =  $\pm 0.015$



## Port Configuration

|                                    |                                     |                                                                                                 |
|------------------------------------|-------------------------------------|-------------------------------------------------------------------------------------------------|
| Pin 3 - VCC 1 (VCO = +5 Vdc)       | Pin 15 - MISO (SPI)                 | Pin 28 - VCC 5 (Converter output = +25 Vdc)**                                                   |
| Pin 6 - RF Out                     | Pin 16 - Latch Enable (LE)          | Pin 35 - GND*                                                                                   |
| Pin 8 - VCC 2 (Analog = 3.3 Vdc)   | Pin 18 - Reset                      | Pin 39 - VCC 6 (PLL = +5 Vdc)                                                                   |
| Pin 9 - NC*                        | Pin 19 - MOSI (SPI)                 | Pin 40 - VCC 7 (PLL = +3.3 Vdc)                                                                 |
| Pin 10 - NC*                       | Pin 20 - RXD (RS-232)***            | Pin 44 - VCC 8 (Vtune = +25 Vdc)**                                                              |
| Pin 11 - VCC 3 (Digital = 3.3 Vdc) | Pin 21 - TXD (RS-232)***            | Pin 43, 45 - NC (No Connection)                                                                 |
| Pin 13 - Clock (SPI)               | Pin 22 - Ref In                     | All Others - Ground (1,2,4,5,7,12,17,23,24,25,<br>26,29,30,31,32,33,34,36,37,38,41,42,46,47,48) |
| Pin 14 - Lock Detect (LD)          | Pin 27 - VCC 4 (Converter = +5 Vdc) |                                                                                                 |

\* Future expansion for modulation options (digital and analog).

\*\* Connect together externally and bypass with shunt 10  $\mu$ F, 35 V tantalum capacitor to ground. (For applications where an external well filtered 25 volts supply is available, leave pin 27 unconnected and apply the 25 volts directly to pin 44.)

\*\*\* Positive CMOS level (Unbuffered).

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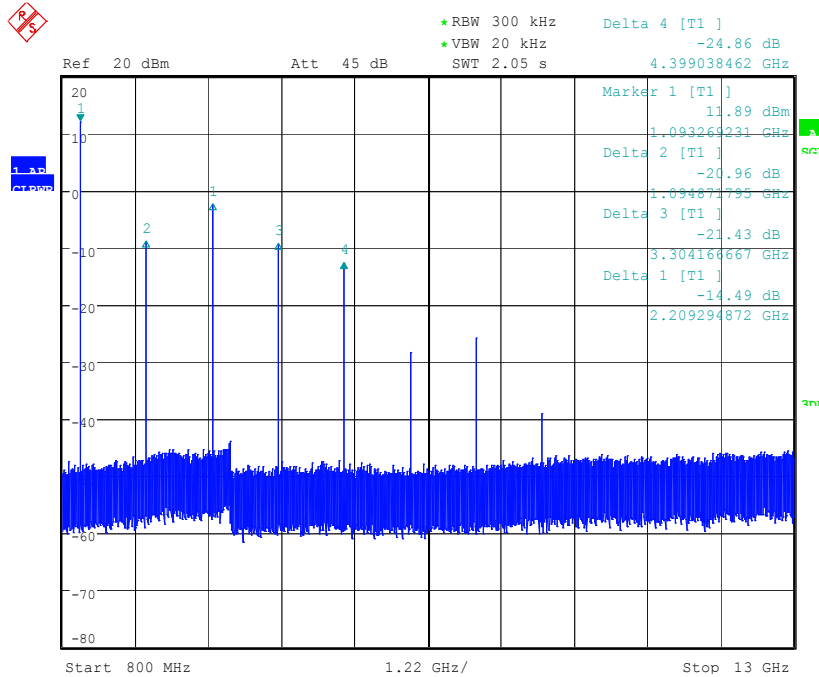


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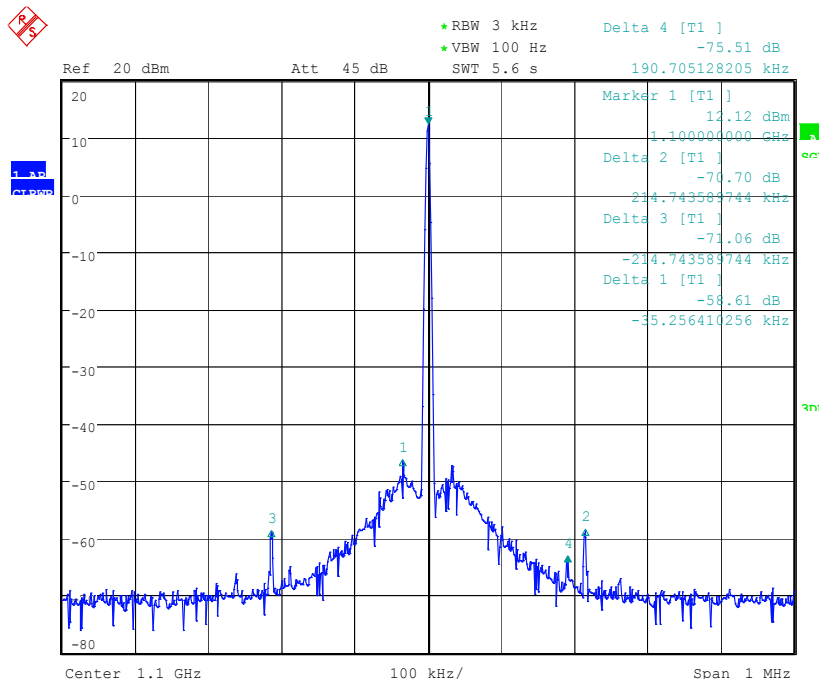
WIDE BANDWIDTH

1100 - 2500 MHz

HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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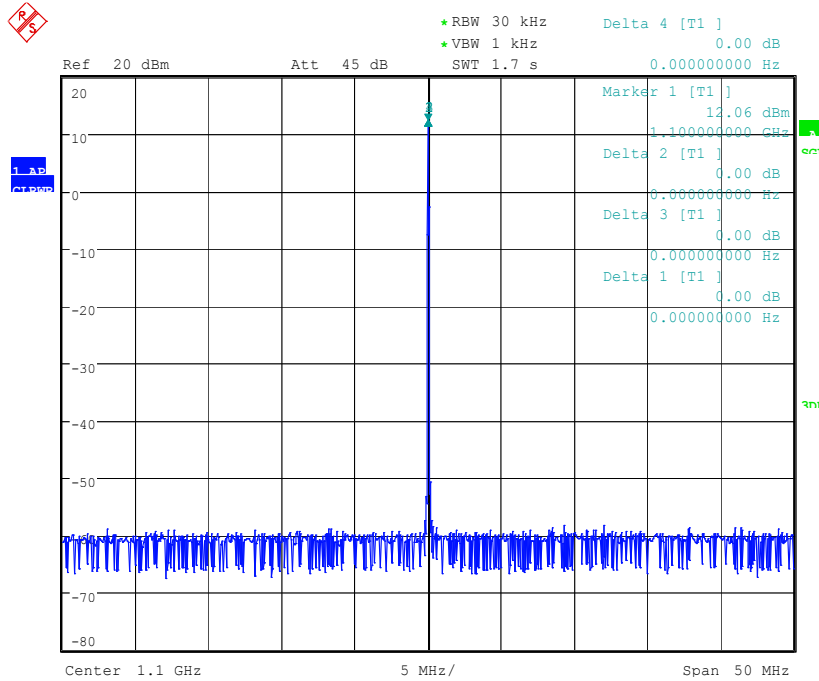


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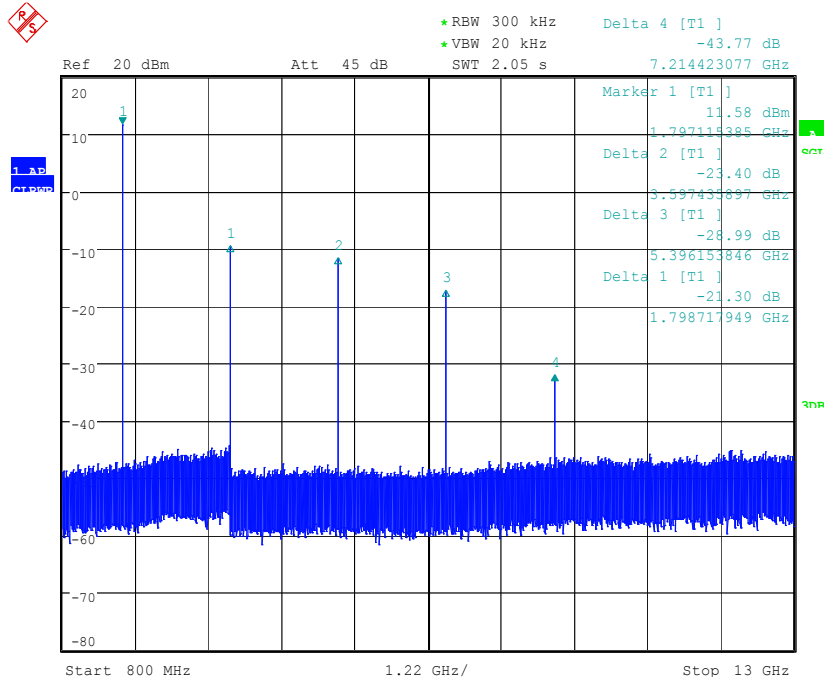


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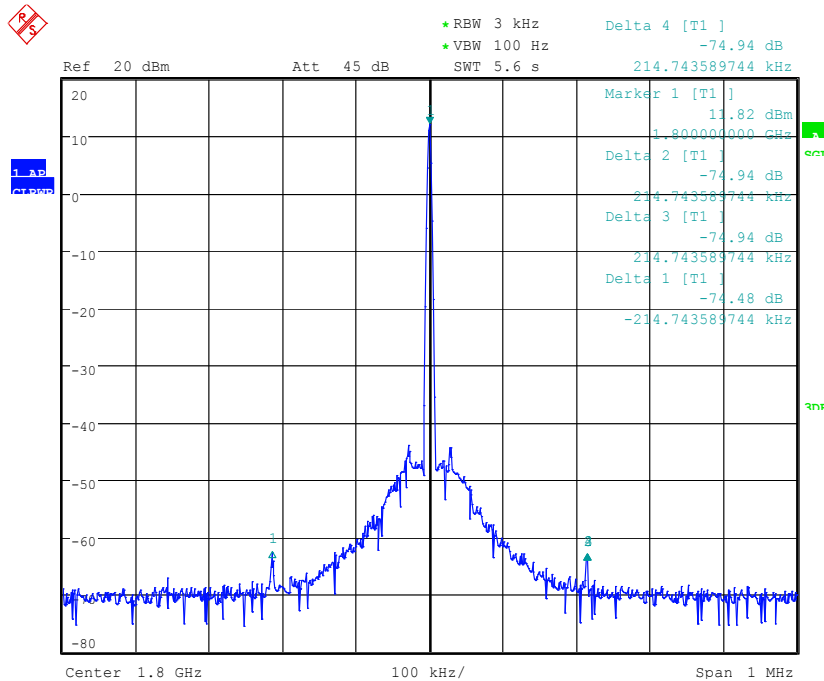
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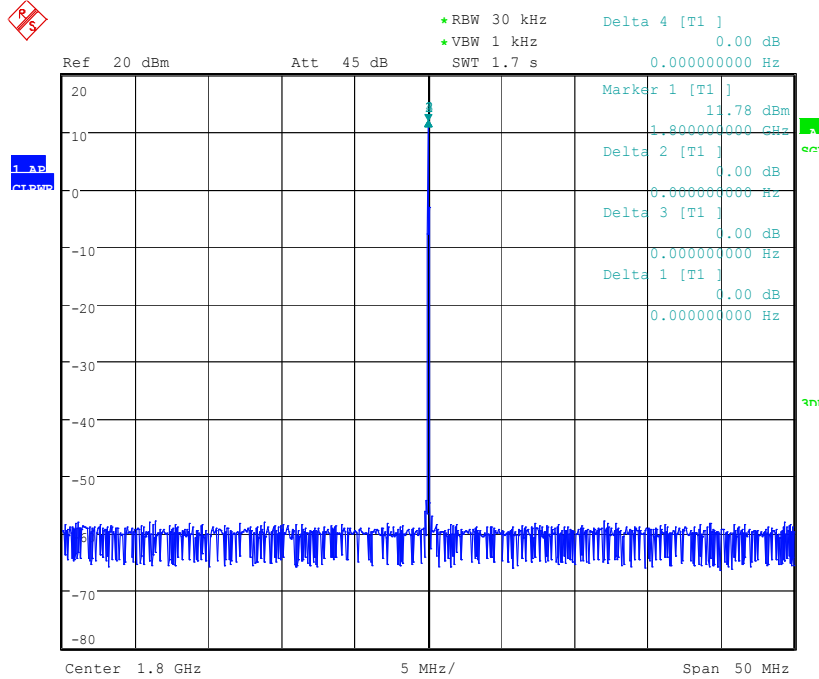


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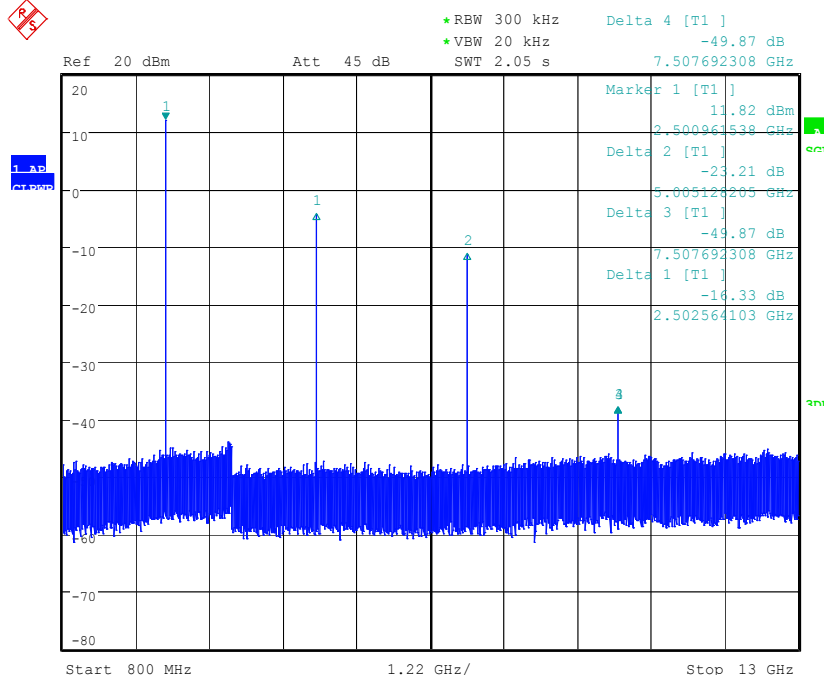


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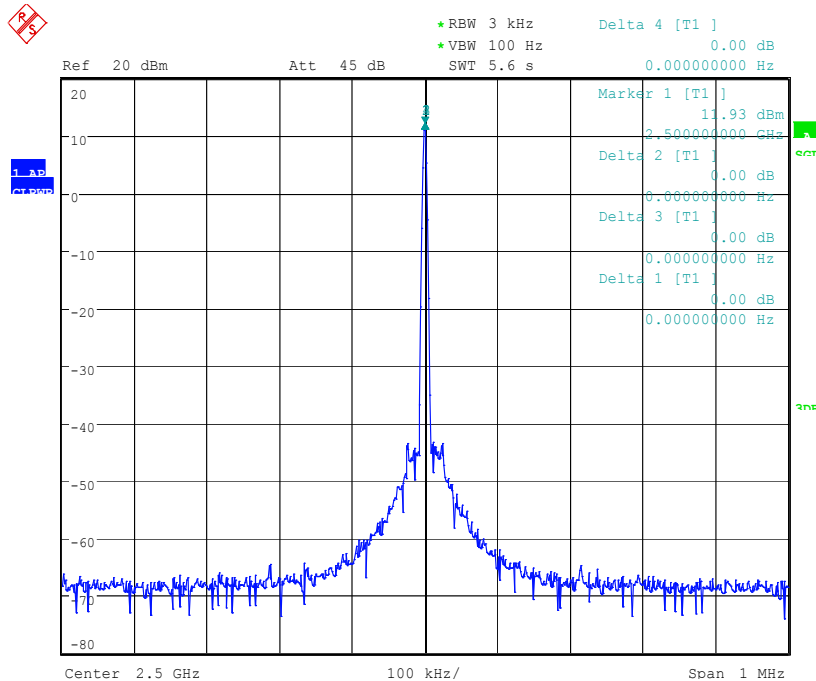
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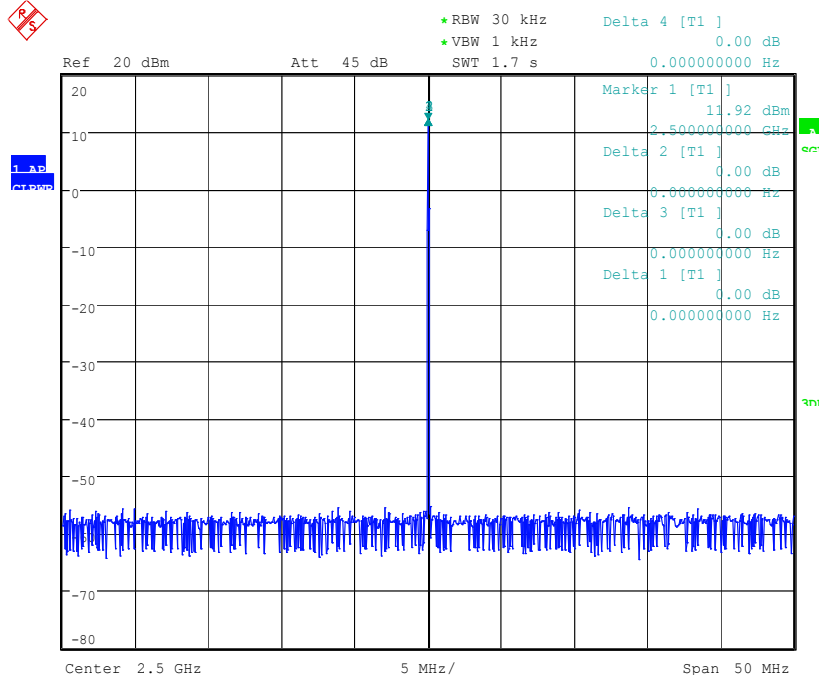


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