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## Introduction

Spartan®-3L Field-Programmable Gate Arrays (FPGAs) consume less static current than corresponding members of the standard Spartan-3 family. Spartan-3L devices provide the identical function, features, timing, and pinout of the original Spartan-3 family. Features include programmable I/Os, Configurable Logic Blocks (CLBs), RAM blocks, Digital Clock Managers (DCMs), and Multiplier blocks.

Another power-saving benefit of the Spartan-3L family beyond static current reduction is the Hibernate mode, which lowers device power consumption to the lowest possible levels. For new designs, consider the Spartan-3A family, which offers both Hibernate and Suspend power-saving modes.

The three-member Spartan-3L family ranges in density from one to four million system gates and offers as many as 633 I/Os. All devices are specified to meet the –4 speed grade over the commercial temperature range.

This data sheet explains how the Spartan-3L family is different from the Spartan-3 family. For specifications and other technical information not contained in this document, refer to the Spartan-3 data sheet ([DS099](#)).

## Features

- Power current reduction compared to Spartan-3 family:
  - Up to 60% less quiescent current
  - Up to 99% less quiescent current in Hibernate mode
- Low cost, low power logic solution for high-volume, consumer-oriented applications
  - Densities as high as 62,000 logic cells
- SelectIO™ signaling
  - Up to 633 I/O pins
  - Eighteen single-ended signal standards
  - Eight differential signal standards including LVDS and RSDS
  - Double Data Rate (DDR) support
- Logic resources
  - Abundant logic cells with shift register capability
  - Wide multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
  - Up to 1,728 Kbits of total block RAM
  - Up to 432 Kbits of total distributed RAM
- Digital Clock Manager (four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High-resolution phase shifting
- Eight global clock lines and abundant routing
- Pin-compatible with Spartan-3 FPGAs
- Pb-free packaging options
- Fully supported by Xilinx ISE® development system
  - Synthesis, mapping, placement, and routing
- MicroBlaze™ processor and other cores
- Power estimation using [XPower](#) tools

Table 1: Summary of Spartan-3L FPGA Attributes

| Device    | System Gates | Equivalent Logic Cells | CLB Array<br>(One CLB = Four Slices) |         |            | Distributed RAM bits <sup>(1)</sup> | Block RAM bits <sup>(1)</sup> | Dedicated Multipliers | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|-----------|--------------|------------------------|--------------------------------------|---------|------------|-------------------------------------|-------------------------------|-----------------------|------|------------------|--------------------------------|
|           |              |                        | Rows                                 | Columns | Total CLBs |                                     |                               |                       |      |                  |                                |
| XC3S1000L | 1M           | 17,280                 | 48                                   | 40      | 1,920      | 120K                                | 432K                          | 24                    | 4    | 333              | 149                            |
| XC3S1500L | 1.5M         | 29,952                 | 64                                   | 52      | 3,328      | 208K                                | 576K                          | 32                    | 4    | 487              | 221                            |
| XC3S4000L | 4M           | 62,208                 | 96                                   | 72      | 6,912      | 432K                                | 1,728K                        | 96                    | 4    | 633              | 300                            |

**Notes:**

1. By convention, one Kb is equivalent to 1,024 bits.

## Architectural Overview

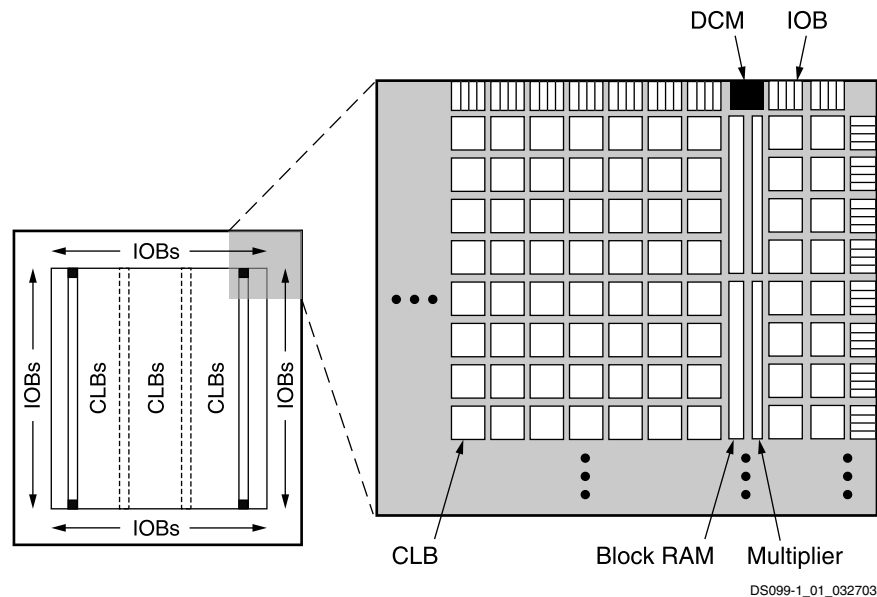
The Spartan-3L family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available, as shown in [Table 2](#). Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.

- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in [Figure 1](#). A ring of IOBs surrounds a regular array of CLBs. The XC3S1000L and XC3S1500L have two columns of block RAM. The XC3S4000L has four RAM columns. Each column is made up of several 18Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3L family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



### Notes:

1. The two additional block RAM columns of the XC3S4000L devices are shown with dashed lines.

Figure 1: Spartan-3L Family Architecture

## Configuration

Spartan-3L FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave

Serial and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

## I/O Capabilities

The SelectIO feature of Spartan-3L devices provides 18 single-ended standards and eight differential standards as listed in [Table 2](#). Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted

signal reflections. [Table 3](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 2: Signal Standards Supported by the Spartan-3L Family

| Standard Category   | Description                                | V <sub>CCO</sub> (V) | Class                | IOSTANDARD      | DCI Option |
|---------------------|--|----------------------|----------------------|-----------------|------------|
| <b>Single-Ended</b> |  |                      |                      |                 |            |
| GTL                 | Gunning Transceiver Logic                  | N/A                  | Terminated           | GTL             | Yes        |
|                     |  |                      | Plus                 | GTLP            | Yes        |
| HSTL                | High-Speed Transceiver Logic               | 1.5                  | I                    | HSTL_I          | Yes        |
|                     |  |                      | III                  | HSTL_III        | Yes        |
|                     |  | 1.8                  | I                    | HSTL_I_18       | Yes        |
|                     |  |                      | II                   | HSTL_II_18      | Yes        |
|                     |  |                      | III                  | HSTL_III_18     | Yes        |
| LVCMOS              | Low-Voltage CMOS                           | 1.2                  | N/A                  | LVCMOS12        | No         |
|                     |  | 1.5                  | N/A                  | LVCMOS15        | Yes        |
|                     |  | 1.8                  | N/A                  | LVCMOS18        | Yes        |
|                     |  | 2.5                  | N/A                  | LVCMOS25        | Yes        |
|                     |  | 3.3                  | N/A                  | LVCMOS33        | Yes        |
| LVTTTL              | Low-Voltage Transistor-Transistor Logic    | 3.3                  | N/A                  | LVTTTL          | No         |
| PCI                 | Peripheral Component Interconnect          | 3.0                  | 33 MHz               | PCI33_3         | No         |
| SSTL                | Stub Series Terminated Logic               | 1.8                  | N/A ( $\pm 6.7$ mA)  | SSTL18_I        | Yes        |
|                     |  |                      | N/A ( $\pm 13.4$ mA) | SSTL18_II       | No         |
|                     |  | 2.5                  | I                    | SSTL2_I         | Yes        |
|                     |  |                      | II                   | SSTL2_II        | Yes        |
| <b>Differential</b> |  |                      |                      |                 |            |
| HSTL                | Differential High-Speed Transceiver Logic  | 1.8                  | II                   | DIFF_HSTL_II_18 | Yes        |
| LDT (ULVDS)         | Lightning Data Transport (HyperTransport™) | 2.5                  | N/A                  | LDT_25          | No         |
| LVDS                | Low-Voltage Differential Signaling         |                      | Standard             | LVDS_25         | Yes        |
|                     |  |                      | Bus                  | BLVDS_25        | No         |
|                     |  | Extended Mode        | LVDSEXT_25           | Yes             |            |
| LVPECL              | Low-Voltage Positive Emitter-Coupled Logic | 2.5                  | N/A                  | LVPECL_25       | No         |
| RSDS                | Reduced-Swing Differential Signaling       | 2.5                  | N/A                  | RSDS_25         | No         |
| SSTL                | Differential Stub Series Terminated Logic  | 2.5                  | II                   | DIFF_SSTL2_II   | Yes        |

Table 3: User I/O and Differential (Diff) I/O Counts

| Device    | FT256<br>FTG256 |      | FG320<br>FGG320 |      | FG456<br>FGG456 |      | FG676<br>FGG676 |      | FG900<br>FGG900 |      |
|-----------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|
|           | User            | Diff | User            | Diff | User            | Diff | User            | Diff | User            | Diff |
| XC3S1000L | 173             | 76   | 221             | 100  | 333             | 149  | -               | -    | -               | -    |
| XC3S1500L | -               | -    | 221             | 100  | 333             | 149  | 487             | 221  | -               | -    |
| XC3S4000L | -               | -    | -               | -    | -               | -    | -               | -    | 633             | 300  |

**Notes:**

1. All Spartan-3L and Spartan-3 devices in the same package are pin-compatible.

## Package Marking

Figure 2 shows the package marking for Spartan-3L FPGAs. The markings on the Spartan-3L package are similar to those on the Spartan-3 package. The 'L' in the last line, indicating low power, distinguishes the Spartan-3L device.

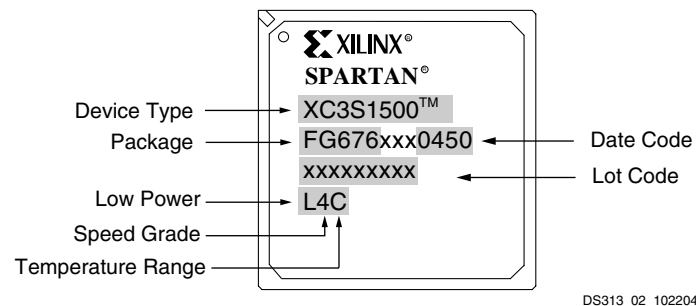
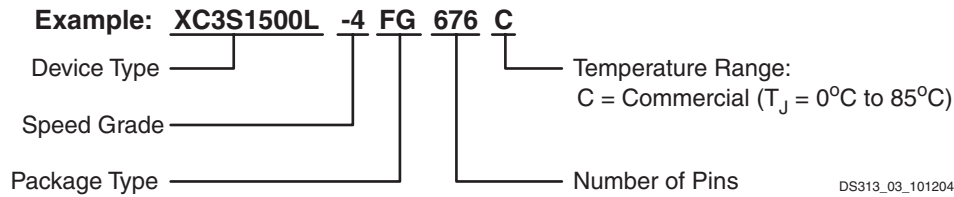


Figure 2: Spartan-3L Package Marking

## Ordering Information

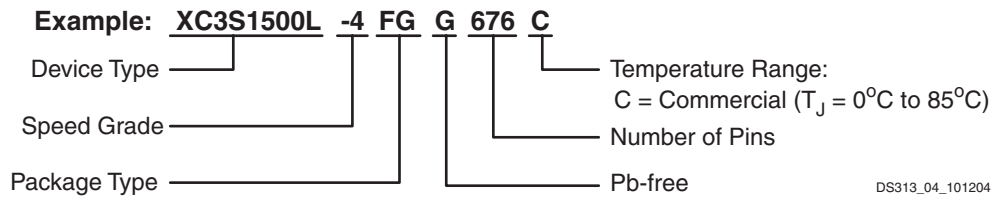
Spartan-3L FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code. Spartan-3L FPGAs are available in a single speed grade, -4, and are specified over the Commercial temperature range.

### Standard Packaging



### Pb-Free Packaging

For additional information on Pb-free packaging, see [XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages](#).



| Device    | Speed Grade | Package Type / Number of Pins |  | Temperature Range (T <sub>J</sub> ) |
|-----------|-------------|-------------------------------|--|-------------------------------------|
| XC3S1000L | -4          | FT(G)256                      | 256-ball Fine-Pitch Thin Ball Grid Array (FTBGA) | C Commercial (0°C to 85°C)          |
| XC3S1500L |             | FG(G)320                      | 320-ball Fine-Pitch Ball Grid Array (FBGA)       |                                     |
| XC3S4000L |             | FG(G)456                      | 456-ball Fine-Pitch Ball Grid Array (FBGA)       |                                     |
|           |             | FG(G)676                      | 676-ball Fine-Pitch Ball Grid Array (FBGA)       |                                     |
|           |             | FG(G)900                      | 900-ball Fine-Pitch Ball Grid Array (FBGA)       |                                     |

## Functional Description

The Spartan-3L FPGA family is identical to the Spartan-3 FPGA family with respect to device function. See the functional description in Module 2 of the Spartan-3 data sheet ([DS099](#)) for more information.

### Achieving Low Quiescent Current Levels

Because of their lower quiescent current specifications, Spartan-3L devices always consume less power than Spartan-3 devices.

For power-sensitive applications that must manage consumption over long periods with no FPGA activity, it is possible to achieve the quiescent current levels specified in [Table 4](#) of the **DC and Switching Characteristics** section on [page 9](#) by meeting the test conditions described below the table. The easiest way to realize these conditions is by pulling PROG\_B Low. This action puts all I/Os into a high-impedance state, ceases all internal switching, and converts the bitmap held in internal memory to all zeros. During and after the Low pulse on PROG\_B, disable the internal pull-up resistors on all I/Os by keeping HSWAP\_EN High. Reconfiguration is necessary before the FPGA can resume operation in the User mode.

As an alternate approach, when it is desirable to retain the programmed bitmap, do not assert PROG\_B. If all other test conditions are met (e.g., no internal switching, I/Os are off), quiescent current levels will be very close to or slightly above what is specified in [Table 4, page 9](#). In this case, make sure internal pull-up and pull-down resistors on all I/Os are disabled.

### Hibernate Mode

Hibernate mode starts with the approach described above. This takes power savings one step further by switching off power rails. This mode reduces quiescent power consump-

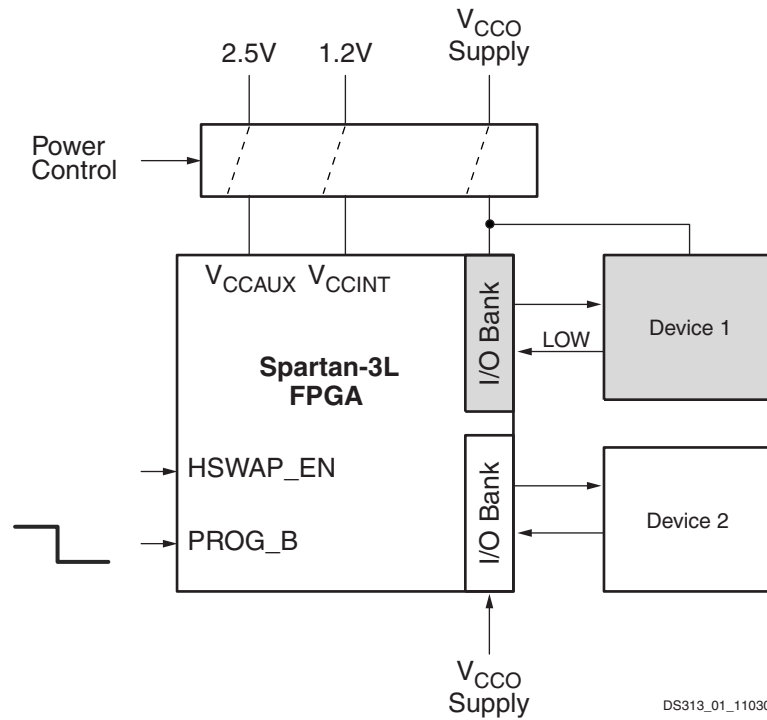
tion to the lowest possible level. The FPGA is put into the Hibernate mode by switching off the  $V_{CCINT}$  (core) and  $V_{CCAUX}$  (auxiliary) power supplies. Power is supplied to  $V_{CCO}$  lines throughout the hibernation period. [Figure 3, page 7](#) is a block diagram that shows how to put Spartan-3L FPGAs into the Hibernate mode.

During the Hibernation period, the  $V_{CCINT}$  and  $V_{CCAUX}$  rails are turned off. It is recommended that power FETs with low on resistance be used to perform the switching action. Configuration data is lost upon entering the Hibernate mode; therefore, reconfiguration is necessary after exiting the mode.

In general, it is safest to maintain  $V_{CCO}$  power for all banks throughout the Hibernation period. This keeps the power diodes inside the IOBs off when signals are applied to the pins. For each I/O, a power diode extends from the pin (the anode side) to the associated  $V_{CCO}$  rail (the cathode side). Power diodes are present on all signal-carrying pins all of the time. In Hibernate mode, the powered  $V_{CCO}$  rails account for little current, because the I/Os are in a high-impedance state.

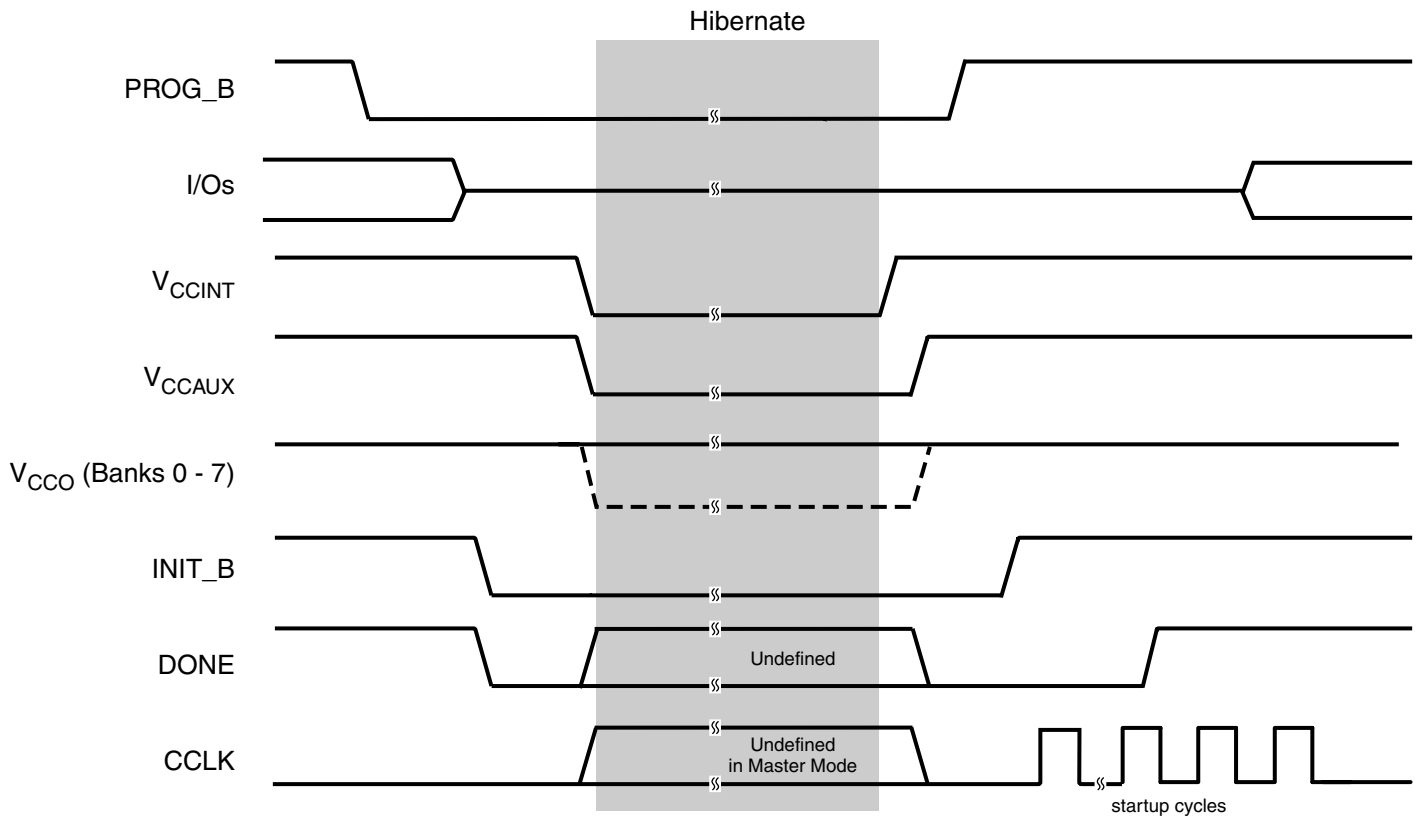
It is also possible to switch off the  $V_{CCO}$  rail for a particular bank. This action eliminates the  $V_{CCO}$  current for those banks—current on the order of a few milliamperes. There are two ways to achieve this. One way is to keep the voltage of all I/Os belonging to that bank under 0.5V. Another way is to disable signals coming from external devices (such as Device 1 in [Figure 3](#)).

Holding the PROG\_B input Low during the transition into Hibernation period keeps all output drivers in a high-impedance state. Release PROG\_B after re-applying power to the  $V_{CCINT}$  and  $V_{CCAUX}$  rails. See **Special Considerations, page 8** for recommended levels on Dedicated and Dual-Purpose pins.



DS313\_01\_110304

Figure 3: Hibernate Diagram



DS313\_05\_110304

**Notes:**

1. See **Special Considerations**, page 8 for recommended levels on Dedicated and Dual-Purpose pins.

Figure 4: Hibernate Mode Waveforms

Figure 4, page 7 shows the waveforms for entering and exiting the Hibernate mode.

*The steps for entering the Hibernate mode are as follows:*

1. Pull the PROG\_B pin Low to put all I/Os into a high-impedance state.
2. The FPGA drives the INIT\_B and DONE pins Low.
3. External switches are used to turn off the  $V_{CCINT}$  and  $V_{CCAUX}$  rails. This action resets the FPGA. As described above, it is possible to switch off  $V_{CCO}$  for a given bank in cases where the I/O pins of the associated bank are Low or disabled throughout the Hibernation period.
4. The FPGA is now in the Hibernate mode. As long as the FPGA is kept in this state, power consumption rests at the lowest possible level.

*The steps for exiting the Hibernate mode are as follows:*

1. Before FPGA initialization can begin, it is necessary to deassert PROG\_B to a High logic level. The rising transition must occur after turning all three power supplies back on.
2. Reapply power to all rails that were switched off. Apply power in any sequence.
3. After logic initialization, the FPGA releases the open-drain INIT\_B signal. Now that INIT\_B is High, reconfiguration can begin.
4. When configuration is complete, the FPGA enters the Startup phase, asserts DONE, and enables the I/Os, according to how the BitGen options are set.
5. The FPGA is now ready for user operation.

## Special Considerations

In the Hibernate mode, whenever one of the  $V_{CCO}$  rails is turned off, keep the voltage on the I/O pins of the associated bank below 0.5V. As an alternative, it is possible to disable any signals that an external device might apply to the bank's I/O pins. Voltages higher than 0.5V can turn on the power diodes. Keeping the diode off prevents "reverse current" from flowing into the  $V_{CCO}$  rail.

$V_{CCO}$  Bank 4 powers the Dual-Purpose inputs: INIT\_B, DIN, BUSY, and D0-D3.  $V_{CCO}$  Bank 5 powers the other Dual-Purpose inputs: RDWR\_B, CS\_B, and D4-D7. The  $V_{CCO}$  lines of Banks 0, 1, 4, and 5 power the Global Clock inputs GCLK0 - GCLK1, GCLK2 - GCLK3, GCLK4 - GCLK5, and GCLK6 - GCLK7, respectively. In the Hibernate mode, if any of these rails is turned off, do not apply voltages in excess of 0.5V to any of the associated Dual-Purpose pins. This measure keeps the power diodes off.

$V_{CCAUX}$  powers the Dedicated inputs: PROG\_B, HSWAP\_EN, M0-M2, CCLK (in Slave mode), TDI, TCK, and TMS. Once in the Hibernate mode, do not apply voltages in excess of 0.5V to any of these pins. In this case, keeping the power diode off prevents a "reverse current" from flowing into the  $V_{CCAUX}$  rail.

$V_{CCAUX}$  powers the Dedicated outputs: DONE, CCLK (in Master mode), and TDO. Once in the Hibernate mode, the states of these pins are undefined.

$V_{CCO}$  Bank 4 powers the Dual-Purpose outputs: BUSY/DOUT. Whenever  $V_{CCO}$  Bank 4 is turned off during the Hibernation period, the state of this pin is undefined.



## DC and Switching Characteristics

Like-density Spartan-3L and Spartan-3 devices share the same AC and DC specifications with the exceptions of reduced quiescent supply current consumption and specifications for the Hibernate mode. The reduced quiescent current levels are shown in [Table 4](#).

When in the Hibernate mode, Spartan-3L devices consume still less quiescent current, as shown in [Table 5](#). In this

mode, the FPGA only dissipates  $I_{CCOH}$  current. The  $V_{CCINT}$  and  $V_{CCAUX}$  rails are electrically disconnected and will not dissipate power.

For all other DC and AC specifications, refer to Module 3 of the Spartan-3 data sheet ([DS099](#)).

**Table 4: Quiescent Supply Current Characteristics**

| Symbol       | Description                          | Device    | Commercial |       | Units |
|--------------|--------------------------------------|-----------|------------|-------|-------|
|              |                                      |           | Typ        | Max   |       |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC3S1000L | 35.0       | 70.0  | mA    |
|              |                                      | XC3S1500L | 45.0       | 110.0 | mA    |
|              |                                      | XC3S4000L | 100.0      | 290.0 | mA    |
| $I_{CCOQ}$   | Quiescent $V_{CCO}$ supply current   | XC3S1000L | 2.0        | 7.5   | mA    |
|              |                                      | XC3S1500L | 2.5        | 8.5   | mA    |
|              |                                      | XC3S4000L | 3.5        | 11.0  | mA    |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC3S1000L | 20.0       | 35.0  | mA    |
|              |                                      | XC3S1500L | 35.0       | 50.0  | mA    |
|              |                                      | XC3S4000L | 55.0       | 80.0  | mA    |

**Notes:**

1. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices measured at ambient room temperature ( $T_A$  of 25°C at  $V_{CCINT} = 1.2V$ ,  $V_{CCO} = 3.3V$ , and  $V_{CCAUX} = 2.5V$ ). Maximum values are the production test limits measured for each device at  $T_J = 85°C$  and with  $V_{CCINT} = 1.26V$ ,  $V_{CCO} = 3.45V$ , and  $V_{CCAUX} = 2.625V$ . The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be slightly higher than the values in the table. Use the Web Power Tool or XPower for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator at <http://www.xilinx.com/power> provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx development software, takes a netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

**Table 5: Supply Current Characteristics for Hibernate Mode**

| Symbol     | Description  | Device    | Commercial |      | Units |
|------------|--|-----------|------------|------|-------|
|            |  |           | Typ        | Max  |       |
| $I_{CCOH}$ | Quiescent $V_{CCO}$ supply current in Hibernate mode | XC3S1000L | 2.0        | 7.5  | mA    |
|            |  | XC3S1500L | 2.5        | 8.5  | mA    |
|            |  | XC3S4000L | 3.5        | 11.0 | mA    |

**Notes:**

1. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with pull-up/pull-down resistors at all I/O pads disabled. For maximum  $I_{CCOH}$  values,  $T_J = 85°C$  with  $V_{CCO}$  (all banks) = 3.45V.  $V_{CCINT} = 0V$  and  $V_{CCAUX} = 0V$ . PROG\_B is Low.

## Pinout Descriptions

Spartan-3L and Spartan-3 devices that correspond in density and package have the same pinout. See the Pinout

Descriptions in Module 4 of the Spartan-3 data sheet ([DS099](#)) for more information.

## Related Documentation

This data sheet only specifies how the Spartan-3L family differs from the Spartan-3 family. Because the two families are identical with respect to function, features, timing, and

pinout, please consult the Spartan-3 FPGA family data sheet for all other information.

[DS099](#), *Spartan-3 FPGA Family Data Sheet*

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## Revision History

The following table shows the revision history for this document.

| Date     | Version | Revision  |
|----------|---------|---|
| 11/03/04 | 1.0     | Initial Xilinx release.   |
| 09/15/04 | 1.1     | Added the SSTL18_II, DIFF_SSTL2_II, and DIFF_HSTL_II_18 standards ( <a href="#">Table 2</a> ). Described option for retaining the bitmap in <b>Achieving Low Quiescent Current Levels</b> , <a href="#">page 6</a> . Removed power sequence restriction for Hibernate mode ( <a href="#">page 8</a> ). Added or updated quiescent current specifications ( <a href="#">Table 4</a> and <a href="#">Table 5</a> ). Updated the worst-case $T_J$ condition in footnote 1 of <a href="#">Table 4</a> . Changed document status to "Preliminary". |
| 04/18/08 | 1.2     | Added reference to <a href="#">Discontinuation Notice</a> . Updated links. Removed Preliminary from document status.  |