

Module 1: Introduction and Ordering Information

DS529-1 (v1.4.1) July 10, 2007

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- Features
- Architectural and Configuration Overview
- General I/O Capabilities
- Production Status
- Supported Packages and Package Marking
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Module 2: Functional Description

DS529-2 (v1.4) July 10, 2007

The functionality of the Spartan™-3A FPGA family is described in the following documents.

- [UG331: Spartan-3 Generation FPGA User Guide](#)
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 - Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
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 - Embedded Multiplier Blocks
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 - ISE™ Design Tools and IP Cores
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 - Master Serial Mode using Platform Flash PROM
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 - Master BPI Mode using Commodity Parallel Flash
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
- ISE iMPACT Programming Examples
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DS529-3 (v1.5) July 10, 2007

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DS529-4 (v1.5) July 10, 2007

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www.xilinx.com/spartan3a

Spartan-3A FPGA	Status
XC3S50A	PRODUCTION
XC3S200A	PRODUCTION
XC3S400A	PRODUCTION
XC3S700A	PRODUCTION
XC3S1400A	PRODUCTION

Introduction

The Spartan™-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in [Table 1](#).

The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families by increasing the amount of I/O per logic, significantly reducing the cost per I/O. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
 - ◆ Up to 502 I/O pins or 227 differential signal pairs
 - ◆ LVCMOS, LVTTTL, HSTL, and SSTL single-ended I/O
 - ◆ 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling

- ◆ Selectable output drive, up to 24 mA per pin
- ◆ QUIETIO standard reduces I/O switching noise
- ◆ Full 3.3V ± 10% compatibility and hot swap compliance
- ◆ 622+ Mb/s data transfer rate per differential I/O
- ◆ LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
- ◆ Enhanced Double Data Rate (DDR) support
- ◆ DDR/DDR2 SDRAM support up to 333 Mb/s
- ◆ Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
 - ◆ Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
 - ◆ Efficient wide multiplexers, wide logic
 - ◆ Fast look-ahead carry logic
 - ◆ Enhanced 18 x 18 multipliers with optional pipeline
 - ◆ IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
 - ◆ Up to 576 Kbits of fast block RAM with byte write enables for processor applications
 - ◆ Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
 - ◆ Clock skew elimination (delay locked loop)
 - ◆ Frequency synthesis, multiplication, division
 - ◆ High-resolution phase shifting
 - ◆ Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
 - ◆ Low-cost, space-saving SPI serial Flash PROM
 - ◆ x8 or x8/x16 parallel NOR Flash PROM
 - ◆ Low-cost Xilinx [Platform Flash](#) with JTAG
 - ◆ Unique Device DNA identifier for design authentication
 - ◆ Load multiple bitstreams under FPGA control
- Complete Xilinx [ISE™](#) and [WebPACK™](#) development system software support plus [Spartan-3A Starter Kit](#)
- [MicroBlaze™](#) and [PicoBlaze™](#) embedded processor cores
- Low-cost QFP and BGA packaging, Pb-free options
 - ◆ Common footprints support easy density migration
 - ◆ Compatible with select [Spartan-3AN](#) nonvolatile FPGAs
 - ◆ Compatible with higher density [Spartan-3A DSP](#) FPGAs

Table 1: Summary of Spartan-3A FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits ⁽¹⁾	Block RAM bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Architectural Overview

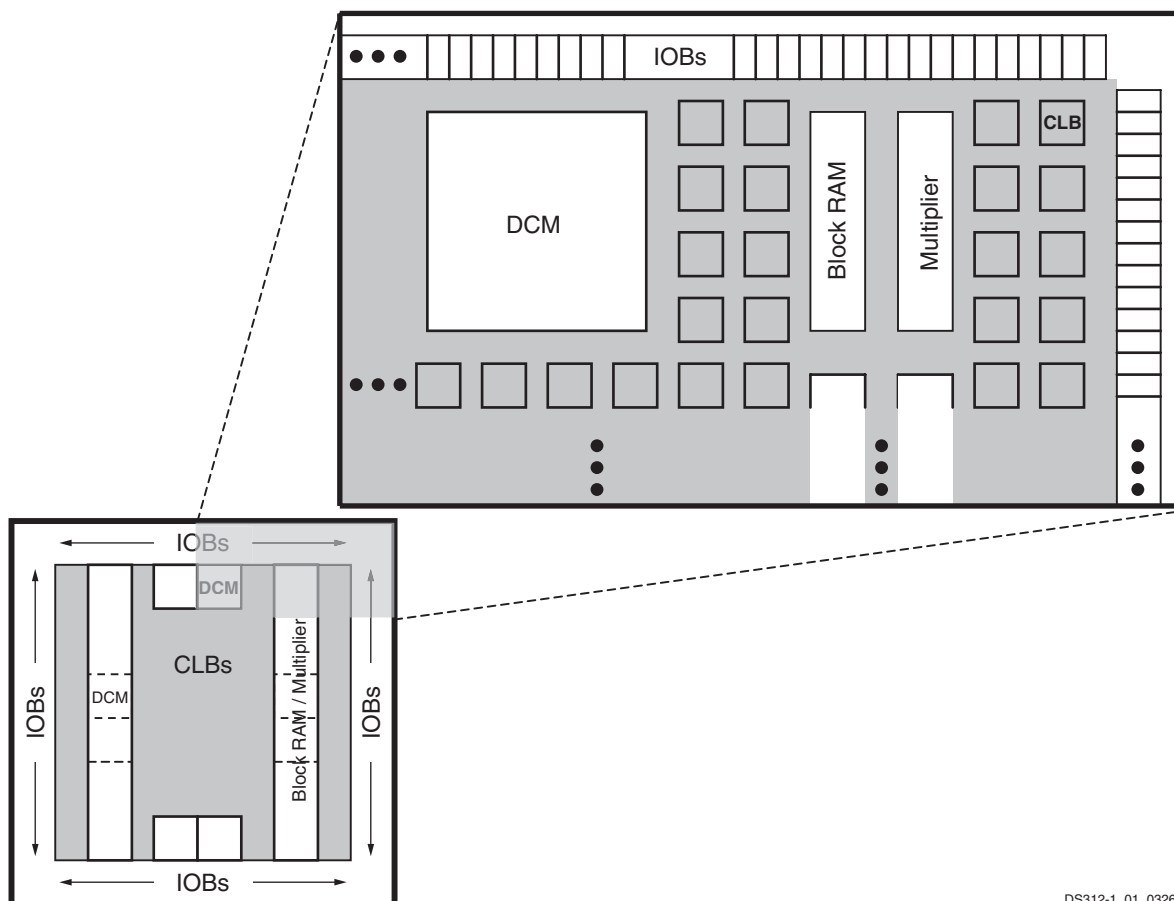
The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.

- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in [Figure 1](#). A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



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Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: Spartan-3A Family Architecture

Configuration

Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a [Xilinx Platform Flash PROM](#)
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

Table 2: Available User I/Os and Differential (Diff) I/O Pairs

Device	TQ144 TQG144		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484		FG676 FGG676	
	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50A	108 (7)	50 (24)	144 (32)	64 (32)	-	-	-	-	-	-	-	-
XC3S200A	-	-	195 (35)	90 (50)	248 (56)	112 (64)	-	-	-	-	-	-
XC3S400A	-	-	195 (35)	90 (50)	251 (59)	112 (64)	311 (63)	142 (78)	-	-	-	-
XC3S700A	-	-	-	-	-	-	311 (63)	142 (78)	372 (84)	165 (93)	-	-
XC3S1400A	-	-	-	-	-	-	-	-	375 (87)	165 (93)	502 (94)	227 (131)

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *italics* indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

I/O Capabilities

The Spartan-3A FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 2](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in [Table 2](#).

Spartan-3A FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3A FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating

a production configuration bitstream. Later versions are also supported.

Table 3: Spartan-3A FPGA Family Production Status (Production Speed File)

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (-4)	High-Performance (-5)	Standard (-4)
Part Number	XC3S50A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S200A	Production (v1.35)	Production (v1.35)	Production (v1.35)
	XC3S400A	Production (v1.36)	Production (v1.36)	Production (v1.36)
	XC3S700A	Production (v1.34)	Production (v1.35)	Production (v1.34)
	XC3S1400A	Production (v1.34)	Production (v1.35)	Production (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

Use the seven digits of the Lot Code to access additional information for a specific device using the Xilinx web-based [Genealogy Viewer](#).

The “5C” and “4I” Speed Grade/Temperature Range part combinations may be dual marked as “5C/4I”.

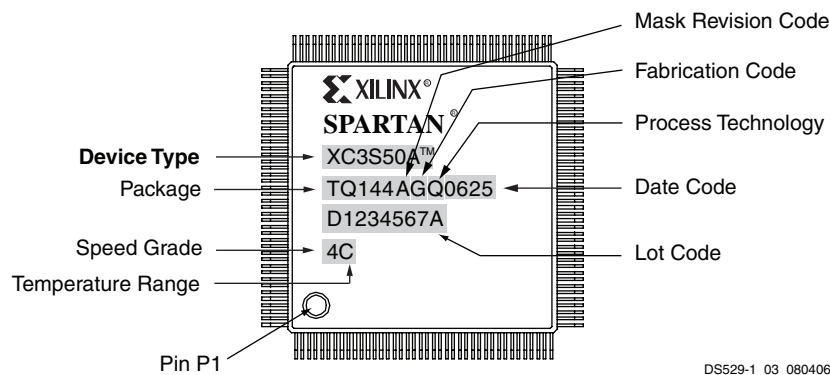


Figure 2: Spartan-3A QFP Package Marking Example

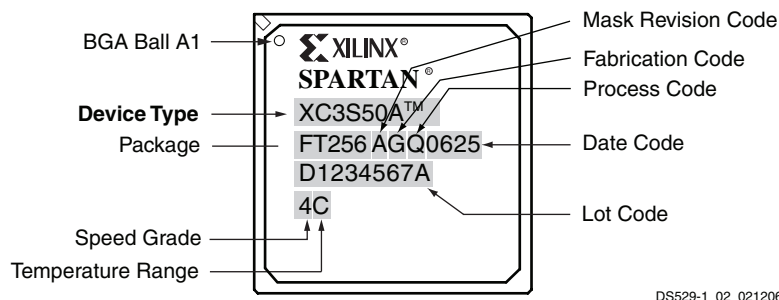
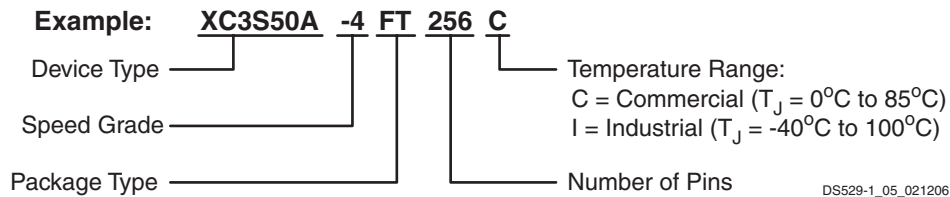


Figure 3: Spartan-3A BGA Package Marking Example

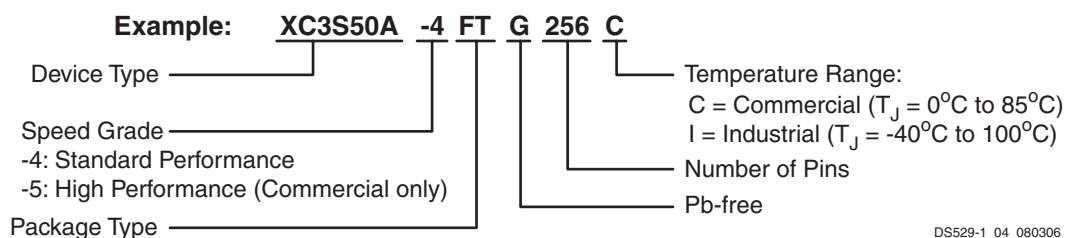
Ordering Information

Spartan-3A FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
	Speed Grade	Performance	Package Type	Description	Temp Range	Temp Range
XC3S50A	-4	Standard Performance	TQ(G)144	144-pin Thin Quad Flat Pack (TQFP)	C	Commercial (0°C to 85°C)
XC3S200A	-5	High Performance	FT(G)256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	I	Industrial (-40°C to 100°C)
XC3S400A			FG(G)320	320-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S700A			FG(G)400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400A			FG(G)484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG(G)676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:

- The -5 speed grade is exclusively available in the Commercial temperature range.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Updated maximum differential I/O count for XC3S50A in Table 1 . Updated differential input-only pin counts in Table 2 .
03/16/07	1.2	Minor formatting updates.
04/23/07	1.3	Added " Production Status " section.
05/08/07	1.4	Updated XC3S400A to Production.
7/10/07	1.4.1	Minor updates.

Introduction

The functionality of the Spartan™-3A FPGA family is described in the following documents. The topics covered in each guide is listed below.

- **UG331: Spartan-3 Generation FPGA User Guide**
<http://www.xilinx.com/bvdocs/userguides/ug331.pdf>
 - ◆ Clocking Resources
 - ◆ Digital Clock Managers (DCMs)
 - ◆ Block RAM
 - ◆ Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
 - ◆ I/O Resources
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 - ◆ Pin Types and Package Overview
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 - ◆ Powering FPGAs
 - ◆ Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
<http://www.xilinx.com/bvdocs/userguides/ug332.pdf>
 - ◆ Configuration Overview
 - Configuration Pins and Behavior
 - Bitstream Sizes

- ◆ Detailed Descriptions by Mode
 - Master Serial Mode using Xilinx Platform Flash PROM
 - Master SPI Mode using Commodity SPI Serial Flash PROM
 - Master BPI Mode using Commodity Parallel NOR Flash PROM
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
- ◆ ISE iMPACT Programming Examples
- ◆ MultiBoot Reconfiguration
- ◆ Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=-1212247

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
<http://www.xilinx.com/s3astarter>
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
<http://www.xilinx.com/bvdocs/userguides/ug334.pdf>

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Related Product Families

The Spartan-3AN nonvolatile FPGA family is architecturally identical to the Spartan-3A FPGA family, except that it has in-system flash memory and is offered in select pin-compatible package options.

- **DS557: Spartan-3AN FPGA Family Data Sheet**
www.xilinx.com/bvdocs/publications/ds557.pdf

The compatible Spartan-3A DSP FPGA family replaces the 18-bit multiplier with the DSP48A block, while also increasing the block RAM capability and quantity. The two members of the Spartan-3A DSP FPGA family extend the Spartan-3A density range up to 37,440 and 53,712 logic cells.

- **DS610: Spartan-3A DSP FPGA Family Data Sheet**
www.xilinx.com/bvdocs/publications/ds610.pdf
- **UG431: XtremeDSP DSP48A for Spartan-3A DSP FPGAs**
www.xilinx.com/bvdocs/userguides/ug431.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status.
03/16/07	1.2	Added cross-reference to nonvolatile Spartan-3AN FPGA family.
04/23/07	1.3	Added cross-reference to compatible Spartan-3A DSP family.
07/10/07	1.4	Updated Starter Kit reference to new UG334.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan™-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under [Table 4](#): Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		-0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		-0.5	3.75	V
V_{CCO}	Output driver supply voltage		-0.5	3.75	V
V_{REF}	Input reference voltage		-0.5	$V_{CCO} + 0.5$	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	-0.95	4.6	V
	Voltage applied to all Dedicated pins		-0.5	4.6	V
V_{ESD}	Electrostatic Discharge Voltage	Human body model	-	± 2000	V
		Charged device model	-	± 500	V
		Machine model	-	± 200	V
T_J	Junction temperature		-	125	°C
T_{STG}	Storage temperature		-65	150	°C

Notes:

- For soldering guidelines, see [UG112: Device Packaging and Thermal Characteristics](#) and [XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages](#).

Power Supply Specifications

Table 5: Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.8	2.0	V

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see [UG331](#) chapter "Powering Spartan-3 Generation FPGAs" for more information).
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see [UG331](#) chapter "Powering Spartan-3 Generation FPGAs" for more information).
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

General Recommended Operating Conditions

Table 8: General Recommended Operating Conditions

Symbol	Description	Min	Nominal	Max	Units	
T_J	Junction temperature	Commercial	0	–	85	°C
		Industrial	–40	–	100	°C
V_{CCINT}	Internal supply voltage	1.140	1.200	1.260	V	
$V_{CCO}^{(1)}$	Output driver supply voltage	1.100	–	3.600	V	
V_{CCAUX}	Auxiliary supply voltage	$V_{CCAUX} = 2.5$	2.250	2.500	2.750	V
		$V_{CCAUX} = 3.3$	3.000	3.300	3.600	V
T_{IN}	Input signal transition time ⁽²⁾	–	–	500	ns	

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 11 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 13 lists that specific to the differential standards.
2. Measured between 10% and 90% V_{CCO} .

General DC Characteristics for I/O Pins

Table 9: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered	Driver is in a high-impedance state, $V_{IN} = 0V$ or V_{CCO} max, sample-tested		-10	-	+10	μA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		-10	-	+10	μA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add $I_{HS} + I_{RPU}$			μA
$I_{RPU}^{(2)}$	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by V_{CCAUX} .	$V_{IN} = GND$	V_{CCO} or $V_{CCAUX} = 3.0V$ to $3.6V$	-151	-315	-710	μA
			V_{CCO} or $V_{CCAUX} = 2.3V$ to $2.7V$	-82	-182	-437	μA
			$V_{CCO} = 1.7V$ to $1.9V$	-36	-88	-226	μA
			$V_{CCO} = 1.4V$ to $1.6V$	-22	-56	-148	μA
			$V_{CCO} = 1.14V$ to $1.26V$	-11	-31	-83	μA
$R_{PU}^{(2)}$	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	$V_{IN} = GND$	$V_{CCO} = 3.0V$ to $3.6V$	5.1	11.4	23.9	$k\Omega$
			$V_{CCO} = 2.3V$ to $2.7V$	6.2	14.8	33.1	$k\Omega$
			$V_{CCO} = 1.7V$ to $1.9V$	8.4	21.6	52.6	$k\Omega$
			$V_{CCO} = 1.4V$ to $1.6V$	10.8	28.4	74.0	$k\Omega$
			$V_{CCO} = 1.14V$ to $1.26V$	15.3	41.1	119.4	$k\Omega$
$I_{RPD}^{(2)}$	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	$V_{CCAUX} = 3.0V$ to $3.6V$	167	346	659	μA
			$V_{CCAUX} = 2.25V$ to $2.75V$	100	225	457	μA
$R_{PD}^{(2)}$	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{CCAUX} = 3.0V$ to $3.6V$	$V_{IN} = 3.0V$ to $3.6V$	5.5	10.4	20.8	$k\Omega$
			$V_{IN} = 2.3V$ to $2.7V$	4.1	7.8	15.7	$k\Omega$
			$V_{IN} = 1.7V$ to $1.9V$	3.0	5.7	11.1	$k\Omega$
			$V_{IN} = 1.4V$ to $1.6V$	2.7	5.1	9.6	$k\Omega$
			$V_{IN} = 1.14V$ to $1.26V$	2.4	4.5	8.1	$k\Omega$
		$V_{CCAUX} = 2.25V$ to $2.75V$	$V_{IN} = 3.0V$ to $3.6V$	7.9	16.0	35.0	$k\Omega$
			$V_{IN} = 2.3V$ to $2.7V$	5.9	12.0	26.3	$k\Omega$
			$V_{IN} = 1.7V$ to $1.9V$	4.2	8.5	18.6	$k\Omega$
			$V_{IN} = 1.4V$ to $1.6V$	3.6	7.2	15.7	$k\Omega$
			$V_{IN} = 1.14V$ to $1.26V$	3.0	6.0	12.5	$k\Omega$
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		-10	-	+10	μA
C_{IN}	Input capacitance	-		3	-	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	$V_{CCO} = 3.3V \pm 10\%$	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		$V_{CCO} = 2.5V \pm 10\%$	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	-	Ω

Notes:

- The numbers in this table are based on the conditions set forth in Table 8.
- This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Quiescent Current Requirements

Table 10: Quiescent Supply Current Characteristics

Symbol	Description	Device	Typical ⁽²⁾	Commercial Maximum ⁽²⁾	Industrial Maximum ⁽²⁾	Units
I _{CCINTQ}	Quiescent V _{CCINT} supply current	XC3S50A	3	20	30	mA
		XC3S200A	8	50	70	mA
		XC3S400A	15	85	125	mA
		XC3S700A	25	120	185	mA
		XC3S1400A	30	220	310	mA
I _{CCOQ}	Quiescent V _{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC3S50A	4.5	8	10	mA
		XC3S200A	8	12	15	mA
		XC3S400A	12	18	24	mA
		XC3S700A	14	28	34	mA
		XC3S1400A	18	50	58	mA

Notes:

- The numbers in this table are based on the conditions set forth in [Table 8](#).
- Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at ambient room temperature (T_A of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
- There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The [Spartan-3A FPGA XPower Estimator](#) provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
- The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
- For information on the power-saving Suspend mode, see [XAPP480: Using Suspend Mode in Spartan-3 Generation FPGAs](#). Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 11: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	V_{CCO} for Drivers ⁽²⁾			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVC MOS33 ⁽⁴⁾	3.0	3.3	3.6				0.8	2.0
LVC MOS25 ^(4,5)	2.3	2.5	2.7				0.7	1.7
LVC MOS18 ⁽⁴⁾	1.65	1.8	1.95				0.38	0.8
LVC MOS15 ⁽⁴⁾	1.4	1.5	1.6				0.38	0.8
LVC MOS12 ⁽⁴⁾	1.1	1.2	1.3				0.38	0.8
PCI33_3	3.0	3.3	3.6				$0.3 \cdot V_{CCO}$	$0.5 \cdot V_{CCO}$
PCI66_3	3.0	3.3	3.6				$0.3 \cdot V_{CCO}$	$0.5 \cdot V_{CCO}$
PCIX	3.0	3.3	3.6				$0.35 \cdot V_{CCO}$	$0.5 \cdot V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

- Descriptions of the symbols used in this table are as follows:
 V_{CCO} – the supply voltage for output drivers
 V_{REF} – the reference voltage for setting the input switching threshold
 V_{IL} – the input voltage that indicates a Low logic level
 V_{IH} – the input voltage that indicates a High logic level
- In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVC MOS25 inputs when $V_{CCAUX} = 3.3V$ range and for PCI I/O standards.
- For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 4.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVC MOS25 or LVC MOS33 standard depending on V_{CCAUX} . The Dual-Purpose configuration pins use the LVC MOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.

Table 12: DC Characteristics of User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	Test Conditions			Logic Level Characteristics	
	I _{OL} (mA)	I _{OH} (mA)	V _{OL} Max (V)	V _{OH} Min (V)	
LVTTTL ⁽³⁾	2	2	-2	0.4	2.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
	24	24	-24		
LVCMOS33 ⁽³⁾	2	2	-2	0.4	V _{CCO} - 0.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
	24 ⁽⁴⁾	24	-24		
LVCMOS25 ⁽³⁾	2	2	-2	0.4	V _{CCO} - 0.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16 ⁽⁴⁾	16	-16		
	24 ⁽⁴⁾	24	-24		
LVCMOS18 ⁽³⁾	2	2	-2	0.45	V _{CCO} - 0.45
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12 ⁽⁴⁾	12	-12		
	16 ⁽⁴⁾	16	-16		
LVCMOS15 ⁽³⁾	2	2	-2	0.25 • V _{CCO}	0.75 • V _{CCO}
	4	4	-4		
	6	6	-6		
	8 ⁽⁴⁾	8	-8		
	12 ⁽⁴⁾	12	-12		
LVCMOS12 ⁽³⁾	2	2	-2	0.4	V _{CCO} - 0.4
	4 ⁽⁴⁾	4	-4		
	6 ⁽⁴⁾	6	-6		

Table 12: DC Characteristics of User I/Os Using Single-Ended Standards (Continued)

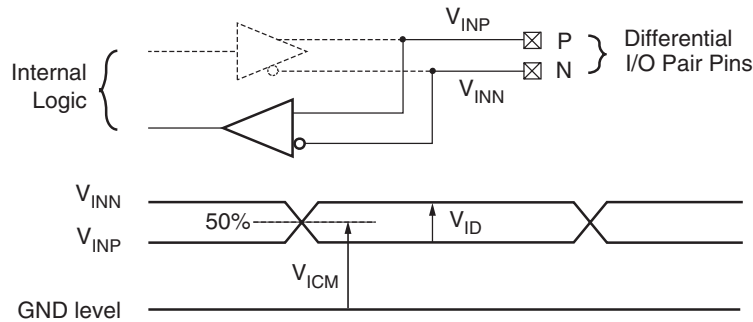
IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I _{OL} (mA)	I _{OH} (mA)	V _{OL} Max (V)	V _{OH} Min (V)
PCI33_3 ⁽⁵⁾	1.5	-0.5	10% V _{CCO}	90% V _{CCO}
PCI66_3 ⁽⁵⁾	1.5	-0.5	10% V _{CCO}	90% V _{CCO}
PCIX	1.5	-0.5	10% V _{CCO}	90% V _{CCO}
HSTL_I ⁽⁴⁾	8	-8	0.4	V _{CCO} - 0.4
HSTL_III ⁽⁴⁾	24	-8	0.4	V _{CCO} - 0.4
HSTL_I_18	8	-8	0.4	V _{CCO} - 0.4
HSTL_II_18 ⁽⁴⁾	16	-16	0.4	V _{CCO} - 0.4
HSTL_III_18	24	-8	0.4	V _{CCO} - 0.4
SSTL18_I	6.7	-6.7	V _{TT} - 0.475	V _{TT} + 0.475
SSTL18_II ⁽⁴⁾	13.4	-13.4	V _{TT} - 0.475	V _{TT} + 0.475
SSTL2_I	8.1	-8.1	V _{TT} - 0.61	V _{TT} + 0.61
SSTL2_II ⁽⁴⁾	16.2	-16.2	V _{TT} - 0.80	V _{TT} + 0.80
SSTL3_I	8	-8	V _{TT} - 0.6	V _{TT} + 0.6
SSTL3_II	16	-16	V _{TT} - 0.8	V _{TT} + 0.8

Notes:

- The numbers in this table are based on the conditions set forth in [Table 8](#) and [Table 11](#).
- Descriptions of the symbols used in this table are as follows:
 I_{OL} — the output current condition under which V_{OL} is tested
 I_{OH} — the output current condition under which V_{OH} is tested
 V_{OL} — the output voltage that indicates a Low logic level
 V_{OH} — the output voltage that indicates a High logic level
 V_{IL} — the input voltage that indicates a Low logic level
 V_{IH} — the input voltage that indicates a High logic level
 V_{CCO} — the supply voltage for output drivers
 V_{REF} — the reference voltage for setting the input switching threshold
 V_{TT} — the voltage applied to a resistor termination
- For the LVCMOS and LVTTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
- These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in [UG331](#).
- Tested according to the relevant PCI specifications.

Differential I/O Standards

Differential Input Pairs



$$V_{ICM} = \text{Input common mode voltage} = \frac{V_{INP} + V_{INN}}{2}$$

$$V_{ID} = \text{Differential input voltage} = |V_{INP} - V_{INN}| \quad \text{DS529-3_10_012907}$$

Figure 4: Differential Input Voltages

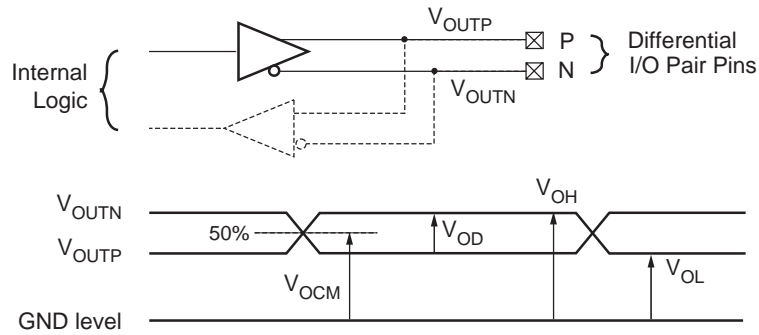
Table 13: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V_{CCO} for Drivers ⁽¹⁾			V_{ID}			V_{ICM} ⁽²⁾		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25 ⁽³⁾	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33 ⁽³⁾	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25 ⁽⁴⁾	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25 ⁽³⁾	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33 ⁽³⁾	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25 ⁽⁵⁾	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33 ⁽⁵⁾	Inputs Only			100	800	1000	0.3	1.2	2.8 ⁽⁶⁾
RSDS_25 ⁽³⁾	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33 ⁽³⁾	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33 ^(3, 4, 7)	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25 ⁽³⁾	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33 ⁽³⁾	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18 ⁽⁸⁾	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68	–	0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II ⁽⁸⁾	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II ⁽⁸⁾	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX} .
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in [UG331](#).
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. Requires $V_{CCAUX}=3.3V \pm 10\%$.
6. LVPECL_33 maximum $V_{ICM} = V_{CCAUX} - (V_{ID} / 2)$
7. Requires $V_{CCAUX} = 3.3V \pm 10\%$ for inputs. $(V_{CCAUX} - 300 \text{ mV}) \leq V_{ICM} \leq (V_{ICM} - 37 \text{ mV})$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in [UG331](#).
9. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in [Table 11](#). Other differential standards do not use V_{REF} .

Differential Output Pairs



$$V_{OCM} = \text{Output common mode voltage} = \frac{V_{OUTP} + V_{OUTN}}{2}$$

$$V_{OD} = \text{Output differential voltage} = |V_{OUTP} - V_{OUTN}|$$

V_{OH} = Output voltage indicating a High logic level

V_{OL} = Output voltage indicating a Low logic level DS529-3_11_012907

Figure 5: Differential Output Voltages

Table 14: DC Characteristics of User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	$V_{CCO} - 0.405$	–	$V_{CCO} - 0.190$	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_I	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	$V_{TT} + 0.475$	$V_{TT} - 0.475$
DIFF_SSTL18_II	–	–	–	–	–	–	$V_{TT} + 0.475$	$V_{TT} - 0.475$
DIFF_SSTL2_I	–	–	–	–	–	–	$V_{TT} + 0.61$	$V_{TT} - 0.61$
DIFF_SSTL2_II	–	–	–	–	–	–	$V_{TT} + 0.81$	$V_{TT} - 0.81$
DIFF_SSTL3_I	–	–	–	–	–	–	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL3_II	–	–	–	–	–	–	$V_{TT} + 0.8$	$V_{TT} - 0.8$

Notes:

- The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
- See "External Termination Requirements for Differential I/O," page 20.
- Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
- At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when $V_{CCO}=2.5V$, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when $V_{CCO} = 3.3V$

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

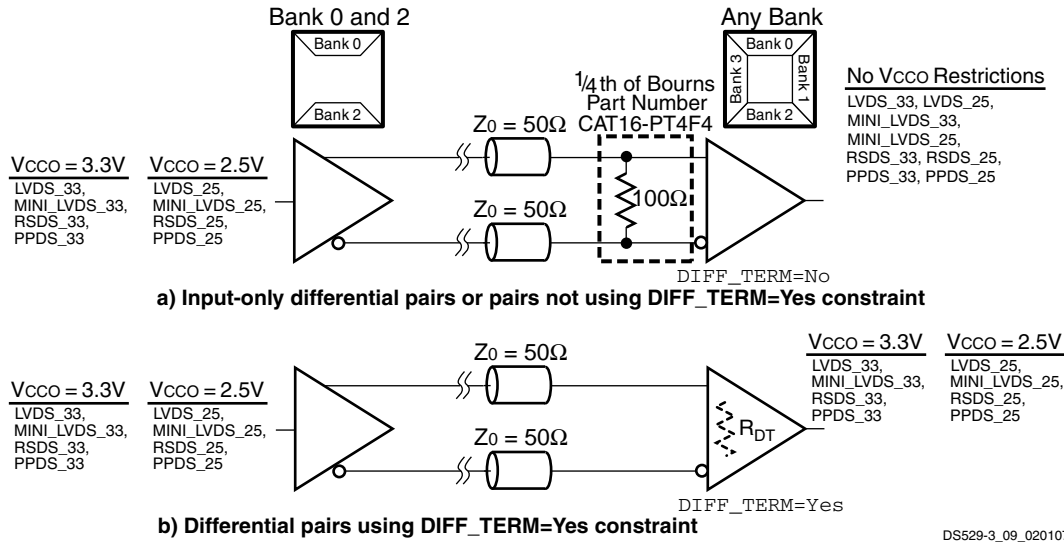


Figure 6: External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

BLVDS_25 I/O Standard

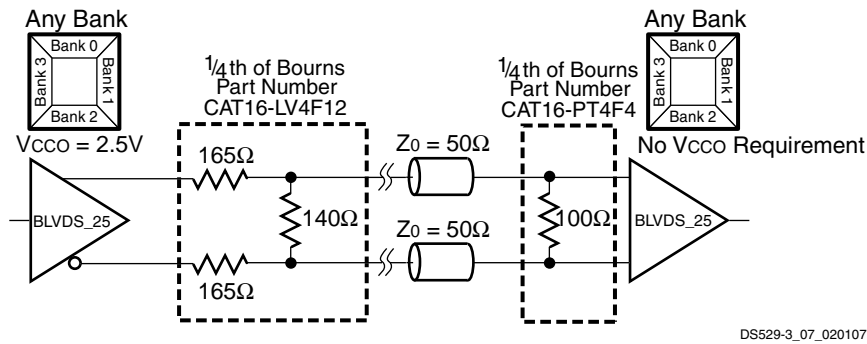


Figure 7: External Termination Resistors for BLVDS_25 I/O Standard

TMDS_33 I/O Standard

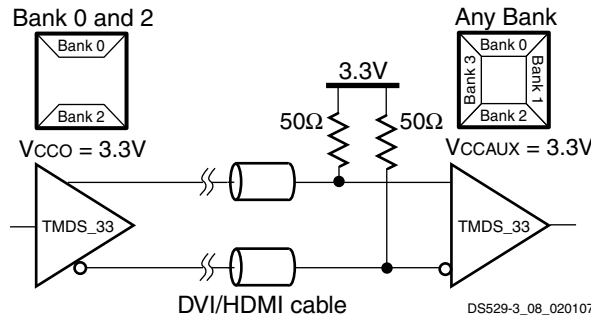


Figure 8: External Input Resistors Required for TMDS_33 I/O Standard

Device DNA Data Retention, Read Endurance

Table 15: Device DNA Identifier Memory Characteristics

Symbol	Description	Minimum	Units
DNA_RETENTION	Data retention.	10	Years
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Preview, Advance, Preliminary, or Production, as shown in [Table 16](#). Each category is defined as follows:

Preview: These specifications are based on estimates only and should not be used for timing analysis.

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE™ software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A FPGA speed files (v1.37), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in [Table 16](#). For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 16: Spartan-3A v1.37 Speed Grade Designations

Device	Preview	Advance	Preliminary	Production
XC3S50A				–4, –5
XC3S200A				–4, –5
XC3S400A				–4, –5
XC3S700A				–4, –5
XC3S1400A				–4, –5

[Table 17](#) provides the recent history of the Spartan-3A FPGA speed files.

Table 17: Spartan-3A Speed File Version History

Version	ISE Release	Description
1.37	ISE 9.2.01i	Updated pin-to-pin setup and hold times (Table 19), TMDS output adjustment (Table 25) multiplier setup/hold times (Table 33), and block RAM clock width (Table 34).
1.36	ISE 9.2i; previously available via Answer Record AR24992	XC3S400A, all speed grades and all temperature grades, upgraded to Production
1.35	Answer Record AR24992	XC3S50A, XC3S200A, XC3S700A, XC3S1400A, all speed grades and all temperature grades, upgraded to Production.
1.34	ISE 9.1.03i	XC3S700A and XC3S1400A –4 speed grade upgraded to Production. Updated pin-to-pin timing numbers.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T _{ICKOFDCM}	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, with DCM ⁽³⁾	XC3S50A	3.18	3.42	ns
			XC3S200A	3.21	3.27	ns
			XC3S400A	2.97	3.33	ns
			XC3S700A	3.39	3.50	ns
			XC3S1400A	3.51	3.99	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, without DCM	XC3S50A	4.59	5.02	ns
			XC3S200A	4.88	5.24	ns
			XC3S400A	4.68	5.12	ns
			XC3S700A	4.97	5.34	ns
			XC3S1400A	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from [Table 22](#). If the latter is true, *add* the appropriate Output adjustment from [Table 25](#).
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0, with DCM ⁽⁴⁾	XC3S50A	2.45	2.68	ns
			XC3S200A	2.59	2.84	ns
			XC3S400A	2.38	2.68	ns
			XC3S700A	2.38	2.57	ns
			XC3S1400A	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25 ⁽²⁾ , IFD_DELAY_VALUE = 5, without DCM	XC3S50A	2.55	2.76	ns
			XC3S200A	2.32	2.76	ns
			XC3S400A	2.21	2.60	ns
			XC3S700A	2.28	2.63	ns
			XC3S1400A	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25 ⁽³⁾ , IFD_DELAY_VALUE = 0, with DCM ⁽⁴⁾	XC3S50A	-0.36	-0.36	ns
			XC3S200A	-0.52	-0.52	ns
			XC3S400A	-0.33	-0.29	ns
			XC3S700A	-0.17	-0.12	ns
			XC3S1400A	-0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25 ⁽³⁾ , IFD_DELAY_VALUE = 5, without DCM	XC3S50A	-0.63	-0.58	ns
			XC3S200A	-0.56	-0.56	ns
			XC3S400A	-0.42	-0.42	ns
			XC3S700A	-0.80	-0.75	ns
			XC3S1400A	-0.69	-0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 20: Setup and Hold Times for the IOB Input Path

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVC MOS25 ⁽²⁾	0	All	1.24	1.91	ns
T_{IOICKD}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVC MOS25 ⁽²⁾	1	All	1.98	2.36	ns
			2		2.93	3.10	ns
			3		3.73	3.98	ns
			4		4.28	4.57	ns
			5		4.11	4.40	ns
			6		5.04	5.45	ns
			7		5.87	6.36	ns
			8		6.42	6.99	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVC MOS25 ⁽²⁾	0	All	-1.04	-1.03	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVC MOS25 ⁽²⁾	1	All	-1.85	-1.85	ns
			2		-2.59	-2.59	ns
			3		-3.01	-2.99	ns
			4		-3.37	-3.34	ns
			5		-3.38	-3.34	ns
			6		-3.77	-3.69	ns
			7		-4.09	-4.00	ns
			8		-4.45	-4.28	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This setup time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from [Table 22](#).
3. These hold times require adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from [Table 22](#). When the hold time is negative, it is possible to change the data before the clock's active edge.

Input Propagation Times

Table 21: Propagation Times for the IOB Input Path

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
Propagation Times							
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVC MOS25 ⁽²⁾	0	All	1.38	2.14	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVC MOS25 ⁽²⁾	1	All	2.12	2.59	ns
			2		3.07	3.33	
			3		3.87	4.21	
			4		4.42	4.80	
			5		4.25	4.63	
			6		5.18	5.68	
			7		6.01	6.59	
			8		6.56	7.22	

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This propagation time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from [Table 22](#).

Input Timing Adjustments

Table 22: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LV TTL	0.62	0.63	ns
LVC MOS33	0.54	0.54	ns
LVC MOS25	0	0	ns
LVC MOS18	0.83	0.83	ns
LVC MOS15	0.60	0.60	ns
LVC MOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
PCIX	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 22: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LV DS_25	0.76	0.76	ns
LV DS_33	0.79	0.79	ns
BLV DS_25	0.79	0.79	ns
MINI_LV DS_25	0.78	0.78	ns
MINI_LV DS_33	0.79	0.79	ns
LV PECL_25	0.78	0.78	ns
LV PECL_33	0.79	0.79	ns
RS DS_25	0.79	0.79	ns
RS DS_33	0.77	0.77	ns
TM DS_33	0.79	0.79	ns
PP DS_25	0.79	0.79	ns
PP DS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVC MOS25 standard to times that correspond to other signal standards.

Output Propagation Times

Table 23: Timing for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin			2.70	2.85	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This time requires adjustment whenever a signal standard other than LVC MOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 25](#).

Three-State Output Propagation Times

Table 24: Timing for the IOB Three-State Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
$T_{IOCKON}^{(2)}$	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
$T_{IOSRON}^{(2)}$	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 26](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 25](#).

Output Timing Adjustments

Table 25: Output Timing Adjustments for IOB

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74	2.74	ns
		Fast	2 mA	3.03	3.03
	4 mA		1.71	1.71	ns
	6 mA		1.71	1.71	ns
	8 mA		0.53	0.53	ns
	12 mA		0.53	0.53	ns
	16 mA		0.59	0.59	ns
	24 mA		0.60	0.60	ns
	QuietIO		2 mA	27.67	27.67
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 25: Output Timing Adjustments for IOB (Continued)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVC MOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55	2.55	ns
		Fast	2 mA	3.02	3.02
	4 mA		1.71	1.71	ns
	6 mA		1.72	1.72	ns
	8 mA		0.53	0.53	ns
	12 mA		0.59	0.59	ns
	16 mA		0.59	0.59	ns
	24 mA		0.51	0.51	ns
	QuietIO		2 mA	27.67	27.67
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 25: Output Timing Adjustments for IOB (Continued)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units	
			Speed Grade			
			-5	-4		
LVC MOS25	Slow	2 mA	5.33	5.33	ns	
		4 mA	2.81	2.81	ns	
		6 mA	2.82	2.82	ns	
		8 mA	1.14	1.14	ns	
		12 mA	1.10	1.10	ns	
		16 mA	0.83	0.83	ns	
		24 mA	2.26	2.26	ns	
	Fast	2 mA	4.36	4.36	ns	
		4 mA	1.76	1.76	ns	
		6 mA	1.25	1.25	ns	
		8 mA	0.38	0.38	ns	
		12 mA	0	0	ns	
		16 mA	0.01	0.01	ns	
		24 mA	0.01	0.01	ns	
	QuietIO	2 mA	25.92	25.92	ns	
		4 mA	25.92	25.92	ns	
		6 mA	25.92	25.92	ns	
		8 mA	15.57	15.57	ns	
		12 mA	15.59	15.59	ns	
		16 mA	14.27	14.27	ns	
	LVC MOS18	Slow	2 mA	4.48	4.48	ns
			4 mA	3.69	3.69	ns
			6 mA	2.91	2.91	ns
			8 mA	1.99	1.99	ns
12 mA			1.57	1.57	ns	
16 mA			1.19	1.19	ns	
Fast		2 mA	3.96	3.96	ns	
		4 mA	2.57	2.57	ns	
		6 mA	1.90	1.90	ns	
		8 mA	1.06	1.06	ns	
		12 mA	0.83	0.83	ns	
		16 mA	0.63	0.63	ns	
		QuietIO	2 mA	24.97	24.97	ns
4 mA			24.97	24.97	ns	
6 mA			24.08	24.08	ns	
8 mA			16.43	16.43	ns	
12 mA			14.52	14.52	ns	
16 mA	13.41		13.41	ns		

Table 25: Output Timing Adjustments for IOB (Continued)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units	
			Speed Grade			
			-5	-4		
LVC MOS15	Slow	2 mA	5.82	5.82	ns	
		4 mA	3.97	3.97	ns	
		6 mA	3.21	3.21	ns	
		8 mA	2.53	2.53	ns	
		12 mA	2.06	2.06	ns	
		24 mA	2.06	2.06	ns	
	Fast	2 mA	5.23	5.23	ns	
		4 mA	3.05	3.05	ns	
		6 mA	1.95	1.95	ns	
		8 mA	1.60	1.60	ns	
		12 mA	1.30	1.30	ns	
		24 mA	1.30	1.30	ns	
	QuietIO	2 mA	34.11	34.11	ns	
		4 mA	25.66	25.66	ns	
		6 mA	24.64	24.64	ns	
8 mA		22.06	22.06	ns		
12 mA		20.64	20.64	ns		
LVC MOS12	Slow	2 mA	7.14	7.14	ns	
		4 mA	4.87	4.87	ns	
		6 mA	5.67	5.67	ns	
	Fast	2 mA	6.77	6.77	ns	
		4 mA	5.02	5.02	ns	
		6 mA	4.09	4.09	ns	
	QuietIO	2 mA	50.76	50.76	ns	
		4 mA	43.17	43.17	ns	
		6 mA	37.31	37.31	ns	
	PCI33_3			0.34	0.34	ns
	PCI66_3			0.34	0.34	ns
	PCIX			0.34	0.34	ns
HSTL_I			0.78	0.78	ns	
HSTL_III			1.16	1.16	ns	
HSTL_I_18			0.35	0.35	ns	
HSTL_II_18			0.30	0.30	ns	
HSTL_III_18			0.47	0.47	ns	
SSTL18_I			0.40	0.40	ns	
SSTL18_II			0.30	0.30	ns	
SSTL2_I			0	0	ns	
SSTL2_II			-0.05	-0.05	ns	
SSTL3_I			0	0	ns	
SSTL3_II			0.17	0.17	ns	

Table 25: Output Timing Adjustments for IOB (Continued)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	1.16	1.16	ns
LVDS_33	0.46	0.46	ns
BLVDS_25	0.11	0.11	ns
MINI_LVDS_25	0.75	0.75	ns
MINI_LVDS_33	0.40	0.40	ns
LVPECL_25	Input Only		
LVPECL_33			
RS DS_25	1.42	1.42	ns
RS DS_33	0.58	0.58	ns
TMDS_33	0.46	0.46	ns
PPDS_25	1.07	1.07	ns
PPDS_33	0.63	0.63	ns
DIFF_HSTL_I_18	0.43	0.43	ns
DIFF_HSTL_II_18	0.41	0.41	ns
DIFF_HSTL_III_18	0.36	0.36	ns
DIFF_HSTL_I	1.01	1.01	ns
DIFF_HSTL_III	0.54	0.54	ns
DIFF_SSTL18_I	0.49	0.49	ns
DIFF_SSTL18_II	0.41	0.41	ns
DIFF_SSTL2_I	0.82	0.82	ns
DIFF_SSTL2_II	0.09	0.09	ns
DIFF_SSTL3_I	1.16	1.16	ns
DIFF_SSTL3_II	0.28	0.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVC MOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

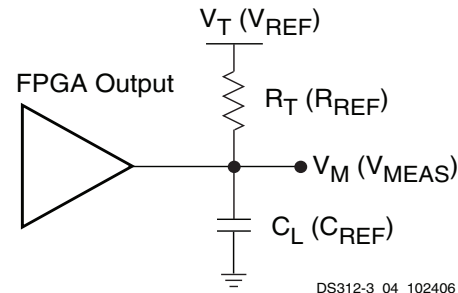
Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H .

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T , the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTTL), then R_T is set to $1M\Omega$ to indicate an open

connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: Output Test Setup

Table 26: Test Methods for Timing Measurement at I/Os

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
LVTTTL	-	0	3.3	1M	0	1.4
LVCMOS33	-	0	3.3	1M	0	1.65
LVCMOS25	-	0	2.5	1M	0	1.25
LVCMOS18	-	0	1.8	1M	0	0.9
LVCMOS15	-	0	1.5	1M	0	0.75
LVCMOS12	-	0	1.2	1M	0	0.6
PCI33_3	Rising	Note 3	Note 3	25	0	0.94
	Falling			25	3.3	2.03
PCI66_3	Rising	Note 3	Note 3	25	0	0.94
	Falling			25	3.3	2.03
PCIX	Rising	Note 3	Note 3	25	0	0.94
	Falling			25	3.3	2.03
HSTL_I	0.75	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.75	V_{REF}
HSTL_III	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.5	V_{REF}
HSTL_I_18	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
HSTL_II_18	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	25	0.9	V_{REF}
HSTL_III_18	1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
SSTL18_I	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
SSTL18_II	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	25	0.9	V_{REF}
SSTL2_I	1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	50	1.25	V_{REF}
SSTL2_II	1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	25	1.25	V_{REF}

Table 26: Test Methods for Timing Measurement at I/Os (Continued)

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
SSTL3_I	1.5	$V_{REF} - 0.75$	$V_{REF} + 0.75$	50	1.5	V_{REF}
SSTL3_II	1.5	$V_{REF} - 0.75$	$V_{REF} + 0.75$	25	1.5	V_{REF}
Differential						
LVDS_25	-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVDS_33	-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
BLVDS_25	-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	1M	0	V_{ICM}
MINI_LVDS_25	-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
MINI_LVDS_33	-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVPECL_25	-	$V_{ICM} - 0.3$	$V_{ICM} + 0.3$	N/A	N/A	V_{ICM}
LVPECL_33	-	$V_{ICM} - 0.3$	$V_{ICM} + 0.3$	N/A	N/A	V_{ICM}
RSDS_25	-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	1.2	V_{ICM}
RSDS_33	-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	1.2	V_{ICM}
TMDS_33	-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	3.3	V_{ICM}
PPDS_25	-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	0.8	V_{ICM}
PPDS_33	-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	0.8	V_{ICM}
DIFF_HSTL_I	0.75	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.75	V_{REF}
DIFF_HSTL_III	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.5	V_{REF}
DIFF_HSTL_I_18	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_HSTL_II_18	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_HSTL_III_18	1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
DIFF_SSTL18_I	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_SSTL18_II	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_SSTL2_I	1.25	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.25	V_{REF}
DIFF_SSTL2_II	1.25	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.25	V_{REF}
DIFF_SSTL3_I	1.5	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.5	V_{REF}
DIFF_SSTL3_II	1.5	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.5	V_{REF}

Notes:

- Descriptions of the relevant symbols are as follows:
 V_{REF} – The reference voltage for setting the input switching threshold
 V_{ICM} – The common mode input voltage
 V_M – Voltage of measurement point on signal transition
 V_L – Low-level test voltage at Input pin
 V_H – High-level test voltage at Input pin
 R_T – Effective termination resistance, which takes on a value of 1 M Ω when no parallel termination is required
 V_T – Termination voltage
- The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
- According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF} , R_{REF} , and V_{MEAS}) correspond directly with the parameters used in [Table 26](#) (V_T , R_T , and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF} is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in [Figure 9](#). Use parameter values V_T , R_T , and V_M from [Table 26](#). C_{REF} is zero.
2. Record the time to V_M .
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment ([Table 25](#)) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 27 and Table 28 provide the essential SSO guidelines. For each device/package combination, Table 27 provides the number of equivalent V_{CCO} /GND pairs. For each output signal standard and drive strength, Table 28 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO} /GND pair within an I/O bank. The guidelines in Table 28 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 27 and Table 28 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

$$SSO_{MAX}/IO \text{ Bank} = \text{Table 27} \times \text{Table 28}$$

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (TQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 27: Equivalent V_{CCO} /GND Pairs per Bank

Device	Package Style (including Pb-free)					
	TQ144	FT256	FG320	FG400	FG484	FG676
XC3S50A	2	3	–	–	–	–
XC3S200A	–	4	4	–	–	–
XC3S400A	–	4	4	5	–	–
XC3S700A	–	–	–	5	5	–
XC3S1400A	–	–	–	–	6	9

Table 28: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair (V_{CCAUX}=3.3V)

Signal Standard (IOSTANDARD)		Package Type				
		TQ144		FT256, FG320, FG400, FG484, FG676		
		Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	
Single-Ended Standards						
LVTTTL	Slow	2	20	20	60	60
		4	10	10	41	41
		6	10	10	29	29
		8	6	6	22	22
		12	6	6	13	13
		16	5	5	11	11
		24	4	4	9	9
		Fast	2	10	10	10
	4		6	6	6	6
	6		5	5	5	5
	8		3	3	3	3
	12		3	3	3	3
	16		3	3	3	3
	24		2	2	2	2
	QuietIO		2	40	40	80
		4	24	24	48	48
		6	20	20	36	36
		8	16	16	27	27
		12	12	12	16	16
		16	9	9	13	13
		24	9	9	12	12

 Table 28: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair (V_{CCAUX}=3.3V)

Signal Standard (IOSTANDARD)		Package Type				
		TQ144		FT256, FG320, FG400, FG484, FG676		
		Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	
LVCMOS33	Slow	2	24	24	76	76
		4	14	14	46	46
		6	11	11	27	27
		8	10	10	20	20
		12	9	9	13	13
		16	8	8	10	10
		24	–	8	–	9
		Fast	2	10	10	10
	4		8	8	8	8
	6		5	5	5	5
	8		4	4	4	4
	12		4	4	4	4
	16		2	2	2	2
	24		–	2	–	2
	QuietIO		2	36	36	76
		4	32	32	46	46
		6	24	24	32	32
		8	16	16	26	26
		12	16	16	18	18
		16	12	12	14	14
		24	–	10	–	10

Table 28: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair (V_{CCAUX}=3.3V)

Signal Standard (IOSTANDARD)		Package Type					
		TQ144		FT256, FG320, FG400, FG484, FG676			
		Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)		
LVCMOS25	Slow	2	16	16	76	76	
		4	10	10	46	46	
		6	8	8	33	33	
		8	7	7	24	24	
		12	6	6	18	18	
		16	–	6	–	11	
		24	–	5	–	7	
	Fast	2	12	12	18	18	
		4	10	10	14	14	
		6	8	8	6	6	
		8	6	6	6	6	
		12	3	3	3	3	
		16	–	3	–	3	
		24	–	2	–	2	
	QuietIO	2	36	36	76	76	
		4	30	30	60	60	
		6	24	24	48	48	
		8	20	20	36	36	
		12	12	12	36	36	
		16	–	12	–	36	
		24	–	8	–	8	
	LVCMOS18	Slow	2	13	13	64	64
			4	8	8	34	34
			6	8	8	22	22
8			7	7	18	18	
12			–	5	–	13	
16			–	5	–	10	
Fast		2	13	13	18	18	
		4	8	8	9	9	
		6	7	7	7	7	
		8	4	4	4	4	
		12	–	4	–	4	
		16	–	3	–	3	
QuietIO		2	30	30	64	64	
		4	24	24	64	64	
		6	20	20	48	48	
		8	16	16	36	36	
		12	–	12	–	36	
	16	–	12	–	24		

Table 28: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair (V_{CCAUX}=3.3V)

Signal Standard (IOSTANDARD)		Package Type				
		TQ144		FT256, FG320, FG400, FG484, FG676		
		Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20
LVCMOS12	Slow	2	17	17	40	40
		4	–	13	–	25
		6	–	10	–	18
	Fast	2	12	9	31	31
		4	–	9	–	13
		6	–	9	–	9
	QuietIO	2	36	36	55	55
		4	–	33	–	36
		6	–	27	–	36
PCI33_3		9	9	16	16	
PCI66_3		–	9	–	13	
PCIX		–	9	–	11	
HSTL_I		–	11	–	20	
HSTL_III		–	7	–	8	
HSTL_I_18		13	13	17	17	
HSTL_II_18		–	5	–	5	
HSTL_III_18		8	8	10	8	
SSTL18_I		7	13	7	15	
SSTL18_II		–	3	–	3	
SSTL2_I		10	10	18	18	
SSTL2_II		–	6	–	9	
SSTL3_I		7	8	8	10	
SSTL3_II		5	6	6	7	

Table 28: Recommended Number of Simultaneously Switching Outputs per V_{CCO} -GND Pair ($V_{CCAUX}=3.3V$)

Signal Standard (IOSTANDARD)	Package Type			
	TQ144		FT256, FG320, FG400, FG484, FG676	
	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)	Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Differential Standards (Number of I/O Pairs or Channels)				
LVDS_25	8	–	22	–
LVDS_33	8	–	27	–
BLVDS_25	1	1	4	4
MINI_LVDS_25	8	–	22	–
MINI_LVDS_33	8	–	27	–
LVPECL_25	Input Only			
LVPECL_33	Input Only			
RSDS_25	8	–	22	–
RSDS_33	8	–	27	–
TMDS_33	8	–	27	–
PPDS_25	8	–	22	–
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	1	–	1
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

- Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to [UG331: Spartan-3 Generation FPGA User Guide](#) for additional information.
- The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
- If more than one signal standard is assigned to the I/Os of a given bank, refer to [XAPP689: Managing Ground Bounce in Large FPGAs](#) for information on how to perform weighted average SSO calculations.

Configurable Logic Block (CLB) Timing

Table 29: CLB (SLICEM) Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 30: CLB Distributed RAM Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output		1.69		2.01	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	-0.07	–	-0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Table 31: CLB Shift Register Switching Characteristics

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output		4.11		4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 32: Clock Distribution Switching Characteristics

Description	Symbol	Minimum	Maximum		Units
			Speed Grade		
			-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	–	0.22	0.23	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	–	0.56	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	0	350	333	MHz

18 x 18 Embedded Multiplier Timing

Table 33: 18 x 18 Embedded Multiplier Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ^(2,3)	–	0.84	–	1.30	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ^(2,4)	–	4.44	–	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	3.56	–	3.98	–	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	0.00	–	0.00	–	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register ⁽¹⁾	0	280	0	250	MHz

Notes:

1. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Block RAM Timing

Table 34: Block RAM Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{RCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.06	–	2.49	ns
Setup Times						
T_{RCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.32	–	0.36	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.28	–	0.31	–	ns
T_{RCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.69	–	0.77	–	ns
T_{RCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.12	–	1.26	–	ns
Hold Times						
T_{RCK_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKD_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCK_ENB}	Hold time on the EN input after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0	–	0	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 35 and Table 36) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 37 through Table 40) supersede any corresponding ones in the DLL tables. DLL specifications that do not

change with the addition of DFS or PS functions are presented in Table 35 and Table 36.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 35: Recommended Operating Conditions for the DLL

Symbol		Description	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Input Frequency Ranges							
F _{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	MHz
Input Pulse Requirements							
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period	F _{CLKIN} ≤ 150 MHz	40%	60%	40%	60%	-
		F _{CLKIN} > 150 MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation⁽⁴⁾							
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input	F _{CLKIN} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_DLL_HF		F _{CLKIN} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input		-	±1	-	±1	ns
CLKFB_DELAY_VAR_EXT	Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		-	±1	-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 37.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock period by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 36: Switching Characteristics for the DLL

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	All	5	280	5	250	MHz	
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs		5	200	5	200	MHz	
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs		10	334	10	334	MHz	
CLKOUT_FREQ_DV	Frequency for the CLKDV output		0.3125	186	0.3125	166	MHz	
Output Clock Jitter^(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	–	±100	–	±100	ps	
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output		–	±150	–	±150	ps	
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output		–	±150	–	±150	ps	
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output		–	±150	–	±150	ps	
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs		–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps	
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division		–	±150	–	±150	ps	
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division		–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps	
Duty Cycle⁽⁴⁾								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps	
Phase Alignment⁽⁴⁾								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	–	±150	–	±150	ps	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps	
		All others	–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps	
Lock Time								
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	$5 \text{ MHz} \leq F_{\text{CLKIN}} \leq 15 \text{ MHz}$	All	–	5	–	5	ms
		$F_{\text{CLKIN}} > 15 \text{ MHz}$		–	600	–	600	µs
Delay Lines								
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps	

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 8 and Table 35.
- Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
- For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of “±[1% of CLKIN period + 150]”. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
- The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 37: Recommended Operating Conditions for the DFS

Symbol	Description	Speed Grade				Units		
		-5		-4				
		Min	Max	Min	Max			
Input Frequency Ranges⁽²⁾								
F _{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333	0.200	333	MHz
Input Clock Jitter Tolerance⁽³⁾								
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F _{CLKFX} ≤ 150 MHz	–	±300	–	±300	ps	
CLKIN_CYC_JITT_FX_HF		F _{CLKFX} > 150 MHz	–	±150	–	±150	ps	
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input		–	±1	–	±1	ns	

Notes:

- DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
- If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 35.
- CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 38: Switching Characteristics for the DFS

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_FX ⁽²⁾	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	320	MHz
Output Clock Jitter^(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	All	Typ	Max	Typ	Max	ps	
			CLKIN ≤ 20 MHz	Use the Spartan-3A Jitter Calculator: www.xilinx.com/bvdocs/publications/s3a_jitter_calc.zip				
			CLKIN > 20 MHz	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]		±[1% of CLKFX period + 200]
Duty Cycle^(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment⁽⁶⁾								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps

Table 38: Switching Characteristics for the DFS (Continued)

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Lock Time								
LOCK_FX ^(2, 3)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	All	$5 \text{ MHz} \leq F_{\text{CLKIN}} \leq 15 \text{ MHz}$	–	5	–	5	ms
			$F_{\text{CLKIN}} > 15 \text{ MHz}$	–	450	–	450	μs

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 8 and Table 37.
- DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
- For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an XC3S1400A FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of “±[1% of CLKFX period + 200]”. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Phase Shifter (PS)

Table 39: Recommended Operating Conditions for the PS in Variable Phase Mode

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F _{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 40: Switching Characteristics for the PS in Variable Phase Mode

Symbol	Description	Phase Shift Amount	Units
Phase Shifting Range			
MAX_STEPS ⁽²⁾	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	$\pm[\text{INTEGER}(10 \cdot (T_{\text{CLKIN}} - 3 \text{ ns}))]$
		CLKIN ≥ 60 MHz	$\pm[\text{INTEGER}(15 \cdot (T_{\text{CLKIN}} - 3 \text{ ns}))]$
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	$\pm[\text{MAX_STEPS} \cdot \text{DCM_DELAY_STEP_MIN}]$	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm[\text{MAX_STEPS} \cdot \text{DCM_DELAY_STEP_MAX}]$	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 8](#) and [Table 39](#).
- The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
- The DCM_DELAY_STEP values are provided at the bottom of [Table 36](#).

Miscellaneous DCM Timing

Table 41: Miscellaneous DCM Timing

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles
DCM_RST_PW_MAX ⁽²⁾	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME ⁽³⁾	Maximum duration from V _{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex™-4 DCM_RESET specification. This specification does not apply for Spartan-3A FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3A FPGAs.

DNA Port Timing

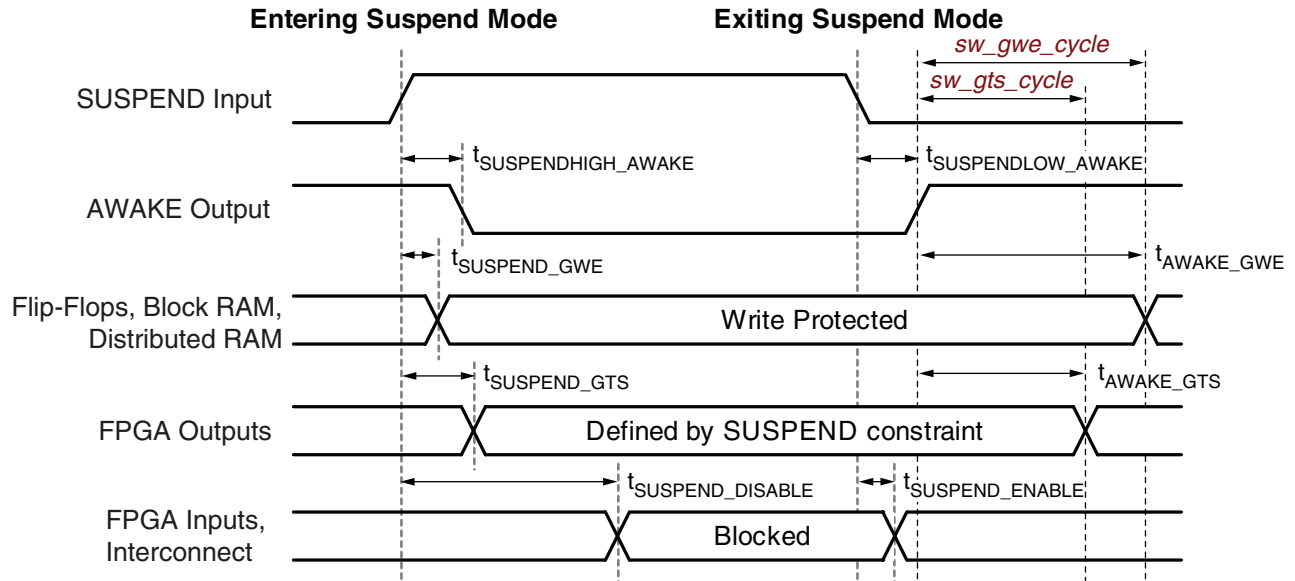
Table 42: DNA_PORT Interface Timing

Symbol	Description	Min	Max	Units
T _{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T _{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T _{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T _{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T _{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T _{DNARH}	Hold time on READ after the rising edge of CLK	0	–	ns
T _{DNADCKO}	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
T _{DNACLKF}	CLK frequency	0	100	MHz
T _{DNACLKL}	CLK High time	1.0	∞	ns
T _{DNACLKH}	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 μs.

Suspend Mode Timing



DS610-3_08_061207

Figure 10: Suspend Mode Timing

Table 43: Suspend Mode Timing Parameters

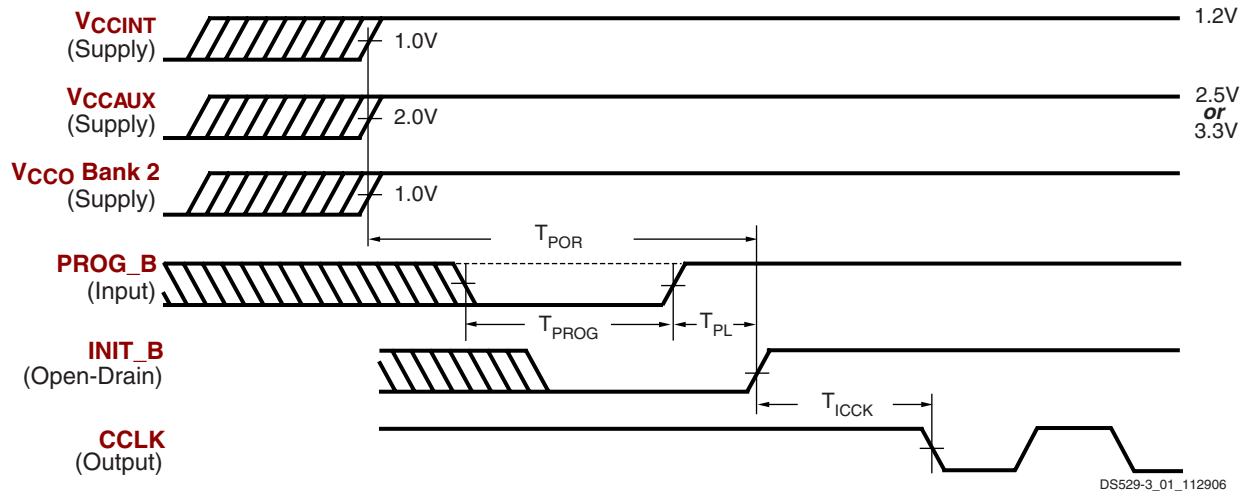
Symbol	Description	Min	Typ	Max
Entering Suspend Mode				
$T_{SUSPENDHIGH_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (<i>suspend_filter:No</i>)	–	7	–
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (<i>suspend_filter:Yes</i>)	+160	+300	+600
$T_{SUSPEND_GWE}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–
$T_{SUSPEND_GTS}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–
$T_{SUSPEND_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–
Exiting Suspend Mode				
$T_{SUSPENDLOW_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–
$T_{SUSPEND_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:1</i> .	–	67	–
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:512</i> .	–	14	–
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:1</i> .	–	57	–
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:512</i> .	–	14	–

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A Suspend feature, see [XAPP480: Using Suspend Mode in Spartan-3 Generation FPGAs](#).

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on $PROG_B$ is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of $INIT_B$ samples the voltage levels applied to the mode pins (M0 - M2).

Figure 11: Waveforms for Power-On and the Beginning of Configuration

Table 44: Power-On Timing and the Beginning of Configuration

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
$T_{POR}^{(2)}$	The time from the application of V_{CCINT} , V_{CCAUX} , and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the $INIT_B$ pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the $PROG_B$ pin	All	0.5	–	μ s
$T_{PL}^{(2)}$	The time from the rising edge of the $PROG_B$ pin to the rising transition on the $INIT_B$ pin	XC3S50A	–	0.5	ms
		XC3S200A	–	0.5	ms
		XC3S400A	–	1	ms
		XC3S700A	–	2	ms
		XC3S1400A	–	2	ms
T_{INIT}	Minimum Low pulse width on $INIT_B$ output	All	250	–	ns
$T_{ICCK}^{(3)}$	The time from the rising edge of the $INIT_B$ pin to the generation of the configuration clock signal at the $CCLK$ output pin	All	0.5	4	μ s

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all V_{CCINT} , V_{CCO} , and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.

Configuration Clock (CCLK) Characteristics

Table 45: Master Mode CCLK Output Period by *ConfigRate* Option Setting

Symbol	Description	<i>ConfigRate</i> Setting	Temperature Range	Minimum	Maximum	Units
T _{CCLK1}	CCLK clock period by <i>ConfigRate</i> setting	1 (power-on value)	Commercial	1,254	2,000	ns
			Industrial	1,180		ns
T _{CCLK3}		3	Commercial	413	667	ns
			Industrial	390		ns
T _{CCLK6}		6	Commercial	207	334	ns
			Industrial	195		ns
T _{CCLK7}		7	Commercial	178	286	ns
			Industrial	168		ns
T _{CCLK8}		8	Commercial	156	250	ns
			Industrial	147		ns
T _{CCLK10}		10	Commercial	123	200	ns
			Industrial	116		ns
T _{CCLK12}		12	Commercial	103	167	ns
			Industrial	97		ns
T _{CCLK13}		13	Commercial	93	154	ns
			Industrial	88		ns
T _{CCLK17}		17	Commercial	72	118	ns
			Industrial	68		ns
T _{CCLK22}		22	Commercial	54	91	ns
			Industrial	51		ns
T _{CCLK25}	25	Commercial	47	80	ns	
		Industrial	45		ns	
T _{CCLK27}	27	Commercial	44	75	ns	
		Industrial	42		ns	
T _{CCLK33}	33	Commercial	36	61	ns	
		Industrial	34		ns	
T _{CCLK44}	44	Commercial	26	46	ns	
		Industrial	25		ns	
T _{CCLK50}	50	Commercial	22	40	ns	
		Industrial	21		ns	
T _{CCLK100}	100	Commercial	11.2	20	ns	
		Industrial	10.6		ns	

Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream.

Table 46: Master Mode CCLK Output Frequency by ConfigRate Option Setting

Symbol	Description	ConfigRate Setting	Temperature Range	Minimum	Maximum	Units
F _{CCLK1}	Equivalent CCLK clock frequency by ConfigRate setting	1 (power-on value)	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F _{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F _{CCLK6}		6	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F _{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F _{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F _{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F _{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F _{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F _{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F _{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F _{CCLK25}	25	Commercial	10.00	20.90	MHz	
		Industrial		22.23	MHz	
F _{CCLK27}	27	Commercial	10.80	22.39	MHz	
		Industrial		23.81	MHz	
F _{CCLK33}	33	Commercial	13.20	27.48	MHz	
		Industrial		29.23	MHz	
F _{CCLK44}	44	Commercial	17.60	37.60	MHz	
		Industrial		40.00	MHz	
F _{CCLK50}	50	Commercial	20.00	44.80	MHz	
		Industrial		47.66	MHz	
F _{CCLK100}	100	Commercial	40.00	88.68	MHz	
		Industrial		94.34	MHz	

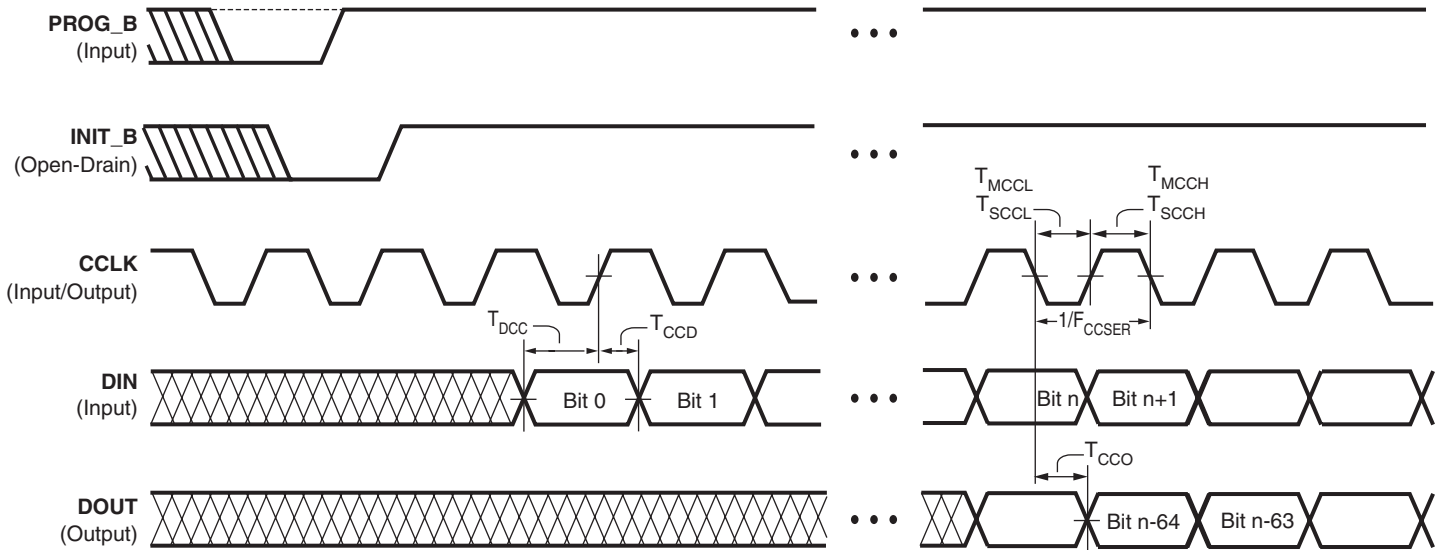
Table 47: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description		ConfigRate Setting																Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T _{MCCL} , T _{MCCH}	Master Mode CCLK	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
	Minimum Low and High Time	Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 48: Slave Mode CCLK Input Low and High Time

Symbol	Description	Min	Max	Units
T _{SCCL} , T _{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing



DS312-3_05_103105

Figure 12: Waveforms for Master Serial and Slave Serial Configuration

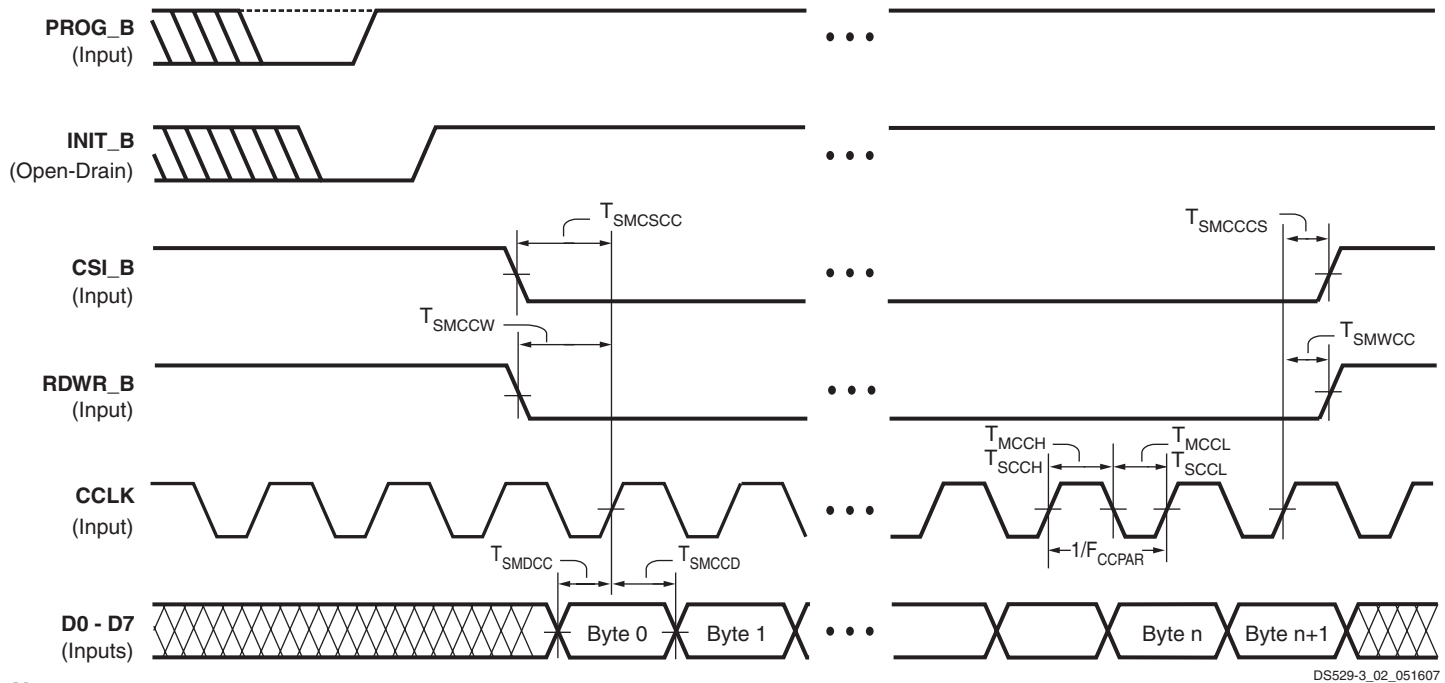
Table 49: Timing for the Master Serial and Slave Serial Configuration Modes

Symbol	Description	Slave/ Master	All Speed Grades		Units	
			Min	Max		
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin	Both	1.5	10	ns	
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	7	–	ns	
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Master	0	–	ns	
		Slave	1.0			
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin	Master	See Table 47			
		Slave	See Table 48			
T_{CCL}	Low pulse width at the CCLK input pin	Master	See Table 47			
		Slave	See Table 48			
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	Slave	No bitstream compression	0	100	MHz
			With bitstream compression	0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



DS529-3_02_051607

Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.

Figure 13: Waveforms for Slave Parallel Configuration

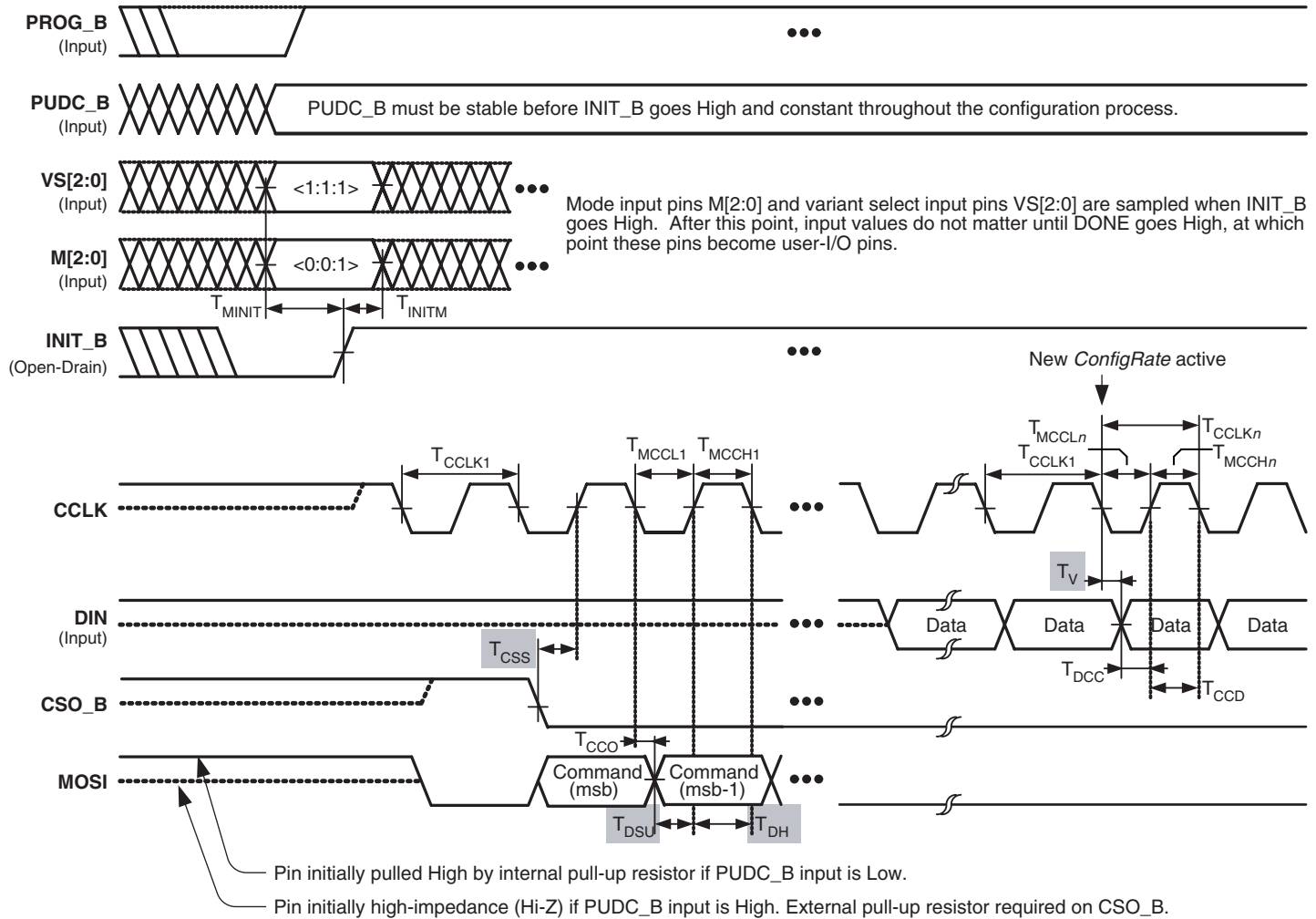
Table 50: Timing for the Slave Parallel Configuration Mode

Symbol	Description	All Speed Grades		Units	
		Min	Max		
Setup Times					
$T_{SMDC}^{(2)}$	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	7	–	ns	
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin	7	–	ns	
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin	15	–	ns	
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	1.0	–	ns	
T_{SMCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin	0	–	ns	
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin	0	–	ns	
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin	5	–	ns	
T_{CCL}	The Low pulse width at the CCLK input pin	5	–	ns	
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Serial Peripheral Interface (SPI) Configuration Timing



Shaded values indicate specifications on attached SPI Flash PROM.

DS529-3_06_102506

Figure 14: Waveforms for Serial Peripheral Interface (SPI) Configuration

Table 51: Timing for Serial Peripheral Interface (SPI) Configuration Mode

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		(see Table 45)	
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate bitstream option setting		(see Table 45)	
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge		See Table 49	
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge		See Table 49	
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge		See Table 49	

Table 52: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing

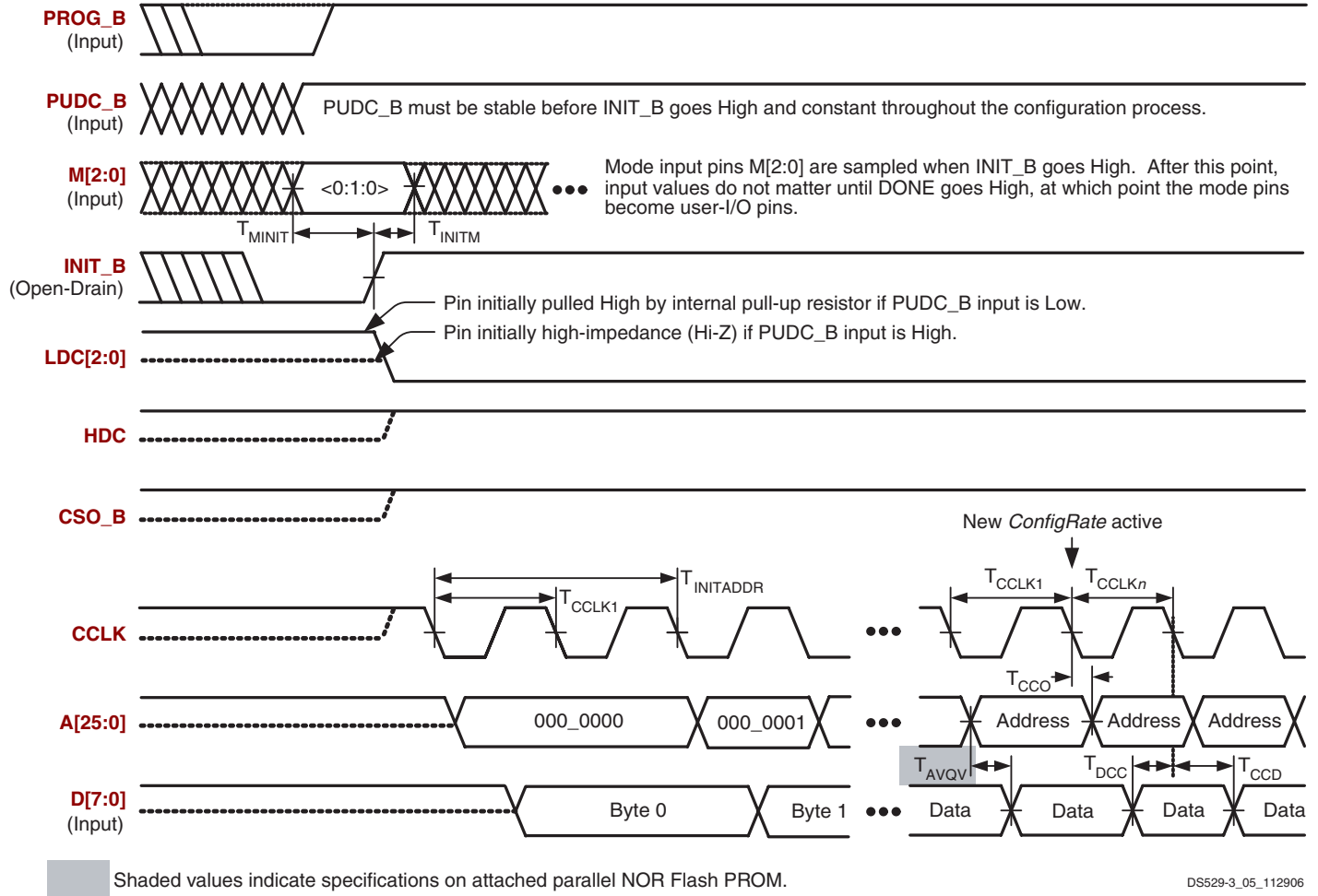


Figure 15: Waveforms for Byte-wide Peripheral Interface (BPI) Configuration

Table 53: Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	(see Table 45)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	(see Table 45)		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 49		
T_{SMDCC}	Setup time on D[7:0] data inputs before CCLK falling edge	See Table 50		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK falling edge	0	–	ns

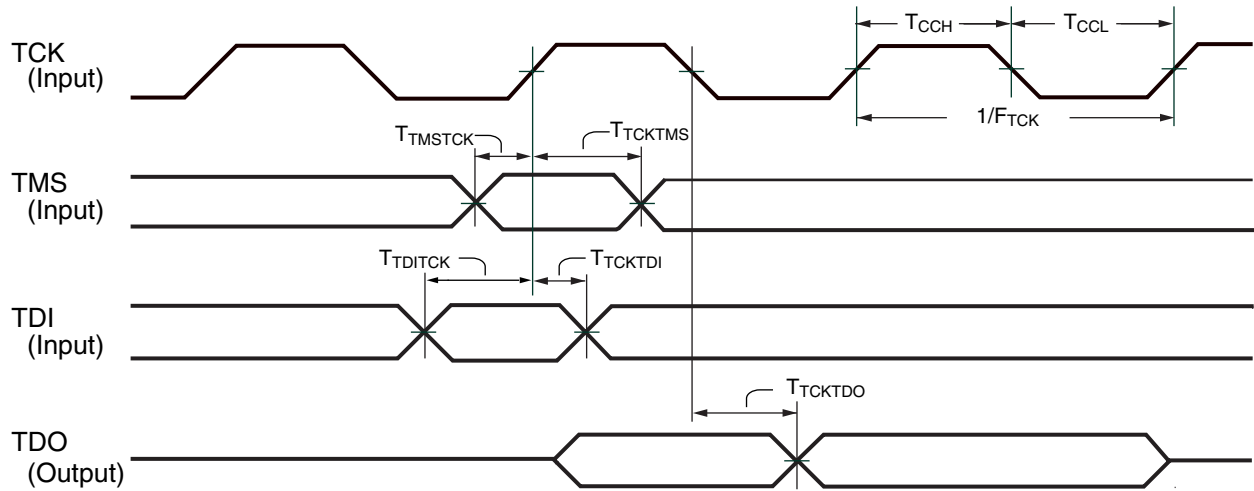
Table 54: Configuration Timing Requirements for Attached Parallel NOR Flash

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time ⁽³⁾	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

IEEE 1149.1/1553 JTAG Test Access Port Timing



DS099_06_040703

Figure 16: JTAG Waveforms

Table 55: Timing for the JTAG Test Access Port

Symbol	Description	All Speed Grades		Units	
		Min	Max		
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns	
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All devices and functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE) on XC3S700A and XC3S1400A FPGAs	11.0		
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	–	ns	
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	2.0		
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	–	ns	
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T_{CCL}	The Low pulse width at the TCK pin		5	–	ns
T_{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T_{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F_{TCK}	Frequency of the TCK signal	All operations on XC3S50A, XC3S200A, and XC3S400A FPGAs and for BYPASS or HIGHZ instructions on all FPGAs	0	33	MHz
		All operations on XC3S700A and XC3S1400A FPGAs, except for BYPASS or HIGHZ instructions		20	

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 8.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Moved Table 15 to under "DC Electrical Characteristics" section. Updated all timing specifications for the v1.32 speed files. Added recommended Simultaneous Switching Output (SSO) limits in Table 28 . Set a 10 μ s maximum pulse width for the DNA_PORT READ signal and the JTAG clock input during the ISC_DNA command, affecting both Table 42 and Table 55 . Described "External Termination Requirements for Differential I/O." Added separate DIN hold time for Slave mode in Table 49 . Corrected wording in Table 51 and Table 53 ; no specifications affected.
03/16/07	1.2	Updated all AC timing specifications to the v1.34 speeds file. Promoted the XC3S700A and XC3S1400A FPGAs offered in the -4 speed grade to Production status, as shown in Table 16 . Added Note 2 to Table 38 regarding the extra logic (one LUT) automatically added by ISE 9.1i and later software revisions for any DCM application that leverages the Digital Frequency Synthesizer (DFS). Separated some JTAG specifications by array size or function, as shown in Table 55 . Updated quiescent current limits in Table 10 .
04/23/07	1.3	Updated all AC timing specifications to the v1.35 speeds file. Promoted all family members except the XC3S400A to Production status, as shown in Table 16 .
05/08/07	1.4	Updated XC3S400A to Production and v1.36 speeds file. Added banking rules and other explanatory footnotes to Table 12 and Table 13 . Corrected DIFF_SSTL3_II V _{OL} Max in Table 14 . Improved XC3S400A Pin-to-Pin Clock-to-Output times in Table 18 . Updated XC3S400A Pin-to-Pin Setup Times in Table 19 . Updated TIOICKPD for -5 in Table 20 . Added SSO numbers to Table 27 and Table 28 . Removed invalid Embedded Multiplier Hold Times in Table 33 . Improved CLKOUT_FREQ_CLK90 in Table 36 . Improved T _{TDITCK} and F _{TCK} performance for XC3S400A in Table 55 .
07/10/07	1.5	Added DIFF_HSTL_I and DIFF_HSTL_III to Table 13 , Table 14 , Table 26 , and Table 28 . Updated TMDS DC characteristics in Table 14 . Updated for speed file v1.37 in ISE 9.2.01i as shown in Table 17 . Updated pin-to-pin setup and hold times in Table 19 . Updated TMDS output adjustment in Table 25 . Updated I/O Test Method values in Table 26 . Added BLVDS SSO numbers in Table 28 . For Multiplier block, updated setup times and added hold times to Table 33 . Updated block RAM clock width in Table 34 . Updated CLKOUT_PER_JITT_2X and CLKOUT_PER_JITT_DV2 in Table 36 . Added CCLK specifications for Commercial in Table 45 through Table 47 .

Introduction

This section describes how the various pins on a Spartan™-3A FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331: *Spartan-3 Generation FPGA User Guide*.

- **UG331: Spartan-3 Generation FPGA User Guide**
<http://www.xilinx.com/bvdocs/userguides/ug331.pdf>

Spartan-3A FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code.

Table 56: Types of Pins on Spartan-3A FPGAs

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: <i>Spartan-3 Generation Configuration User Guide</i> for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are the TQ144 and the XC3S50A in the FT256 package). The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: <i>Spartan-3 Generation FPGA User Guide</i> for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: <i>Spartan-3 Generation Configuration User Guide</i> for additional information on the DONE and PROG_B signals.	DONE, PROG_B
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin. AWAKE is a Dual-Purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE

Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A FPGA packages, as outlined in Table 56. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 56: Types of Pins on Spartan-3A FPGAs (Continued)

Type / Color Code	Description	Pin Name(s) in Type
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

- # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 57.

Table 57: Power and Ground Supply Pins by Package

Package	VCCINT	VCCAUX	VCCO	GND
TQ144	4	4	8	13
FT256	6	4	16	28
FG320	6	8	16	32
FG400	9	8	22	43
FG484	15	10	24	53
FG676	23	14	36	77

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 58. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a Dual-Purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSFS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the chapter "Using I/O Resources" in UG331.

Table 58: Maximum User I/O by Package

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S50A	TQ144	108	7	50	42	2	26	8	30	0
XC3S50A	FT256	144	32	64	53	20	26	15	30	51
XC3S200A		195	35	90	69	21	52	21	32	0
XC3S400A		195	35	90	69	21	52	21	32	0
XC3S200A	FG320	248	56	112	101	40	52	23	32	3
XC3S400A		251	59	112	101	42	52	24	32	0

Table 58: Maximum User I/O by Package (Continued)

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK	N.C.
XC3S400A	FG400	311	63	142	155	46	52	26	32	0
XC3S700A		311	63	142	155	46	52	26	32	0
XC3S700A	FG484	372	84	165	194	61	52	33	32	3
XC3S1400A		375	87	165	195	62	52	34	32	0
XC3S1400A	FG676	502	94	227	313	67	52	38	32	17

Notes:

- Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/bvdocs/publications/s3a_pin.zip

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A FPGA is reported using either the [XPower Power Estimator](#) or the [XPower Analyzer](#) calculator integrated in the Xilinx ISE development software. [Table 59](#) provides the thermal characteristics for the various

Spartan-3A FPGA package offerings. This information is also available using the Thermal Query tool on [xilinx.com](http://www.xilinx.com) (<http://www.xilinx.com/cgi-bin/thermal/thermal.pl>).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 59: Spartan-3A Package Thermal Characteristics

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
TQ144 TQG144	XC3S50A	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
FT256 FTG256	XC3S50A	12.4	27.6	35.8	29.4	28.4	28.1	°C/Watt
	XC3S200A	12.2	27.2	35.4	29.0	28.1	27.7	°C/Watt
	XC3S400A	8.9	21.0	30.1	24.1	23.0	22.6	°C/Watt
FG320 FGG320	XC3S200A	11.3	18.3	28.8	23.2	22.1	21.3	°C/Watt
	XC3S400A	9.4	14.9	25.5	20.1	18.8	18.0	°C/Watt
FG400 FGG400	XC3S400A	9.4	15.0	25.0	19.8	18.6	17.9	°C/Watt
	XC3S700A	8.2	13.0	23.1	17.9	16.7	16.0	°C/Watt
FG484 FGG484	XC3S700A	7.9	12.8	22.3	17.4	16.2	15.5	°C/Watt
	XC3S1400A	6.1	9.9	19.5	14.7	13.4	12.8	°C/Watt
FG676 FGG676	XC3S1400A	5.8	9.4	17.8	13.5	12.4	11.8	°C/Watt

TQ144: 144-lead Thin Quad Flat Package

The XC3S50A is available in the 144-lead thin quad flat package, TQ144.

Table 60 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 60: Spartan-3A TQ144 Pinout

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT
0	IP_0/VREF_0	P123	VREF

Table 60: Spartan-3A TQ144 Pinout (Continued)

Bank	Pin Name	Pin	Type
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	SUSPEND	P74	PWR MGMT
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

Table 60: Spartan-3A TQ144 Pinout (Continued)

Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O

Table 60: Spartan-3A TQ144 Pinout (Continued)

Bank	Pin Name	Pin	Type
3	IO_L10P_3	P27	I/O
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

User I/Os by Bank

Table 61 indicates how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 61: User I/Os Per Bank for the XC3S50A in the TQ144 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	27	14	1	1	3	8
Right	1	25	11	0	4	2	8
Bottom	2	30	2	0	21	1	6
Left	3	26	15	1	0	2	8
TOTAL		108	42	2	26	8	30

Footprint Migration Differences

The XC3S50A FPGA is the only Spartan-3A device offered in the TQ144 package.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.

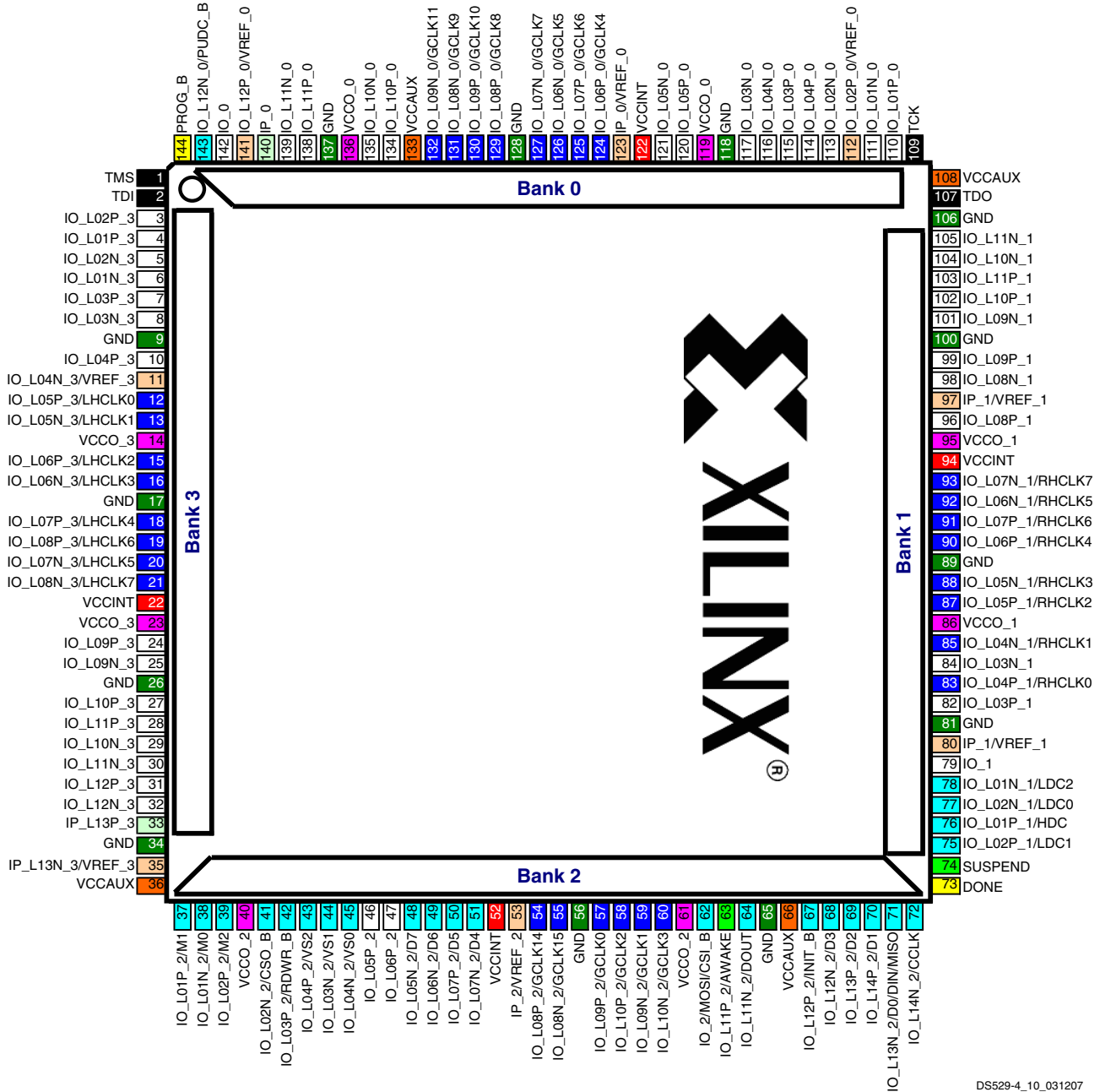


Figure 17: TQ144 Package Footprint (top view)

42	I/O: Unrestricted, general-purpose user I/O	26	DUAL: Configuration, AWAKE pins, then possible user I/O	8	VREF: User I/O or input voltage reference for bank
2	INPUT: Unrestricted, general-purpose input pin	30	CLK: User I/O, input, or global buffer input	8	VCCO: Output voltage supply for bank
3	CONFIG: Dedicated configuration pins, SUSPEND pin	4	JTAG: Dedicated JTAG port pins	4	VCCINT: Internal core supply voltage (+1.2V)
0	N.C.: Not connected	13	GND: Ground	4	VCCAUX: Auxiliary supply voltage

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3A FPGAs, including the XC3S50A, the XC3S200A, and the XC3S400A.

Table 62 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S50A, the XC3S200A, and the XC3S400A FPGAs. The XC3S50A has 51 unconnected balls, indicated as N.C. (No Connection) in Table 62 and Figure 18 and with the black diamond character (◆) in Table 62. Figure 19 provides the common footprint for the XC3S200A and XC3S400A.

Table 62 also indicates that some differential I/O pairs have different assignments between the XC3S50A and the XC3S200A/XC3S400A, highlighted in light blue. See "Footprint Migration Differences," page 83 for additional information.

All other balls have nearly identical functionality on all three devices. Table 65 summarizes the Spartan-3A FPGA footprint migration differences for the FT256 package.

The XC3S50A does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 62: Spartan-3A FT256 Pinout

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/ VREF_0	IO_L02P_0/ VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C. (◆)	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C. (◆)	IO_L06N_0/ VREF_0	E10	VREF
0	N.C. (◆)	IO_L06P_0	D10	I/O

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/ GCLK5	IO_L09N_0/ GCLK5	D9	GCLK
0	IO_L09P_0/ GCLK4	IO_L09P_0/ GCLK4	C10	GCLK
0	IO_L10N_0/ GCLK7	IO_L10N_0/ GCLK7	A9	GCLK
0	IO_L10P_0/ GCLK6	IO_L10P_0/ GCLK6	C9	GCLK
0	IO_L11N_0/ GCLK9	IO_L11N_0/ GCLK9	D8	GCLK
0	IO_L11P_0/ GCLK8	IO_L11P_0/ GCLK8	C8	GCLK
0	IO_L12N_0/ GCLK11	IO_L12N_0/ GCLK11	B8	GCLK
0	IO_L12P_0/ GCLK10	IO_L12P_0/ GCLK10	A8	GCLK
0	N.C. (◆)	IO_L13N_0	C7	I/O
0	N.C. (◆)	IO_L13P_0	A7	I/O
0	N.C. (◆)	IO_L14N_0/ VREF_0	E7	VREF
0	N.C. (◆)	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O
0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	B4	I/O
0	IO_L18P_0	IO_L18P_0	A4	I/O
0	IO_L19N_0	IO_L19N_0	B3	I/O
0	IO_L19P_0	IO_L19P_0	A3	I/O
0	IO_L20N_0/ PUDC_B	IO_L20N_0/ PUDC_B	D5	DUAL
0	IO_L20P_0/ VREF_0	IO_L20P_0/ VREF_0	C4	VREF
0	IP_0	IP_0	D6	INPUT
0	IP_0	IP_0	D12	INPUT
0	IP_0	IP_0	E6	INPUT
0	IP_0	IP_0	F7	INPUT
0	IP_0	IP_0	F9	INPUT
0	IP_0	IP_0	F10	INPUT
0	IP_0/VREF_0	IP_0/VREF_0	E9	VREF

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	B9	VCCO
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	E8	VCCO
1	IO_L01N_1/ LDC2	IO_L01N_1/ LDC2	N14	DUAL
1	IO_L01P_1/ HDC	IO_L01P_1/ HDC	N13	DUAL
1	IO_L02N_1/ LDC0	IO_L02N_1/ LDC0	P15	DUAL
1	IO_L02P_1/ LDC1	IO_L02P_1/ LDC1	R15	DUAL
1	IO_L03N_1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1	IO_L03P_1/A0	P16	DUAL
1	N.C. (◆)	IO_L05N_1/ VREF_1	M14	VREF
1	N.C. (◆)	IO_L05P_1	M13	I/O
1	N.C. (◆)	IO_L06N_1/A3	K13	DUAL
1	N.C. (◆)	IO_L06P_1/A2	L13	DUAL
1	N.C. (◆)	IO_L07N_1/A5	M16	DUAL
1	N.C. (◆)	IO_L07P_1/A4	M15	DUAL
1	N.C. (◆)	IO_L08N_1/A7	L16	DUAL
1	N.C. (◆)	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1	IO_L10N_1/A9	J13	DUAL
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/ RHCLK1	IO_L11N_1/ RHCLK1	K14	RHCLK
1	IO_L11P_1/ RHCLK0	IO_L11P_1/ RHCLK0	K15	RHCLK
1	IO_L12N_1/ TRDY1/RHCLK3	IO_L12N_1/ TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/ RHCLK2	IO_L12P_1/ RHCLK2	K16	RHCLK
1	IO_L14N_1/ RHCLK5	IO_L14N_1/ RHCLK5	H14	RHCLK
1	IO_L14P_1/ RHCLK4	IO_L14P_1/ RHCLK4	J14	RHCLK
1	IO_L15N_1/ RHCLK7	IO_L15N_1/ RHCLK7	H16	RHCLK
1	IO_L15P_1/ IRDY1/RHCLK6	IO_L15P_1/ IRDY1/RHCLK6	H15	RHCLK
1	N.C. (◆)	IO_L16N_1/A11	F16	DUAL
1	N.C. (◆)	IO_L16P_1/A10	G16	DUAL
1	N.C. (◆)	IO_L17N_1/A13	G14	DUAL
1	N.C. (◆)	IO_L17P_1/A12	H13	DUAL
1	N.C. (◆)	IO_L18N_1/A15	F15	DUAL
1	N.C. (◆)	IO_L18P_1/A14	E16	DUAL
1	N.C. (◆)	IO_L19N_1/A17	F14	DUAL
1	N.C. (◆)	IO_L19P_1/A16	G13	DUAL

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/ VREF_1	IP_L04N_1/ VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C. (◆)	IP_L09N_1	J11	INPUT
1	N.C. (◆)	IP_L09P_1/ VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/ VREF_1	IP_L21P_1/ VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/ VREF_1	IP_L25P_1/ VREF_1	F12	VREF
1	SUSPEND	SUSPEND	R16	PWR MGMT
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO
2	IO_L01N_2/M0	IO_L01N_2/M0	P4	DUAL
2	IO_L01P_2/M1	IO_L01P_2/M1	N4	DUAL
2	IO_L02N_2/ CSO_B	IO_L02N_2/ CSO_B	T2	DUAL
2	IO_L02P_2/M2	IO_L02P_2/M2	R2	DUAL
2	IO_L04P_2/VS2	IO_L03N_2/VS2	T3	DUAL
2	IO_L03P_2/ RDWR_B	IO_L03P_2/ RDWR_B	R3	DUAL
2	IO_L04N_2/VS0	IO_L04N_2/VS0	P5	DUAL
2	IO_L03N_2/VS1	IO_L04P_2/VS1	N6	DUAL
2	IO_L06P_2	IO_L05N_2	R5	I/O
2	IO_L05P_2	IO_L05P_2	T4	I/O
2	IO_L06N_2/D6	IO_L06N_2/D6	T6	DUAL
2	IO_L05N_2/D7	IO_L06P_2/D7	T5	DUAL
2	N.C. (◆)	IO_L07N_2	P6	I/O
2	N.C. (◆)	IO_L07P_2	N7	I/O
2	IO_L08N_2/D4	IO_L08N_2/D4	N8	DUAL
2	IO_L08P_2/D5	IO_L08P_2/D5	P7	DUAL

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	N.C. (◆)	IO_L09N_2/ GCLK13	T7	GCLK
2	N.C. (◆)	IO_L09P_2/ GCLK12	R7	GCLK
2	IO_L10N_2/ GCLK15	IO_L10N_2/ GCLK15	T8	GCLK
2	IO_L10P_2/ GCLK14	IO_L10P_2/ GCLK14	P8	GCLK
2	IO_L11N_2/ GCLK1	IO_L11N_2/ GCLK1	P9	GCLK
2	IO_L11P_2/ GCLK0	IO_L11P_2/ GCLK0	N9	GCLK
2	IO_L12N_2/ GCLK3	IO_L12N_2/ GCLK3	T9	GCLK
2	IO_L12P_2/ GCLK2	IO_L12P_2/ GCLK2	R9	GCLK
2	N.C. (◆)	IO_L13N_2	M10	I/O
2	N.C. (◆)	IO_L13P_2	N10	I/O
2	IO_L14P_2/ MOSI/CSI_B	IO_L14N_2/ MOSI/CSI_B	P10	DUAL
2	IO_L14N_2	IO_L14P_2	T10	I/O
2	IO_L15N_2/ DOUT	IO_L15N_2/ DOUT	R11	DUAL
2	IO_L15P_2/ AWAKE	IO_L15P_2/ AWAKE	T11	PWR MGMT
2	IO_L16N_2	IO_L16N_2	N11	I/O
2	IO_L16P_2	IO_L16P_2	P11	I/O
2	IO_L17N_2/D3	IO_L17N_2/D3	P12	DUAL
2	IO_L17P_2/ INIT_B	IO_L17P_2/ INIT_B	T12	DUAL
2	IO_L20P_2/D1	IO_L18N_2/D1	R13	DUAL
2	IO_L18P_2/D2	IO_L18P_2/D2	T13	DUAL
2	N.C. (◆)	IO_L19N_2	P13	I/O
2	N.C. (◆)	IO_L19P_2	N12	I/O
2	IO_L20N_2/ CCLK	IO_L20N_2/ CCLK	R14	DUAL
2	IO_L18N_2/D0/ DIN/MISO	IO_L20P_2/D0/ DIN/MISO	T14	DUAL
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C. (◆)	IO_L05N_3	E2	I/O
3	N.C. (◆)	IO_L05P_3	E3	I/O
3	N.C. (◆)	IO_L07N_3	G4	I/O
3	N.C. (◆)	IO_L07P_3	F3	I/O
3	IO_L08N_3/ VREF_3	IO_L08N_3/ VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C. (◆)	IO_L09N_3	H4	I/O
3	N.C. (◆)	IO_L09P_3	G3	I/O
3	N.C. (◆)	IO_L10N_3	H5	I/O
3	N.C. (◆)	IO_L10P_3	H6	I/O
3	IO_L11N_3/ LHCLK1	IO_L11N_3/ LHCLK1	H1	LHCLK
3	IO_L11P_3/ LHCLK0	IO_L11P_3/ LHCLK0	G2	LHCLK
3	IO_L12N_3/ IRDY2/LHCLK3	IO_L12N_3/ IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/ LHCLK2	IO_L12P_3/ LHCLK2	H3	LHCLK
3	IO_L14N_3/ LHCLK5	IO_L14N_3/ LHCLK5	J1	LHCLK
3	IO_L14P_3/ LHCLK4	IO_L14P_3/ LHCLK4	J2	LHCLK
3	IO_L15N_3/ LHCLK7	IO_L15N_3/ LHCLK7	K1	LHCLK
3	IO_L15P_3/ TRDY2/LHCLK6	IO_L15P_3/ TRDY2/LHCLK6	K3	LHCLK
3	N.C. (◆)	IO_L16N_3	L2	I/O
3	N.C. (◆)	IO_L16P_3/ VREF_3	L1	VREF
3	N.C. (◆)	IO_L17N_3	J6	I/O
3	N.C. (◆)	IO_L17P_3	J4	I/O
3	N.C. (◆)	IO_L18N_3	L3	I/O
3	N.C. (◆)	IO_L18P_3	K4	I/O
3	N.C. (◆)	IO_L19N_3	L4	I/O
3	N.C. (◆)	IO_L19P_3	M3	I/O
3	IO_L20N_3	IO_L20N_3	N1	I/O
3	IO_L20P_3	IO_L20P_3	M1	I/O
3	IO_L22N_3	IO_L22N_3	P1	I/O
3	IO_L22P_3	IO_L22P_3	N2	I/O

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
3	IO_L23N_3	IO_L23N_3	P2	I/O
3	IO_L23P_3	IO_L23P_3	R1	I/O
3	IO_L24N_3	IO_L24N_3	M4	I/O
3	IO_L24P_3	IO_L24P_3	N3	I/O
3	IP_L04N_3/ VREF_3	IP_L04N_3/ VREF_3	F4	VREF
3	IP_L04P_3	IP_L04P_3	E4	INPUT
3	N.C. (◆)	IP_L06N_3/ VREF_3	G5	VREF
3	N.C. (◆)	IP_L06P_3	G6	INPUT
3	IP_L13N_3	IP_L13N_3	J7	INPUT
3	IP_L13P_3	IP_L13P_3	H7	INPUT
3	IP_L21N_3	IP_L21N_3	K6	INPUT
3	IP_L21P_3	IP_L21P_3	K5	INPUT
3	IP_L25N_3/ VREF_3	IP_L25N_3/ VREF_3	L6	VREF
3	IP_L25P_3	IP_L25P_3	L5	INPUT
3	VCCO_3	VCCO_3	D2	VCCO
3	VCCO_3	VCCO_3	H2	VCCO
3	VCCO_3	VCCO_3	J5	VCCO
3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	A1	GND
GND	GND	GND	A16	GND
GND	GND	GND	B7	GND
GND	GND	GND	B11	GND
GND	GND	GND	C3	GND
GND	GND	GND	C14	GND
GND	GND	GND	E5	GND
GND	GND	GND	E12	GND
GND	GND	GND	F2	GND
GND	GND	GND	F6	GND
GND	GND	GND	G8	GND
GND	GND	GND	G10	GND
GND	GND	GND	G15	GND
GND	GND	GND	H9	GND
GND	GND	GND	J8	GND
GND	GND	GND	K2	GND
GND	GND	GND	K7	GND
GND	GND	GND	K9	GND
GND	GND	GND	L11	GND
GND	GND	GND	L15	GND
GND	GND	GND	M5	GND
GND	GND	GND	M12	GND
GND	GND	GND	P3	GND

Table 62: Spartan-3A FT256 Pinout (Continued)

Bank	XC3S50A	XC3S200A XC3S400A	FT256 Ball	Type
GND	GND	GND	P14	GND
GND	GND	GND	R6	GND
GND	GND	GND	R10	GND
GND	GND	GND	T1	GND
GND	GND	GND	T16	GND
VCCAUX	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	A2	CONFIG
VCCAUX	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	B1	JTAG
VCCAUX	TDO	TDO	B16	JTAG
VCCAUX	TMS	TMS	B2	JTAG
VCCAUX	VCCAUX	VCCAUX	E11	VCCAUX
VCCAUX	VCCAUX	VCCAUX	F5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	L12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	M6	VCCAUX
VCCINT	VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	VCCINT	G9	VCCINT
VCCINT	VCCINT	VCCINT	H8	VCCINT
VCCINT	VCCINT	VCCINT	J9	VCCINT
VCCINT	VCCINT	VCCINT	K8	VCCINT
VCCINT	VCCINT	VCCINT	K10	VCCINT

User I/Os by Bank

Table 63 and Table 64 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S50A FPGA in the FT256 package has 51 unconnected balls, labeled with an "N.C." type. These pins are also indicated in Figure 18. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 63: User I/Os Per Bank on XC3S50A in the FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	40	21	7	1	3	8
Right	1	32	12	5	4	3	8
Bottom	2	40	5	2	21	6	6
Left	3	32	15	6	0	3	8
TOTAL		144	53	20	26	15	30

Table 64: User I/Os Per Bank on XC3S200A and XC3S400A in the FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	47	27	6	1	5	8
Right	1	50	1	6	30	5	8
Bottom	2	48	11	2	21	6	8
Left	3	50	30	7	0	5	8
TOTAL		195	69	21	52	21	32

Footprint Migration Differences

Unconnected Balls on XC3S50A

Table 65 summarizes any footprint and functionality differences between the XC3S50A and the XC3S200A or XC3S400A FPGAs that might affect easy migration between devices in the FT256 package. The XC3S200A and XC3S400A have identical pinouts. The XC3S50A pinout is compatible, but there are 52 balls that are different. Generally, designs easily migrate upward from the XC3S50A to either the XC3S200A or XC3S400A. If using differential I/O, see Table 66. If using the BPI configuration mode (parallel Flash), see Table 67.

Table 65: FT256 Footprint Migration Differences

FT256 Ball	Bank	XC3S50A Type	Migration	XC3S200A/ XC3S400A Type
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O
E10	0	N.C.	→	I/O
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O
K13	1	N.C.	→	I/O
L1	3	N.C.	→	I/O

Table 65: FT256 Footprint Migration Differences (Continued)

FT256 Ball	Bank	XC3S50A Type	Migration	XC3S200A/ XC3S400A Type
L2	3	N.C.	→	I/O
L3	3	N.C.	→	I/O
L4	3	N.C.	→	I/O
L13	1	N.C.	→	I/O
L14	1	N.C.	→	I/O
L16	1	N.C.	→	I/O
M3	3	N.C.	→	I/O
M10	2	N.C.	→	I/O
M13	1	N.C.	→	I/O
M14	1	N.C.	→	I/O
M15	1	N.C.	→	I/O
M16	1	N.C.	→	I/O
N7	2	N.C.	→	I/O
N10	2	N.C.	→	I/O
N12	2	N.C.	→	I/O
P6	2	N.C.	→	I/O
P13	2	N.C.	→	I/O
R7	2	N.C.	→	I/O
T7	2	N.C.	→	I/O
DIFFERENCES			52	

Legend:



This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Differential I/O Alignment Differences

Also, some differential I/O pairs on the XC3S50A FPGA are aligned differently than the corresponding pairs on the XC3S200A or XC3S400A FPGAs, as shown in Table 66. All the mismatched pairs are in I/O Bank 2. The shading highlights the differences.

Table 66: Differential I/O Differences in FT256

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
T3	2	IO_L04P_2/VS2	IO_L03N_2/VS2
N6		IO_L03N_2/VS1	IO_L04P_2/VS1
R5		IO_L06P_2	IO_L05N_2
T5		IO_L05N_2/D7	IO_L06P_2/D7
R13		IO_L20P_2	IO_L18N_2
T14		IO_L18N_2	IO_L20P_2

XC3S50A Does Not Have BPI Mode Address Outputs

The XC3S50A FPGA does not generate the BPI-mode address pins during configuration. [Table 67](#) summarizes these differences.

Table 67: XC3S50A BPI Functional Differences

FT256 Ball	Bank	XC3S50A	XC3S200A XC3S400A
N16	1	IO_L03N_1	IO_L03N_1/A1
P16		IO_L03P_1	IO_L03P_1/A0
J13		IO_L10N_1	IO_L10N_1/A9
J12		IO_L10P_1	IO_L10P_1/A8
F13		IO_L20N_1	IO_L20N_1/A19
E14		IO_L20P_1	IO_L20P_1/A18
D15		IO_L22N_1	IO_L22N_1/A21
D16		IO_L22P_1	IO_L22P_1/A20
D14		IO_L23N_1	IO_L23N_1/A23
E13		IO_L23P_1	IO_L23P_1/A22
C15		IO_L24N_1	IO_L24N_1/A25
C16		IO_L24P_1	IO_L24P_1/A24

FT256 Footprint (XC3S50A)

		(Differential Outputs)				Bank 0				(Differential Outputs)							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	(High Output Drive)	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	N.C.	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	N.C.	I/O L04N_0	I/O L04P_0	TCK	GND
		TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	INPUT	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
		I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	N.C.	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1	I/O L24P_1
D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	N.C.	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1	I/O L22N_1	I/O L22P_1	
E	I/O L03N_3	N.C.	N.C.	INPUT L04P_3	GND	INPUT	N.C.	VCCO_0	INPUT VREF_0	N.C.	VCCAUX	GND	I/O L23P_1	I/O L20P_1	VCCO_1	N.C.	
F	I/O L08P_3	GND	N.C.	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	N.C.	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1	N.C.	N.C.	N.C.	
G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	N.C.	N.C.	N.C.	N.C.	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	N.C.	N.C.	GND	N.C.	
H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	N.C.	N.C.	N.C.	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	N.C.	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7	
J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	N.C.	VCCO_3	N.C.	INPUT L13N_3	GND	VCCINT	N.C.	N.C.	I/O L10P_1	I/O L10N_1	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3	
K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	N.C.	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	N.C.	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2	
L	N.C.	N.C.	N.C.	N.C.	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	N.C.	N.C.	GND	N.C.	
M	I/O L20P_3	VCCO_3	N.C.	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	N.C.	INPUT VREF_2	GND	N.C.	N.C.	N.C.	N.C.	
N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L03N_2 VS1	N.C.	I/O L08N_2 D4	I/O L11P_2 GCLK0	N.C.	I/O L16N_2	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1	
P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	N.C.	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14P_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	N.C.	GND	I/O L02N_1 LDC0	I/O L03P_1	
R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L06P_2	GND	N.C.	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L20P_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND	
T	GND	I/O L02N_2 CSO_B	I/O L04P_2 VS2	I/O L05P_2	I/O L05N_2 D7	I/O L06N_2 D6	N.C.	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14N_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L18N_2 D0 DIN/MISO	DONE	GND	
		(Differential Outputs)				Bank 2				(Differential Outputs)							

Figure 18: XC3S50A FT256 Package Footprint (top view)

DS529-4_09_012407

- | | | | | | |
|----|---|----|---|----|--|
| 53 | I/O: Unrestricted, general-purpose user I/O | 26 | DUAL: Configuration, AWAKE pins, then possible user I/O | 15 | VREF: User I/O or input voltage reference for bank |
| 20 | INPUT: Unrestricted, general-purpose input pin | 30 | CLK: User I/O, input, or global buffer input | 16 | VCCO: Output voltage supply for bank |
| 3 | CONFIG: Dedicated configuration pins, SUSPEND pin | 4 | JTAG: Dedicated JTAG port pins | 6 | VCCINT: Internal core supply voltage (+1.2V) |
| 51 | N.C.: Not connected (XC3S50A only) | 28 | GND: Ground | 4 | VCCAUX: Auxiliary supply voltage |

FT256 Footprint (XC3S200A, XC3S400A)

		Bank 0																
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Bank 3	A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	I/O L13P_0	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	I/O L05N_0	I/O L04N_0	I/O L04P_0	TCK	GND	
	B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	I/O L05P_0	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO	
	C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	I/O L13N_0	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1 A25	I/O L24P_1 A24	
	D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	I/O L06P_0	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1 A23	I/O L22N_1 A21	I/O L22P_1 A20	
	E	I/O L03N_3	I/O L05N_3	I/O L05P_3	INPUT L04P_3	GND	INPUT	I/O L14N_0 VREF_0	VCCO_0	INPUT VREF_0	I/O L06N_0 VREF_0	VCCAUX	GND	I/O L23P_1 A22	I/O L20P_1 A19	I/O L19N_1 A17	VCCO_1	I/O L18P_1 A14
	F	I/O L08P_3	GND	I/O L07P_3	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	I/O L14P_0	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1 A19	I/O L19N_1 A17	I/O L18N_1 A15	I/O L16N_1 A11	
	G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	I/O L09P_3	I/O L07N_3	INPUT L06N_3 VREF_3	INPUT L06P_3	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	I/O L19P_1 A16	I/O L17N_1 A13	GND	I/O L16P_1 A10	
	H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	I/O L09N_3	I/O L10N_3	I/O L10P_3	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	I/O L17P_1 A12	I/O L17N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7	
	J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	I/O L17P_3	VCCO_3	I/O L17N_3	INPUT L13N_3	GND	VCCINT	INPUT L09P_1 VREF_1	INPUT L09N_1	I/O L10P_1 A8	I/O L10N_1 A9	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3	
	K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	I/O L18P_3	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L06N_1 A3	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2	
	L	I/O L16P_3 VREF_3	I/O L16N_3	I/O L18N_3	I/O L19N_3	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	I/O L06P_1 A2	I/O L08P_1 A6	GND	I/O L08N_1 A7	
	M	I/O L20P_3	VCCO_3	I/O L19P_3	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	I/O L13N_2	INPUT VREF_2	GND	I/O L05P_1	I/O L05N_1 VREF_1	I/O L07P_1 A4	I/O L07N_1 A5	
	N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L04P_2 VS1	I/O L07P_2	I/O L08N_2 D4	I/O L11P_2 GCLK0	I/O L13P_2	I/O L16N_2	I/O L19P_2	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1 A1	
	P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	I/O L07N_2	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14N_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	I/O L19N_2	GND	I/O L02N_1 LDC0	I/O L03P_1 A0	
	R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L05N_2	GND	I/O L09P_2 GCLK12	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L18N_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND	
	T	GND	I/O L02N_2 CSO_B	I/O L03N_2 VS2	I/O L05P_2	I/O L06P_2 D7	I/O L06N_2 D6	I/O L09N_2 GCLK13	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14P_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L20P_2 D0 DIN/MISC	DONE	GND	
		Bank 2																

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Figure 19: XC3S200A and XC3S400A FT256 Package Footprint (top view)

- | | | |
|--|---|--|
| 69 I/O: Unrestricted, general-purpose user I/O | 52 DUAL: Configuration, AWAKE pins, then possible user I/O | 21 VREF: User I/O or input voltage reference for bank |
| 21 INPUT: Unrestricted, general-purpose input pin | 32 CLK: User I/O, input, or global buffer input | 16 VCCO: Output voltage supply for bank |
| 3 CONFIG: Dedicated configuration pins, SUSPEND pin | 4 JTAG: Dedicated JTAG port pins | 6 VCCINT: Internal core supply voltage (+1.2V) |
| 0 N.C.: Not connected | 28 GND: Ground | 4 VCCAUX: Auxiliary supply voltage |

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports two Spartan-3A FPGAs, the XC3S200A and the XC3S400A, as shown in Table 68 and Figure 20.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 68 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S200A and the XC3S400A FPGAs. The XC3S200A has three unconnected balls, indicated as N.C. (No Connection) in Table 68 and with the black diamond character (◆) in Table 68 and Figure 20.

All other balls have nearly identical functionality on all three devices. Table 71 summarizes the Spartan-3A FPGA footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 68: Spartan-3A FG320 Pinout

Bank	Pin Name	FG320 Ball	Type
0	IO_L01N_0	C15	I/O
0	IO_L01P_0	C16	I/O
0	IO_L02N_0	A16	I/O
0	IO_L02P_0/VREF_0	B16	VREF
0	IO_L03N_0	A14	I/O
0	IO_L03P_0	A15	I/O
0	IO_L04N_0	C14	I/O
0	IO_L04P_0	B15	I/O
0	IO_L05N_0	D12	I/O
0	IO_L05P_0	C13	I/O
0	IO_L06N_0/VREF_0	A13	VREF
0	IO_L06P_0	B13	I/O
0	IO_L07N_0	B12	I/O
0	IO_L07P_0	C12	I/O
0	IO_L08N_0	F11	I/O
0	IO_L08P_0	E11	I/O
0	IO_L09N_0	A11	I/O
0	IO_L09P_0	B11	I/O
0	IO_L10N_0	D10	I/O
0	IO_L10P_0	C11	I/O
0	IO_L11N_0/GCLK5	C9	GCLK
0	IO_L11P_0/GCLK4	B10	GCLK

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
0	IO_L12N_0/GCLK7	B9	GCLK
0	IO_L12P_0/GCLK6	A10	GCLK
0	IO_L13N_0/GCLK9	B7	GCLK
0	IO_L13P_0/GCLK8	A8	GCLK
0	IO_L14N_0/GCLK11	C8	GCLK
0	IO_L14P_0/GCLK10	B8	GCLK
0	IO_L15N_0	C7	I/O
0	IO_L15P_0	D8	I/O
0	IO_L16N_0	E9	I/O
0	IO_L16P_0	D9	I/O
0	IO_L17N_0	B6	I/O
0	IO_L17P_0	A6	I/O
0	IO_L18N_0/VREF_0	A4	VREF
0	IO_L18P_0	A5	I/O
0	IO_L19N_0	E7	I/O
0	IO_L19P_0	F8	I/O
0	IO_L20N_0	D6	I/O
0	IO_L20P_0	C6	I/O
0	IO_L21N_0	A3	I/O
0	IO_L21P_0	B4	I/O
0	IO_L22N_0	D5	I/O
0	IO_L22P_0	C5	I/O
0	IO_L23N_0	A2	I/O
0	IO_L23P_0	B3	I/O
0	IO_L24N_0/PUDC_B	E5	DUAL
0	IO_L24P_0/VREF_0	E6	VREF
0	IP_0	D13	INPUT
0	IP_0	D14	INPUT
0	IP_0	E12	INPUT
0	XC3S400A: IP_0 XC3S200A: N.C. (◆)	E13	INPUT
0	IP_0	F7	INPUT
0	IP_0	F9	INPUT
0	IP_0	F10	INPUT
0	IP_0	F12	INPUT
0	IP_0	G7	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G11	INPUT
0	IP_0/VREF_0	E10	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	D11	VCCO
0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	T17	DUAL
1	IO_L01P_1/HDC	R16	DUAL

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	U17	DUAL
1	IO_L03N_1/A1	R17	DUAL
1	IO_L03P_1/A0	T18	DUAL
1	IO_L05N_1	N16	I/O
1	IO_L05P_1	P16	I/O
1	IO_L06N_1	M14	I/O
1	IO_L06P_1	N15	I/O
1	IO_L07N_1/VREF_1	P18	VREF
1	IO_L07P_1	R18	I/O
1	IO_L09N_1/A3	M17	DUAL
1	IO_L09P_1/A2	M16	DUAL
1	IO_L10N_1/A5	N18	DUAL
1	IO_L10P_1/A4	N17	DUAL
1	IO_L11N_1/A7	L12	DUAL
1	IO_L11P_1/A6	L13	DUAL
1	IO_L13N_1/A9	K16	DUAL
1	IO_L13P_1/A8	L17	DUAL
1	IO_L14N_1/RHCLK1	K17	RHCLK
1	IO_L14P_1/RHCLK0	L18	RHCLK
1	IO_L15N_1/TRDY1/RHCLK3	J17	RHCLK
1	IO_L15P_1/RHCLK2	K18	RHCLK
1	IO_L17N_1/RHCLK5	K15	RHCLK
1	IO_L17P_1/RHCLK4	J16	RHCLK
1	IO_L18N_1/RHCLK7	H17	RHCLK
1	IO_L18P_1/IRDY1/RHCLK6	H18	RHCLK
1	IO_L19N_1/A11	G16	DUAL
1	IO_L19P_1/A10	H16	DUAL
1	IO_L21N_1	F17	I/O
1	IO_L21P_1	G17	I/O
1	IO_L22N_1/A13	E18	DUAL
1	IO_L22P_1/A12	F18	DUAL
1	IO_L23N_1/A15	H15	DUAL
1	IO_L23P_1/A14	J14	DUAL
1	IO_L25N_1	D17	I/O
1	IO_L25P_1	D18	I/O
1	IO_L26N_1/A17	E16	DUAL
1	IO_L26P_1/A16	F16	DUAL
1	IO_L27N_1/A19	F15	DUAL
1	IO_L27P_1/A18	G15	DUAL
1	IO_L29N_1/A21	E15	DUAL
1	IO_L29P_1/A20	D16	DUAL
1	IO_L30N_1/A23	B18	DUAL
1	IO_L30P_1/A22	C18	DUAL
1	IO_L31N_1/A25	B17	DUAL
1	IO_L31P_1/A24	C17	DUAL
1	IP_L04N_1/VREF_1	N14	VREF

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
1	IP_L04P_1	P15	INPUT
1	IP_L08N_1/VREF_1	L14	VREF
1	IP_L08P_1	M13	INPUT
1	IP_L12N_1	L16	INPUT
1	IP_L12P_1/VREF_1	M15	VREF
1	IP_L16N_1	K14	INPUT
1	IP_L16P_1	K13	INPUT
1	IP_L20N_1	J13	INPUT
1	IP_L20P_1/VREF_1	K12	VREF
1	IP_L24N_1	G14	INPUT
1	IP_L24P_1	H13	INPUT
1	IP_L28N_1	G13	INPUT
1	IP_L28P_1/VREF_1	H12	VREF
1	IP_L32N_1	F13	INPUT
1	IP_L32P_1/VREF_1	F14	VREF
1	SUSPEND	T16	PWR MGMT
1	VCCO_1	E17	VCCO
1	VCCO_1	H14	VCCO
1	VCCO_1	L15	VCCO
1	VCCO_1	P17	VCCO
2	IO_L01N_2/M0	U3	DUAL
2	IO_L01P_2/M1	T3	DUAL
2	IO_L02N_2/CSO_B	V3	DUAL
2	IO_L02P_2/M2	V2	DUAL
2	IO_L03N_2/VS2	U4	DUAL
2	IO_L03P_2/RDWR_B	T4	DUAL
2	IO_L04N_2	T5	I/O
2	IO_L04P_2	R5	I/O
2	IO_L05N_2/VS0	V5	DUAL
2	IO_L05P_2/VS1	V4	DUAL
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T6	I/O
2	IO_L07N_2	P8	I/O
2	IO_L07P_2	N8	I/O
2	IO_L08N_2/D6	T7	DUAL
2	IO_L08P_2/D7	R7	DUAL
2	IO_L09N_2	R9	I/O
2	IO_L09P_2	T8	I/O
2	IO_L10N_2/D4	V6	DUAL
2	IO_L10P_2/D5	U7	DUAL
2	IO_L11N_2/GCLK13	V8	GCLK
2	IO_L11P_2/GCLK12	U8	GCLK
2	IO_L12N_2/GCLK15	V9	GCLK
2	IO_L12P_2/GCLK14	U9	GCLK
2	IO_L13N_2/GCLK1	T10	GCLK
2	IO_L13P_2/GCLK0	U10	GCLK
2	IO_L14N_2/GCLK3	U11	GCLK

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
2	IO_L14P_2/GCLK2	V11	GCLK
2	IO_L15N_2	R10	I/O
2	IO_L15P_2	P10	I/O
2	IO_L16N_2/MOSI/CSI_B	T11	DUAL
2	IO_L16P_2	R11	I/O
2	IO_L17N_2	V13	I/O
2	IO_L17P_2	U12	I/O
2	IO_L18N_2/DOUT	U13	DUAL
2	IO_L18P_2/AWAKE	T12	PWR MGMT
2	IO_L19N_2	P12	I/O
2	IO_L19P_2	N12	I/O
2	IO_L20N_2/D3	R13	DUAL
2	IO_L20P_2/INIT_B	T13	DUAL
2	IO_L21N_2	T14	I/O
2	IO_L21P_2	V14	I/O
2	IO_L22N_2/D1	U15	DUAL
2	IO_L22P_2/D2	V15	DUAL
2	IO_L23N_2	T15	I/O
2	IO_L23P_2	R14	I/O
2	IO_L24N_2/CCLK	U16	DUAL
2	IO_L24P_2/D0/DIN/MISO	V16	DUAL
2	IP_2	M8	INPUT
2	IP_2	M9	INPUT
2	IP_2	M12	INPUT
2	XC3S400A: IP_2 XC3S200A: N.C. (◆)	N7	INPUT
2	IP_2	N9	INPUT
2	IP_2	N11	INPUT
2	IP_2	R6	INPUT
2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	N10	VREF
2	IP_2/VREF_2	P6	VREF
2	IP_2/VREF_2	P7	VREF
2	IP_2/VREF_2	P9	VREF
2	IP_2/VREF_2	P13	VREF
2	XC3S400A: IP_2/VREF_2 XC3S200A: N.C. (◆)	P14	VREF
2	VCCO_2	P11	VCCO
2	VCCO_2	R8	VCCO
2	VCCO_2	U5	VCCO
2	VCCO_2	U14	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	D3	I/O

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	F5	I/O
3	IO_L06N_3	E3	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	E1	I/O
3	IO_L07P_3	D1	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O
3	IO_L10N_3/VREF_3	F1	VREF
3	IO_L10P_3	F2	I/O
3	IO_L11N_3	J6	I/O
3	IO_L11P_3	J7	I/O
3	IO_L13N_3	H1	I/O
3	IO_L13P_3	H2	I/O
3	IO_L14N_3/LHCLK1	J3	LHCLK
3	IO_L14P_3/LHCLK0	H3	LHCLK
3	IO_L15N_3/IRDY2/LHCLK3	J1	LHCLK
3	IO_L15P_3/LHCLK2	J2	LHCLK
3	IO_L17N_3/LHCLK5	K5	LHCLK
3	IO_L17P_3/LHCLK4	J4	LHCLK
3	IO_L18N_3/LHCLK7	K3	LHCLK
3	IO_L18P_3/TRDY2/LHCLK6	K2	LHCLK
3	IO_L19N_3	L2	I/O
3	IO_L19P_3/VREF_3	L1	VREF
3	IO_L21N_3	M2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	N2	I/O
3	IO_L22P_3	P1	I/O
3	IO_L23N_3	L4	I/O
3	IO_L23P_3	L3	I/O
3	IO_L25N_3	R2	I/O
3	IO_L25P_3	R1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L27N_3	T2	I/O
3	IO_L27P_3	T1	I/O
3	IO_L29N_3	N6	I/O
3	IO_L29P_3	N5	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	P3	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	G6	INPUT
3	IP_L08N_3/VREF_3	H5	VREF
3	IP_L08P_3	H6	INPUT
3	IP_L12N_3	G2	INPUT

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
3	IP_L12P_3	G3	INPUT
3	IP_L16N_3	K6	INPUT
3	IP_L16P_3	J5	INPUT
3	IP_L20N_3	L6	INPUT
3	IP_L20P_3	L7	INPUT
3	IP_L24N_3	M4	INPUT
3	IP_L24P_3	M3	INPUT
3	IP_L28N_3	M5	INPUT
3	IP_L28P_3	M6	INPUT
3	IP_L32N_3/VREF_3	P4	VREF
3	IP_L32P_3	P5	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L5	VCCO
3	VCCO_3	P2	VCCO
GND	GND	A1	GND
GND	GND	A7	GND
GND	GND	A12	GND
GND	GND	A18	GND
GND	GND	C10	GND
GND	GND	D4	GND
GND	GND	D7	GND
GND	GND	D15	GND
GND	GND	F6	GND
GND	GND	G1	GND
GND	GND	G12	GND
GND	GND	G18	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	J11	GND
GND	GND	J15	GND
GND	GND	K4	GND
GND	GND	K8	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	M1	GND
GND	GND	M7	GND
GND	GND	M18	GND
GND	GND	N13	GND
GND	GND	R4	GND
GND	GND	R12	GND
GND	GND	R15	GND
GND	GND	T9	GND
GND	GND	V1	GND
GND	GND	V7	GND
GND	GND	V12	GND
GND	GND	V18	GND

Table 68: Spartan-3A FG320 Pinout (Continued)

Bank	Pin Name	FG320 Ball	Type
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A17	JTAG
VCCAUX	TDI	E4	JTAG
VCCAUX	TDO	E14	JTAG
VCCAUX	TMS	C3	JTAG
VCCAUX	VCCAUX	A9	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	J12	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	M10	VCCAUX
VCCAUX	VCCAUX	V10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT

User I/Os by Bank

Table 69 and Table 70 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 69: User I/Os Per Bank for XC3S200A in the FG320 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	60	35	11	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	60	19	6	21	6	8
Left	3	64	38	13	0	5	8
TOTAL		248	101	40	52	23	32

Table 70: User I/Os Per Bank for XC3S400A in the FG320 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	61	35	12	1	5	8
Right	1	64	9	10	30	7	8
Bottom	2	62	19	7	21	7	8
Left	3	64	38	13	0	5	8
TOTAL		251	101	42	52	24	32

Footprint Migration Differences

Table 71 summarizes any footprint and functionality differences between the XC3S200A and the XC3S400A FPGAs that might affect easy migration between devices available in the FG320 package. There are three such balls. All other pins not listed in Table 71 unconditionally migrate between Spartan-3A devices available in the FG320 package.

The arrows indicate the direction for easy migration.

Table 71: FG320 Footprint Migration Differences

Pin	Bank	XC3S200A	Migration	XC3S400A
E13	0	N.C.	→	INPUT
N7	2	N.C.	→	INPUT
P14	2	N.C.	→	INPUT/VREF
DIFFERENCES			3	

Legend:

- This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FG320 Footprint

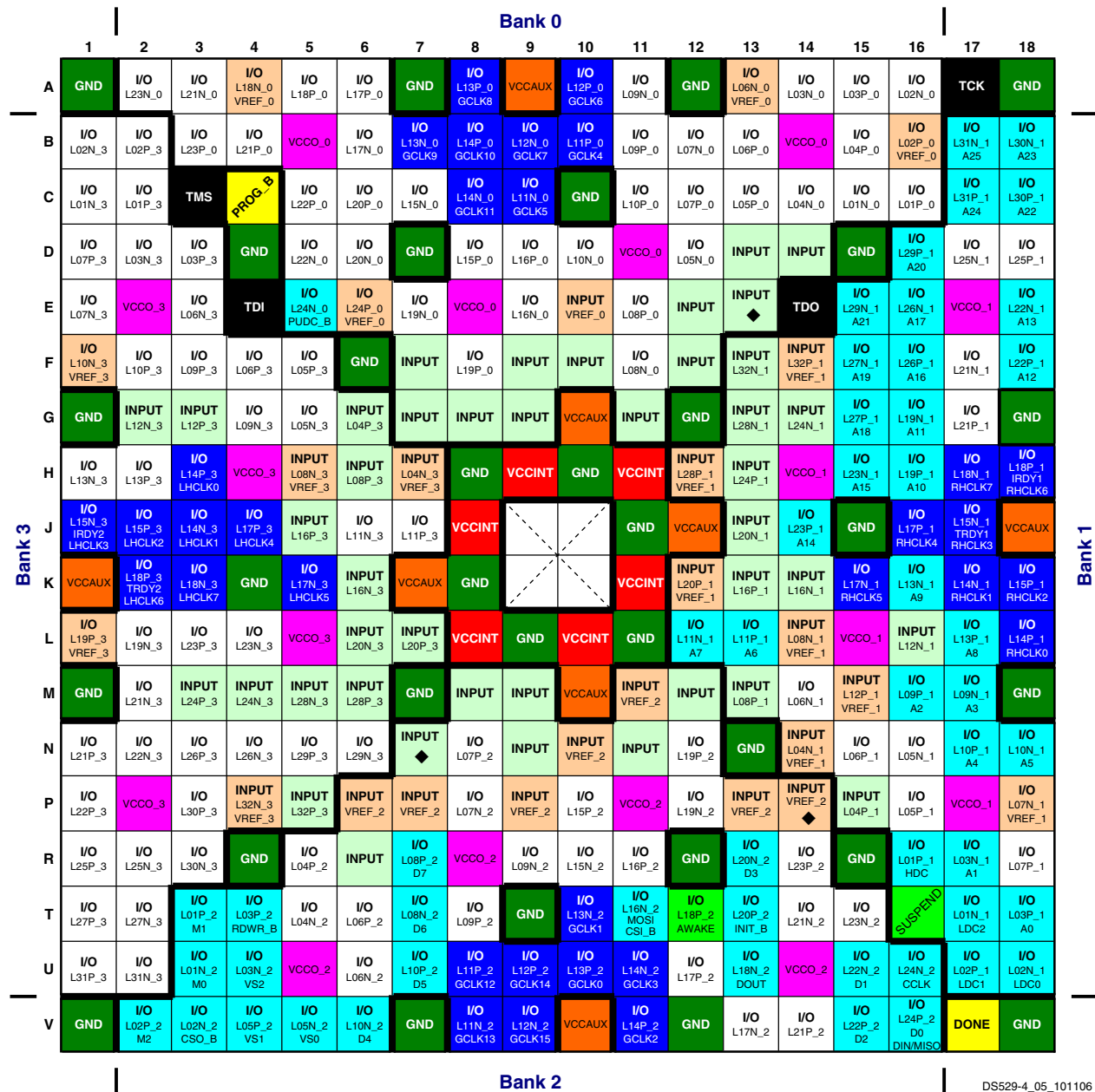


Figure 20: FG320 Package Footprint (top view)

101	I/O: Unrestricted, general-purpose user I/O	52	DUAL: Configuration, AWAKE pins, then possible user-I/O	23 - 24	VREF: User I/O or input voltage reference for bank
40 - 42	INPUT: Unrestricted, general-purpose input pin	32	CLK: User I/O, input, or global buffer input	16	VCC0: Output voltage supply for bank
3	CONFIG: Dedicated configuration pins, SUSPEND pin	4	JTAG: Dedicated JTAG port pins	6	VCCINT: Internal core supply voltage (+1.2V)
3	N.C.: Not connected. Only the XC3S200A has these pins (◆).	32	GND: Ground	8	VCCAUX: Auxiliary supply voltage

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3A FPGAs, the XC3S400A and the XC3S700A. Both devices share a common footprint for this package as shown in [Table 72](#) and [Figure 21](#).

[Table 72](#) lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 72: Spartan-3A FG400 Pinout

Bank	Pin Name	FG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O
0	IO_L32N_0/PUDC_B	B2	DUAL
0	IO_L32P_0/VREF_0	A2	VREF
0	IP_0	E14	INPUT
0	IP_0	F11	INPUT
0	IP_0	F14	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
0	IP_0	G10	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	H9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H11	INPUT
0	IP_0	H12	INPUT
0	IP_0/VREF_0	G11	VREF
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/LDC2	V20	DUAL
1	IO_L01P_1/HDC	W20	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	V19	DUAL
1	IO_L03N_1/A1	R16	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	T20	I/O
1	IO_L05P_1	T18	I/O
1	IO_L06N_1	U20	I/O
1	IO_L06P_1	U19	I/O
1	IO_L07N_1	P17	I/O
1	IO_L07P_1	P16	I/O
1	IO_L08N_1	R17	I/O
1	IO_L08P_1	R18	I/O
1	IO_L09N_1	R20	I/O
1	IO_L09P_1	R19	I/O
1	IO_L10N_1/VREF_1	P20	VREF
1	IO_L10P_1	P18	I/O
1	IO_L12N_1/A3	N17	DUAL
1	IO_L12P_1/A2	N15	DUAL
1	IO_L13N_1/A5	N19	DUAL
1	IO_L13P_1/A4	N18	DUAL
1	IO_L14N_1/A7	M18	DUAL
1	IO_L14P_1/A6	M17	DUAL
1	IO_L16N_1/A9	L16	DUAL
1	IO_L16P_1/A8	L15	DUAL
1	IO_L17N_1/RHCLK1	M20	RHCLK
1	IO_L17P_1/RHCLK0	M19	RHCLK

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
1	IO_L18N_1/TRDY1/RHCLK3	L18	RHCLK
1	IO_L18P_1/RHCLK2	L19	RHCLK
1	IO_L20N_1/RHCLK5	L17	RHCLK
1	IO_L20P_1/RHCLK4	K18	RHCLK
1	IO_L21N_1/RHCLK7	J20	RHCLK
1	IO_L21P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L22N_1/A11	J18	DUAL
1	IO_L22P_1/A10	J19	DUAL
1	IO_L24N_1	K16	I/O
1	IO_L24P_1	J17	I/O
1	IO_L25N_1/A13	H18	DUAL
1	IO_L25P_1/A12	H19	DUAL
1	IO_L26N_1/A15	G20	DUAL
1	IO_L26P_1/A14	H20	DUAL
1	IO_L28N_1	H17	I/O
1	IO_L28P_1	G18	I/O
1	IO_L29N_1/A17	F19	DUAL
1	IO_L29P_1/A16	F20	DUAL
1	IO_L30N_1/A19	F18	DUAL
1	IO_L30P_1/A18	G17	DUAL
1	IO_L32N_1	E19	I/O
1	IO_L32P_1	E20	I/O
1	IO_L33N_1	F17	I/O
1	IO_L33P_1	E18	I/O
1	IO_L34N_1	D18	I/O
1	IO_L34P_1	D20	I/O
1	IO_L36N_1/A21	F16	DUAL
1	IO_L36P_1/A20	G16	DUAL
1	IO_L37N_1/A23	C19	DUAL
1	IO_L37P_1/A22	C20	DUAL
1	IO_L38N_1/A25	B19	DUAL
1	IO_L38P_1/A24	B20	DUAL
1	IP_1/VREF_1	N14	VREF
1	IP_L04N_1/VREF_1	P15	VREF
1	IP_L04P_1	P14	INPUT
1	IP_L11N_1/VREF_1	M15	VREF
1	IP_L11P_1	M16	INPUT
1	IP_L15N_1	M13	INPUT
1	IP_L15P_1/VREF_1	M14	VREF
1	IP_L19N_1	L13	INPUT
1	IP_L19P_1	L14	INPUT
1	IP_L23N_1	K14	INPUT

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
1	IP_L23P_1/VREF_1	K15	VREF
1	IP_L27N_1	J15	INPUT
1	IP_L27P_1	J16	INPUT
1	IP_L31N_1	J13	INPUT
1	IP_L31P_1/VREF_1	J14	VREF
1	IP_L35N_1	H14	INPUT
1	IP_L35P_1	H15	INPUT
1	IP_L39N_1	G14	INPUT
1	IP_L39P_1/VREF_1	G15	VREF
1	SUSPEND	R15	PWR MGMT
1	VCCO_1	D19	VCCO
1	VCCO_1	H16	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N16	VCCO
1	VCCO_1	T19	VCCO
2	IO_L01N_2/M0	V4	DUAL
2	IO_L01P_2/M1	U4	DUAL
2	IO_L02N_2/CSO_B	Y2	DUAL
2	IO_L02P_2/M2	W3	DUAL
2	IO_L03N_2	W4	I/O
2	IO_L03P_2	Y3	I/O
2	IO_L04N_2	R7	I/O
2	IO_L04P_2	T6	I/O
2	IO_L05N_2	U5	I/O
2	IO_L05P_2	V5	I/O
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T7	I/O
2	IO_L07N_2/VS2	U7	DUAL
2	IO_L07P_2/RDWR_B	T8	DUAL
2	IO_L08N_2	Y5	I/O
2	IO_L08P_2	Y4	I/O
2	IO_L09N_2/VS0	W6	DUAL
2	IO_L09P_2/VS1	V6	DUAL
2	IO_L10N_2	Y7	I/O
2	IO_L10P_2	Y6	I/O
2	IO_L11N_2	U9	I/O
2	IO_L11P_2	T9	I/O
2	IO_L12N_2/D6	W8	DUAL
2	IO_L12P_2/D7	V7	DUAL
2	IO_L13N_2	V9	I/O
2	IO_L13P_2	V8	I/O
2	IO_L14N_2/D4	T10	DUAL

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
2	IO_L14P_2/D5	U10	DUAL
2	IO_L15N_2/GCLK13	Y9	GCLK
2	IO_L15P_2/GCLK12	W9	GCLK
2	IO_L16N_2/GCLK15	W10	GCLK
2	IO_L16P_2/GCLK14	V10	GCLK
2	IO_L17N_2/GCLK1	V11	GCLK
2	IO_L17P_2/GCLK0	Y11	GCLK
2	IO_L18N_2/GCLK3	V12	GCLK
2	IO_L18P_2/GCLK2	U11	GCLK
2	IO_L19N_2	R12	I/O
2	IO_L19P_2	T12	I/O
2	IO_L20N_2/MOSI/CSI_B	W12	DUAL
2	IO_L20P_2	Y12	I/O
2	IO_L21N_2	W13	I/O
2	IO_L21P_2	Y13	I/O
2	IO_L22N_2/DOUT	V13	DUAL
2	IO_L22P_2/AWAKE	U13	PWR MGMT
2	IO_L23N_2	R13	I/O
2	IO_L23P_2	T13	I/O
2	IO_L24N_2/D3	W14	DUAL
2	IO_L24P_2/INIT_B	Y14	DUAL
2	IO_L25N_2	T14	I/O
2	IO_L25P_2	V14	I/O
2	IO_L26N_2/D1	V15	DUAL
2	IO_L26P_2/D2	Y15	DUAL
2	IO_L27N_2	T15	I/O
2	IO_L27P_2	U15	I/O
2	IO_L28N_2	W16	I/O
2	IO_L28P_2	Y16	I/O
2	IO_L29N_2	U16	I/O
2	IO_L29P_2	V16	I/O
2	IO_L30N_2	Y18	I/O
2	IO_L30P_2	Y17	I/O
2	IO_L31N_2	U17	I/O
2	IO_L31P_2	V17	I/O
2	IO_L32N_2/CCLK	Y19	DUAL
2	IO_L32P_2/D0/DIN/MISO	W18	DUAL
2	IP_2	P9	INPUT
2	IP_2	P12	INPUT
2	IP_2	P13	INPUT
2	IP_2	R8	INPUT
2	IP_2	R10	INPUT

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
2	IP_2	T11	INPUT
2	IP_2/VREF_2	N9	VREF
2	IP_2/VREF_2	N12	VREF
2	IP_2/VREF_2	P8	VREF
2	IP_2/VREF_2	P10	VREF
2	IP_2/VREF_2	P11	VREF
2	IP_2/VREF_2	R14	VREF
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D3	I/O
3	IO_L01P_3	D4	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	C1	I/O
3	IO_L05N_3	E1	I/O
3	IO_L05P_3	D1	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	J5	I/O
3	IO_L07P_3	J6	I/O
3	IO_L08N_3	H4	I/O
3	IO_L08P_3	H6	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O
3	IO_L10N_3	F2	I/O
3	IO_L10P_3	E3	I/O
3	IO_L12N_3	H2	I/O
3	IO_L12P_3	G3	I/O
3	IO_L13N_3/VREF_3	G1	VREF
3	IO_L13P_3	F1	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	J4	I/O
3	IO_L16N_3	J2	I/O
3	IO_L16P_3	J3	I/O
3	IO_L17N_3/LHCLK1	K2	LHCLK
3	IO_L17P_3/LHCLK0	J1	LHCLK
3	IO_L18N_3/IRDY2/LHCLK3	L3	LHCLK

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
3	IO_L18P_3/LHCLK2	K3	LHCLK
3	IO_L20N_3/LHCLK5	L5	LHCLK
3	IO_L20P_3/LHCLK4	K4	LHCLK
3	IO_L21N_3/LHCLK7	M1	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	L1	LHCLK
3	IO_L22N_3	M3	I/O
3	IO_L22P_3/VREF_3	M2	VREF
3	IO_L24N_3	M5	I/O
3	IO_L24P_3	M4	I/O
3	IO_L25N_3	N2	I/O
3	IO_L25P_3	N1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P4	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	R2	I/O
3	IO_L32N_3	T2	I/O
3	IO_L32P_3/VREF_3	T1	VREF
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	T3	I/O
3	IO_L34N_3	U3	I/O
3	IO_L34P_3	U1	I/O
3	IO_L36N_3	T4	I/O
3	IO_L36P_3	R5	I/O
3	IO_L37N_3	V2	I/O
3	IO_L37P_3	V1	I/O
3	IO_L38N_3	W2	I/O
3	IO_L38P_3	W1	I/O
3	IP_3	H7	INPUT
3	IP_L04N_3/VREF_3	G6	VREF
3	IP_L04P_3	G7	INPUT
3	IP_L11N_3/VREF_3	J7	VREF
3	IP_L11P_3	J8	INPUT
3	IP_L15N_3	K7	INPUT
3	IP_L15P_3	K8	INPUT
3	IP_L19N_3	K5	INPUT
3	IP_L19P_3	K6	INPUT
3	IP_L23N_3	L6	INPUT
3	IP_L23P_3	L7	INPUT

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
3	IP_L27N_3	M7	INPUT
3	IP_L27P_3	M8	INPUT
3	IP_L31N_3	N7	INPUT
3	IP_L31P_3	M6	INPUT
3	IP_L35N_3	N6	INPUT
3	IP_L35P_3	P5	INPUT
3	IP_L39N_3/VREF_3	P7	VREF
3	IP_L39P_3	P6	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	N5	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B6	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D9	GND
GND	GND	E5	GND
GND	GND	E12	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	H13	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N8	GND
GND	GND	N11	GND

Table 72: Spartan-3A FG400 Pinout (Continued)

Bank	Pin Name	FG400 Ball	Type
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R9	GND
GND	GND	T16	GND
GND	GND	U12	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W15	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	W19	CONFIG
VCCAUX	PROG_B	D5	CONFIG
VCCAUX	TCK	A19	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E17	JTAG
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 73 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FG400 package. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 73: User I/Os Per Bank for the XC3S400A and XC3S700A in the FG400 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
TOTAL		311	155	46	52	26	32

Footprint Migration Differences

The XC3S400A and XC3S700A FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S400A and XC3S700A FPGAs without further consideration.

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FG400 Footprint

Left Half of FG400 Package (top view)

- 155 **I/O:** Unrestricted, general-purpose user I/O
- 46 **INPUT:** Unrestricted, general-purpose input pin
- 52 **DUAL:** Configuration, AWAKE pins, then possible user I/O
- 26 **VREF:** User I/O or input voltage reference for bank
- 32 **CLK:** User I/O, input, or clock buffer input
- 3 **CONFIG:** Dedicated configuration pins, SUSPEND pin
- 4 **JTAG:** Dedicated JTAG port pins
- 43 **GND:** Ground
- 22 **VCCO:** Output voltage supply for bank
- 9 **VCCINT:** Internal core supply voltage (+1.2V)
- 8 **VCCAUX:** Auxiliary supply voltage

		Bank 0									
		1	2	3	4	5	6	7	8	9	10
Bank 3	A	GND	I/O L32P_0 VREF_0	I/O L30P_0	I/O L29P_0	I/O L26P_0	I/O L25P_0	I/O L24N_0	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10	I/O L16P_0 GCLK6
	B	I/O L02P_3	I/O L32N_0 PUDC_B	I/O L30N_0	VCCO_0	I/O L26N_0	GND	I/O L24P_0	I/O L20P_0	I/O L19P_0	VCCO_0
	C	I/O L03P_3	I/O L02N_3	GND	I/O L29N_0	I/O L28P_0	I/O L25N_0	I/O L21P_0	I/O L20N_0	I/O L19N_0	I/O L16N_0 GCLK7
	D	I/O L05P_3	I/O L03N_3	I/O L01N_3	I/O L01P_3	PROG_B	I/O L28N_0	VCCO_0	I/O L21N_0	GND	I/O L17P_0 GCLK8
	E	I/O L05N_3	VCCO_3	I/O L10P_3	TMS	GND	I/O L31P_0	I/O L27P_0	I/O L23P_0	I/O L22P_0	I/O L17N_0 GCLK9
	F	I/O L13P_3	I/O L10N_3	I/O L09P_3	I/O L06P_3	TDI	I/O L31N_0	I/O L27N_0	I/O L23N_0	I/O L22N_0 VREF_0	VCCO_0
	G	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L09N_3	I/O L06N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT	INPUT	INPUT
	H	VCCAUX	I/O L12N_3	I/O L14N_3	I/O L08N_3	VCCO_3	I/O L08P_3	INPUT	GND	INPUT	INPUT
	J	I/O L17P_3 LHCLK0	I/O L16N_3	I/O L16P_3	I/O L14P_3	I/O L07N_3	I/O L07P_3	INPUT L11N_3 VREF_3	INPUT L11P_3	GND	VCCINT
	K	GND	I/O L17N_3 LHCLK1	I/O L18P_3 LHCLK2	I/O L20P_3 LHCLK4	INPUT L19N_3	INPUT L19P_3	INPUT L15N_3	INPUT L15P_3	VCCINT	GND
	L	I/O L21P_3 TRDY2 LHCLK6	VCCO_3	I/O L18N_3 IRDY2 LHCLK3	GND	I/O L20N_3 LHCLK5	INPUT L23N_3	INPUT L23P_3	VCCAUX	GND	VCCINT
	M	I/O L21N_3 LHCLK7	I/O L22P_3 VREF_3	I/O L22N_3	I/O L24P_3	I/O L24N_3	INPUT L31P_3	INPUT L27N_3	INPUT L27P_3	VCCINT	GND
	N	I/O L25P_3	I/O L25N_3	I/O L26P_3	I/O L26N_3	VCCO_3	INPUT L35N_3	INPUT L31N_3	GND	INPUT VREF_2	VCCINT
	P	I/O L28P_3	GND	I/O L29P_3	I/O L29N_3	INPUT L35P_3	INPUT L39P_3	INPUT L39N_3 VREF_3	INPUT VREF_2	INPUT	INPUT VREF_2
	R	I/O L28N_3	I/O L30P_3	I/O L30N_3	I/O L33N_3	I/O L36P_3	GND	I/O L04N_2	INPUT	GND	INPUT
	T	I/O L32P_3 VREF_3	I/O L32N_3	I/O L33P_3	I/O L36N_3	VCCAUX	I/O L04P_2	I/O L06P_2	I/O L07P_2 RDWR_B	I/O L11P_2	I/O L14N_2 D4
	U	I/O L34P_3	VCCO_3	I/O L34N_3	I/O L01P_2 M1	I/O L05N_2	I/O L06N_2	I/O L07N_2 VS2	VCCO_2	I/O L11N_2	I/O L14P_2 D5
	V	I/O L37P_3	I/O L37N_3	GND	I/O L01N_2 M0	I/O L05P_2	I/O L09P_2 VS1	I/O L12P_2 D7	I/O L13P_2	I/O L13N_2	I/O L16P_2 GCLK14
	W	I/O L38P_3	I/O L38N_3	I/O L02P_2 M2	I/O L03N_2	VCCO_2	I/O L09N_2 VS0	GND	I/O L12N_2 D6	I/O L15P_2 GCLK12	I/O L16N_2 GCLK15
Y	GND	I/O L02N_2 CSO_B	I/O L03P_2	I/O L08P_2	I/O L08N_2	I/O L10P_2	I/O L10N_2	VCCAUX	I/O L15N_2 GCLK13	GND	
		Bank 2									

Figure 21: FG400 Package Footprint (top view)

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Bank 0										A
11	12	13	14	15	16	17	18	19	20	
GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND	B
I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24	C
I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22	D
I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1	E
I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1	F
INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16	G
INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15	H
INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14	J
GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7	K
VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6	L
GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND	M
VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1	N
GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX	P
INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1	R
VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1	T
INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1	U
I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1	V
I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2	W
VCCO_2	I/O L20N_2 MOSI CSL_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC	Y
I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND	

Right Half of FG400 Package (top view)

Bank 2

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FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports both the XC3S700A and the XC3S1400A FPGAs. There are three pinout differences, as described in [Table 77](#).

[Table 74](#) lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The shaded rows indicate pinout differences between the XC3S700A and the XC3S1400A FPGAs. The XC3S700A has three unconnected balls, indicated as N.C. (No Connection) in [Table 74](#) and with the black diamond character (◆) in [Table 74](#) and [Figure 22](#).

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 74: Spartan-3A FG484 Pinout

Bank	Pin Name	FG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O
0	IO_L30P_0	E9	I/O
0	IO_L31N_0	B4	I/O
0	IO_L31P_0	A4	I/O
0	IO_L32N_0	D5	I/O
0	IO_L32P_0	C5	I/O
0	IO_L33N_0	B3	I/O
0	IO_L33P_0	A3	I/O

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
0	IO_L34N_0	F8	I/O
0	IO_L34P_0	E7	I/O
0	IO_L35N_0	E6	I/O
0	IO_L35P_0	F7	I/O
0	IO_L36N_0/PUDC_B	A2	DUAL
0	IO_L36P_0/VREF_0	B2	VREF
0	IP_0	E16	INPUT
0	IP_0	E8	INPUT
0	IP_0	F10	INPUT
0	IP_0	F12	INPUT
0	IP_0	F16	INPUT
0	IP_0	G10	INPUT
0	IP_0	G11	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	G14	INPUT
0	IP_0	G15	INPUT
0	IP_0	G16	INPUT
0	IP_0	G7	INPUT
0	IP_0	G9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H13	INPUT
0	IP_0	H14	INPUT
0	IP_0/VREF_0	G8	VREF
0	IP_0/VREF_0	H12	VREF
0	IP_0/VREF_0	H9	VREF
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	F9	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	AA22	DUAL
1	IO_L02N_1/LDC0	W20	DUAL
1	IO_L02P_1/LDC1	W19	DUAL
1	IO_L03N_1/A1	T18	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	W21	I/O
1	IO_L05P_1	Y22	I/O
1	IO_L06N_1	V20	I/O
1	IO_L06P_1	V19	I/O
1	IO_L07N_1	V22	I/O

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
1	IO_L07P_1	W22	I/O
1	IO_L09N_1	U21	I/O
1	IO_L09P_1	U22	I/O
1	IO_L10N_1	U19	I/O
1	IO_L10P_1	U20	I/O
1	IO_L11N_1	T22	I/O
1	IO_L11P_1	T20	I/O
1	IO_L13N_1	T19	I/O
1	IO_L13P_1	R20	I/O
1	IO_L14N_1	R22	I/O
1	IO_L14P_1	R21	I/O
1	IO_L15N_1/VREF_1	P22	VREF
1	IO_L15P_1	P20	I/O
1	IO_L17N_1/A3	P18	DUAL
1	IO_L17P_1/A2	R19	DUAL
1	IO_L18N_1/A5	N21	DUAL
1	IO_L18P_1/A4	N22	DUAL
1	IO_L19N_1/A7	N19	DUAL
1	IO_L19P_1/A6	N20	DUAL
1	IO_L20N_1/A9	N17	DUAL
1	IO_L20P_1/A8	N18	DUAL
1	IO_L21N_1/RHCLK1	L22	RHCLK
1	IO_L21P_1/RHCLK0	M22	RHCLK
1	IO_L22N_1/TRDY1/RHCLK3	L20	RHCLK
1	IO_L22P_1/RHCLK2	L21	RHCLK
1	IO_L24N_1/RHCLK5	M20	RHCLK
1	IO_L24P_1/RHCLK4	M18	RHCLK
1	IO_L25N_1/RHCLK7	K19	RHCLK
1	IO_L25P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L26N_1/A11	J22	DUAL
1	IO_L26P_1/A10	K22	DUAL
1	IO_L28N_1	L19	I/O
1	IO_L28P_1	L18	I/O
1	IO_L29N_1/A13	J20	DUAL
1	IO_L29P_1/A12	J21	DUAL
1	IO_L30N_1/A15	G22	DUAL
1	IO_L30P_1/A14	H22	DUAL
1	IO_L32N_1	K18	I/O
1	IO_L32P_1	K17	I/O
1	IO_L33N_1/A17	H20	DUAL
1	IO_L33P_1/A16	H21	DUAL
1	IO_L34N_1/A19	F21	DUAL
1	IO_L34P_1/A18	F22	DUAL

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
1	IO_L36N_1	G20	I/O
1	IO_L36P_1	G19	I/O
1	IO_L37N_1	H19	I/O
1	IO_L37P_1	J18	I/O
1	IO_L38N_1	F20	I/O
1	IO_L38P_1	E20	I/O
1	IO_L40N_1	F18	I/O
1	IO_L40P_1	F19	I/O
1	IO_L41N_1	D22	I/O
1	IO_L41P_1	E22	I/O
1	IO_L42N_1	D20	I/O
1	IO_L42P_1	D21	I/O
1	IO_L44N_1/A21	C21	DUAL
1	IO_L44P_1/A20	C22	DUAL
1	IO_L45N_1/A23	B21	DUAL
1	IO_L45P_1/A22	B22	DUAL
1	IO_L46N_1/A25	G17	DUAL
1	IO_L46P_1/A24	G18	DUAL
1	IP_L04N_1/VREF_1	R16	VREF
1	IP_L04P_1	R15	INPUT
1	IP_L08N_1	P16	INPUT
1	IP_L08P_1	P15	INPUT
1	IP_L12N_1/VREF_1	R18	VREF
1	IP_L12P_1	R17	INPUT
1	IP_L16N_1/VREF_1	N16	VREF
1	IP_L16P_1	N15	INPUT
1	IP_L23N_1	M16	INPUT
1	IP_L23P_1	M17	INPUT
1	IP_L27N_1	L16	INPUT
1	IP_L27P_1/VREF_1	M15	VREF
1	IP_L31N_1	K16	INPUT
1	IP_L31P_1	L15	INPUT
1	IP_L35N_1	K15	INPUT
1	IP_L35P_1/VREF_1	K14	VREF
1	IP_L39N_1	H18	INPUT
1	IP_L39P_1	H17	INPUT
1	IP_L43N_1/VREF_1	J15	VREF
1	IP_L43P_1	J16	INPUT
1	IP_L47N_1	H15	INPUT
1	IP_L47P_1/VREF_1	H16	VREF
1	SUSPEND	U18	PWR MGMT
1	VCCO_1	E21	VCCO

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
1	VCCO_1	J17	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P17	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01N_2/M0	W5	DUAL
2	IO_L01P_2/M1	V6	DUAL
2	IO_L02N_2/CSO_B	Y4	DUAL
2	IO_L02P_2/M2	W4	DUAL
2	IO_L03N_2	AA3	I/O
2	IO_L03P_2	AB2	I/O
2	IO_L04N_2	AA4	I/O
2	IO_L04P_2	AB3	I/O
2	IO_L05N_2	Y5	I/O
2	IO_L05P_2	W6	I/O
2	IO_L06N_2	AB5	I/O
2	IO_L06P_2	AB4	I/O
2	IO_L07N_2	Y6	I/O
2	IO_L07P_2	W7	I/O
2	IO_L08N_2	AB6	I/O
2	IO_L08P_2	AA6	I/O
2	IO_L09N_2/VS2	W9	DUAL
2	IO_L09P_2/RDWR_B	V9	DUAL
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/ DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400A: IP_2 XC3S700A: N.C. (◆)	U16	INPUT
2	XC3S1400A: IP_2 XC3S700A: N.C. (◆)	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400A: IP_2/VREF_2 XC3S700A: N.C. (◆)	T8	VREF
2	IP_2/VREF_2	V8	VREF
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND
GND	GND	F11	GND
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND

Table 74: Spartan-3A FG484 Pinout (Continued)

Bank	Pin Name	FG484 Ball	Type
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	DONE	Y19	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E19	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	H11	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	P11	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

User I/Os by Bank

Table 75 and Table 76 indicate how the user-I/O pins are distributed between the four I/O banks on the FG484

package. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 75: User I/Os Per Bank for the XC3S700A in the FG484 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	92	42	12	21	9	8
Left	3	94	61	17	0	8	8
TOTAL		372	194	61	52	33	32

Table 76: User I/Os Per Bank for the XC3S1400A in the FG484 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	95	43	13	21	10	8
Left	3	94	61	17	0	8	8
TOTAL		375	195	62	52	34	32

Footprint Migration Differences

Table 77 summarizes any footprint and functionality differences between the XC3S700A and the XC3S1400A FPGAs that might affect easy migration between devices available in the FG484 package. There are three such balls. All other pins not listed in Table 77 unconditionally migrate between Spartan-3A devices available in the FG484 package.

The arrows indicate the direction for easy migration.

Table 77: **FG484 Footprint Migration Differences**

Pin	Bank	XC3S700A	Migration	XC3S1400A
T8	0	N.C.	→	INPUT
U7	2	N.C.	→	INPUT
U16	2	N.C.	→	I/O
DIFFERENCES			3	

Legend:

- This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FG484 Footprint

Left Half of FG484 Package (top view)

- 194-195 **I/O:** Unrestricted, general-purpose user I/O
- 61-62 **INPUT:** Unrestricted, general-purpose input pin
- 52 **DUAL:** Configuration, AWAKE pins, then possible user I/O
- 33-34 **VREF:** User I/O or input voltage reference for bank
- 32 **CLK:** User I/O, input, or clock buffer input
- 3 **CONFIG:** Dedicated configuration pins, SUSPEND pin
- 4 **JTAG:** Dedicated JTAG port pins
- 53 **GND:** Ground
- 24 **VCCO:** Output voltage supply for bank
- 15 **VCCINT:** Internal core supply voltage (+1.2V)
- 10 **VCCAUX:** Auxiliary supply voltage
- 3 **N.C.:** Not connected (XC3S700A only)

		Bank 0										
		1	2	3	4	5	6	7	8	9	10	11
Bank 3	A	GND	I/O L36N_0 PUDC_B	I/O L33P_0	I/O L31P_0	I/O L28N_0	I/O L26N_0	I/O L26P_0	I/O L22N_0	I/O L22P_0	I/O L21P_0	I/O L18N_0 GCLK7
	B	I/O L02P_3	I/O L36P_0 VREF_0	I/O L33N_0	I/O L31N_0	VCCO_0	I/O L28P_0	GND	I/O L25P_0	I/O L24P_0	VCCO_0	I/O L19P_0 GCLK8
	C	I/O L01P_3	I/O L02N_3	GND	PROG_B	I/O L32P_0	I/O L29P_0	I/O L27N_0	I/O L25N_0	I/O L24N_0 VREF_0	I/O L21N_0	I/O L19N_0 GCLK9
	D	I/O L06P_3	I/O L01N_3	I/O L03P_3	TMS	I/O L32N_0	I/O L29N_0	I/O L27P_0	I/O L30N_0	GND	I/O L23P_0	I/O L20P_0 GCLK10
	E	I/O L06N_3	VCCO_3	I/O L07N_3	I/O L03N_3	VCCAUX	I/O L35N_0	I/O L34P_0	INPUT	I/O L30P_0	I/O L23N_0	I/O L20N_0 GCLK11
	F	I/O L12N_3	I/O L12P_3	I/O L08P_3	I/O L07P_3	TDI	GND	I/O L35P_0	I/O L34N_0	VCCO_0	INPUT	GND
	G	I/O L13N_3	GND	I/O L13P_3	I/O L08N_3	I/O L05N_3	I/O L05P_3	INPUT	INPUT VREF_0	INPUT	INPUT	INPUT
	H	I/O L16N_3	I/O L16P_3	I/O L14N_3	I/O L14P_3	I/O L09P_3	I/O L09N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT VREF_0	INPUT	VCCAUX
	J	I/O L17N_3 VREF_3	VCCO_3	I/O L17P_3	GND	I/O L10N_3	VCCO_3	INPUT L11P_3	INPUT VREF_3	GND	VCCINT	GND
	K	I/O L22P_3 LHCLK2	I/O L20N_3	I/O L20P_3	I/O L18N_3	I/O L18P_3	I/O L10P_3	INPUT L15P_3	INPUT L11N_3	VCCINT	GND	VCCINT
	L	I/O L22N_3 IRDY2 LHCLK3	GND	I/O L21N_3 LHCLK1	VCCAUX	I/O L21P_3 LHCLK0	GND	INPUT L19P_3	INPUT L15N_3 VREF_3	GND	VCCINT	GND
	M	I/O L24P_3 LHCLK4	I/O L24N_3 LHCLK5	I/O L25P_3 TRDY2 LHCLK6	I/O L25N_3 LHCLK7	I/O L30P_3	INPUT L23N_3	INPUT L23P_3	INPUT L19N_3	VCCINT	GND	VCCINT
	N	I/O L26P_3 VREF_3	VCCO_3	I/O L26N_3	I/O L30N_3	INPUT L31N_3	INPUT L31P_3	INPUT L35P_3	INPUT L27P_3	INPUT L27N_3	VCCINT	GND
	P	I/O L28P_3	I/O L28N_3	I/O L29P_3	GND	I/O L29N_3	VCCO_3	INPUT L39P_3	INPUT L35N_3	GND	GND	VCCAUX
	R	I/O L32P_3	I/O L32N_3	I/O L33P_3	I/O L33N_3	I/O L34P_3	INPUT VREF_3	INPUT L46P_3	INPUT L39N_3	INPUT	INPUT	INPUT
	T	I/O L36P_3 VREF_3	GND	I/O L36N_3	I/O L34N_3	I/O L40P_3	INPUT L46N_3 VREF_3	INPUT VREF_2	INPUT VREF_2	INPUT	INPUT VREF_2	INPUT VREF_2
	U	I/O L37P_3	I/O L37N_3	I/O L41P_3	I/O L41N_3	I/O L40N_3	GND	INPUT	INPUT	VCCO_2	INPUT	I/O L17P_2 GCLK12
	V	I/O L38P_3	VCCO_3	I/O L38N_3	I/O L43P_3	VCCAUX	I/O L01P_2 M1	INPUT	INPUT VREF_2	I/O L09P_2 RDWR_B	I/O L13P_2	I/O L17N_2 GCLK13
	W	I/O L42P_3	I/O L42N_3	I/O L43N_3	I/O L02P_2 M2	I/O L01N_2 M0	I/O L05P_2	I/O L07P_2	I/O L11P_2 VS1	I/O L09N_2 VS2	GND	VCCAUX
Y	I/O L44P_3	I/O L44N_3	GND	I/O L02N_2 CSO_B	I/O L05N_2	I/O L07N_2	I/O L10P_2	I/O L11N_2 VS0	I/O L14P_2 D7	I/O L13N_2	I/O L16P_2 D5	
A	I/O L45P_3	I/O L45N_3	I/O L03N_2	I/O L04N_2	VCCO_2	I/O L08P_2	GND	I/O L12P_2	VCCO_2	I/O L15P_2	GND	
A	GND	I/O L03P_2	I/O L04P_2	I/O L06P_2	I/O L06N_2	I/O L08N_2	I/O L10N_2	I/O L12N_2	I/O L14N_2 D6	I/O L15N_2	I/O L16N_2 D4	
		Bank 2										

Figure 22: FG484 Package Footprint (top view)

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Bank 0											A
12	13	14	15	16	17	18	19	20	21	22	
I/O L18P_0 GCLK6	I/O L16N_0	I/O L13N_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L10N_0	I/O L05N_0	I/O L08N_0	I/O L03N_0	TCK	GND	B
GND	I/O L16P_0	VCCO_0	I/O L13P_0	GND	I/O L10P_0	VCCO_0	I/O L06P_0 VREF_0	I/O L03P_0	I/O L45N_1 A23	I/O L45P_1 A22	C
I/O L17P_0 GCLK4	I/O L15N_0	I/O L09P_0	I/O L11N_0	I/O L08N_0	I/O L07N_0	I/O L05P_0	I/O L02N_0	GND	I/O L44N_1 A21	I/O L44P_1 A20	D
VCCAUX	I/O L15P_0	GND	I/O L11P_0	I/O L08P_0	I/O L07P_0	I/O L01N_0	I/O L02P_0 VREF_0	I/O L42N_1	I/O L42P_1	I/O L41N_1	E
I/O L17N_0 GCLK5	I/O L14N_0	I/O L09N_0	I/O L04P_0	INPUT	I/O L01P_0	VCCAUX	TDO	I/O L38P_1	VCCO_1	I/O L41P_1	F
INPUT	I/O L14P_0	VCCO_0	I/O L04N_0	INPUT	GND	I/O L40N_1	I/O L40P_1	I/O L38N_1	I/O L34N_1 A19	I/O L34P_1 A18	G
INPUT	INPUT	INPUT	INPUT	INPUT	I/O L46N_1 A25	I/O L46P_1 A24	I/O L36P_1	I/O L36N_1	GND	I/O L30N_1 A15	H
INPUT VREF_0	INPUT	INPUT	INPUT L47N_1	INPUT L47P_1 VREF_1	INPUT L39P_1	INPUT L39N_1	I/O L37N_1	I/O L33N_1 A17	I/O L33P_1 A16	I/O L30P_1 A14	J
VCCINT	GND	GND	INPUT L43N_1 VREF_1	INPUT L43P_1	VCCO_1	I/O L37P_1	GND	I/O L29N_1 A13	I/O L29P_1 A12	I/O L26N_1 A11	K
GND	VCCINT	INPUT L35P_1 VREF_1	INPUT L35N_1	INPUT L31N_1	I/O L32P_1	I/O L32N_1	I/O L25N_1 RHCLK7	I/O L25P_1 IRDY1 RHCLK6	VCCO_1	I/O L26P_1 A10	L
VCCINT	GND	VCCINT	INPUT L31P_1	INPUT L27N_1	GND	I/O L28P_1	I/O L28N_1	I/O L22N_1 TRDY1 RHCLK3	I/O L22P_1 RHCLK2	I/O L21N_1 RHCLK1	M
GND	VCCINT	GND	INPUT L27P_1 VREF_1	INPUT L23N_1	INPUT L23P_1	I/O L24P_1 RHCLK4	VCCAUX	I/O L24N_1 RHCLK5	GND	I/O L21P_1 RHCLK0	N
VCCINT	GND	VCCINT	INPUT L16P_1	INPUT L16N_1 VREF_1	I/O L20N_1 A9	I/O L20P_1 A8	I/O L19N_1 A7	I/O L19P_1 A6	I/O L18N_1 A5	I/O L18P_1 A4	P
INPUT	VCCINT	GND	INPUT L08P_1	INPUT L08N_1	VCCO_1	I/O L17N_1 A3	GND	I/O L15P_1	VCCO_1	I/O L15N_1 VREF_1	R
INPUT VREF_2	INPUT VREF_2	INPUT VREF_2	INPUT L04P_1	INPUT L04N_1 VREF_1	INPUT L12P_1	INPUT L12N_1 VREF_1	I/O L17P_1 A2	I/O L13P_1	I/O L14P_1	I/O L14N_1	T
GND	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	I/O L03P_1 A0	I/O L03N_1 A1	I/O L13N_1	I/O L11P_1	GND	I/O L11N_1	U
I/O L20N_2 GCLK3	I/O L26N_2 D3	VCCO_2	INPUT	INPUT ◆	GND	SUSPEND	I/O L10N_1	I/O L10P_1	I/O L09N_1	I/O L09P_1	V
I/O L20P_2 GCLK2	I/O L26P_2 INIT_B	I/O L30P_2	I/O L30N_2	I/O L31N_2	I/O L33N_2	VCCAUX	I/O L06P_1	I/O L06N_1	VCCO_1	I/O L07N_1	W
I/O L18P_2 GCLK14	I/O L23P_2	GND	I/O L25P_2	I/O L31P_2	I/O L34N_2	I/O L33P_2	I/O L02P_1 LDC1	I/O L02N_1 LDC0	I/O L05N_1	I/O L07P_1	Y
I/O L18N_2 GCLK15	I/O L21N_2	I/O L23N_2	I/O L25N_2	I/O L27N_2	I/O L28N_2 D1	I/O L34P_2	DONE	GND	I/O L01N_1 LDC2	I/O L05P_1	A
I/O L19P_2 GCLK0	VCCO_2	I/O L22P_2	I/O L24N_2 DOUT	GND	I/O L28P_2 D2	VCCO_2	I/O L32N_2	I/O L36N_2 CCLK	I/O L35N_2	I/O L01P_1 HDC	A
I/O L19N_2 GCLK1	I/O L21P_2	I/O L22N_2 MOSI CS1_B	I/O L24P_2 AWAKE	I/O L27P_2	I/O L29P_2	I/O L29N_2	I/O L32P_2	I/O L36P_2 D0 DIN/MISO	I/O L35P_2	GND	A

Right Half of FG484 Package (top view)

Bank 2										
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FG676: 676-ball Fine-pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports the XC3S1400A FPGA.

Table 78 lists all the FG676 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The XC3S1400A has 17 unconnected balls, indicated as N.C. (No Connection) in Table 78 and with the black diamond character (◆) in Table 78 and Figure 23.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3a_pin.zip.

Pinout Table

Table 78: Spartan-3A FG676 Pinout

Bank	Pin Name	FG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C. (◆)	A24	N.C.
0	N.C. (◆)	B24	N.C.
0	N.C. (◆)	D5	N.C.
0	N.C. (◆)	E9	N.C.
0	N.C. (◆)	F18	N.C.
0	VREF (N.C. ◆)	E6	VREF
0	VREF (N.C. ◆)	F9	VREF
0	VREF (N.C. ◆)	G18	VREF
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O
1	IO_L51P_1	G23	I/O
1	IO_L53N_1	K20	I/O
1	IO_L53P_1	L20	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L56N_1	F23	I/O
1	IO_L56P_1	E24	I/O
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L58N_1	G22	I/O
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L59N_1	J20	I/O
1	IO_L59P_1	J19	I/O
1	IO_L60N_1	D26	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L62N_1/A21	H21	DUAL
1	IO_L62P_1/A20	J21	DUAL
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IO_L64N_1/A25	G21	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IP_L16N_1	Y26	INPUT
1	IP_L16P_1	W25	INPUT

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
1	IP_L20N_1/VREF_1	V26	VREF
1	IP_L20P_1	W26	INPUT
1	IP_L24N_1/VREF_1	U26	VREF
1	IP_L24P_1	U25	INPUT
1	IP_L28N_1	R24	INPUT
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IP_L36N_1	N23	INPUT
1	IP_L36P_1/VREF_1	M24	VREF
1	IP_L40N_1	L23	INPUT
1	IP_L40P_1	K24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IP_L48N_1	H24	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52N_1/VREF_1	G25	VREF
1	IP_L52P_1	G26	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L65P_1/VREF_1	B26	VREF
1	SUSPEND	V20	PWR MGMT
1	VCCO_1	AB25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	W22	VCCO
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L05P_2	W9	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L08N_2	AD6	I/O
2	IO_L08P_2	AC6	I/O
2	IO_L09N_2	W10	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
2	IO_L09P_2	V10	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L11P_2	AD7	I/O
2	IO_L12N_2	AA10	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L13N_2	U11	I/O
2	IO_L13P_2	V11	I/O
2	IO_L14N_2	AB7	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L16N_2	W12	I/O
2	IO_L16P_2	V12	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L18N_2	AF8	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L20N_2	W13	I/O
2	IO_L20P_2	V13	I/O
2	IO_L21N_2	AC12	I/O
2	IO_L21P_2	AB12	I/O
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L23N_2	AC11	I/O
2	IO_L23P_2	AD11	I/O
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IO_L29N_2	AC14	I/O
2	IO_L29P_2	AD14	I/O
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L30P_2	AC15	I/O
2	IO_L31N_2	W15	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
2	IO_L31P_2	V14	I/O
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L32P_2/AWAKE	AD15	PWR MGMT
2	IO_L33N_2	AD17	I/O
2	IO_L33P_2	AE17	I/O
2	IO_L34N_2/D3	Y15	DUAL
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L35N_2	U15	I/O
2	IO_L35P_2	V15	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L37P_2	AF19	I/O
2	IO_L38N_2	AB16	I/O
2	IO_L38P_2	AC16	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L39P_2	AF20	I/O
2	IO_L40N_2	AC19	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L42N_2	U16	I/O
2	IO_L42P_2	V16	I/O
2	IO_L43N_2	Y17	I/O
2	IO_L43P_2	AA17	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L45N_2	AC21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L46N_2	V17	I/O
2	IO_L46P_2	W17	I/O
2	IO_L47N_2	AA18	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L48P_2	AF23	I/O
2	IO_L51N_2	AE25	I/O
2	IO_L51P_2	AF25	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IP_2	AA19	INPUT
2	IP_2	AB13	INPUT
2	IP_2	AB17	INPUT
2	IP_2	AB20	INPUT

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
2	IP_2	AC7	INPUT
2	IP_2	AC13	INPUT
2	IP_2	AC17	INPUT
2	IP_2	AC18	INPUT
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C. (◆)	AA8	N.C.
2	N.C. (◆)	AC5	N.C.
2	N.C. (◆)	AC22	N.C.
2	N.C. (◆)	AD5	N.C.
2	N.C. (◆)	Y18	N.C.
2	N.C. (◆)	Y19	N.C.
2	VREF (N.C. ◆)	AD23	VREF
2	VREF (N.C. ◆)	W18	VREF
2	VREF (N.C. ◆)	Y8	VREF
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L31N_3	N2	I/O
3	IO_L31P_3	N1	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L36N_3	R2	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L37N_3	R4	I/O
3	IO_L37P_3	R3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L38P_3	T3	I/O
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L40N_3	R6	I/O
3	IO_L40P_3	R5	I/O
3	IO_L41N_3	P9	I/O
3	IO_L41P_3	P8	I/O
3	IO_L42N_3	U4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L44N_3	U2	I/O
3	IO_L44P_3	U1	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L47N_3	V2	I/O
3	IO_L47P_3	V1	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L49N_3	V5	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L51P_3	T7	I/O
3	IO_L52N_3	W4	I/O
3	IO_L52P_3	W3	I/O
3	IO_L53N_3	Y2	I/O
3	IO_L53P_3	Y1	I/O
3	IO_L55N_3	AA3	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L56N_3	U8	I/O
3	IO_L56P_3	U7	I/O

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
3	IO_L57N_3	Y6	I/O
3	IO_L57P_3	Y5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L61N_3	V8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L65P_3	AD1	I/O
3	IP_L04N_3/VREF_3	C1	VREF
3	IP_L04P_3	C2	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L12N_3/VREF_3	H4	VREF
3	IP_L12P_3	G5	INPUT
3	IP_L16N_3	G1	INPUT
3	IP_L16P_3	G2	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IP_L24N_3	K1	INPUT
3	IP_L24P_3	J1	INPUT
3	IP_L46N_3	V4	INPUT
3	IP_L46P_3	U3	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IP_L50P_3	W1	INPUT
3	IP_L54N_3	Y4	INPUT
3	IP_L54P_3	Y3	INPUT
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	V3	GND
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	A25	JTAG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX

Table 78: Spartan-3A FG676 Pinout (Continued)

Bank	Pin Name	FG676 Ball	Type
VCCAUX	VCCAUX	AB22	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX
VCCAUX	VCCAUX	V9	VCCAUX
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	U12	VCCINT

User I/Os by Bank

Table 79 indicates how the 502 available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a Dual-Purpose I/O.

Table 79: User I/Os Per Bank for the XC3S1400A in the FG676 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	120	82	20	1	9	8
Right	1	130	67	15	30	10	8
Bottom	2	120	67	14	21	10	8
Left	3	132	97	18	0	9	8
TOTAL		502	313	67	52	38	32

Footprint Migration Differences

The XC3S1400A FPGA is the only Spartan-3A device offered in the FG676 package. However, [Table 80](#) summarizes footprint and functionality differences between the XC3S1400A and the XC3SD1800A in the Spartan-3A DSP platform. There are 17 unconnected balls in the XC3S1400A that become 16 input-only pins and one I/O pin in the XC3SD1800A. All other pins not listed in [Table 80](#) unconditionally migrate between the Spartan-3A platform devices and the Spartan-3A DSP platform devices available in the FG676 package. The arrows indicate the direction for easy migration. For more details on the Spartan-3A DSP platform and pinouts, and additional differences in the FG676 pinout for the XC3SD3400A device, see [DS610](#).

Table 80: FG676 Footprint Differences

Pin	Bank	XC3S1400A	Migration	XC3SD1800A
A24	0	N.C.	→	INPUT
B24	0	N.C.	→	INPUT
D5	0	N.C.	→	INPUT
E6	0	N.C.	→	VREF (INPUT)
E9	0	N.C.	→	INPUT
F9	0	N.C.	→	VREF (INPUT)
F18	0	N.C.	→	INPUT
G18	0	N.C.	→	VREF (INPUT)
W18	2	N.C.	→	VREF (INPUT)
Y8	2	N.C.	→	VREF (INPUT)
Y18	2	N.C.	→	INPUT
Y19	2	N.C.	→	INPUT
AA8	2	N.C.	→	INPUT
AC5	2	N.C.	→	INPUT
AC22	2	N.C.	→	I/O
AD5	2	N.C.	→	INPUT
AD23	2	N.C.	→	VREF(INPUT)
DIFFERENCES			17	

Legend:

- This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

FG676 Footprint

Left Half of FG676 Package (top view)

- 313 I/O: Unrestricted, general-purpose user I/O
- 67 INPUT: Unrestricted, general-purpose input pin
- 52 DUAL: Configuration, AWAKE pins, then possible user I/O
- 38 VREF: User I/O or input voltage reference for bank
- 32 CLK: User I/O, input, or clock buffer input
- 3 CONFIG: Dedicated configuration pins, SUSPEND pin
- 4 JTAG: Dedicated JTAG port pins
- 77 GND: Ground
- 36 VCCO: Output voltage supply for bank
- 23 VCCINT: Internal core supply voltage (+1.2V)
- 14 VCCAUX: Auxiliary supply voltage
- 17 N.C.: Not connected

		Bank 0												
		1	2	3	4	5	6	7	8	9	10	11	12	13
Bank 3	A	GND	PROG_B	I/O L51P_0	I/O L45P_0	INPUT	GND	INPUT	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
	B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
	C	INPUT L04N_3	INPUT L04P_3	GND	INPUT	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
	D	INPUT L08N_3	INPUT L08P_3	I/O L06P_3	TMS	N.C.	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0	INPUT	I/O L30P_0
	E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VREF_0	I/O L48N_0	VCCO_0	N.C.	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
	F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0	VREF_0	INPUT	GND	I/O L31N_0	I/O L27P_0 GCLK8
	G	INPUT L16N_3	INPUT L16P_3	I/O L14P_3	I/O L09N_3	INPUT L12P_3	I/O L03P_3	TDI	I/O L52N_0	PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0
	H	I/O L17N_3	I/O L17P_3	GND	INPUT L12N_3	VREF_3	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0
	J	INPUT L24P_3	INPUT L24P_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
	K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
	L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
	M	I/O L29N_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
	N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3	I/O L32N_3	GND	I/O L35P_3	TRDY2	VCCAUX	GND	VCCINT
	P	I/O L33P_3	I/O L33N_3	I/O L34N_3	I/O L34P_3	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L43P_3	VCCINT	GND	VCCINT
	R	I/O L36P_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3	GND	VCCINT	GND
	T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
	U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2	
W	INPUT L50P_3	INPUT L50N_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2	
Y	I/O L53P_3	I/O L53N_3	INPUT L54P_3	INPUT L54N_3	I/O L57P_3	I/O L57N_3	I/O L02P_2	VREF_2	I/O L05N_2	I/O L12P_2	INPUT	I/O L17P_2	I/O L25N_2	
A	GND	I/O L55P_3	I/O L55N_3	INPUT L58P_3	INPUT L58N_3	VREF_3	GND	I/O L02N_2	N.C.	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2	
A	I/O L60P_3	VCCO_3	INPUT L62P_3	INPUT L62N_3	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	INPUT VREF_2	VCCAUX	I/O L21P_2	INPUT	
A	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2	N.C.	I/O L08P_2	INPUT	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT	
A	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2	N.C.	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND	
A	INPUT L66P_3	INPUT L66N_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2	I/O L22P_2	VCCO_2	I/O L24N_2	I/O L28N_2	
A	GND	INPUT	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	INPUT	I/O L18N_2	I/O L19N_2	I/O L22N_2	GND	I/O L24P_2	I/O L28P_2	

Figure 23: FG676 Package Footprint (top view)

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Bank 0													A
14	15	16	17	18	19	20	21	22	23	24	25	26	
I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C.	TCK	GND	B
I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C.	INPUT L65N_1	INPUT L65P_1 VREF_1	C
GND	I/O L22N_0	I/O L21N_0	I/O L19P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22	D
INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1	E
I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	F
I/O L24N_0	I/O L20P_0	GND	I/O L13P_0	N.C.	I/O L02N_0	I/O L01N_0	GND	I/O L58P_1 VREF_1	I/O L56N_1	I/O L54N_1	I/O L54P_1	GND	G
INPUT	I/O L16P_0	INPUT	I/O L08N_0	VREF_0	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1	H
GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1	J
I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L59P_1	I/O L59N_1	I/O L62P_1 A20	I/O L49N_1	I/O L49P_1	GND	I/O L43N_1 A19	I/O L43P_1 A18	K
I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1	L
VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	M
GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	N
VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK6	INPUT L32N_1	INPUT L32P_1	P
VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2	R
VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1	I/O L29N_1	T
GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND	U
VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1	V
I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1	W
GND	I/O L31N_2	VCCO_2	I/O L46P_2	VREF_2	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1	Y
I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT_2 VREF_2	I/O L43N_2	N.C.	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1	A
I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND	A
VCCO_2	I/O L30N_2 MOSI CSI_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1	A
I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C.	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1	A
I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	VREF_2	GND	I/O L02N_1 LDC0	I/O L05P_1	A
I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1	A
I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 DO DIN/MISO	I/O L51P_2	GND	A

Right Half of FG676 Package (top view)

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Added DOUT pin to DUAL-type pins in Table 56 . Corrected counts for DUAL pins and differential pairs in Table 58 . Corrected minor typographical error on pin names for pin numbers P24 and P25 in Table 60 . Highlighted the differences in differential I/O pairs between the XC3S50A and XC3S200A in the FT256 package, shown in Table 62 and added Table 66 and Table 67 to summarize the differences.
03/16/07	1.2	Corrected minor typographical error in Figure 17 .
04/23/07	1.3	Added reference to compatible Spartan-3A DSP family.
05/08/07	1.4	Added note regarding banking rules.
07/10/07	1.5	Update Thermal Characteristics in Table 59 .



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