W90N740CD/W90N740CDG
DATA SHEET

WINBOND

32-BIT ARM7TDMI-BASED MICRO-CONTROLLER

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1. GENERAL DESCRIPTION

The **W90N740** micro-controller is 16/32 bit, **ARM7TDMI based RISC** micro-controller for **network** as well as **embedded** applications. An integrated dual Ethernet MAC, the W90N740, is designed for use in broadband routers, wireless access points, residential gateways and LAN camera.

The W90N740N is built around The ARM7TDMI CPU core designed by Advanced RISC Machines, Ltd. And achieves **80MHz** under **worse conditions**. Its small size, fully static design is particularly suitable for cost-sensitive and power-sensitive applications. It designs as Harvard architecture by offering an **8K-byte I-cache/SRAM and an 2K-byte D-cache/SRAM** with flexible configuration and two way set associative structure to balance data movement between CPU and external memory. Four stages **write buffer** also improves latency for write operations.

The **external bus interface (EBI)** controller provides single bus architecture, 8/16/32 bit data width to access external SDRAM, ROM/SRAM, flash memory and I/O devices. It achieves same frequency as CPU core to minimize latency if internal cache misses. Memory controller supports different kinds of SDRAM types and configurations to ease system design. The System Manager includes an internal 32-bit system bus arbiter and a PLL clock controller. Generic I/O bus is easily served as PCMCIA-like interface for 802.11b wireless LAN connection.

Two 10/100Mb MACs of Ethernet controller is built in to reduce total system cost and increase performance between WAN and LAN port. Either **MII or RMII** of MAC is selected for external 10/100 PHY chip to design for varieties of applications. A powerful **NAT accelerator** (**Patent Pending**) between LAN and WAN reduces the software loading of CPU and speeds up performance between LAN and WAN.

W90N740 integrates **root hub of USB 1.1 host controller with one port transceiver** and uses additional port with external transceiver if necessary, which can add valuable functions like flash disk, printer server, Bluetooth device via USB port. The important peripheral functions include **one full wired high speed UART** channel, **2-Channel GDMA**, **one watch-dog timer**, **two 24-bit timers** with 8-bit pre-scale, **20 programmable I/O ports**, and **an advanced interrupt controller**.

2. FEATURES

Architecture

- Highly-integrated system for embedded Ethernet applications
- Powerful ARM7TDMI core and fully 16/32-bit RISC architecture
- Big /Little-Endian mode supported
- Cost-effective JTAG-based debug solution

System Manager

- System memory map & on-chip peripherals memory map
- The data bus width of external memory address & data bus connection with external memory
- Bus arbitration supports the Fixed Priority Mode & Rotate Priority Mode
- Power-On setting
- On-Chip PLL module control & Clock select control

External Bus Interface (EBI)

- External I/O Control with 8/16/32 bit external data bus
- Cost-effective memory-to-peripheral DMA interface
- SDRAM Controller supports up to 2 external SDRAM & the maximum size of each device is 32MB
- ROM/FLASH & External I/O interface
- Support for PCMCIA 16-bit PC Card devices

On-Chip Instruction and Data Cache

- Two-way, Set-associative, 8K-byte I-cache and 2K-byte D-cache
- Support for LRU (Least Recently Used) Protocol
- Cache can be configured as an internal SRAM
- Support Cache Lock function

Ethernet MAC Controller (EMC)

- IEEE 802.3 protocol engine with programmable MII or RMII interface for 10/100 Mbits/s
- DMA engine with burst mode
- 256 bytes transmit & 256 bytes receive FIFO for MAC protocol engine and DMA access
- Built-in 16 entry CAM Address Register
- Support long frame (more than 1518 bytes) and short frame (less than 64 bytes)
- Re-transmit (during collision) the frame without DMA access
- Half or full duplex function option
- Support Station Management for external PHY
- On-Chip Pad generation

NAT Accelerator (Patent Pending)

- Hardware acceleration on IP address / port number look up and replacement for network address translation, including MAC address translation
- Provide 64 entries of translation table
- Support TCP / UDP packets

GDMA Controller

- 2 Channel GDMA for memory-to-memory data transfers without CPU intervention
- Increase or decrease source / destination address in 8-bit, 16-bit, or 32-bit data transfers
- Supports 4-data burst mode to boost performance
- Support external GDMA request

USB Host Controller

- USB 1.1 compatible
- Open Host Controller Interface (OHCI) 1.1 compatible.
- Supports both low-speed (1.5 Mbps) and full-speed (12Mbps) USB devices.
- Built-in DMA for real-time data transfer

UART

- One UART (serial I/O) blocks with interrupt-based operation
- Full set of MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
- Break generation and detection
- False start bit detection
- Parity, overrun, and framing error detection
- Full prioritized interrupt system controls

Timers

- Two programmable 24-bit timers with 8-bit pre-scalar
- One programmable 24-bit Watch-Dog timer
- One-short mode, period mode or toggle mode operation

Programmable I/Os

- 21 programmable I/O ports
- I/O ports Configurable for Multiple functions

Advanced Interrupt Controller (AIC)

- 18 interrupt sources, including 4 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 4 external interrupt sources
- Programmable as either low-active or high-active for 4 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting

GPIO Controller

- Programmable as an input or output pin

On-Chip PLL

- One PLL for both CPU and USB host controller
- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- Programmable clock frequency, and the input frequency range is 3-30MHz; 15MHz is preferred.

Operation Voltage Range

- 2.7 – 3.6 V for IO Buffer
- 1.62 – 1.98 V for Core Logic

Operation Temperature Range

- 0 – 70 Degree C

Operating Frequency

- 80 MHz (default)

Package Type

- 176-pin LQFP

3. PIN CONFIGURATION

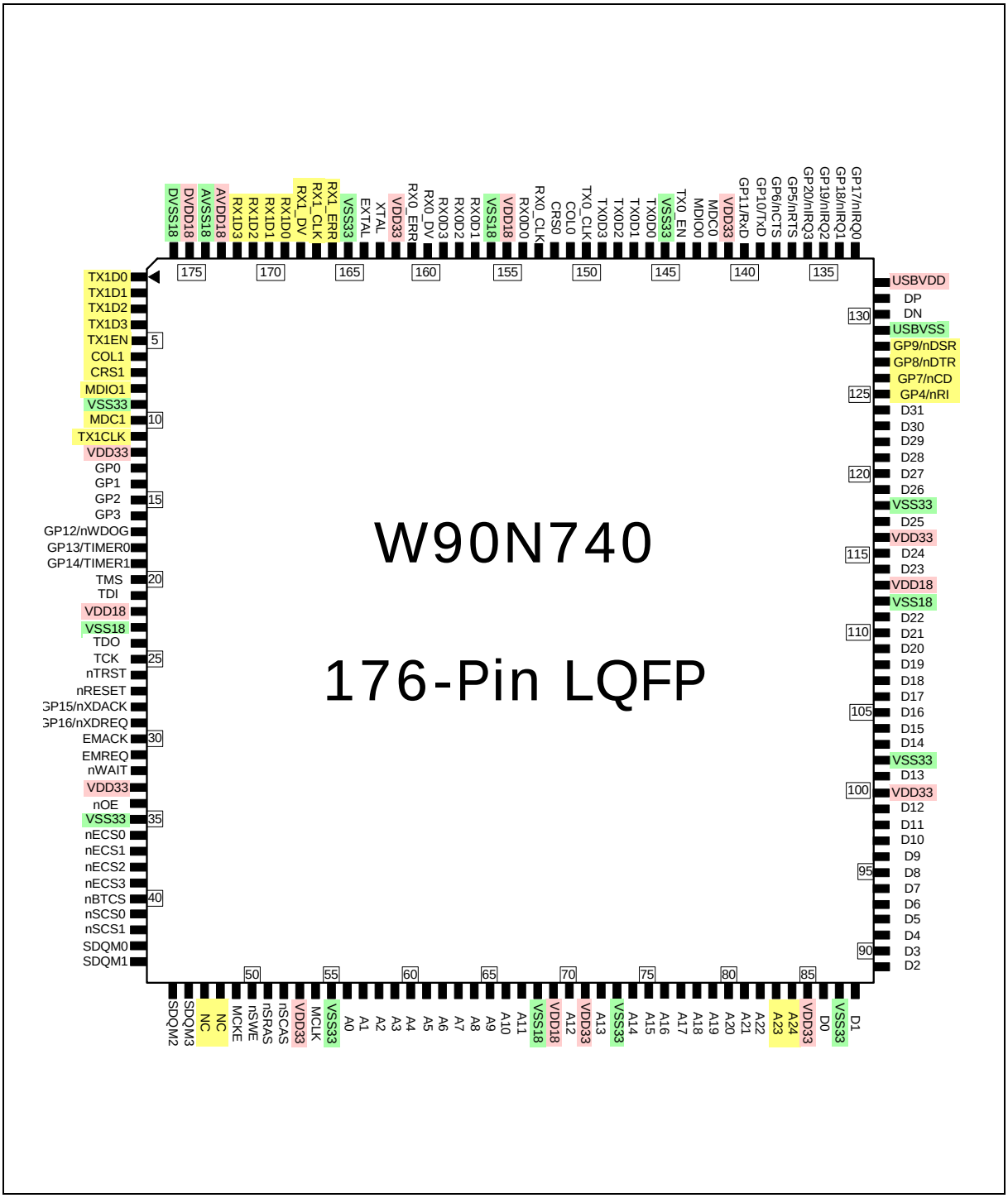


Fig 3.1 176-Pin LQFP Pin Diagram

4. PIN ASSIGNMENT

Table 4 W90N740 Pins Assignment

PIN NAME	176-PIN LQFP	
Clock & Reset	**(4 pins)**	
EXTAL	●	164
XTAL	●	163
MCLK	●	54
nRESET	●	27
TAP Interface	**(5 pins)**	
TCK	●	25
TMS	●	20
TDI	●	21
TDO	●	24
nTRST	●	26
External Bus Interface	**(78 pins)**	
A [24:22]	●	84-82
A [21:0]	●	81-74, 72, 70,67-56
D [31:16]	●	124-119, 117, 115-114, 111-105
D [15:0]	●	104-103, 101, 99-88, 86
nWBE [3:0]/ SDQM [3:0]	●	46-43
nSCS[1:0]	●	42, 41
NSRAS	●	51
NSCAS	●	52
NSWE	●	50
MCKE	●	49
NC	●	48
NC	●	47
EMREQ	●	31
EMACK	●	30
nWAIT	●	32
NBTCS	●	40
nECS[3:0]	●	39-36
NOE	●	34

Table 4 W90N740 Pins Assignment, continued

PIN NAME	176-PIN LQFP	
Ethernet Interface (0)	**(17 pins)**	
MDC0	●	142
MDIO0	●	143
COL0 /	●	151
CRS0 / R1B_CRSDV	●	152
TX0_CLK	●	150
TX0D [3:0] / R1B_TXD [1:0], R0_TXD [1:0]	●	149-146
TX0_EN / R0_TXEN	●	144
RX0_CLK / R0_REFCLK	●	153
RX0D [3:0] / R1B_RXD [1:0], R0_RXD [1:0]	●	159-157, 154
RX0_DV / R0_CRSDV	●	160
RX0_ERR	●	161
Ethernet Interface (1)	**(17 pins)**	
MDC1	●	10
MDIO1	●	8
COL1	●	6
CRS1	●	7
TX1_CLK	●	11
TX1D [3:0] / R1A_TX [1:0]	●	4-1
TX1_EN /R1A_TXEN	●	5
RX1_CLK / R1A_REFCLK	●	167
RX1D [3:0] / R1A_RXD [1:0]	●	172-169
RX1_DV / R1A_CRSDV	●	168
RX1_ERR / R1A_RXERR	●	166

Table 4 W90N740 Pins Assignment, continued

NAME	176-PIN LQFP	
USB Interface	**(2 pins)**	
DP	●	131
DN	●	130
Miscellaneous	**(21 pins)**	
GP [20:17] / nIRQ [3:0]	●	136-133
GP16 / nXDREQ	●	29
GP15 /nXDACK	●	28
GP14 / TIMER1/ SPEED	●	19
GP13 / TIMER0/ STDBY	●	18
GP12 /nWDOG	●	17
GP11 /RxD	●	140
GP10 /TxD	●	139
GP9/nDSR/nTOE	●	128
GP8 /nDTR/FSE0	●	127
GP7 /nCD / VO	●	126
GP6 /nCTS/ VM	●	138
GP5 /nRTS/ VP	●	137
GP4 /nRI / RCV	●	125
GP [3:0]	●	16-13
Power/Ground	**(32 pins)**	
VDD18	●	22, 69, 113, 155
VSS18	●	23, 68, 112, 156
VDD33	●	12, 33, 53, 71, 85, 100, 116, 141, 162
VSS33	●	9, 35, 55, 73, 87, 102, 118, 145, 165
USBVDD	●	132
USBVSS	●	129
DVDD18	●	175
DVSS18	●	176
AVDD18	●	173
AVSS18	●	174

5. PIN DESCRIPTION

Table 5.1 W90N740 Pins Description

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
System Clock & Reset			
EXTAL	I	-	External Clock / Crystal Input
XTAL	O	-	Crystal Output
MCLK	O	-	System Master Clock Out, SDRAM clock
nRESET	I	-	System Reset, active-low
TAP Interface			
TCK	ID	internal pull-down	JTAG Test Clock,
TMS	IU	internal pull-up	JTAG Test Mode Select,
TDI	IU	internal pull-up	JTAG Test Data in,
TDO	O	-	JTAG Test Data out
nTRST	IU	internal pull-up	JTAG Reset, active-low,
External Bus Interface			
A [24:22]	O	-	Address Bus (MSB) of external memory and IO devices
A [21:0]	IO	-	Address Bus of external memory and IO devices
D [31:16]	IO	-	Data Bus (MSB) of external memory and IO device,
D [15:0]	IO	-	Data Bus (LSB) of external memory and IO device
nWBE [3:0]/ SDQM [3:0]	IO	-	Write Byte Enable for specific device(nECS[3:0]), Data input/output Mask signal for SDRAM (nSCS[1:0]), active-low These pins are always Output in normal mode, and Input type in internal SRAM test mode.
nSCS [1:0]	O	-	SDRAM chip select for two external banks, active-low.
nSRAS	O	-	Row Address Strobe for SDRAM, active-low
nSCAS	O	-	Column Address Strobe for SDRAM, active-low
nSWE	O	-	SDRAM Write Enable, active-low
MCKE	O	-	SDRAM Clock Enable, active-high
EMREQ	ID	internal pull-down	External Master Bus Request This is used to request external bus. When EMACK active, indicates the bus grants the bus, chip drives all the output pins of the external bus to high impedance.
EMACK	O	-	External Bus Acknowledge
nWAIT	IU	internal pull-up	External Wait, active-low
nBTCS	O	-	ROM/Flash Chip Select, active-low
nECS [3:0]	IO	-	External I/O Chip Select, active-low.
nOE	O	-	ROM/Flash, External Memory Output Enable, active-low

Pins Description, continued

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
Ethernet Interface (0)			
MDC0	O	-	MII Management Data Clock for Ethernet 0. It is the reference clock of MDIO0. Each MDIO0 data will be latched at the rising edge of MDC0 clock.
MDIO0	IO	-	MII Management Data I/O for Ethernet 0. It is used to transfer MII control and status information between PHY and MAC.
COL0	I	-	Collision Detect for Ethernet 0 in MII mode. This shall be asserted by PHY upon detecting a collision happened over the medium. It will be asserted and lasted until collision condition vanishes.
CRS0	I	-	Carrier Sense for Ethernet 0 in MII mode. In RMII mode, external pull-up is necessary.
TX0_CLK	I	-	Transmit Data Clock for Ethernet 0 in MII mode. TX0_CLK is driven by PHY and provides the timing reference for TX0_EN and TX0D. The clock will be 25MHz or 2.5 MHz.
TX0D [3:0]/ --, R0_TXD [1:0]	O	-	Transmit Data bus (4-bit) for Ethernet 0 in MII mode. The nibble transmit data bus is synchronized with TX0_CLK. It should be latched by PHY at the rising edge of TX0_CLK. In RMII mode, TX0D [1:0] are used as R0_TXD [1:0], 2-bit Transmit Data bus for Ethernet 0;
TX0_EN / R0_TXEN	O	-	Transmit Enable for Ethernet 0 in MII. It indicates the transmit activity to external PHY. It will be synchronized with TX0_CLK. In RMII mode, R0_TXEN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. Of course, it is synchronized with R0_REFCLK.
RX0_CLK / R0_REFCLK	I	-	Receive Data Clock for Ethernet 0 in MII mode When it is used as a received clock pin, it is from PHY. The clock will be either 25 MHz or 2.5 MHz. The minimum duty cycle at its high or low state should be 35% of the nominal period for all conditions. In RMII mode, this pin is used as R0_REFCLK, Reference Clock; The clock shall be 50MHz +/- 50 ppm with minimum 35% duty cycle at high or low state.
RX0D [3:0] / --, R0_RXD [1:0]	I	-	Receive Data bus (4-bit) for Ethernet 0 in MII mode. They are driven by external PHY, and should be synchronized with RX0_CLK and valid only when RX0_DV is valid. In RMII mode, RX0D [1:0] are used as R0_RXD [1:0], 2-bit Receive Data bus for Ethernet 0;
RX0_DV / R0_CRSDV	I	-	Receive Data Valid for Ethernet 0 in MII mode. It will be asserted when received data is coming and present, and de-asserted at the end of the frame. In RMII mode, this pin is used as the R0_CRSDV, Carrier Sense / Receive Data Valid for Ethernet 0. The R0_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of R0_CRSDV synchronous to the cycle of R0_REFCLK, and only on nibble boundaries.
RX0_ERR	I	-	Receive Data Error for Ethernet 0 in MII mode. It indicates a data error detected by PHY. The assertion should be lasted for longer than a period of RX0_CLK. When RX0_ERR is asserted, the MAC will report a CRC error.

Pins Description, continued

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
Ethernet Interface (1)			
MDC1	O	-	MII Management Data Clock for Ethernet 1. It is the reference clock of MDIO1. Each MDIO1 data will be latched at the rising edge of MDC1 clock.
MDIO1	IO	-	MII Management Data I/O for Ethernet 1. It is used to transfer MII control and status information between PHY and MAC.
COL1	I	-	Collision Detect for Ethernet 1 in MII mode. This shall be asserted by PHY upon detecting a collision happened over the medium. It will be asserted and lasted until collision condition vanishes. External pull-up is necessary in RMII mode.
CRS1	I	-	Carrier Sense for Ethernet 1 in MII mode. External pull-up is necessary in RMII mode.
TX1_CLK	I	-	Transmit Data Clock for Ethernet 1 in MII mode, TX1_CLK is driven by PHY and provides the timing reference for TX1_EN and TX1D. The clock will be 25MHz or 2.5 MHz. External pull-up will be necessary in RMII mode.
TX1D [3:0] / --,R1A_TXD [1:0]	O	-	Transmit Data bus (4-bit) for Ethernet 1 in MII mode. The nibble transmit data bus is synchronized with TX1_CLK. It should be latched by PHY at the rising edge of TX1_CLK. In RMII mode, TX1D [1:0] are used as R1A_TXD [1:0], 2-bit Transmit Data bus for Ethernet 1
TX1_EN/ R1A_TXEN/R1B_ TXEN	O	-	Transmit Enable for Ethernet 1 in MII and RMII mode. It indicates the transmit activity to external PHY. It will be synchronized with TX1_CLK in MII mode.
RX1_CLK / R1A_REFCLK	I	-	Receive Data Clock for Ethernet 1 in MII mode. When it is used as a received clock pin, it is from PHY. The clock will be either 25 MHz or 2.5 MHz. The minimum duty cycle at its high or low state should be 35% of the nominal period for all conditions. In RMII mode, this pin is used as R1A_REFCLK, Reference Clock and only available for 176-pin package. The clock shall be 50MHz +/-50 ppm with minimum 35% duty cycle at high or low state.
RX1D [3:0] / --, R1A_RXD[1:0]	I	-	Receive Data bus (4-bit) for Ethernet 1 in MII mode. They are driven by external PHY, and should be synchronized with RX1_CLK and valid only when RX1_DV is valid. In RMII mode, RX1D [1:0] are used as R1A_RXD [1:0], 2-bit Receive Data bus for Ethernet 1.
RX1_DV/ R1A_CRSDV	I	-	Receive Data Valid for Ethernet 1 in MII mode. It will be asserted when received data is coming and present, and de-asserted at the end of the frame. In RMII mode, this pin is used as the R1A_CRSDV, Carrier Sense / Receive Data Valid for Ethernet 1 and only available for 176-pin package. The R1A_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of R1A_CRSDV synchronous to the cycle of R1A_REFCLK, and only on nibble boundaries.
RX1_ERR / R1A_RXERR	I	-	Receive Data Error for Ethernet 1 in MII and RMII mode. It indicates a data error detected by PHY. The assertion should be lasted for longer than a period of RX0_CLK. When RX0_ERR is asserted, the MAC will report a CRC error.

Pins Description, continued

NAME	IO TYPE	PAD TYPE	DESCRIPTION
USB Interface			
DP	IO	-	Differential Positive USB IO signal
DN	IO	-	Differential Negative (Minus) USB IO signal
Miscellaneous			
GP[20:17] / nIRQ[3:0]	IO	-	External Interrupt Request or General Purpose I/O
GP16 / nXDREQ	IO	-	External DMA Request or General Purpose I/O
GP15 /nXDACK	IO	-	External DMA Acknowledge or General Purpose I/O
GP14 / TIMER1/SPEED	IO	-	Timer 1 or General Purpose I/O. This pin is also used as SPEED, Speed mode control for external USB transceiver
GP13 / TIMER0/STDBY	IO	-	Timer 0 or General Purpose I/O. This pin is also used as STDBY, StandBy control for external USB transceiver
GP12 /nWDOG	IO	-	Watchdog Timer Timeout Flag (active-low) or General Purpose I/O
GP11 /RxD	IO	-	UART Receive Data or General Purpose I/O
GP10 /TxD	IO	-	UART Transmit Data or General Purpose I/O
GP9/nDSR/nTOE	IO	-	UART Receive Clock or General Purpose I/O. This pin is also used as nTOE, Output Enable control (active-low) for external USB transceiver.
GP8 /nDTR/FSE0	IO	-	UART Transmit Clock or General Purpose I/O. This pin is also used as SE0, Differential Data Transceiver Output for external USB transceiver. T
GP7 /nCD /VO	IO	-	UART Carrier Detector or General Purpose I/O. This pin is also used as VO, Data Output for external USB transceiver.
GP6 /nCTS/ VM	IO	-	UART Clear to Send or General Purpose I/O. This pin is also used as VM, Data Negative (Minus) Input for external USB receiver.
GP5 /nRTS/ VP	IO	-	UART Ready to Send or General Purpose I/O. This pin is also used as VP, Data Positive Input for external USB receiver.
GP4 /nRI /RCV	IO	-	UART Ring Indicator or General Purpose I/O. This pin is also used as RCV, Difference Receiver Input.
GP[3:0]	IO	-	General Purpose I/O.
Power/Ground			
VDD18	P	-	Core Logic power (1.8V)
VSS18	G	-	Core Logic ground (0V)
VDD33	P	-	IO Buffer power (3.3V)
VSS33	G	-	IO Buffer ground (0V)
USBVDD	P	-	USB power (3.3V)
USBVSS	G	-	USB ground (0V)
DVDD18	P	-	PLL Digital power (1.8V)
DVSS18	G	-	PLL Digital ground (0V)
AVDD18	P	-	PLL Analog power (1.8V)
AVSS18	G	-	PLL Analog ground (0V)

6. FUNCTIONAL DESCRIPTION

6.1 ARM7TDMI CPU Core

The ARM7TDMI CPU core is a member of the ARM family of general-purpose 32-bit microprocessors, which offer high performance for very low power consumption. The architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro-programmed Complex Instruction Set Computer (CISC) systems. Pipelining is employed so that all parts of the processing and memory systems can operate continuously. The high instruction throughput and impressive real-time interrupt response are the major benefits.

The ARM7TDMI core can execute two instruction sets:

(1) The standard 32-bit ARM instruction set

(2) The 16-bit THUMB instruction set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM core while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. THUMB instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and THUMB states. Each 16-bit THUMB instruction has a corresponding 32-bit ARM instruction with the same effect on the processor model. In the other words, the THUMB architecture give 16-bit systems a way to access the 32-bit performance of the ARM Core without requiring the full overhead of 32-bit processing.

ARM7TDMI CPU core has 31 x 32-bit registers. At any one time, 16 set are visible; the other registers are used to speed up exception processing. All the register specifies in ARM instructions can address any of the 16 registers. The CPU also supports 5 types of exception, such as two levels of interrupt, memory aborts, attempted execution of an undefined instruction and software interrupts.

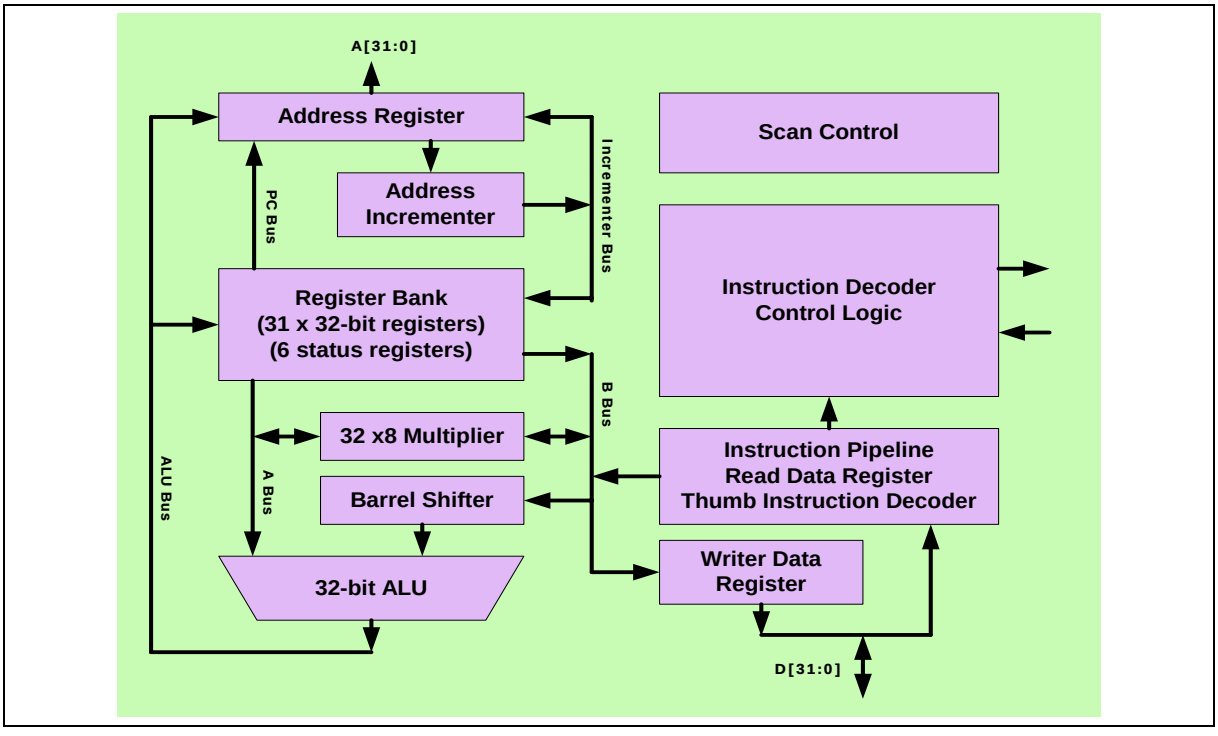


Fig 6.1 ARM7TDMI CPU Core Block Diagram

6.2 System Manager

6.2.1 Overview

The functions of the System Manager:

- System memory map & on-chip peripherals memory map
- The data bus width of external memory address & data bus connection with external memory
- Bus arbitration supports the Fixed Priority Mode & Rotate Priority Mode
- Power-On setting
- On-Chip PLL module control & Clock select control

6.2.2 System Memory Map

W90N740 provides 2G bytes cacheable address space and the other 2G bytes are non-cacheable. The On-Chip Peripherals bank is on 1M bytes top of the space (0xFFF0.0000 – 0xFFFF.FFFF) and the On-Chip RAM bank's start address is 0xFFE0.0000, the other banks can be located anywhere (cacheable space: 0x0~0x7FDF.FFFF if Cache ON; non-cacheable space: 0x8000.0000 ~ 0xFFDF.FFFF).

The size and location of each bank is determined by the register settings for "current bank base address pointer" and "current bank size". (*Note: The address boundaries of consecutive banks must not overlap, when setting the bank control registers.)

The start address of each memory bank is not fixed, except On-Chip Peripherals and On-Chip RAM. You can use bank control registers to assign a specific bank start address by setting the bank's base pointer (13 bits). The address resolution is 256K bytes. The bank's start address is defined as "base pointer << 18" and the bank's size is "current bank size".

In the event of an access request to an address outside any programmed bank size, an abort signal is generated. The maximum accessible memory size of each external IO bank is 32M bytes, and 64M bytes on SDRAM banks.

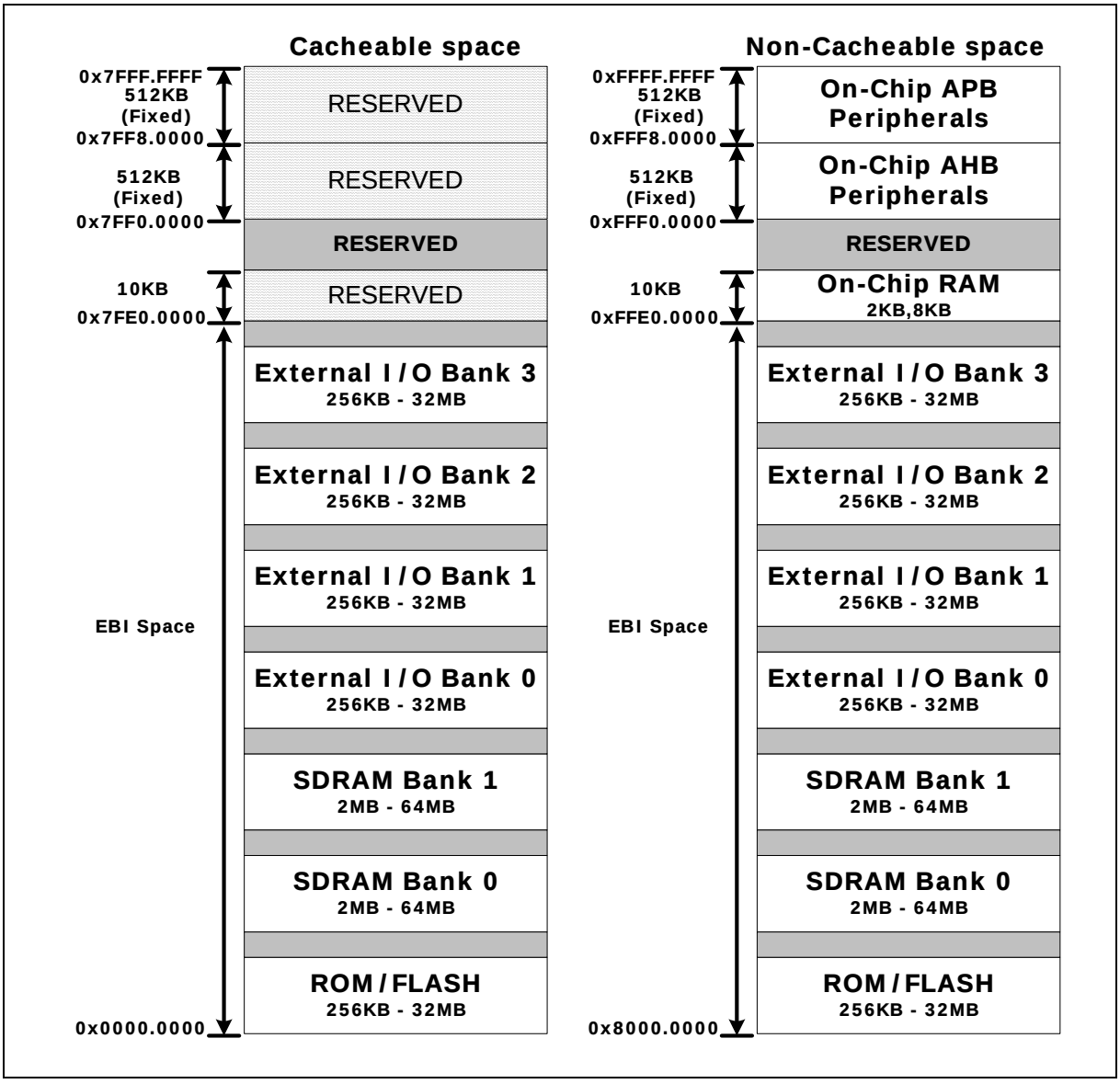


Fig6.2.1 System Memory Map

Table 6.2.1 On-Chip Peripherals Memory Map

BASE ADDRESS	DESCRIPTION
AHB PERIPHERALS	
0xFFF0.0000	Product Identifier Register (PDID)
0xFFF0.0004	Arbitration Control Register (ARBCON)
0xFFF0.0008	PLL Control Register (PLLCON)
0xFFF0.000C	Clock Select Register (CLKSEL)
0xFFF0.1000	EBI Control Register (EBICON)
0xFFF0.1004	ROM/FLASH (ROMCON)
0xFFF0.1008	SDRAM bank 0 - 1
0xFFF0.1018	External I/O 0 - 3
0xFFF0.2000	Cache Controller
0xFFF0.3000	Ethernet MAC Controller 0 - 1
0xFFF0.4000	GDMA 0 - 1
0xFFF0.5000	USB (Host)
0xFFF0.6000	NAT Accelerator
0xFFF6.0000	Reserved
0xFFF7.0000	Reserved
APB Peripherals	
0xFFF8.0000	UART
0xFFF8.1000	Timer 0 - 1, WDOG Timer
0xFFF8.2000	Interrupt Controller
0xFFF8.3000	GPIO

6.2.3 Address Bus Generation

The W90N740 address bus generation is depended on the required data bus width of each memory bank. The data bus width is determined by **DBWD** bits in each bank's control register.

The maximum accessible memory size of each external IO bank is 32M bytes .

Table 6.2.2 Address Bus Generation Guidelines

DATA BUS	EXTERNAL ADDRESS PINS			MAXIMUM ACCESSIBLE
WIDTH	**A [22:0]**	**A23**	**A24**	**MEMORY SIZE**
8-BIT	A22 – A0 (Internal)	A23 (Internal)	A24 (Internal)	32M bytes
16-BIT	A23 – A1 (Internal)	A24 (Internal)	NA	16M half-words
32-BIT	A24 – A2 (Internal)	NA	NA	8M words

6.2.4 Data Bus Connection with External Memory

6.2.4.1. Memory formats

The internal architecture is big endian. The little endian mode only support for external memory. The W90N740 can be configured as big endian or little endian mode by pull up or down the data D14 pin. If D14 is pull-up then it is a little endian mode, otherwise, it is a big endian mode.

Big Endian

In Big endian format, the W90N740 stores the most significant byte of a word at the lowest numbered byte, and the least significant byte at the highest-numbered byte. So the byte at address 0 of the memory system connects to data lines 31 through 24.

For a word aligned address A, Fig6.2.2 shows how the word at address A, the half-word at addresses A and A+2, and the bytes at addresses A, A+1, A+2, and A+3 map on to each other when the **LITTLE** pin is Low.

<table>
<tr><td colspan="32">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="32">Word at address A</td></tr>
<tr><td colspan="16">Half-word at address A</td><td colspan="16">Half-word at address A+2</td></tr>
<tr><td colspan="8">Byte at address A</td><td colspan="8">Byte at address A+1</td><td colspan="8">Byte at address A+2</td><td colspan="8">Byte at address A+3</td></tr>
</table>

Fig. 6.2.2 Big endian addresses of bytes and half-words within words

Little Endian

In Little endian format, the lowest addressed byte in a word is considered the least significant byte of the word and the highest addressed bye is the most significant. So the byte at address 0 of the memory system connects to data lines 7 through 0.

For a word aligned address A, Fig6.2.3 shows how the word at address A, the half-word at addresses A and A+2, and the bytes at addresses A, A+1, A+2, and A+3 map on to each other when **LITTLE** pin is High.

<table>
<tr><td colspan="32">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="32">Word at address A</td></tr>
<tr><td colspan="16">Half-word at address A+2</td><td colspan="16">Half-word at address A</td></tr>
<tr><td colspan="8">Byte at address A+3</td><td colspan="8">Byte at address A+2</td><td colspan="8">Byte at address A+1</td><td colspan="8">Byte at address A</td></tr>
</table>

Fig. 6.2.3 Little endian addresses of bytes and half-words within words

6.2.4.2. Connection of External Memory with Various Data Width

The system diagram for W90N740 connecting with the external memory is shown in Fig. 6.2.4. Below tables (Table6.2.3 – Table6.2.14) show the program/data path between CPU register and the external memory using little / big endian and word/half-word/byte access.

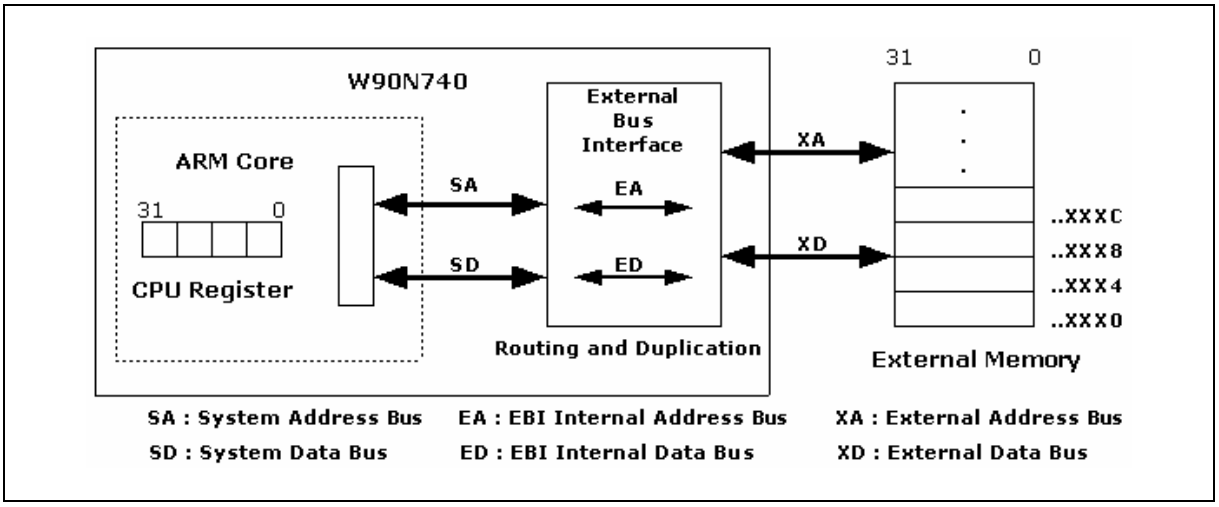


Fig. 6.2.4 Address/Data bus connection with external memory

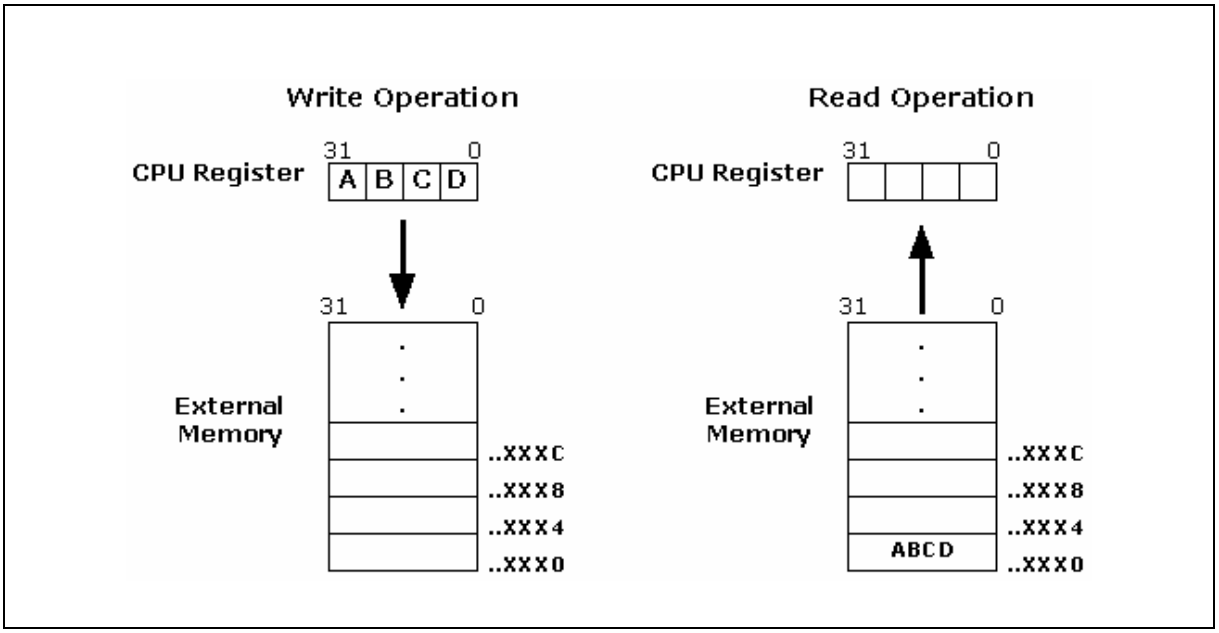


Fig. 6.2.5 CPU register Read/Write with external memory

Table 6.2.3 and Table 6.2.4

Using big-endian and word access, Program/Data path between register and external memory

WA = Address whose LSB is 0, 4, 8, C X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table6.2.3 Word access write operation with Big Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER ➔ EXTERNAL MEMORY)						
XD WIDTH	**WORD**	**HALF WORD**		**BYTE**			
BIT NUMBER **CPU REG DATA**	31 0 ABCD	31 0 ABCD		31 0 ABCD			
SA	WA	WA		WA			
BIT NUMBER **SD**	31 0 ABCD	31 0 AB CD		31 0 A B C D			
BIT NUMBER **ED**	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
NWBE [3-0] / **SDQM [3-0]**	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
BIT NUMBER **XD**	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
BIT NUMBER **EXT. MEM DATA**	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
TIMING SEQUENCE		1st write	2nd write	1st write	2nd write	3rd write	4th write

Table6.2.4 Word access read operation with Big Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)						
XD WIDTH	WORD	HALF WORD		BYTE			
Bit Number CPU Reg Data	31 0 ABCD	31 0 CDAB		31 0 DCBA			
SA	WA	WA		WA			
Bit Number SD	31 0 ABCD	31 0 CD AB		31 0 D C B A			
Bit Number ED	31 0 ABCD	31 0 CD XX	31 0 CD AB	31 0 D X X X	31 0 D C X X	31 0 D C B X	31 0 D C B A
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
SDQM [3-0]	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
Bit Number XD	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
Bit Number Ext. Mem Data	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
Timing Sequence		1st read	2nd read	1st read	2nd read	3rd read	4th read

Table 6.2.5 and Table 6.2.6

Using big-endian and half-word access, Program/Data path between register and external memory.

HA = Address whose LSB is 0, 2, 4, 6, 8, A, C, E HAL = Address whose LSB is 0, 4, 8, C

HAU = Address whose LSB is 2, 6, A, E X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table6.2.5 Half-word access write operation with Big Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER → EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	31 0 ABCD		31 0 ABCD	31 0 ABCD	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD
BIT NUMBER ED	31 0 CD CD	31 0 CD CD	31 0 CD CD	7 0 C	7 0 D
XA	HAL	HAL	HA	HA	HA+1
NWBE [3-0] / SDQM [3-0]	AAUU	UUAA	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 CD CD	31 0 CD CD	15 0 CD	7 0 C	7 0 D
BIT NUMBER EXT. MEM DATA	31 16 CD	15 0 CD	15 0 CD	7 0 C	7 0 D
TIMING SEQUENCE				1st write	2nd write

Table6.2.6 Half-word access read operation with Big Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	15 0 AB	15 0 CD	15 0 CD	15 0 DC	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	15 0 AB	15 0 CD	15 0 CD	15 0 DC	
BIT NUMBER ED	15 0 AB	15 0 CD	15 0 CD	15 0 DX	15 0 DC
XA	HAL	HAL	HA	HA	HA+1
SDQM [3-0]	AAUU	UUAA	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 AB CD	31 0 AB CD	15 0 CD	7 0 D	7 0 C
BIT NUMBER EXT. MEM DATA	31 0 ABCD		15 0 CD	7 0 D	7 0 C
TIMING SEQUENCE				1st read	2nd read

Table 6.2.7 and Table 6.2.8

Using big-endian and byte access, Program/Data path between register and external memory.

BA = Address whose LSB is 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

BAL = Address whose LSB is 0, 2, 4, 6, 8, A, C, E BAU = Address whose LSB is 1, 3, 5, 7, 9, B, D, F

BA0 = Address whose LSB is 0, 4, 8, C BA1 = Address whose LSB is 1, 5, 9, D

BA2 = Address whose LSB is 2, 6, A, E BA3 = Address whose LSB is 3, 7, B, F

Table6.2.7 Byte access write operation with Big Endian

ACCESS OPERATION	**WRITE OPERATION (CPU REGISTER ➔ EXTERNAL MEMORY)**						
XD WIDTH	**WORD**				**HALF WORD**		**BYTE**
Bit Number **CPU Reg Data**	31 0 ABCD				31 0 ABCD		31 0 ABCD
SA	BA0	BA1	BA2	BA3	BAL	BAU	BA
Bit Number **SD**	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D
Bit Number **ED**	31 24 D	23 16 D	15 8 D	7 0 D	15 8 D	7 0 D	7 0 D
XA	BA0	BA0	BA0	BA0	BAL	BAL	BA
nWBE [3-0] / **SDQM [3-0]**	AUUU	UAUU	UUAU	UUUA	XXAU	XXUA	XXXA
Bit Number **XD**	31 0 D X X X	31 0 X D X X	31 0 X X D X	31 0 X X X D	15 0 D X	15 0 X D	7 0 D
Bit Number **Ext. Mem Data**	31 24 D	23 16 D	15 8 D	7 0 D	15 8 D	7 0 D	7 0 D
Timing Sequence							

Table6.2.8 Byte access read operation with Big Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)						
XD WIDTH	WORD				HALF WORD		BYTE
BIT NUMBER CPU REG DATA	7 0 A	7 0 B	7 0 C	7 0 D	7 0 C	7 0 D	7 0 D
SA	BA0	BA1	BA2	BA3	BAL	BAU	BA
BIT NUMBER SD	7 0 A	7 0 B	7 0 C	7 0 D	7 0 C	7 0 D	7 0 D
BIT NUMBER ED	7 0 A	15 8 B	23 16 C	31 24 D	7 0 C	15 8 D	7 0 D
XA	BA0	BA0	BA0	BA0	BAL	BAL	BA
SDQM [3-0]	AUUU	UAUU	UUAU	UUUA	XXAU	XXUA	XXXA
BIT NUMBER XD	31 0 ABCD	31 0 ABCD	31 0 ABCD	31 0 ABCD	15 0 CD	15 0 CD	7 0 D
BIT NUMBER EXT. MEM DATA	31 0 ABCD				15 0 CD		7 0 D
TIMING SEQUENCE							

Table 6.2.9 and Table 6.2.10

Using little-endian and word access, Program/Data path between register and external memory

WA = Address whose LSB is 0, 4, 8, C X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table6.2.9 Word access write operation with Little Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER → EXTERNAL MEMORY)						
XD WIDTH	WORD	HALF WORD		BYTE			
BIT NUMBER CPU REG DATA	31 0 ABCD	31 0 ABCD		31 0 ABCD			
SA	WA	WA		WA			
BIT NUMBER SD	31 0 ABCD	31 0 AB CD		31 0 A B C D			
BIT NUMBER ED	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
NWBE [3-0] / SDQM [3-0]	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
BIT NUMBER XD	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
BIT NUMBER EXT. MEM DATA	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
TIMING SEQUENCE		1st write	2nd write	1st write	2nd write	3rd write	4th write

Table6.2.10 Word access read operation with Little Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)						
XD WIDTH	WORD	HALF WORD		BYTE			
BIT NUMBER CPU REG DATA	31 0 ABCD	31 0 ABCD		31 0 ABCD			
SA	WA	WA		WA			
BIT NUMBER SD	31 0 ABCD	31 0 AB CD		31 0 A B C D			
BIT NUMBER ED	31 0 ABCD	31 0 XX CD	31 0 AB CD	31 0 X X X D	31 0 X X C D	31 0 X B C D	31 0 A B C D
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
SDQM [3-0]	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
BIT NUMBER XD	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
BIT NUMBER EXT. MEM DATA	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
TIMING SEQUENCE		1st read	2nd read	1st read	2nd read	3rd read	4th read

Table 6.2.11 and Table 6.2.12

Using little-endian and half-word access, Program/Data path between register and external memory.

HA = Address whose LSB is 0, 2, 4, 6, 8, A, C, E HAL = Address whose LSB is 0,4,8,C

HAU = Address whose LSB is 2, 6, A, E X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table6.2.11 Half-word access write operation with Little Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER → EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	31 0 ABCD		31 0 ABCD	31 0 ABCD	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD
BIT NUMBER ED	31 0 CD CD	31 0 CD CD	31 0 CD CD	7 0 D	7 0 C
XA	HAL	HAL	HA	HA	HA+1
NWBE [3-0] / SDQM [3-0]	UUAA	AAUU	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 CD CD	31 0 CD CD	15 0 CD	7 0 D	7 0 C
BIT NUMBER EXT. MEM DATA	15 0 CD	31 16 CD	15 0 CD	7 0 D	7 0 C
TIMING SEQUENCE				1st write	2nd write

Table6.2.12 Half-word access read operation with Little Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	15 0 CD	15 0 AB	15 0 CD	15 0 CD	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	15 0 CD	15 0 AB	15 0 CD	15 0 CD	
BIT NUMBER ED	15 0 CD	15 0 AB	15 0 CD	15 0 XD	15 0 CD
XA	HAL	HAL	HA	HA	HA+1
SDQM [3-0]	UUAA	AAUU	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 AB CD	31 0 AB CD	15 0 CD	7 0 D	7 0 C
BIT NUMBER EXT. MEM DATA	31 0 ABCD		15 0 CD	7 0 D	7 0 C
TIMING SEQUENCE				1st read	2nd read

Table 6.2.13 and Table 6.2.14

Using little-endian and byte access, Program/Data path between register and external memory.

BA = Address whose LSB is 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

BAL = Address whose LSB is 0, 2, 4, 6, 8, A, C, E BAU = Address whose LSB is 1, 3, 5, 7, 9, B, D, F

BA0 = Address whose LSB is 0, 4, 8, C BA1 = Address whose LSB is 1, 5, 9, D

BA2 = Address whose LSB is 2, 6, A, E BA3 = Address whose LSB is 3, 7, B, F

Table6.2.13 Byte access write operation with Little Endian

ACCESS OPERATION	**WRITE OPERATION (CPU REGISTER → EXTERNAL MEMORY)**						
XD WIDTH	**WORD**				**HALF WORD**		**BYTE**
BIT NUMBER **CPU REG DATA**	31 0 ABCD				31 0 ABCD		31 0 ABCD
SA	BA0	BA1	BA2	BA3	BAL	BAU	BA
BIT NUMBER **SD**	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D	31 0 D D D D
BIT NUMBER **ED**	7 0 D	15 8 D	23 16 D	31 24 D	7 0 D	15 8 D	7 0 D
XA	BA0	BA0	BA0	BA0	BAL	BAL	BA
NWBE [3-0] / **SDQM [3-0]**	UUUA	UUAU	UAUU	AUUU	XXUA	XXAU	XXXA
BIT NUMBER **XD**	31 0 X X X D	31 0 X X D X	31 0 X D X X	31 0 D X X X	15 0 X D	15 0 D X	7 0 D
BIT NUMBER **EXT. MEM DATA**	7 0 D	15 8 D	23 16 D	31 24 D	7 0 D	15 8 D	7 0 D
TIMING SEQUENCE							

Table6.2.14 Byte access read operation with Little Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)						
XD WIDTH	WORD				HALF WORD		BYTE
BIT NUMBER CPU REG DATA	7 0 D	7 0 C	7 0 B	7 0 A	7 0 D	7 0 C	7 0 D
SA	BA0	BA1	BA2	BA3	BAL	BAU	BA
BIT NUMBER SD	7 0 D	7 0 C	7 0 B	7 0 A	7 0 D	7 0 C	7 0 D
BIT NUMBER ED	7 0 D	7 0 C	7 0 B	7 0 A	7 0 D	7 0 C	7 0 D
XA	BA0	BA0	BA0	BA0	BAL	BAL	BA
SDQM [3-0]	UUUA	UUAU	UAUU	AUUU	XXUA	XXAU	XXXA
BIT NUMBER XD	31 0 ABCD	31 0 ABCD	31 0 ABCD	31 0 ABCD	15 0 CD	15 0 CD	7 0 D
BIT NUMBER EXT. MEM DATA	31 0 ABCD				15 0 CD		7 0 D
TIMING SEQUENCE							

6.2.5 Bus Arbitration

The W90N740's internal function blocks or external devices can request mastership of the system bus and then hold the system bus in order to perform data transfers. The design of W90N740 bus allows only one bus master at a time, a bus controller is required to arbitrate when two or more internal units or external devices simultaneously request bus mastership. When bus mastership is granted to an internal function block or an external device, other pending requests are not acknowledged until the previous bus master has released the bus.

W90N740 supports two priority modes, the **Fixed Priority Mode** and the **Rotate Priority Mode**, depends on the **PRTMOD** bit setting.

6.2.5.1. Fixed Priority Mode

In **Fixed Priority Mode** (**PRTMOD** = 0, default value), to facilitate bus arbitration, priorities are assigned to each internal W90N740 function block. The bus controller arbitration requests for the bus mastership according to these fixed priorities. In the event of contention, mastership is granted to the function block with the highest assigned priority. These priorities are listed in Table 6.2.15.

W90N740 allows raising ARM Core priority to second if an unmasked interrupt occurred. If **IPEN** bit, Bit 22 of the **Arbitration Control Register (ARBCON)**, is set to "0", the priority of ARM Core is fixed to lowest. If **IPEN** bit is set to "1" and if no unmasked interrupt request, then the ARM Core's priority is still lowest and the **IPACT** = 0, Bit 23 of the **Arbitration Control Register (ARBCON)** ; If there is an unmasked interrupt request, then the ARM Core's priority is raised to second and **IPACT** = 1.

If **IPEN** is set, an interrupt handler will normally clear **IPACT** at the end of the interrupt routine to allow an alternate bus master to regain the bus; however, if **IPEN** is cleared, no additional action need be taken in the interrupt handler. The **IPACT** bit can be read and write. Writing with "0", the **IPACT** bit is cleared, but it will be no effect as writing with "1".

Table 6.2.15 Bus Priorities for Arbitration in Fixed Priority Mode

BUS	FUNCTION BLOCK	
PRIORITY	**IPACT = 0**	**IPEN = 1 AND IPACT = 1**
1 (HIGHEST)	External Bus Master	External Bus Master
2	NAT Accelerator	ARM Core
3	General DMA0	NAT Accelerator
4	General DMA1	General DMA0
5	EMC0 DMA	General DMA1
6	EMC1 DMA	EMC0 DMA
7	USB (Host)	EMC1 DMA
8 (LOWEST)	ARM Core	USB (Host)

6.2.5.2. Rotate Priority Mode

In **Rotate Priority Mode** (**PRTMOD** = 1), the **IPEN** and **IPACT** bits have no function (i.e. ignore). W90N740 used a round robin arbitration scheme ensures that all bus masters (except the **External Bus Master**, it always has the first priority) have equal chance to gain the bus and that a retracted master does not lock up the bus.

6.2.6 Power-On Setting

After power on reset, there are four Power-On setting pins to configure W90N740 system configuration.

POWER-ON SETTING	PIN
Internal System Clock Select	D15
Little/Big Endian Mode Select	D14
Boot ROM/FLASH Data Bus Width	D [13:12]

D15 pin：Internal System Clock Select

If pin D15 is pull-down, the external clock from EXTAL pin is served as internal system clock.

If pin D15 is pull-up, the PLL output clock is used as internal system clock.

D14 pin：Little/Big Endian Mode Select

If pin D14 is pull-down, the external memory format is Big Endian mode.

If pin D14 is pull-up, the external memory format is Little Endian mode.

D [13:12] ： Boot ROM/FLASH Data Bus Width

D [13:12]		BUS WIDTH
Pull-down	Pull-down	8-bit
Pull-down	Pull-up	16-bit
Pull-up	Pull-down	32-bit
Pull-up	Pull-up	RESERVED

Note: Related Power-On Setting Pin

D [11:10] ：

D [15]	D [11:10]	DESCRIPTION
Pull-up	Pull High	W90N740 normal operation

D [9:8] ：

D [9:8]	
Pull-up	Pull-up

6.2.7 System Manager Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
PDID	0xFFF0.0000	R	Product Identifier Register	0xX090.0740
ARBCON	0xFFF0.0004	R/W	Arbitration Control Register	0x0000.0000
PLLCON	0xFFF0.0008	R/W	PLL Control Register	0x0000.2F01
CLKSEL	0xFFF0.000C	R/W	Clock Select Register	0x0000.3FX8

Product Identifier Register （PDID）

This register is for read only and enables software to recognize certain characteristics of the chip ID and the version number.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
PDID	0xFFF0.0000	R	Product Identifier Register	0xX090.0740

31	30	29	28	27	26	25	24
PACKAGE		1					
23	22	21	20	19	18	17	16
CHPID							
15	14	13	12	11	10	9	8
CHPID							
7	6	5	4	3	2	1	0
CHPID							

PACKAGE [31:30] Package Type

PACKAGE [31:30]		BUS WIDTH
1	1	176-pin Package

CHPID [23:0]: Chip identifier

The Chip identifier of W90N740 is 0x90.0740

Arbitration Control Register (ARBCON)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
ARBCON	0xFFF0.0004	R/W	Arbitration Control Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					IPACT	IPEN	PRTMOD

IPACT [2] ： Interrupt priority active

When **IPEN**="1", this bit is set when the ARM core has an unmasked interrupt request.

This bit is available only when the **PRTMOD** = 0.

IPEN [1] ： Interrupt priority enable bit

0 = the ARM core has the lowest priority.

1 = enable to raise the ARM core priority to second

This bit is available only when the **PRTMOD** = 0.

PRTMOD [0] ： Priority mode select

0 = Fixed Priority Mode (default)

1 = Rotate Priority Mode

PLL Control Register （PLLCON）

W90N740 provides two options for clock generation - crystal and oscillator.

The external clock via **EXTAL** input pin as the reference clock input of **PLL** module. The external clock can bypass the **PLL** and be used to the internal system clock by pull-down the data D15 pin. Using **PLL**'s output clock for the internal system clock, D15 pin must be pull-up.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
PLLCON	0xFFF0.0008	R/W	PLL Control Register	0x0000.2F01

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							PWDEN
15	14	13	12	11	10	9	8
FBDV							
7	6	5	4	3	2	1	0
FBDV	OTDV		INDV				

PWDEN [16] ：Power down mode enable

0 = PLL is in normal mode (default)

1 = PLL is in power down mode

FBDV [15:7] ：PLL VCO output clock feedback divider

Feedback Divider divides the output clock from VCO of PLL.

OTDV [6:5] ：PLL output clock divider

OTDV [6:5]		DIVIDED BY
0	0	1
0	1	2
1	0	2
1	1	4

INDV [4:0] ：PLL input clock divider

Input Divider divides the input reference clock into the PLL.

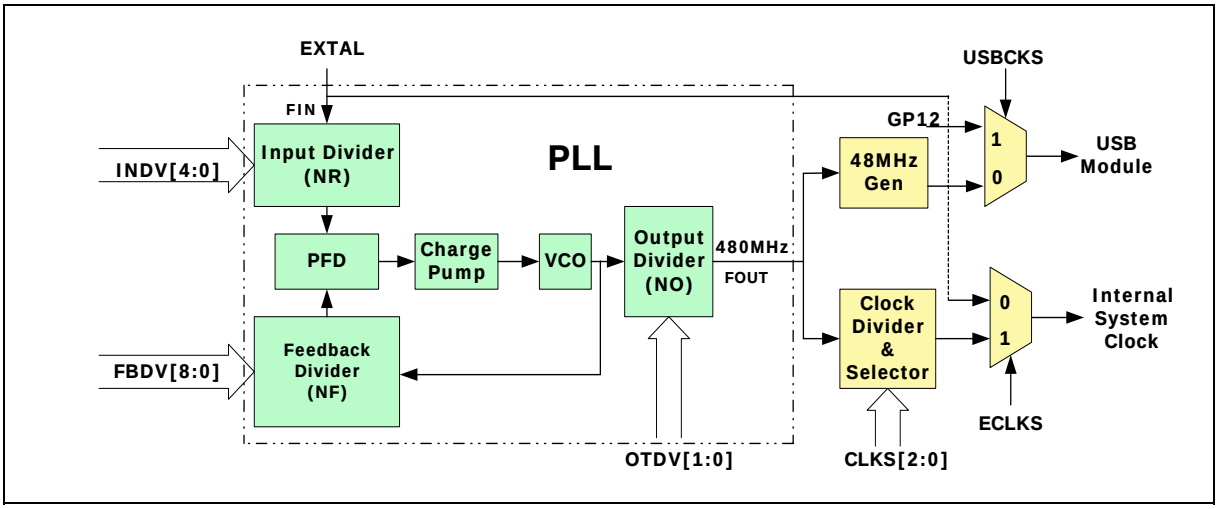


Fig 6.2.6 System PLL block diagram

The formula of output clock of PLL is:

$$F_{OUT} = F_{IN} * \frac{NF}{NR} * \frac{1}{NO}$$

FOUT：Output clock of **Output Divider**

FIN：External clock into the **Input Divider**

NR：Input divider value (NR = INDV + 2)

NF：Feedback divider value (NF = FBDV + 2)

NO：Output divider value (NO = OTDV)

Clock Select Register (CLKSEL)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CLKSEL	0xFFF0.000C	R/W	Clock Select Register	0x0000.3FX8

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
USBCKS	RESERVED	GDMA	NATA	EMC1	EMC0	WDTS	WDT
7	6	5	4	3	2	1	0
USB	TIMER	UART	ECLKS	CLKS			RESET

USBCKS [15] ： USB clock source Select bit

0 = USB clock 48MHz input from internal PLL (480MHz/10)

1 = USB clock 48MHz input from external GP12 pin, this GPIO pin direction must set to input.

GDMA [13] ： GDMA clock enable bit

0 = Disable GDMA clock

1 = Enable GDMA clock

NATA [12] ： NATA clock enable bit

0 = Disable NATA clock

1 = Enable NATA clock

EMC1 [11] ： EMC1 clock enable bit

0 = Disable EMC1 clock

1 = Enable EMC1 clock

EMC0 [10] ： EMC0 clock enable bit

0 = Disable EMC0 clock

1 = Enable EMC0 clock

WDTS [9] : WDTS clock selected bit

0 = Clock from EXTAL pin is used as WDT counting clock

1 = Clock from EXTAL pin is divided by 256, which is used as WDT counting clock

WDT [8] ： WDT clock enable bit

0 = Disable WDT counting clock

1 = Enable WDT counting clock

USB [7] ： USB clock enable bit

0 = Disable USB clock

1 = Enable USB clock

TIMER [6] ： Timer clock enable bit

0 = Disable Timer clock

1 = Enable Timer clock

UART [5] ： UART clock enable bit

0 = Disable UART clock

1 = Enable UART clock

ECLKS [4] ： External clock select

0 = External clock from EXTAL pin is used as system clock

1 = PLL output clock is used as system clock

After power on reset, the content of **ECLKS** is the Power-On Setting value. You can program this bit to change the system clock source.

CLKS [3:1] ： PLL output clock select

CLKS [3:1]			PLL OUTPUT CLOCK
0	0	0	58.594 KHz*
0	0	1	24 MHz
0	1	0	48 MHz
0	1	1	60 MHz
1	0	0	80 MHz
1	0	1	RESERVED
1	1	0	RESERVED
1	1	1	RESERVED

When 24Mhz ~ 120MHz is setting, the ECLKS bit is needed to set on PLL output clock mode (logic 1).

*About 58.594KHz setting, two steps are needed.

First step, the ECLKS bit is set to External Clock mode (logic 0, 15MHz), then set CLKS bits to 0.

RESET [0] ： Reset

This is a software reset control bit. Set logic 1 to generate an internal reset pulse. This bit is auto-clear to logic 0 at the end of the reset pulse.

6.3 External Bus Interface (EBI)

6.3.1 EBI Overview

External Bus Interface (**EBI**) controls the access to the external memory (ROM/SRAM/FLASH, SDRAM) and External I/O devices. The **EBI** has seven chip selects to select one ROM/FLASH bank, two SDRAM banks, and four External I/O banks and 25-bit address bus. It supports 8-bit, 16-bit, and 32-bit external data bus width for each bank.

The Features of the EBI：

- External I/O Control with 8/16/32 bit external data bus
- Cost-effective memory-to-peripheral DMA interface
- SDRAM Controller supports up to 2 external SDRAM & the maximum size of each device is 32MB
- ROM/FLASH & External I/O interface
- Support for PCMCIA 16-bit PC Card devices

6.3.2 SDRAM Controller

The W90N740's SDRAM Controller contains configuration registers, timing control registers, common control register and other logic. The SDRAM Controller provides 8/16/32 bits SDRAM interface with a single 8/16/32 bits SDRAM device or two 8-bit devices wired to give a 16-bit data path or two 16-bit devices wired to give a 32-bit data path. The maximum memory size of each bank is 32MB(Mbytes). One of two banks can be connected to the SDRAM interface, so the maximum memory can be up to 64MB.

The Features of the SDRAM Controller：

- 8/16/32-bit data interface
- Supports up to 2 external SDRAM devices and Maximum size of each device is 32MB
- Programmable CAS Latency： 1、2 and 3
- Fixed Burst Length： 1
- Sequential burst type
- Write Burst Length mode is Burst
- Auto Refresh Mode and Self Refresh Mode
- Adjustable Refresh Rate
- Power up sequence

6.3.2.1. SDRAM Components Supported

- 16M bit SDRAM
  - 2Mx8 with 2 banks ；RA0 ~ RA10, CA0 ~ CA8
  - 1Mx16 with 2 banks；RA0 ~ RA10, CA0 ~ CA7
- 64M bit SDRAM
  - 8Mx8 with 4 banks；RA0 ~ RA11, CA0 ~ CA8
  - 4Mx16 with 4 banks；RA0 ~ RA11, CA0 ~ CA7
  - 2Mx32 with 4 banks ；RA0 ~ RA10, CA0 ~ CA7
- 128M bit SDRAM
  - 16Mx8 with 4 banks；RA0 ~ RA11, CA0 ~ CA9
  - 8Mx16 with 4 banks；RA0 ~ RA11, CA0 ~ CA8
  - 4Mx32 with 4 banks；RA0 ~ RA11, CA0 ~ CA7
- 256M bit SDRAM
  - 32Mx8 with 4 banks；RA0 ~ RA12, CA0 ~ CA9
  - 16Mx16 with 4 banks；RA0 ~ RA12, CA0 ~ CA8

6.3.2.2. AHB Bus Address Mapping to SDRAM Bus

Note: * indicates the signal is not used; ** indicates the signal is fixed at logic 0 and is not used;
The HADDR prefixes have been omitted on the following tables.
A14 ~ A0 are the Address pins of the W90N740 EBI interface;

A14 and A13 are the Bank Selected Signal of SDRAM.

SDRAM Data Bus Width: 32-bit

Total	Type	R x C	R/C	A14 (BS1)	A13 (BS0)	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16M	2Mx8	11x9	R	**	11	**	11*	22	21	20	19	18	17	16	15	14	13	12
			C	**	11	**	11*	AP	25*	10	9	8	7	6	5	4	3	2
16M	1Mx16	11x8	R	**	10	**	10*	11	21	20	19	18	17	16	15	14	13	12
			C	**	10	**	10*	AP	25*	10*	9	8	7	6	5	4	3	2
64M	8Mx8	12x9	R	11	12	11*	23	22	21	20	19	18	17	16	15	14	13	24
			C	11	12	11*	23*	AP	25*	10	9	8	7	6	5	4	3	2
64M	4Mx16	12x8	R	11	10	11*	23	22	21	20	19	18	17	16	15	14	13	12
			C	11	10	11*	23*	AP	25*	24*	9	8	7	6	5	4	3	2
64M	2Mx32	11x8	R	11	10	11*	23*	22	21	20	19	18	17	16	15	14	13	12
			C	11	10	11*	23*	AP	25*	24*	9	8	7	6	5	4	3	2
128M*	16Mx8	12x10	R	11	12	11*	23	22	21	20	19	18	17	16	15	14	13	24
			C	11	12	11*	23*	AP	25	10	9	8	7	6	5	4	3	2
128M	8Mx16	12x9	R	11	12	11*	23	22	21	20	19	18	17	16	15	14	13	24
			C	11	12	11*	23*	AP	25*	10	9	8	7	6	5	4	3	2
128M	4Mx32	12x8	R	11	10	11*	23	22	21	20	19	18	17	16	15	14	13	12
			C	11	10	11*	23*	AP	25*	10*	9	8	7	6	5	4	3	2
256M*	32Mx8	13x10	R	11	12	24	23	22	21	20	19	18	17	16	15	14	13	25
			C	11	12	24*	23*	AP	26*	10	9	8	7	6	5	4	3	2
256M*	16Mx16	13x9	R	11	12	24	23	22	21	20	19	18	17	16	15	14	13	25
			C	11	12	24*	23*	AP	26*	10*	9	8	7	6	5	4	3	2

SDRAM Data Bus Width: 16-bit

Total	Type	R x C	R/C	A14 (BS1)	A13 (BS0)	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16M	2Mx8	11x9	R	**	10	**	10*	21	20	19	18	17	16	15	14	13	12	11
			C	**	10	**	10*	AP	24*	9	8	7	6	5	4	3	2	1
16M	1Mx16	11x8	R	**	9	**	9*	10	20	19	18	17	16	15	14	13	12	11
			C	**	9	**	9*	AP	24*	9*	8	7	6	5	4	3	2	1
64M	8Mx8	12x9	R	10	11	10*	22	21	20	19	18	17	16	15	14	13	12	23
			C	10	11	10*	22*	AP	24*	9	8	7	6	5	4	3	2	1
64M	4Mx16	12x8	R	10	9	10*	22	21	20	19	18	17	16	15	14	13	12	11
			C	10	9	10*	22*	AP	24*	23*	8	7	6	5	4	3	2	1
64M	2Mx32	11x8	R	10	9	10*	22*	21	20	19	18	17	16	15	14	13	12	11
			C	10	9	10*	22*	AP	24*	23*	8	7	6	5	4	3	2	1
128M	16Mx8	12x10	R	10	11	10*	22	21	20	19	18	17	16	15	14	13	12	23
			C	10	11	10*	22*	AP	24	9	8	7	6	5	4	3	2	1
128M	8Mx16	12x9	R	10	11	10*	22	21	20	19	18	17	16	15	14	13	12	23
			C	10	11	10*	22*	AP	24*	9	8	7	6	5	4	3	2	1
128M	4Mx32	12x8	R	10	9	10*	22	21	20	19	18	17	16	15	14	13	12	11
			C	10	9	10*	22*	AP	24*	9*	8	7	6	5	4	3	2	1
256M*	32Mx8	13x10	R	10	11	23	22	21	20	19	18	17	16	15	14	13	12	24
			C	10	11	23*	22*	AP	25*	9	8	7	6	5	4	3	2	1
256M	16Mx16	13x9	R	10	11	23	22	21	20	19	18	17	16	15	14	13	12	24
			C	10	11	23*	22*	AP	25*	9	8	7	6	5	4	3	2	1

SDRAM Data Bus Width: 8-bit

Total	Type	R x C	R/C	A14 (BS1)	A13 (BS0)	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16M	2Mx8	11x9	R	**	9	**	9*	20	19	18	17	16	15	14	13	12	11	10
			C	**	9	**	9*	AP	23*	8	7	6	5	4	3	2	1	0
16M	1Mx16	11x8	R	**	8	**	8*	9	19	18	17	16	15	14	13	12	11	10
			C	**	8	**	8*	AP	23*	8*	7	6	5	4	3	2	1	0
64M	8Mx8	12x9	R	9	10	9*	21	20	19	18	17	16	15	14	13	12	11	22
			C	9	10	9*	21*	AP	23*	8	7	6	5	4	3	2	1	1
64M	4Mx16	12x8	R	9	8	9*	21	20	19	18	17	16	15	14	13	12	11	10
			C	9	8	9*	21*	AP	23*	22*	7	6	5	4	3	2	1	0
64M	2Mx32	11x8	R	9	8	9*	21*	20	19	18	17	16	15	14	13	12	11	10
			C	9	8	9*	21*	AP	23*	22*	7	6	5	4	3	2	1	0
128M	16Mx8	12x10	R	9	10	9*	21	20	19	18	17	16	15	14	13	12	11	22
			C	9	10	9*	21*	AP	23	8	7	6	5	4	3	2	1	0
128M	8Mx16	12x9	R	9	10	9*	21	20	19	18	17	16	15	14	13	12	11	22
			C	9	10	9*	21*	AP	23*	8	7	6	5	4	3	2	1	0
128M	4Mx32	12x8	R	9	8	9*	21	20	19	18	17	16	15	14	13	12	11	10
			C	9	8	9*	21*	AP	23*	8*	7	6	5	4	3	2	1	0
256M	32Mx8	13x10	R	9	10	22	21	20	19	18	17	16	15	14	13	12	11	23
			C	9	10	22*	21*	AP	24	8	7	6	5	4	3	2	1	0
256M	16Mx16	13x9	R	9	10	22	21	20	19	18	17	16	15	14	13	12	11	23
			C	9	10	22*	21*	AP	24*	8	7	6	5	4	3	2	1	0

SDRAM Power Up Sequence

The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. W90N740 supports the function of Power Up Sequence, that is, after system power on the W90N740 SDRAM Controller automatically executes the commands needed for Power Up Sequence and set the mode register of each bank to default value. The default value is:

- Burst Length = 1
- Burst Type = Sequential (fixed)
- CAS Latency = 2
- Write Burst Length = Burst (fixed)

The value of mode register can be changed after power up sequence by setting the value of corresponding bank's configuration register "**LENGTH**" and "**LATENCY**" bits and set the **MRSET** bit enable to execute the Mode Register Set command.

6.3.2.3. SDRAM Interface

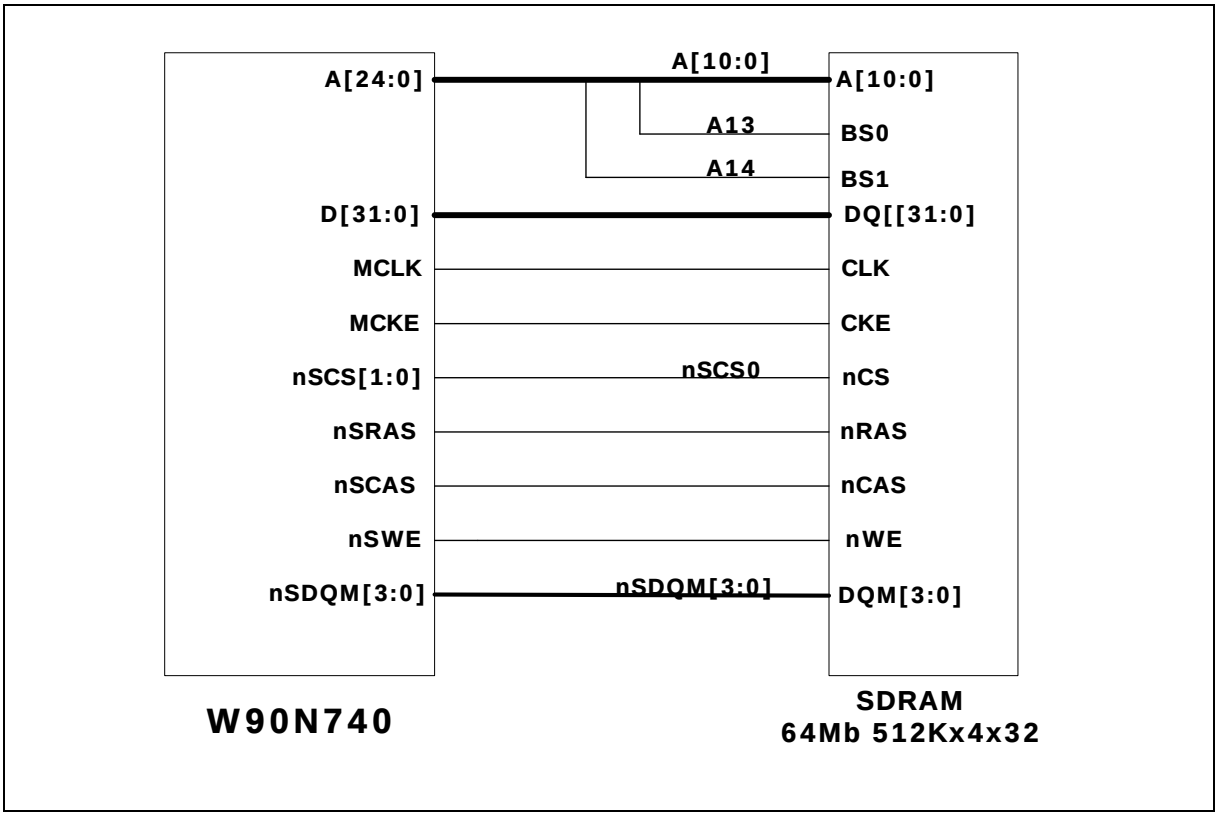


Fig 6.3.1 SDRAM Interface

6.3.3 External Bus Mastership

The W90N740 can receive and acknowledge bus request signals that are generated by an external bus master. When the CPU asserts an external bus acknowledge signal, mastership is granted to the external bus master, assuming the external bus request is still active.

When the external bus acknowledge signal is active, the W90N740's memory interface signals go to high impedance state so that the external bus master can drive the required external memory interface signals.

The W90N740 does not perform SDRAM refreshes when it is not the bus master. When an external bus master is in control of the external bus, and if it retains control for a long period of time, it must assume the responsibility of performing the necessary SDRAM refresh operations.

6.3.4 EBI Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
EBICON	0xFFF0.1000	R/W	EBI control register	0x0001.0000
ROMCON	0xFFF0.1004	R/W	ROM/FLASH control register	0x0000.0XFC
SDCONF0	0xFFF0.1008	R/W	SDRAM bank 0 configuration register	0x0000.0800
SDCONF1	0xFFF0.100C	R/W	SDRAM bank 1 configuration register	0x0000.0800
SDTIME0	0xFFF0.1010	R/W	SDRAM bank 0 timing control register	0x0000.0000
SDTIME1	0xFFF0.1014	R/W	SDRAM bank 1 timing control register	0x0000.0000
EXT0CON	0xFFF0.1018	R/W	External I/O 0 control register	0x0000.0000
EXT1CON	0xFFF0.101C	R/W	External I/O 1 control register	0x0000.0000
EXT2CON	0xFFF0.1020	R/W	External I/O 2 control register	0x0000.0000
EXT3CON	0xFFF0.1024	R/W	External I/O 3 control register	0x0000.0000
CKSKEW	0xFFF0.1F00	R/W	Clock skew control register	0xXXXX.0038

EBI Control Register (EBICON)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
EBICON	0xFFF0.1000	R/W	EBI control register	0x0001.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					REFEN	REFMOD	CLKEN
15	14	13	12	11	10	9	8
REFRAT							
7	6	5	4	3	2	1	0
REFRAT					WAITVT		LITTLE

REFEN [18]: Enable SDRAM refresh cycle for SDRAM bank0 & bank1

This bit set will start the auto-refresh cycle to SDRAM. The refresh rate is according to REFRAT bits.

REFMOD [17]: The refresh mode of SDRAM for SDRAM bank

Defines the refresh mode type of external SDRAM bank

0 = Auto refresh mode

1 = Self refresh mode

CLKEN [16]: Clock enable for SDRAM

Enables the SDRAM clock enable (**CKE**) control signal

0 = Disable (power down mode)

1 = Enable （Default）

REFRAT [15:3]: Refresh count value for SDRAM

The refresh period is calculated as $period = \frac{value}{fMCLK}$

The SDRAM Controller automatically provides an auto refresh cycle for every refresh period programmed into the **REFRAT** bits when the **REFEN** bit of each bank is set.

WAITVT [2:1]: Valid time of nWAIT signal

W90N740 recognizes the **nEWAIT** signal at the next "nth" **MCLK** rising edge after the **nOE** or **nWBE** active cycle. **WAITVT** bits determine the n.

WAITVT [2:1]		NTH MCLK
0	0	1
0	1	2
1	0	3
1	1	4

LITTLE [0] ：Read only, Little Endian mode

0 = EBI memory format is Big Endian mode

1 = EBI memory format is Little Endian mode

After power on reset, the content of **LITTLE** is the Power-On Setting value from D14 pin.

If pin D14 is pull-down, the external memory format is Big Endian mode.

If pin D14 is pull-up, the external memory format is Little Endian mode.

For more detail, refer to **Power-On Setting** of **System Manager**.

ROM/Flash Control Register （ROMCON）

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
ROMCON	0xFFF0.1004	R/W	ROM/FLASH control register	0x0000.0XFC

31	30	29	28	27	26	25	24
BASADDR							
23	22	21	20	19	18	17	16
BASADDR					SIZE		
15	14	13	12	11	10	9	8
RESERVED				tPA			
7	6	5	4	3	2	1	0
tACC				BTSIZE		PGMODE	

BASADDR [31:19] ：Base address pointer of ROM/Flash bank

The start address is calculated as ROM/Flash bank base pointer << 18. The base address pointer together with the "**SIZE**" bits constitutes the whole address range of each bank.

SIZE [18:16] ：The size of ROM/FLASH memory

SIZE [10:8]			BYTE
0	0	0	256K
0	0	1	512K
0	1	0	1M
0	1	1	2M
1	0	0	4M
1	0	1	8M
1	1	0	16M
1	1	1	32M

tPA [11:8]：Page mode access cycle time

tPA [11:8]				MCLK
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8

tPA [11:8]				MCLK
1	0	0	0	10
1	0	0	1	12
1	0	1	0	14
1	0	1	1	16
1	1	0	0	18
1	1	0	1	20
1	1	1	0	22
1	1	1	1	24

tACC [7:4]：Access cycle time

tACC [7:4]				MCLK
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8

tACC [7:4]				MCLK
1	0	0	0	10
1	0	0	1	12
1	0	1	0	14
1	0	1	1	16
1	1	0	0	18
1	1	0	1	20
1	1	1	0	22
1	1	1	1	24

BTSIZE [3:2] ：Read only, the boot ROM/FLASH data bus width

This ROM/Flash bank is designed for a boot ROM. **BASADDR** bits determine its start address. The external data bus width is determined by the data bus signals D [13:12] power-on setting.

BTSIZE [3:2]		BUS WIDTH
0	0	8-bit
0	1	16-bit
1	0	32-bit
1	1	RESERVED

D [13:12]		BUS WIDTH
Pull-down	Pull-down	8-bit
Pull-down	Pull-up	16-bit
Pull-up	Pull-down	32-bit
Pull-up	Pull-up	RESERVED

PGMODE [1:0] ：Page mode configuration

PGMODE [1:0]		MODE
0	0	Normal ROM
0	1	4 word page
1	0	8 word page
1	1	16 word page

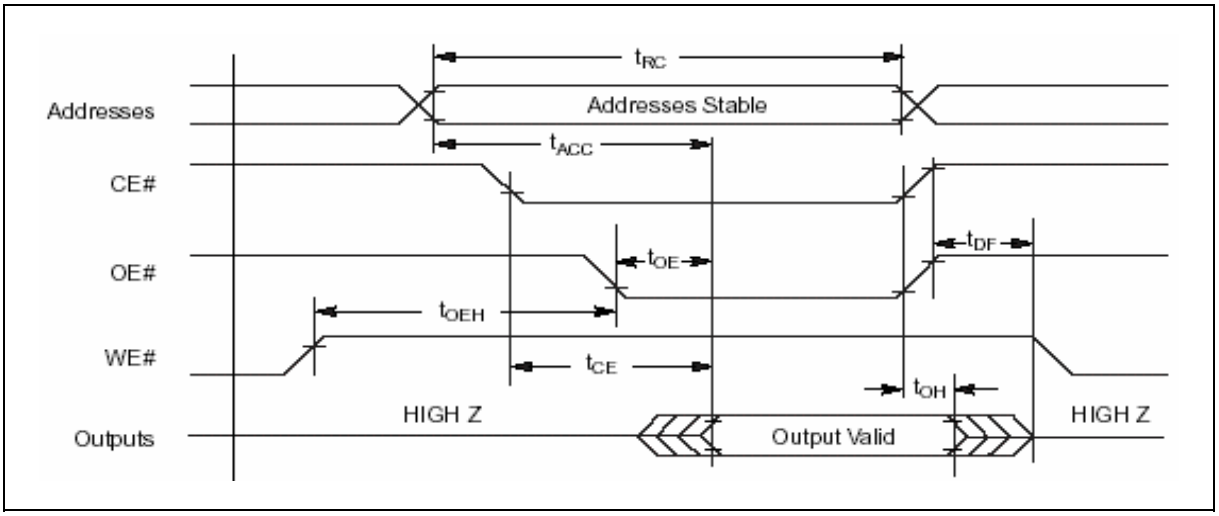


Fig6.3.2 ROM/FLASH Read Operation Timing

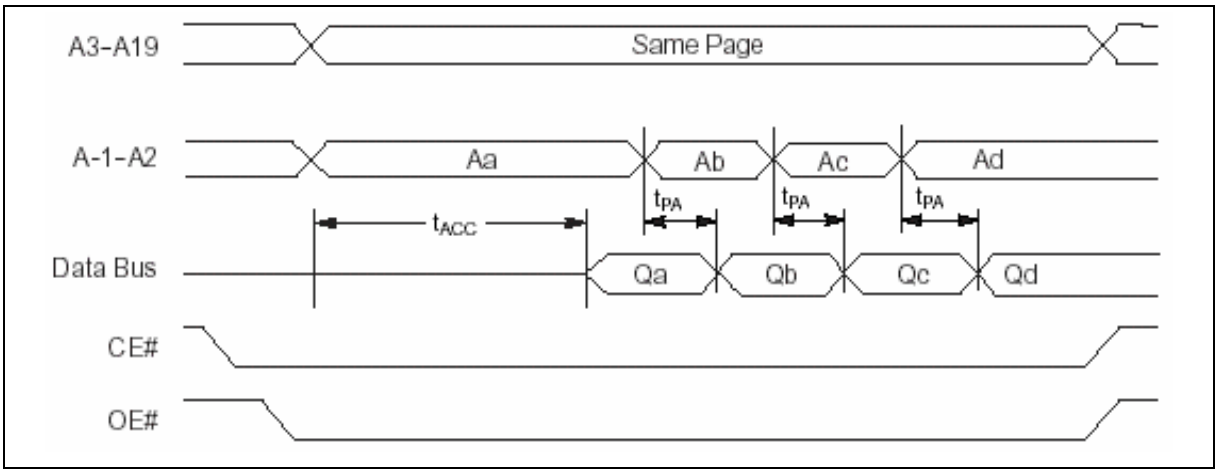


Fig 6.3.3 ROM/FLASH Page Read Operation Timing

Configuration Registers（SDCONF0/1）

The configuration registers enable software to set a number of operating parameters for the SDRAM controller. There are two configuration registers SDCONF0、SDCONF1 for SDRAM bank 0、bank 1 respectively. Each bank can have a different configuration.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
SDCONF0	0xFFF0.1008	R/W	SDRAM bank 0 configuration register	0x0000.0800
SDCONF1	0xFFF0.100C	R/W	SDRAM bank 1 configuration register	0x0000.0800

31	30	29	28	27	26	25	24
BASADDR							
23	22	21	20	19	18	17	16
BASADDR					RESERVED		
15	14	13	12	11	10	9	8
MRSET	RESERVED	AUTOPR	LATENCY		RESERVED		
7	6	5	4	3	2	1	0
COMPBK	DBWD		COLUMN		SIZE		

BASADDR [31:19] ：Base address pointer of SDRAM bank 0/1

The start address is calculated as SDRAM bank 0/1 base pointer << 18. The SDRAM base address pointer together with the "**SIZE**" bits constitutes the whole address range of each SDRAM bank.

MRSET [15] ：SDRAM Mode register set command for SDRAM bank 0/1

This bit set will issue a mode register set command to SDRAM.

AUTOPR [13] ：Auto pre-charge mode of SDRAM for SDRAM bank 0/1

Enable the auto pre-charge function of external SDRAM bank 0/1

0 = Auto pre-charge

1 = No auto pre-charge

LATENCY [12:11] ：The CAS Latency of SDRAM bank 0/1

Defines the CAS latency of external SDRAM bank 0/1

LATENCY [12:11]		MCLK
0	0	1
0	1	2
1	0	3
1	1	REVERSED

COMPBK [7] ： Number of component bank in SDRAM bank 0/1

Indicates the number of component bank (2 or 4 banks) in external SDRAM bank 0/1.

0 = 2 banks

1 = 4 banks

DBWD [6:5] ：Data bus width for SDRAM bank 0/1

Indicates the external data bus width connect with SDRAM bank 0/1

If DBWD = 00, the assigned SDRAM access signal is not generated i.e. disable.

DBWD [6:5]		BITS
0	0	Bank disable
0	1	8-bit (byte)
1	0	16-bit (half-word)
1	1	32-bit (word)

COLUMN [4:3] ：Number of column address bits in SDRAM bank 0/1

Indicates the number of column address bits in external SDRAM bank 0/1.

COLUMN [4:3]		BITS
0	0	8
0	1	9
1	0	10
1	1	REVERSED

SIZE [2:0] ：Size of SDRAM bank 0/1

Indicates the memory size of external SDRAM bank 0/1

SIZE [2:0]			Size of SDRAM （Byte）
0	0	0	Bank disable
0	0	1	2M
0	1	0	4M
0	1	1	8M
1	0	0	16M
1	0	1	32M
1	1	0	64M
1	1	1	REVERSED

Timing Control Registers （SDTIME0/1）

W90N740 offers the flexible timing control registers to control the generation and processing of the control signals and can achieve you use different speed of SDRAM

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
SDTIME0	0xFFF0.1010	R/W	SDRAM bank 0 timing control register	0x0000.0000
SDTIME1	0xFFF0.1014	R/W	SDRAM bank 1 timing control register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					tRCD		
7	6	5	4	3	2	1	0
tRDL		tRP			tRAS		

tRCD [10:8] ：SDRAM bank 0/1, /RAS to /CAS delay (see Fig 6.3.4)

tRCD [10:8]			MCLK
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

tRDL [7:6] ：SDRAM bank 0/1, Last data in to pre-charge command (see Fig 6.3.5)

tRDL [7:6]		MCLK
0	0	1
0	1	2
1	0	3
1	1	4

tRP [5:3] ：SDRAM bank 0/1, Row pre-charge time (see Fig 6.3.4)

tRP [5:3]			MCLK
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

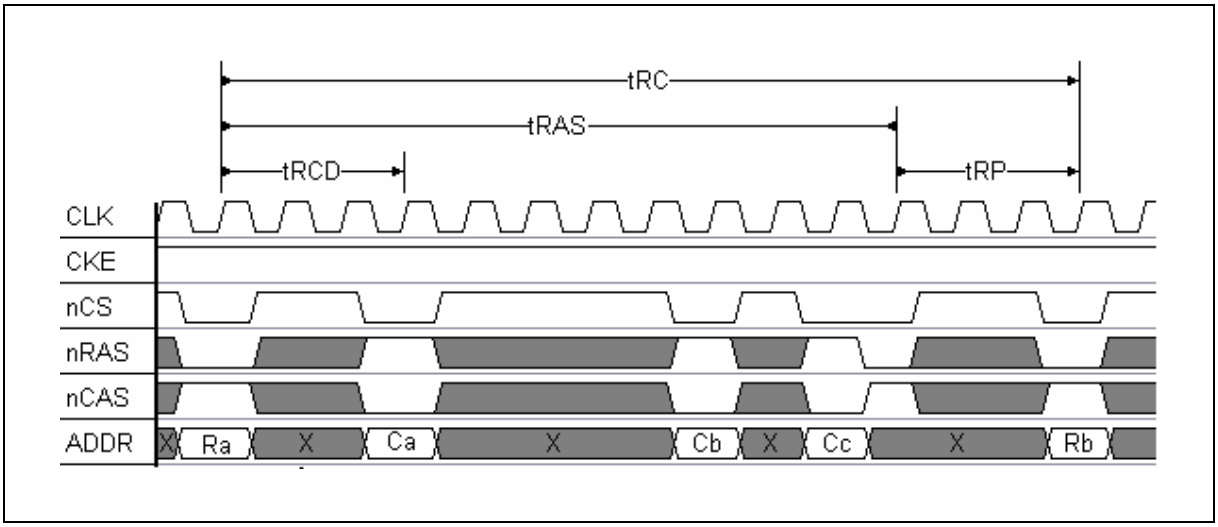


Fig 6.3.4 Access timing 1 of SDRAM

tRAS [2:0] ：SDRAM bank 0/1, Row active time (see Fig 6.3.4)

tRAS [2:0]			MCLK
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

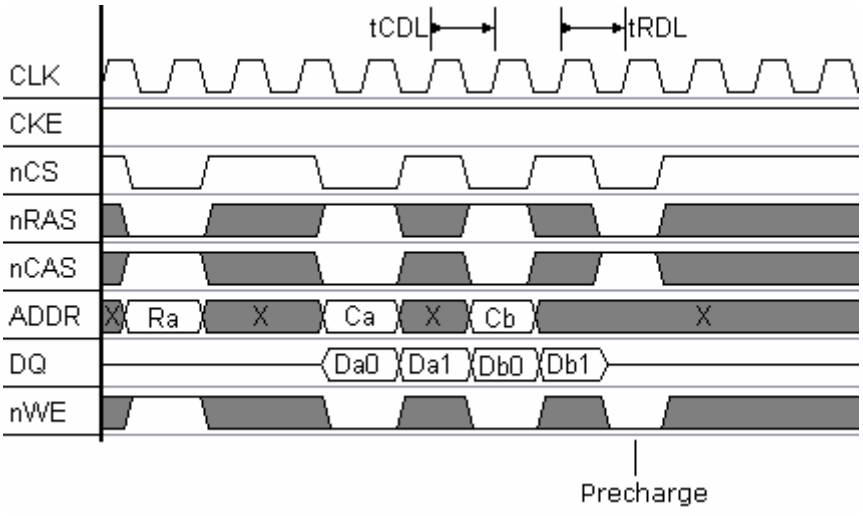


Fig 6.3.5 Access timing 2 of SDRAM

External I/O Control Registers（EXT0CON – EXT3CON）

The W90N740 supports an external device control without glue logic. It is very cost effective because address decoding and control signals timing logic are not needed. Using these control registers you can configure special external I/O devices for providing the low cost external devices control solution.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
EXT0CON	0xFFF0.1018	R/W	External I/O 0 control register	0x0000.0000
EXT1CON	0xFFF0.101C	R/W	External I/O 1 control register	0x0000.0000
EXT2CON	0xFFF0.1020	R/W	External I/O 2 control register	0x0000.0000
EXT3CON	0xFFF0.1024	R/W	External I/O 3 control register	0x0000.0000

31	30	29	28	27	26	25	24
BASADDR							
23	22	21	20	19	18	17	16
BASADDR					SIZE		
15	14	13	12	11	10	9	8
ADRS	tACC				tCOH		
7	6	5	4	3	2	1	0
tACS			tCOS			DBWD	

BASADDR [31:19] ：Base address pointer of external I/O bank 0~3

The start address of each external I/O bank is calculated as “**BASADDR”** base pointer << 18.

Each external I/O bank base address pointer together with the “**SIZE**” bits constitutes the whole address range of each external I/O bank.

SIZE [18:16] ：The size of the external I/O bank 0~3

SIZE [18:16]			Byte
0	0	0	256K
0	0	1	512K
0	1	0	1M
0	1	1	2M
1	0	0	4M
1	0	1	8M
1	1	0	16M
1	1	1	32M

ADRS [15] ：Address bus alignment for external I/O bank 0~3

When **ADRS** is set, EBI bus is alignment to byte address format, and ignores **DBWD [1:0]** setting.

tACC [14:11] ：Access cycles （nOE or nWE active time）for external I/O bank 0~3

tACC [14:11]				MCLK
0	0	0	0	Reserved
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

tACC [14:11]				MCLK
1	0	0	0	9
1	0	0	1	11
1	0	1	0	13
1	0	1	1	15
1	1	0	0	17
1	1	0	1	19
1	1	1	0	21

tCOH [10:8] ：Chip selection hold-on time on nWBE for external I/O bank 0~3

tCOH [10:8]			MCLK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

tACS [7:5] ：Address set-up before nECS for external I/O bank 0~3

tACS [7:5]			MCLK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

tCOS [4:2]：Chip selection set-up time on nOE or nWBE for external I/O bank 0~3

When ROM/Flash memory bank is configured, the access to its bank stretches chip selection time before the nOE or new signal is activated.

tCOS [4:2]			MCLK
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

DBWD [1:0] ：Programmable data bus width for external I/O bank 0~3

DBWD [1:0]		WIDTH OF DATA BUS
0	0	Disable bus
0	1	8-bit
1	0	16-bit
1	1	32-bit

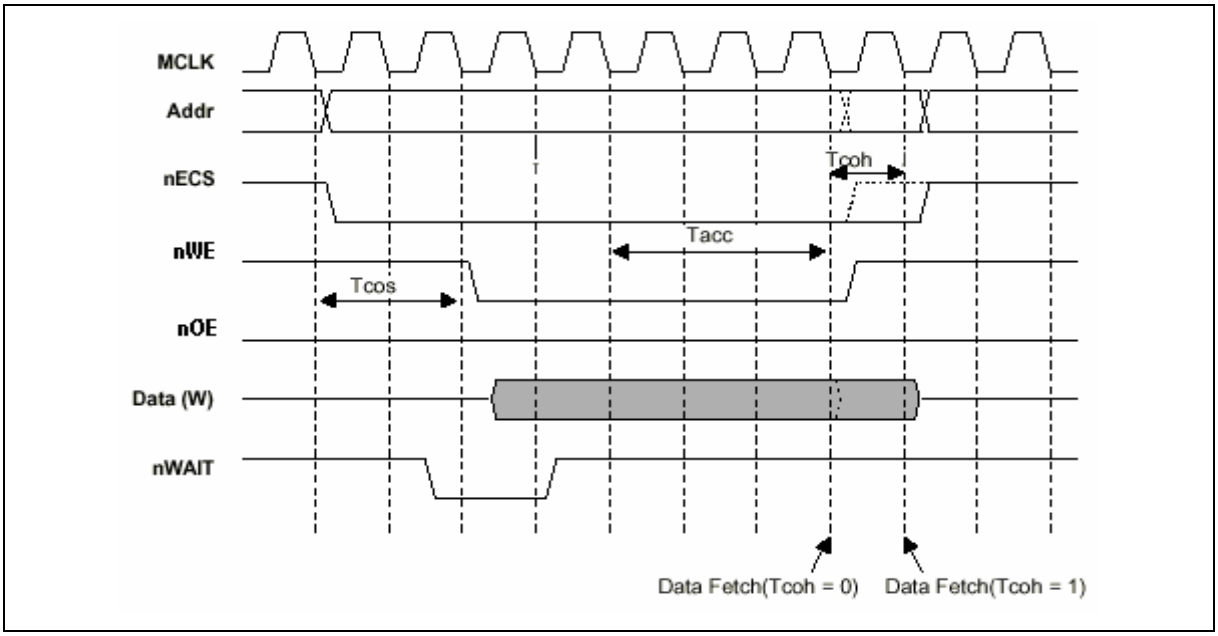


Fig 6.3.6 External I/O write operation timing

Clock Skew Control Register （CKSKEW）

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CKSKEW	0xFFF7.1F00	R/W	Clock skew control register	0xXXXX.0038

31	30	29	28	27	26	25	24
DLH_CLK_REF							
23	22	21	20	19	18	17	16
DLH_CLK_REF							
15	14	13	12	11	10	9	8
RESVERED							SWPON
7	6	5	4	3	2	1	0
DLH_CLK_SKEW				MCLK_O_D			

DLH_CLK_REF [31:16]: Latch DLH_CLK clock tree by HCLK positive edge. (Read Only)

SWPON [8]: SDRAM Initialization by Software trigger

Set this bit will issue a SDRAM power on default setting command, this bit will be auto-clear by hardware.

DLH_CLK_SKEW [7:4] ：Data latch clock skew adjustment

DLH_CLK_SKEW [7:4]				GATE DELAY
0	0	0	0	P-0
0	0	0	1	P-1
0	0	1	0	P-2
0	0	1	1	P-3
0	1	0	0	P-4
0	1	0	1	P-5
0	1	1	0	P-6

DLH_CLK_SKEW [7:4]				GATE DELAY
1	0	0	0	N-0
1	0	0	1	N-1
1	0	1	0	N-2
1	0	1	1	N-3
1	1	0	0	N-4
1	1	0	1	N-5
1	1	1	0	N-6

Note: P-x means Data latched Clock shift “X” gates delays by refer MCLKO positive edge,
N-x means Data latched Clock shift “X” gates delays by refer MCLKO negative edge.

MCLK_O_D [3:0] ：MCLK output delay adjustment

MCLK_O_D [3:0]				GATE DELAY
0	0	0	0	P-0
0	0	0	1	P-1
0	0	1	0	P-2
0	0	1	1	P-3
0	1	0	0	P-4
0	1	0	1	P-5
0	1	1	0	P-6

MCLK_O_D [3:0]				GATE DELAY
1	0	0	0	N-0
1	0	0	1	N-1
1	0	1	0	N-2
1	0	1	1	N-3
1	1	0	0	N-4
1	1	0	1	N-5
1	1	1	0	N-6

Note: P-x means MCLKO shift “X” gates delay by refer HCLK positive edge,
N-x means MCLKO shift “X” gates delay by refer HCLK negative edge.
MCLK is the output pin of MCLKO, which is a internal signal on chip.

6.4 Cache Controller

The W90N740 has an 8KB Instruction cache, 2KB Data cache, and 8 words write buffer. The I-Cache and D-Cache are similar except the cache size. To enhance the hit ratio, these two caches are configured two-way set associative addressing. Each cache has four words cache line size. When a miss occurs, four words must be fetched consecutively from external memory. The replacement algorithm is a LRU (Least Recently Used).

The W90N740 also provides a write buffer to improve system performance. The write buffer can buffer up to eight words of data.

6.4.1 On-Chip RAM

If I-Cache or D-Cache is disabled, it can be served as On-Chip RAM. If D-Cache is disabled, there has 2KB On-Chip RAM, its start address is 0xFFE02000. If I-Cache is disabled, there has 8KB On-Chip RAM and the start address of this RAM is 0xFFE00000. If both the I-Cache and D-Cache are disabled, it has 10KB On-Chip RAM starting from 0xFFE00000.

The size of On-Chip RAM is depended on the I-Cache and D-Cache enable bits **ICAEN**, **DCAEN** in Cache Control Register (CAHCON).

Table6.4.1 The size and start address of On-Chip RAM

ICAEN	DCAEN	ON-CHIP RAM	
		Size	Start Address
0	0	10KB	0xFFE0.0000
0	1	8KB	0xFFE0.0000
1	0	2KB	0xFFE0.2000
1	1	Unavailable	

6.4.2 Non-Cacheable Area

Although the cache affects the entire 2GB system memory, it is sometimes necessary to define non-cacheable areas when the consistency of data stored in memory and the cache must be ensured. To support this, the W90N740 provides a non-cacheable area control bit in the address field, A [31].

If A [31] in the ROM/FLASH, SDRAM, or external I/O bank's access address is "0", then the accessed data is cacheable. If the A [31] value is "1", the accessed data is non-cacheable.

6.4.3 Instruction Cache

The Instruction cache (I-cache) is an 8K bytes two-way set associative cache. The cache organization is 256 sets, two lines per set, and four words per line. Cache lines are aligned on 4-word boundaries in memory.

The cache access cycle begins with an instruction request from the instruction unit in the core. In the case of a cache hit, the instruction is delivered to the instruction unit. In case of a cache miss, the cache initiates a burst read cycle on the internal bus with the address of the requested instruction. The first word received from the bus is the requested instruction. The cache forwards this instruction to the instruction unit of the core as soon as it is received from the internal bus. A cache line is then selected to receive the data that will be coming from the bus. A least recently used (LRU) replacement algorithm is used to select a line when no empty lines are available.

When I-Cache is disabled, the cache memory is served as 8KB On-chip RAM.

The I-Cache is always disabled on reset.

The Features of the Instruction Cache：

- 8K bytes instruction cache
- Two-way set associative
- Four words in a cache line
- LRU replacement policy
- Lockable on a per-line basis
- Critical word first, burst access

Instruction Cache Operation

On an instruction fetch, bits 11～4 of the instruction's address point into the cache to retrieve the tags and data of one set. The tags from both ways are then compared against bits 30～12 of the instruction's address. If a match is found and the matched entry is valid, then it is a cache hit. If neither tags match or the matched tag is not valid, it is a cache miss.

6.4.3.1. Instruction Cache Hit

In case of a cache hit, bits 3～2 of the instruction address is used to select one word from the cache line whose tag matches. The instruction is immediately transferred to the instruction unit of the core.

6.4.3.2. Instruction Cache Miss

On an instruction cache miss, the address of the missed instruction is driven on the internal bus with a 4-word burst transfer read request. A cache line is then selected to receive the data that will be coming from the bus. The selection algorithm gives first priority to invalid lines. If neither of the two lines in the selected set is invalid, then the least recently used line is selected for replacement. Locked lines are never replaced. The transfer begins with the word requested by the instruction unit (critical word first), followed by the remaining words of the line, then by the word at the beginning of the lines (wraparound).

6.4.3.3. Instruction Cache Flushing

The W90N740 does not support external memory snooping. Therefore, if self-modifying code is written, the instructions in the I-Cache may become invalid. The entire I-Cache can be flushed by software in one operation, or can be flushed one line at a time by setting the **CAHCON** register bit **FLHS** or **FLHA** with the **ICAH** bit is set. As flushing the cache line, the "**V**" bit of the line is cleared to "0". The I-Cache is automatically flushed during reset.

6.4.3.4. Instruction Cache Load and Lock

The W90N740 supports a cache-locking feature that can be used to lock critical sections of code into I-Cache to guarantee quick access. Lockdown can be performed with a granularity of one cache line. The smallest space, which can be locked down, is 4 words. After a line is locked, it operates as a regular instruction SRAM. Lines locked are not replaced during misses and not affected by flush per line command.

To load and lock instruction, the following sequence should be followed:

1. Write the start address of the instructions to be locked into **CAHADR** register.
2. Set **LDLK** and **ICAH** bits in the **CAHCON** register.
3. Increased the address by 16 and written into **CAHADR** register.
4. Set **LDLK** and **ICAH** bits in the **CAHCON** register.
5. Repeat the steps 3 and 4, until the desired instructions are all locked.

When using I-Cache load and lock command, there are some notes should be cared.

- The programs executing load and lock operation should be held in a non-cacheable area of memory.
- The cache should be enabled and interrupts should be disabled.
- Software must flush the cache before execute load and lock to ensure that the code to be locked down is not already in the cache.

Instruction Cache Unlock

The unlock operation is used to unlock previously locked cache lines. After unlock, the "**L**" bit of the line is cleared to "0". W90N740 has two unlock command, unlock line and unlock all.

The unlock line operation is performed on a cache line granularity. In case the line is found in the cache, it is unlocked and starts to operate as a regular valid cache line. In case the line is not found in the cache, no operation is done and the command terminates with no exception. To unlock one line the following unlock line sequence should be followed:

1. Write the address of the line to be unlocked into the **CAHADR** Register.
2. Set the **ULKS** and **ICAH** bits in the **CAHCON** register.

The unlock all operation is used to unlock the whole I-Cache. This operation is performed on all cache lines. In case a line is locked, it is unlocked and starts to operate as regular valid cache line. In case a line is not locked or if it is invalid, no operation is performed. To unlock the whole cache, set the **ULKA** and **ICAH** bits.

6.4.4 Data Cache

The W90N740 data cache (D-Cache) is a 2KB two-way set associative cache. The cache organization is 64 sets, two lines per set, and four words per line. Cache lines are aligned on 4-word boundaries in memory. The cache is designed for **buffer write-through** mode of operation and a least recently used (LRU) replacement algorithm is used to select a line when no empty lines are available.

When D-Cache is disabled, the cache memory is served as 2KB On-chip RAM.

The D-Cache is always disabled on reset.

The Features of the Data Cache：

- 2K bytes data cache
- Two-way set associative
- Four words in a cache line
- LRU replacement policy
- Lockable on a per-line basis
- Critical word first, burst access
- Buffer Write-through mode
- words write buffer
- Drain write buffer

DATA CACHE OPERATION

On a data fetch, bits 9～4 of the data's address point into the cache to retrieve the tags and data of one set. The tags from both ways are then compared against bits 30～10 of the data's address. If a match is found and the matched entry is valid, then it is a cache hit. If neither tags match or the matched tag is not valid, it is a cache miss.

6.4.4.1. Data Cache Read

Read Hit：On a cache hit, the requested word is immediately transferred to the core.

Read Miss：A line in the cache is selected to hold the data, which will be fetched from memory. The selection algorithm gives first priority to invalid lines and if both lines are invalid the line in way zero is selected first. If neither of the two candidate lines in the selected set is invalid, then one of the lines is selected by the LRU algorithm to replace. The transfer begins with the aligned word containing the missed data (critical word first), followed by the remaining word in the line, then by the word at the beginning of the line (wraparound). As the missed word is received from the bus, it is delivered directly to the core.

6.4.4.2. Data Cache Write

As buffer write-through mode, store operations always update memory. The buffer write-through mode is used when external memory and internal cache images must always agree.

Write Hit：Data is written into both the cache and write buffer. The processor then continues to access the cache, while the cache controller simultaneously downloads the contents of the write buffer to main memory. This reduces the effective write memory cycle time from the time required for a main memory cycle to the cycle time of the high-speed cache.

Write Miss：Data is only written into write buffer, not to the cache (write no allocate).

6.4.4.3. Data Cache Flushing

The W90N740 allows flushing of the data cache under software control. The data cache may be invalidated through writing flush line (**FLHS**) or flush all (**FLHA**) commands to the **CAHCON** register. Flushing the entire D-Cache also flushed any locked down code. As flushing the data cache, the "**V**" bit of the line is cleared to "0". The D-cache is automatically flushed during reset.

6.4.4.4. Data Cache Load and Lock

The W90N740 supports a cache-locking feature that can be used to lock critical sections of data into D-Cache to guarantee quick access. Lockdown can be performed with a granularity of one cache line. The smallest space, which can be locked down, is 4 words. After a line is locked, it operates as a regular instruction SRAM. The locked lines are not replaced during misses and it is not affected by flush per line command.

To load and lock data, the following sequence should be followed:

1. Write the start address of the data to be locked into **CAHADR** register.
2. Set **LDLK** and **DCAH** bits in the **CAHCON** register.
3. Increased the address by 16 and written into **CAHADR** register.
4. Set **LDLK** and **DCAH** bits in the **CAHCON** register.
5. Repeat the steps 3 and 4, until the desired data are all locked.

When using D-Cache load and lock command, there are some notes should be cared.

- The programs executing load and lock operation should be held in a non-cacheable area of memory.
- The cache should be enabled and interrupts should be disabled.
- Software must flush the cache before execute load and lock to ensure that the data to be locked down is not already in the cache.

6.4.4.5. Data Cache Unlock

The unlock operation is used to unlock previously locked cache lines. After unlock, the "**L**" bit of the line is cleared to "0". W90N740 has two unlock command, unlock line and unlock all.

The unlock line operation is performed on a cache line granularity. In case the line is found in the cache, it is unlocked and starts to operate as a regular valid cache line. In case the line is not found in the cache, no operation is done and the command terminates with no exception. To unlock one line the following unlock line sequence should be followed:

1. Write the address of the line to be unlocked into the **CAHADR** Register.
2. Set the **ULKS** and **DCAH** bits in the **CAHCON** register.

The unlock all operation is used to unlock the whole D-Cache. This operation is performed on all cache lines. In case a line is locked, it is unlocked and starts to operate as regular valid cache line. In case a line is not locked or if it is invalid, no operation is performed. To unlock the whole cache, set the **ULKA** and **DCAH** bits.

6.4.5 Write Buffer

The W90N740 provides a write buffer to improve system performance. The write buffer can buffer up to eight words of data. The write buffer may be enabled or be disabled via the **WRBEN** bit in the **CAHCNF** register, and the buffer is disabled and flushed on reset.

Drain write buffer

To force data, which is in write buffer, to be written to external main memory. This operation is useful in real time applications where the processor needs to be sure that a write to a peripheral has completed before program execution continues.

To perform this command, you can set the **DRWB** and **DCAH** bits in **CAHCON** register.

Cache Control Registers Map

Register	Address	R/W	Description	Reset Value
CAHCNF	0xFFF0.2000	R/W	Cache configuration register	0x0000.0000
CAHCON	0xFFF0.2004	R/W	Cache control register	0x0000.0000
CAHADR	0xFFF0.2008	R/W	Cache address register	0x0000.0000
CTEST0	0xFFF6.0000	R/W	Cache test register 0	0x0000.0000
CTEST1	0xFFF6.0004	R	Cache test register 1	0x0000.0000

Cache Configuration Register (CAHCNF)

Cache controller has a configuration register to enable or disable the I-Cache, D-Cache, and Write buffer.

Register	Address	R/W	Description	Reset Value
CAHCNF	0xFFF0.2000	R/W	Cache configuration register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					WRBEN	DCAEN	ICAEN

WRBEN [2] ：Write buffer enable

When set to “1”, write buffer operation is enabled.

Write buffer is disabled after reset.

DCAEN [1] ： D-Cache enable

When set to “1”, Data cache operation is enabled.

D-Cache is disabled after reset.

ICAEN [0] ： I-Cache enable

When set to “1”, Instruction cache operation is enabled.

I-Cache is disabled after reset.

Cache Control Register (CAHCON)

Cache controller supports one Control register used to control the following operations.

- Flush I-Cache and D-Cache
- Load and lock I-Cache and D-Cache
- Unlock I-Cache and D-Cache
- Drain write buffer

These command set bits in **CAHCON** register are auto-clear bits. As the end of execution, that command set bit will be cleared to “0” automatically.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAHCON	0xFFF0.2004	R/W	Cache control register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
DRWB	ULKS	ULKA	LDLK	FLHS	FLHA	DCAH	ICAH

DRWB [7] ：Drain write buffer

Forces write buffer data to be written to main memory.

ULKS [6] ：Unlock I-Cache/D-Cache single line

Unlocks the I-Cache/D-Cache per line. Both **WAY** and **ADDR** bits in **CAHADR** register must be specified.

ULKA [5] ：Unlock I-Cache/D-Cache entirely

Unlocks the entire I-Cache/D-Cache, the lock bit “**L**” will be cleared to 0.

LDLK [4] ：Load and Lock I-Cache/D-Cache

Loads the instruction or data from external memory and locks into cache. Both **WAY** and **ADDR** bits in **CAHADR** register must be specified.

FLHS [3] ：Flush I-Cache/D-Cache single line

Flushes the entire I-Cache/D-Cache per line. Both **WAY** and **ADDR** bits in **CAHADR** register must be specified.

FLHA [2] ：Flush I-Cache/D-Cache entirely

To flush the entire I-Cache/D-Cache, also flushes any locked-down code. If the I-Cache/D-Cache contains locked down code, the programmer must flush lines individually.

DCAH [1] ：D-Cache selected

When set to “1”, the command set is executed with D-Cache.

ICAH [0] ：I-Cache selected

When set to “1”, the command set is executed with I-Cache.

Notes：When using the **FLHA** or **ULKA** command, you can set **both ICAH** and **DCAH** bits to execute entire I-Cache **and** D-Cache flushing or unlocking. But, **FLHS** and **ULKS** commands can only be executed with a cache line specified by **CAHADR** register in I-Cache **or** D-Cache at a time. If you set **both ICAH** and **DCAH** bits, and set **FLHS** or **ULKS** command bit, it will be treated as an invalid command and no operation is done and the command terminates with no exception.

The **Drain Write Buffer** operation is only for D-Cache. To perform this operation, you must set **DRWB** and **DCAH** bits. If the **ICAH** bit is set when using **DRWB** command, it will be an invalid command and no operation is done and the command terminates with no exception.

Cache Address Register (CAHADR)

W90N740 Cache Controller supports one address register. This address register is used with the command set in the control register (**CAHCON**) by specifying instruction/data address.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAHADR	0xFFF0.2008	R/W	Cache address register	0x0000.0000

31	30	29	28	27	26	25	24
WAY	ADDR						
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

WAY [31] ：Way selection

0 = Way0 is selected

1 = Way1 is selected

ADDR [30:0] ：The absolute address of instruction or data

6.5 Ethernet MAC Controller (EMC)

The W90N740 has two Ethernet MAC Controllers (EMC) for WAN/LAN application. Each EMC has its DMA controller, transmit FIFO, and receive FIFO. The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM address register for entry address comparison, Transmit-FIFO, Receive-FIFO, TX/RX state machine controller and status controller. The EMC supplies selectable MII (Media Independent Interface) or RMII (Reduced MII), for 10/100Mbits/s PHY operated with 25M/2.5M Hz TXCLK/RXCLK.

The Features of each EMC:

- IEEE 802.3 protocol engine with programmable MII or RMII interface for 10/100 Mbits/s
- DMA engine with burst mode
- 256 bytes transmit & 256 bytes receive FIFO for MAC protocol engine and DMA access
- Built-in 16 entry CAM Address Register
- Support long frame (more than 1518 bytes) and short frame (less than 64 bytes)
- Re-transmit (during collision) the frame without DMA access
- Half or full duplex function option
- Support Station Management for external PHY
- On-Chip Pad generation

6.5.1 EMC Descriptors

Buffer descriptors are used to handle the control, status and data information of each received/transmitted frame. There is much information contained in the descriptors. The W90N740 totally implements four registers for receiving and four registers for transmitting, respectively. All the registers are described below.

6.5.1.1. Rx Buffer Descriptor (RXBD)

31	30	29 ... 16	15 ... 0
O		Rx Status	Frame Length
Data Buffer Starting Address			
NAT Information (Reserved)			
Next Descriptor Starting Address			

O: Ownership bits

BIT [31: 30]

00 = CPU

= DMA

11 = NATA

01 = Undefined

W90N740 EMC receive DMA is allowed to access current descriptor if bit 31 is set to 1 by the user driver program. If the entire frame is received successfully, then the ownership bit 31 is cleared and the ownership is granted to CPU.

If NATA is enabled, NATA is also allowed to access current descriptor and bit 30 is set to 1 by NATA when NATA is processing.

6.5.1.2. Rx Status: Receive Status

This field is updated by EMC after reception completed. The detail description is on next page.

Frame Length: Received Frame Length

This field is the size of the received frame.

Data Buffer Starting Address

This field is the starting address of the frame data to be received.

Next Descriptor Start Address

This field is the start address of the next frame descriptor.

6.5.1.3. NAT Information

This field is reserved for MAC Rx to send information for NAT processing. For user driver program, it is forbidden to modify these bits.

Rx Status (RXSTA): Receive Status

		29	28	27	26	25	24
		Hit	IPHit	PortHit	Inverse	NATFSH	Nop
23	22	21	20	19	18	17	16
Reserved	RP	ALIE	RXGD	PTLE	Reserved	CRCE	RXINTR

Bits 29-24 are NAT information for the NAT accelerator, and reserved if the NATA is disabled.

Hit: current packet is hit with NAT entry table

The value is 1 if current packet IP/port is in the entry list. If NATA is disabled, the bit is reserved.

6.5.1.4. IPHit: current packet is hit on IP address

The value is 1 if current packet IP/port is hit in the IP address location.

PortHit: current packet is hit on Port Number

The value is 1 if current packet IP/port is hit in the port number location.

Inverse: current hit entry is setting on inverse mode

The value is 1 if current hit entry is on inverse mode.

6.5.1.5. NATFSH: NAT Processing Finish

The value is 1 if current packet NAT processing is finished and successful. This bit will be written while NATA finish the NAT processing.

NOP: No Operation

This bit indicates the packet is hit in NAT table but no need to be replaced by NATA. This bit will be set to 1 if the packet hit the NAT table and the corresponding NOP and Discard bit of hit entry is 2'b10.

RP: Runt Packet

Set if the received packet length is less than 64 bytes.

ALIE: Alignment Error

Set if the Frame length bits are not a multiple of eight.

RXGD: Receiving Good packet received

Set if the MAC successfully receives a packet with no errors. If **EnRXGD** = 1, an interrupt is generated on each time this bit is being set.

PTLE: Packet Too Long Error

Set if a received frame longer than 1518 bytes. Not set if the **ALP** (Accept Long Packet) bit is set.

CRCE: CRC Error

Set if the CRC at end of packet does not match the computed value, or else the PHY asserts Rx_er during packet reception.

RXINTR: Interrupt on receive

Set if reception of packet caused an interrupt condition. This includes Good received, if the **EnRXGD** is set.

NAT INFORMATION (Reserved if disabled)

31	30	29	28	27	26	25	24
Reserved		TCP information					
23	22	21	20	19	18	17	16
Reserved	UCK_Err	TU_Err	NH_Err	IP Header Length			
15	14	13	12	11	10	9	8
Reserved		Hit Entry Number					
7	6	5	4	3	2	1	0
Reserved	PPPCaps	PPPoE	UCKS	UDP	TCP	L/W	Hit

TCP information: URG (bit 29), ACK, PSH, RST, SYN, FIN (bit 24)

The six bit values show current TCP status, and are transparent to the six bits in TCP header. The values are valid if current packet is TCP type and **Hit** is set.

UCK_Err: TCP/UCKS Error

TU_Err: TCP/UDP Error

NH_Err: No Hit Error

These bits records error status if NAT processing error is occurred and are wrote by NATA.

(1) UCK_Err: TCP = 1 and UCKS = 1

(2) TU_Err: TCP = 1 and UDP = 1

(3) NH_Err: No hit error

IP Header Length: TCP/UDP header location offset

The offset value lets the NAT accelerator to identify the starting address of TCP or UDP header, which is used for NAT to parsing port data. The value is valid if **Hit** is set.

Hit Entry Number: the entry number hit with the input address

The value indicates which entry is hit to let NAT accelerator to take corresponding data. The value is valid if Hit is set.

PPPCaps: PPPoE datagram encapsulated

The value is 1 if PPP encapsulation is used (8 bits protocol field), and 0 if encapsulation is not used (16 bits protocol field).

PPPoE: PPPoE protocol

The value is 1 if the packet takes PPPoE protocol instead of IP protocol. The value is 0 if the packet takes IP protocol.

UCKS: UDP protocol with skip checksum replacement

The value is 1 if the packet takes UDP protocol, and its checksum is zero. The NAT accelerator will skip the checksum replacement procedure.

UDP: apply UDP protocol

It tell NAT engine to apply UDP protocol. The value is 1 if the packet takes UDP protocol, and 0 if the packet takes non-UDP protocol. The value is valid if **Hit** is set.

TCP: apply TCP protocol

It tell NAT engine to apply TCP protocol. The value is 1 if the packet takes TCP protocol, and 0 if the packet takes non-TCP protocol. The value is valid if **Hit** is set.

L/W: hit port; the value is 1 if internal (LAN) port gets hit, and 0 if external (WAN) port is hit

The S/W program must specify LAN port and WAN port with the two EMCs. For example, EMC 0 is connected to WAN port, and EMC 1 is connected to LAN port. If NAT is enabled, EMC 0 is connected to external port for {MA, MP} comparison, and EMC 1 is connected to internal port for {LA, LP} comparison. The L/W value is 1 if the hit port is internal port, and 0 if the hit port is external port. The value is valid if Hit is set.

Hit: current packet is hit with NAT entry table

The value is 1 if current packet IP/port is in the entry list. If NAT is disabled, the bit is reserved.

Tx Buffer Descriptor (TXBD)

31	30	16	15	4	3	2	1	0
O					I	C	P	
Data Buffer Starting Address								
Tx Status					Frame Length			
Next Descriptor Starting Address								

O: Ownership bit

0 = CPU 1 = DMA

W90N740 transmit DMA is allowed to access current descriptor if this bit is set to '1' by the user driver program. If the entire frame is transmitted successfully, then the ownership bit is cleared and the ownership is granted to CPU.

I: MAC transmit interrupt enable after transmission complete of the frame

0 = Disable

1 = Enable

6.5.1.6. C: CRC mode bit

0 = Disable CRC mode

1 = Enable CRC mode

6.5.1.7. P: Padding mode bit

0 = Disable padding mode

1 = Enable padding mode

Data Buffer Starting Address

This field is the starting address of the frame data to be transmitted.

6.5.1.8. Tx Status: Transmit Status

This field is updated by the EMC after transmission.

6.5.1.9. Frame Length

This field is the size of the transmit frame.

Next Descriptor Starting Address

This field is the starting address of the next frame descriptor.

Tx Status (TXSTA)

31	30	29	28	27	26	25	24
CCNT					SEQ	PAU	TXHA
23	22	21	20	19	18	17	16
LC	TXABT	NCS	EXDEF	TXCP	Reserved	DEF	TXINTR

TXINTR: Interrupt on Transmit

Set if transmission of packet causes an interrupt condition. It includes **TXCP**.

DEF: Transmit deferred

Set when MAC has to defer, if MAC is ready to transmit a frame, because the carrier sense input is asserted before the MAC gets granted to acquire the network media.

TXCP: Transmission Completion

Set when MAC completes a transmission or discard one packet.

EXDEF: Exceed Deferral

Set if MAC deferring time to transmit exceeds 0.32768ms for 100Mbit/s or 3.2768ms for 10Mbit/s.

NCS: No Carrier Sense Error

Set if carrier sense is not detected during the entire transmission of a packet..

TXABT: Transmission Abort

Set if transmitting aborted because 16 collisions occurred in the same packet.

LC: Late Collision

Set if there is collision occurs after 64 bytes collision window.

TXHA: Transmission halted

Transmission halted by clearing **TXON** bit in the **MCMDR**.

PAU: Paused

Transmit is paused by a remote flow control command.

SQE: SQE error

After transmitting a frame, set if the fake collision signal did not come from the PHY for 1.6 µs.

CCNT: Transmit Collision Count

Count of collisions during transmission of a single packet. After 16 collisions, **CCNT** is 1111, and **TXABT** is set.

7.5.2 EMC Register Mapping

This set of registers is used to convey status/control information to/from the Ethernet MAC controller. These registers are used for loading commands generated by user, indicating transmit and receive status, buffering data to/from memory, and providing interrupt control. The registers used by W90N740 EMC (Ethernet MAC controller) are divided into three groups:

- **CAM REGISTERS**
- **MAC REGISTERS**
- **DMA REGISTERS**

Note: registers are named as xxxx_0 or xxxx_1, where xxxx_0 is the register in EMC 0, and xxxx_1 is the register in EMC 1.

EMC 0 Control registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAMCMR_0	0xFFF0.3000	R/W	CAM Command Register	0x0000.0000
CAMEN_0	0xFFF0.3004	R/W	CAM enable register	0x0000.0000
CAM0M_0	0xFFF0.3008	R/W	CAM0 Most Significant Word Register	0x0000.0000
CAM0L_0	0xFFF0.300C	R/W	CAM0 Least Significant Word Register	0x0000.0000
CAM1M_0	0xFFF0.3010	R/W	CAM1 Most Significant Word Register	0x0000.0000
CAM1L_0	0xFFF0.3014	R/W	CAM1 Least Significant Word Register	0x0000.0000
CAM2M_0	0xFFF0.3018	R/W	CAM2 Most Significant Word Register	0x0000.0000
CAM2L_0	0xFFF0.301C	R/W	CAM2 Least Significant Word Register	0x0000.0000
CAM3M_0	0xFFF0.3020	R/W	CAM3 Most Significant Word Register	0x0000.0000
CAM3L_0	0xFFF0.3024	R/W	CAM3 Least Significant Word Register	0x0000.0000
CAM4M_0	0xFFF0.3028	R/W	CAM4 Most Significant Word Register	0x0000.0000
CAM4L_0	0xFFF0.302C	R/W	CAM4 Least Significant Word Register	0x0000.0000
CAM5M_0	0xFFF0.3030	R/W	CAM5 Most Significant Word Register	0x0000.0000
CAM5L_0	0xFFF0.3034	R/W	CAM5 Least Significant Word Register	0x0000.0000
CAM6M_0	0xFFF0.3038	R/W	CAM6 Most Significant Word Register	0x0000.0000
CAM6L_0	0xFFF0.303C	R/W	CAM6 Least Significant Word Register	0x0000.0000
CAM7M_0	0xFFF0.3040	R/W	CAM7 Most Significant Word Register	0x0000.0000
CAM7L_0	0xFFF0.3044	R/W	CAM7 Least Significant Word Register	0x0000.0000
CAM8M_0	0xFFF0.3048	R/W	CAM8 Most Significant Word Register	0x0000.0000
CAM8L_0	0xFFF0.304C	R/W	CAM8 Least Significant Word Register	0x0000.0000
CAM9M_0	0xFFF0.3050	R/W	CAM9 Most Significant Word Register	0x0000.0000

EMC 0 Control registers, continued

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAM9L_0	0xFFF0.3054	R/W	CAM9 Least Significant Word Register	0x0000.0000
CAM10M_0	0xFFF0.3058	R/W	CAM10 Most Significant Word Register	0x0000.0000
CAM10L_0	0xFFF0.305C	R/W	CAM10 Least Significant Word Register	0x0000.0000
CAM11M_0	0xFFF0.3060	R/W	CAM11 Most Significant Word Register	0x0000.0000
CAM11L_0	0xFFF0.3064	R/W	CAM11 Least Significant Word Register	0x0000.0000
CAM12M_0	0xFFF0.3068	R/W	CAM12 Most Significant Word Register	0x0000.0000
CAM12L_0	0xFFF0.306C	R/W	CAM12 Least Significant Word Register	0x0000.0000
CAM13M_0	0xFFF0.3070	R/W	CAM13 Most Significant Word Register	0x0000.0000
CAM13L_0	0xFFF0.3074	R/W	CAM13 Least Significant Word Register	0x0000.0000
CAM14M_0	0xFFF0.3078	R/W	CAM14 Most Significant Word Register	0x0000.0000
CAM14L_0	0xFFF0.307C	R/W	CAM14 Least Significant Word Register	0x0000.0000
CAM15M_0	0xFFF0.3080	R/W	CAM15 Most Significant Word Register	0x0000.0000
CAM15L_0	0xFFF0.3084	R/W	CAM15 Least Significant Word Register	0x0000.0000
MAC REGISTERS				
MIEN_0	0xFFF0.3088	R/W	MAC Interrupt Enable Register	0x0000.0000
MCMDR_0	0xFFF0.308C	R/W	MAC Command Register	0x0000.0000
MIID_0	0xFFF0.3090	R/W	MII Management Data Register	0x0000.0000
MIIDA_0	0xFFF0.3094	R/W	MII Management Data Control and Address Register	0x0090.0000
MPCNT_0	0xFFF0.3098	R/W	Missed Packet counter register	0x0000.7FFF
DMA REGISTERS				
TXDLSA_0	0xFFF0.309C	R/W	Transmit Descriptor Link List Start Address register	0xFFFF.FFFC
RXDLSA_0	0xFFF0.30A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC
DMARFC_0	0xFFF0.30A4	R/W	DMA Receive Frame Control Register	0x0000.0800
TSDR_0	0xFFF0.30A8	W	Transmit Start Demand Register	Undefined
RSDR_0	0xFFF0.30AC	W	Receive Start Demand Register	Undefined
FIFOTHD_0	0xFFF0.30B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101

EMC 0 Status Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MAC REGISTERS				
MISTA_0	0xFFF0.30B4	R/W	MAC Interrupt Status Register	0x0000.0000
MGSTA_0	0xFFF0.30B8	R/W	MAC General Status Register	0x0000.0000
MRPC_0	0xFFF0.30BC	R	MAC Receive Pause count register	0x0000.0000
MRPCC_0	0xFFF0.30C0	R	MAC Receive Pause Current Count Register	0x0000.0000
MREPC_0	0xFFF0.30C4	R	MAC Remote pause count register	0x0000.0000
DMA REGISTERS				
DMARFS_0	0xFFF0.30C8	R/W	DMA Receive Frame Status Register	0x0000.0000
CTXDSA_0	0xFFF0.30CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000
CTXBSA_0	0xFFF0.30D0	R	Current Transmit Buffer Start Address Register	0x0000.0000
CRXDSA_0	0xFFF0.30D4	R	Current Receive Descriptor Start Address Register	0x0000.0000
CRXBSA_0	0xFFF0.30D8	R	Current Receive Buffer Start Address Register	0x0000.0000

EMC 1 Control Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAMCMR_1	0xFFF0.3800	R/W	CAM Command Register	0x0000.0000
CAMEN_1	0xFFF0.3804	R/W	CAM enable register	0x0000.0000
CAM0M_1	0xFFF0.3808	R/W	CAM0 Most Significant Word Register	0x0000.0000
CAM0L_1	0xFFF0.380C	R/W	CAM0 Least Significant Word Register	0x0000.0000
CAM1M_1	0xFFF0.3810	R/W	CAM1 Most Significant Word Register	0x0000.0000
CAM1L_1	0xFFF0.3814	R/W	CAM1 Least Significant Word Register	0x0000.0000
CAM2M_1	0xFFF0.3818	R/W	CAM2 Most Significant Word Register	0x0000.0000
CAM2L_1	0xFFF0.381C	R/W	CAM2 Least Significant Word Register	0x0000.0000
CAM3M_1	0xFFF0.3820	R/W	CAM3 Most Significant Word Register	0x0000.0000
CAM3L_1	0xFFF0.3824	R/W	CAM3 Least Significant Word Register	0x0000.0000
CAM4M_1	0xFFF0.3828	R/W	CAM4 Most Significant Word Register	0x0000.0000
CAM4L_1	0xFFF0.382C	R/W	CAM4 Least Significant Word Register	0x0000.0000

EMC 1 Control Registers, continued

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAM5M_1	0xFFF0.3830	R/W	CAM5 Most Significant Word Register	0x0000.0000
CAM5L_1	0xFFF0.3834	R/W	CAM5 Least Significant Word Register	0x0000.0000
CAM6M_1	0xFFF0.3838	R/W	CAM6 Most Significant Word Register	0x0000.0000
CAM6L_1	0xFFF0.383C	R/W	CAM6 Least Significant Word Register	0x0000.0000
CAM7M_1	0xFFF0.3840	R/W	CAM7 Most Significant Word Register	0x0000.0000
CAM7L_1	0xFFF0.3844	R/W	CAM7 Least Significant Word Register	0x0000.0000
CAM8M_1	0xFFF0.3848	R/W	CAM8 Most Significant Word Register	0x0000.0000
CAM8L_1	0xFFF0.384C	R/W	CAM8 Least Significant Word Register	0x0000.0000
CAM9M_1	0xFFF0.3850	R/W	CAM9 Most Significant Word Register	0x0000.0000
CAM9L_1	0xFFF0.3854	R/W	CAM9 Least Significant Word Register	0x0000.0000
CAM10M_1	0xFFF0.3858	R/W	CAM10 Most Significant Word Register	0x0000.0000
CAM10L_1	0xFFF0.385C	R/W	CAM10 Least Significant Word Register	0x0000.0000
CAM11M_1	0xFFF0.3860	R/W	CAM11 Most Significant Word Register	0x0000.0000
CAM11L_1	0xFFF0.3864	R/W	CAM11 Least Significant Word Register	0x0000.0000
CAM12M_1	0xFFF0.3868	R/W	CAM12 Most Significant Word Register	0x0000.0000
CAM12L_1	0xFFF0.386C	R/W	CAM12 Least Significant Word Register	0x0000.0000
CAM13M_1	0xFFF0.3870	R/W	CAM13 Most Significant Word Register	0x0000.0000
CAM13L_1	0xFFF0.3874	R/W	CAM13 Least Significant Word Register	0x0000.0000
CAM14M_1	0xFFF0.3878	R/W	CAM14 Most Significant Word Register	0x0000.0000
CAM14L_1	0xFFF0.387C	R/W	CAM14 Least Significant Word Register	0x0000.0000
CAM15M_1	0xFFF0.3880	R/W	CAM15 Most Significant Word Register	0x0000.0000
CAM15L_1	0xFFF0.3884	R/W	CAM15 Least Significant Word Register	0x0000.0000
MAC REGISTERS				
MIEN_1	0xFFF0.3888	R/W	MAC Interrupt Enable Register	0x0000.0000
MCMDR_1	0xFFF0.388C	R/W	MAC Command Register	0x0000.0000
MIID_1	0xFFF0.3890	R/W	MII Management Data Register	0x0000.0000
MIIDA_1	0xFFF0.3894	R/W	MII Management Data Control and Address Register	0x0090.0000
MPCNT_1	0xFFF0.3898	R/W	Missed Packet counter register	0x0000.7FFF

EMC 1 Control Registers, continued

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DMA REGISTERS				
TXDLSA_1	0xFFF0.389C	R/W	Transmit Descriptor Link List Start Address register	0xFFFF.FFFC
RXDLSA_1	0xFFF0.38A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC
DMARFC_1	0xFFF0.38A4	R/W	DMA Receive Frame Control Register	0x0000.0800
TSDR_1	0xFFF0.38A8	W	Transmit Start Demand Register	Undefined
RSDR_1	0xFFF0.38AC	W	Receive Start Demand Register	Undefined
FIFOTHD_1	0xFFF0.38B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101

EMC 1 Status Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MAC REGISTERS				
MISTA_1	0xFFF0.38B4	R/W	MAC Interrupt Status Register	0x0000.0000
MGSTA_1	0xFFF0.38B8	R/W	MAC General Status Register	0x0000.0000
MRPC_1	0xFFF0.38BC	R	MAC Receive Pause count register	0x0000.0000
MRPCC_1	0xFFF0.38C0	R	MAC Receive Pause Current Count Register	0x0000.0000
MREPC_1	0xFFF0.38C4	R	MAC Remote pause count register	0x0000.0000
DMA REGISTERS				
DMARFS_1	0xFFF0.38C8	R/W	DMA Receive Frame Status Register	0x0000.0000
CTXDSA_1	0xFFF0.38CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000
CTXBSA_1	0xFFF0.38D0	R	Current Transmit Buffer Start Address Register	0x0000.0000
CRXDSA_1	0xFFF0.38D4	R	Current Receive Descriptor Start Address Register	0x0000.0000
CRXBSA_1	0xFFF0.38D8	R	Current Receive Buffer Start Address Register	0x0000.0000

CAM Command Register (CAMCMR_0, CAMCMR_1)

The three accept bits in the CAMCMR_x are used to override CAM rejections or accept ion. To place the MAC in promiscuous mode, use CAMCMR_x settings to accept packets with all three types of destination address. The three types of destination address packets are as follows:

1. Station packets, xxxxxxx0-xxxxxxxx-xxxxxxxx-xxxxxxxx-xxxxxxxx-xxxxxxxx
2. Multicast packet, xxxxxxx1-xxxxxxxx-xxxxxxxx-xxxxxxxx-xxxxxxxx-xxxxxxxx. (but x not all 1)
3. Broadcast packet, 11111111-11111111-11111111-11111111-11111111-11111111

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAMCMR_0	0xFFF0.3000	R/W	CAM Command Register	0x0000.0000
CAMCMR_1	0xFFF0.3800	R/W	CAM Command Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			ECMP	CCAM	ABP	AMP	AUP

ECMP [4]: Enable CAM Compare

Default value: 0

Set this bit to enable compare mode.

CCAM [3]: Complement CAM

Default value: 0

Set this bit to do complement CAM compare logic, and data packets rejected by CAM which can recognize the destination address.

ABP [2]: Accept Broadcast Packet

Default value: 0

Set this bit to accept any packet with a broadcast address.

AMP [1]: Accept Multicast Packet

Default value: 0

Set this bit to accept any packet with a multicast address.

AUP [0]: Accept Unicast Packet

Default value: 0

Set this bit to accept any packet with a unicast address.

CAM Enable Register (CAMEN_0, CAMEN_1)

The CAM enable register, CAMEN_x, indicates which CAM entries are valid, using a direct comparison mode. Up to 16 entries, numbered 0 through 15, may be active, depending on the CAM size. If the CAM is smaller than 16 entries, the higher bits are ignored.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAMEN_0	0xFFF0.3004	R/W	CAM enable register	0x0000.0000
CAMEN_1	0xFFF0.3804	R/W	CAM enable register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CAM15EN	CAM14EN	CAM13EN	CAM12EN	CAM11EN	CAM10EN	CAM9EN	CAM8EN
7	6	5	4	3	2	1	0
CAM7EN	CAM6EN	CAM5EN	CAM4EN	CAM3EN	CAM2EN	CAM1EN	CAM0EN

CAMxEN (x: 15 ~ 0) [15:0] : CAM Enable bits

Default value: 0

Set the bits in this 16-bit value to selectively enable entry locations from 0 through 15. For example, bit 0 is associated with Entry CAM0, and bit 1 is associated with Entry CAM1, …etc. To disable an entry location, clear the appropriate bit.

Note: The CAM13EN, CAM14EN, and CAM15EN has to be set for sending pause control packet**.**

CAM Address Registers (CAMxx_0, CAMxx_1)

There are 16 entries for the Destination Address (entries 0~12) and the Pause Control Packet (entries 13~15). For the destination address values, one destination address consists of 6 bytes with 2-word access port.

To send a Pause Control Packet, write in the register set **{CAM13M, CAM13L}** with the destination address, the **{CAM14M, CAM14L}** entry with the source address, and the **{CAM15M, CAM15L}** entry with length/type, op-code, and operand, then set the **SDPZ** bit in the **MCMDR** (MAC Command Register).

The CPU uses the CAM address register as a database for destination address. To activate the CAM function, the appropriate enable bit has to be set in the **CAMEN** register.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM0M_0	0xFFF0.3008		CAM0 Most Significant Word Register	0x0000.0000
CAM0L_0	0xFFF0.300C		CAM0 Least Significant Word Register	0x0000.0000
I	I	R/W	I	I
CAM15M_0	0xFFF0.3080		CAM15 Most Significant Word Register	0x0000.0000
CAM15L_0	0xFFF0.3084		CAM15 Least Significant Word Register	0x0000.0000
CAM0M_1	0xFFF0.3808		CAM0 Most Significant Word Register	0x0000.0000
CAM0L_1	0xFFF0.380C		CAM0 Least Significant Word Register	0x0000.0000
I	I	R/W	I	I
CAM15M_1	0xFFF0.3880		CAM15 Most Significant Word Register	0x0000.0000
CAM15L_1	0xFFF0.3884		CAM15 Least Significant Word Register	0x0000.0000

CAMxM (CAM15M excluded)

31	30	29	28	27	26	25	24
Destination Address Byte 6 (Most Significant Byte)							
23	22	21	20	19	18	17	16
Destination Address Byte 5							
15	14	13	12	11	10	9	8
Destination Address Byte 4							
7	6	5	4	3	2	1	0
Destination Address Byte 3							

CAMxL (CAM15L excluded)

31	30	29	28	27	26	25	24
Destination Address Byte 2							
23	22	21	20	19	18	17	16
Destination Address Byte 1							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

{CAMxM, CAMxL} : destination address (6 byte), with 2 bytes in CAMxL and 4 bytes in CAMxM, (CAM15M and CAM15L excluded).

For example, if the address of Entry CAM 1 is desired to store 12-34-56-78-90-13, then the content of CAM1M is 12-34-56-78, and the content of CAM1L is 90-13-00-00.

CAM15M (for Pause Control Packet)

31	30	29	28	27	26	25	24
Length / Type (2 bytes) (Most Significant Byte)							
23	22	21	20	19	18	17	16
Length / Type (2 bytes)							
15	14	13	12	11	10	9	8
Op-code (2 bytes) (Most Significant Byte)							
7	6	5	4	3	2	1	0
Op-code (2 bytes)							

CAM15L (for Pause Control Packet)

31	30	29	28	27	26	25	24
Operand (2 bytes) (Most Significant Byte)							
23	22	21	20	19	18	17	16
Operand (2 bytes)							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

{CAM15M, CAM15L} entry is the Length/Type, Op-code, and operand of the Pause Control Frame. The Length/Type field is 88-08(h), and the Op-code is 00-01(h).

MAC Interrupt Enable Register (MIEN_0, MIEN_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MIEN_1	0xFFF0.3088	R/W	MAC Interrupt Enable Register	0x0000.0000
MIEN_2	0xFFF0.3888	R/W	MAC Interrupt Enable Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							EnTxBErr
23	22	21	20	19	18	17	16
EnTDU	EnLC	EnTXABT	EnNCS	EnEXDEF	EnTXCP	EnTXEMP	EnTXINTR
15	14	13	12	11	10	9	8
Reserved	EnCFR	EnNATErr	EnNATOK	EnRxBErr	EnRDU	EnDEN	EnDFO
7	6	5	4	3	2	1	0
EnMMP	EnRP	EnALIE	EnRXGD	EnPTLE	EnRXOV	EnCRCE	EnRXINTR

EnTxBErr [24]: Enable Transmit Bus ERROR interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if system bus access error from Tx to system memory occurred. If the interrupt is triggered, the Tx state machine will stay at Halt state. The software reset is recommended while this interrupt occurred.

EnTDU [23]: Enable Transmit Descriptor Unavailable interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if transmit descriptors owned to the TxDMA is unavailable. That means, if the TxDMA finds the ownership of descriptors is not belonged to TxDMA, it will generate an interrupt and Tx operation will be ceased till the user issues a write command to Transmit Start Demand register to restart Tx operation.

EnLC [22]: Enable Late Collision interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if a collision occurs after 512 bit times.

EnTXABT [21]: Enable Transmit Abort interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated to indicate 16 collisions occur while transmitting the same packet.

EnNCS [20]: Enable No Carrier Sense interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated to indicate no carrier sense is presented during transmission.

EnEXDEF [19]: Enable Defer interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated to indicate that the defer time exceeding 0.32768ms operated at 100Mbs/s or 3.2768ms operated at 10Mbs/s.

EnTXCP [18]: Enable Transmit Completion interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated when the MAC transmits, or discards one packet.

EnTXEMP [17]: Enable Transmit FIFO Empty interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated when MAC transmit FIFO becomes empty (underflow) during a packet transmission.

EnTXINTR [16]: Enable Interrupt on Transmit interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if a transmission of a packet causes an interrupt condition.

EnCFR [13]: Enable Control Frame Receive Interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the incoming frame is a MAC control frame.

EnNATErr [13]: Enable NAT Processing Error Interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if there is any error during NATA do the NAT processing.

EnNATOK [12]: Enable NAT Processing OK Interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if there is no error during NATA do the NAT processing.

EnRxBErr [11]: Enable Receive Bus ERROR interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if system bus access error from Rx to system memory occurred. If the interrupt is triggered, the Rx state machine will stay at Halt state. The software reset is recommended while this interrupt occurred.

EnRDU [10]: Enable Receive Descriptor Unavailable interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if receive descriptors owned to the RxDMA is unavailable. That means, if the RxDMA finds the ownership of descriptors is not belonged to RxDMA, it will generate an interrupt and Rx operation will be ceased till the user issues a write command to Receive Start Demand register to restart the Rx operation.

EnDEN [9]: Enable DMA early notification interrupts

Default value: 0

Set this bit to enable the interrupt, when the length field of the current frame is received.

EnDFO [8]: Enable DMA receive frame over maximum size interrupt

Default value: 0

Set this bit to enable the interrupt, when the received frame size is larger than the value stored in **RXMS**.

EnMMP [7]: Enable More Missed Packets interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated when the missed error counter rolls over.

EnRP [6]: Enable Runt Packet on Receive interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the MAC receives a frame shorter less than 64 bytes.

EnALIE [5]: Enable Alignment Error interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the frame length in bits was not a multiple of eight.

EnRXGD [4]: Enable Receive Good interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if a packet was successfully received with no errors.

EnPTLE [3]: Enable Packet Too Long interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the MAC received a frame longer than 1518 bytes (unless ALP in MCMDR is set).

EnRXOV [2]: Enable Receive FIFO Overflow interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the MAC receives FIFO was full when receiving a frame.

EnCRCE [1]: Enable CRC Error interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the CRC at the end of a packet is not correct, or else the PHY asserted Rx_er during packet reception.

EnRXINTR [0]: Enable Interrupt on Receive interrupt

Default value: 0

Set this bit to enable the interrupt, which is generated if the reception of a packet caused an interrupt to be generated. This includes a good received interrupt, if the EnRXGD bit is set.

MAC Command Register (MCMDR_0, MCMDR_1)

The MAC command register provides global control information for the MAC. MAC command register settings affect both transmission and reception. The user can also control transmit and receive operation separately. To select customized operating features, users should write this register during system initialization. This way, users will not need to write or read it again during normal operation. However, if users change setting during operation, the updated setting will take effect after the current frame is completed.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MCMDR_0	0xFFF0.308C	R/W	MAC Command Register	0x0000.0000
MCMDR_1	0xFFF0.388C	R/W	MAC Command Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved						Reserved	LAN
23	22	21	20	19	18	17	16
LPCS	EnRMII	LBK	OPMOD	EnMDC	FDUP	Reserved	SDPZ
15	14	13	12	11	10	9	8
Reserved						NDEF	TXON
7	6	5	4	3	2	1	0
Reserved		SPCRC	AEP	ACP	ARP	ALP	RXON

Reserved [25]:
Default value: 0

LAN [24]: LAN Port Setting Mode
Default value: 0
Set this bit to set this EMC port as a LAN port, and clear this bit to set the EMC port as a WAN port. The S/W program must initial an EMC as a LAN port, and another EMC as a WAN port (for example, EMC 0 as a LAN port and EMC 1 as a WAN port) to let the NAT accelerator work properly.

LPCS [23]: Low Pin Count Package Switch
Always set: 0

EnRMII [22]: Enable RMII
Default value: 0
Set this bit to select RMII interface.

MAC 1 BIT [23:22] LPCS: ENRMII	MAC 0 BIT [23:22] LPCS*1: ENRMII	MAC 1 INTERFACE	MAC 0 INTERFACE	NOTE
00	X0	MII	MII	*1: the LPCS of MAC0 bit23 is undefined, which not affect MAC 0 Interface.
00	X1	MII	RMII	
01	X0	RMII	MII	
01	X1	RMII	RMII	

LBK [21]: Loop Back
Default value: 0
Set this bit to enable MAC internal loop back mode.

OPMOD [20]: Operation Mode
Default value: 0
Set this bit to enable MAC to be operated at 100Mb/s. Clear this bit to enable MAC to be operated at 10Mb/s.

EnMDC [19]: Enable MDC signal
Default value: 0
Set this bit to enable MDC clock generation. Clear this bit to disable MDC clock generation.
If users want to access the MII management data, the **EnMDC** bit should be set to enable MDC clock.

FDUP [18]: Full Duplex
Default value: 0
Set this bit to perform the full duplex function.

Reserved [17]:
Default value: 0

SDPZ [16]: Send Pause
Default value: 0
Set this bit to send a pause command or other MAC control packet. The SDPZ bit will be automatically cleared after the MAC control packet has been transmitted. Write zero to this bit has no effect.

NDEF [9]: No defer
Default value: 0
Set this bit to disable defer counter.

TXON [8]: Transmit On
Default value: 0
When this bit is set, the transmission process will be started. If the bit is clear, transmissions will stop after the current packet is transmitted completely. Users should change the bit when the MAC is in idle state.

SPCRC [5]: Accept Strip CRC Value
Default value: 0
Set this bit to enable MAC to check the CRC and then strip it from the message.

AEP [4]: Accept Error Packet
Default value: 0
Set this bit to enable MAC to accept error (CRC error) packet.

ACP [3]: Accept Control Packet
Default value : 0
Set this bit to enable accept control packets.

ARP [2]: Accept Runt Packet
Default value: 0
Set this bit to enable accepting frames with lengths less than 64 bytes.

ALP [1]: Accept Long Packet
Default value: 0
Set this bit to enable accepting frames with lengths greater than 1518 bytes.

RXON [0]: Receive ON

Default value: 0

This bit is set to enable MAC reception operation. If the bit is clear, receptions will stop after the current packet is received completely. Users should change the bit when the MAC is in idle state.

MAC MII Management Data Register (MIID_0, MIID_1)

W90N740 provides MII management function to let user access the registers of the external physical layer device. Setting options in MII management registers does not affect the MAC controller operation.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MIID_0	0xFFF0.3090	R/W	MII Management Data Register	0x0000.0000
MIID_1	0xFFF0.3890	R/W	MII Management Data Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MIIData							
7	6	5	4	3	2	1	0
MIIData							

MIIData [15:0]: MII station management data

This register contains a 16-bit data value for the MII station management function.

MAC MII Management Data Control and Address Register (MIIDA_0, MIIDA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MIIDA_0	0xFFF0.3094	R/W	MII Management Data Control and Address Register	0x00A0.0000
MIIDA_1	0xFFF0.3894	R/W	MII Management Data Control and Address Register	0x00A0.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
MDCCR				MDCON	PreSP	BUSY	WR
15	14	13	12	11	10	9	8
Reserved			PHYAD				
7	6	5	4	3	2	1	0
Reserved			PHYRAD				

MDCCR [23:20]: MDC clock rating

Default value: **0x009**

The 4-bit value is to set the MDC clock period.

MDCCR [23:20]				MDC clock period
0	0	0	0	4 x (1/Fmclk)
0	0	0	1	6 x (1/Fmclk)
0	0	1	0	8 x (1/Fmclk)
0	0	1	1	12 x (1/Fmclk)
0	1	0	0	16 x (1/Fmclk)
0	1	0	1	20 x (1/Fmclk)
0	1	1	0	24 x (1/Fmclk)
0	1	1	1	28 x (1/Fmclk)
1	0	0	0	30 x (1/Fmclk)
1	0	0	1	32 x (1/Fmclk)
1	0	1	0	36 x (1/Fmclk)
1	0	1	1	40 x (1/Fmclk)
1	1	0	0	44 x (1/Fmclk)
1	1	0	1	48 x (1/Fmclk)
1	1	1	0	54 x (1/Fmclk)
1	1	1	1	60 x (1/Fmclk)

Default MDCCR [23:20] = 9

Users should set the MDC clock setting to meet the PHY requirement (maximum 2.5MHz). Besides, the MCLK (HCLK) frequency ranges from 10 MHz to 150 MHz (set MDC 2.5MHz).

MDCON [19]: MDC Clock On Always
Default value: 0
If this bit was set, the MDC clock will always active. Otherwise, the MDC clock will active only when the EnMDC of MCMDR and BUSY of MIIDA are both set. In other words, the MDC clock will be turned off after the station management command finished. This bit is only for debug.

PreSP [18]: Preamble Suppress
Default value: 0
If this bit is set, then the preamble is not sent to PHY.

BUSY [17]: Busy bit
Default value: 0
Set this bit to start a MII management read or write-operation. The MAC controller clears this bit automatically when the operation is completed.

WR [16]: Write/Read
Default value: 0
Set this bit for a MII management write-operation. Reset the bit for a read operation.

PHYAD [12:8]: PHY Address
Default value: 0
The 5-bit address is the PHY device address to be accessed.

PHYRAD [4:0]: PHY Register Address

Default value: 0

The 5-bit address is the register address contained in the PHY to be accessed.

The MIIDA register is used to specify the control function and the data message passing for the external physical layer device (PHY). The detail protocol and timings for the read and the write operation, respectively, of the MII management function are illustrated as the figure below. Each bit in the management data frame (MDIO) are synchronized at the rising edge of the MII management clock (MDC).

MII Management Protocol

	MII MANAGEMENT PROTOCOL							
ACCESS	**PREAMBLE**	**START**	**OPERATION**	**PHYADDR**	**PHYREGADDR**	**TA**	**DATA**	**IDLE**
READ	1…. 1	01	10	AAAAA	RRRRR	Z0	16 bits	Z
WRITE	1…. 1	01	01	AAAAA	RRRRR	10	16 bits	Z

MAC Missed Packet Count register (MPCNT_0, MPCNT_1)

The value in the MAC Missed Packet Count register (MPCNT) indicates the number of packets that were discarded due to various types of errors. Together with status information on packets transmitted and received, the **MPCNT** and these two pause count registers provide the information required for station management.

Users can read the **MPCNT** to get current missed packet counter value and clears the register (read clear). It is the responsibility of software to maintain a global count with more bits of precision. However, users can write the **MPCNT** to set the initial value of counter overflow and start to count. The counter overflow value ranges from 0x0000 to 0xFFFF (default value: 0x7FFF). It sets the corresponding bit (MMP) in the MISTA and generates an interrupt if overflow is occurred and the corresponding interrupt enable bit is set.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MPCNT_0	0xFFF0.3098	R/W	Missed Packet counter register	0x0000.7FFF
MPCNT_1	0xFFF0.3898	R/W	Missed Packet counter register	0x0000.7FFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MPCNT							
7	6	5	4	3	2	1	0
MPCNT							

MPCNT [15:0]: MAC Missed Packet Count
Default value: **0x7FFF**
It indicates the number of packets that were discarded due to various types of errors.
This counter indicates the following kinds of error:

Dribbling Bits error count (AECnt): The number of packets received with alignment errors. The counter will be increment at the end of packet reception if the MISTA indicates the alignment errors.

Frame discarded error count (RXFDCnt): The number of packets discarded by MAC because of receive FIFO overflows, or because the RxON bit is cleared. This count does not include the number of packets rejected by the CAM.

CRC error count (CECnt): The number of packets received with a CRC error. The counter will be increment at the end of packet reception if the MISTA indicates the CRC errors.

DMA Transmit Descriptor Link-list Start Address Register (TXDLSA_0, TXDLSA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
TXDLSA_0	0xFFF0.309C	R/W	Transmit Descriptor Link-list Start Address register	0xFFFF.FFFC
TXDLSA_1	0xFFF0.389C	R/W	Transmit Descriptor Link-list Start Address register	0xFFFF.FFFC

31	30	29	28	27	26	25	24
TXDLSA							
23	22	21	20	19	18	17	16
TXDLSA							
15	14	13	12	11	10	9	8
TXDLSA							
7	6	5	4	3	2	1	0
TXDLSA							

TXDLSA [31:0]: DMA transmit descriptor link list start address

Default value: 0xFFFF.FFFC

This register defines the transmit descriptor link list start address for transmission process. While software first turn on TxDMA after the hardware reset or software reset, the content of this register will be loaded into the current transmit descriptor start address. The value of this register will not be updated during any hardware operation. The system would ignore the least 2 significant bits to fit word alignment.

DMA Receive Descriptor Link List Start Address Register (RXDLSA_0, RXDLSA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
RXDLSA_0	0xFFF0.30A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC
RXDLSA_1	0xFFF0.38A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC

31	30	29	28	27	26	25	24
RXDLSA							
23	22	21	20	19	18	17	16
RXDLSA							
15	14	13	12	11	10	9	8
RXDLSA							
7	6	5	4	3	2	1	0
RXDLSA							

RXDLSA [31:0]: DMA receive descriptor link list start address

Default value: 0xFFFF.FFFC

This register defines the receive descriptor link list start address for frame reception process. While software first turn on RxDMA after the hardware reset or software reset, the content of this register will be loaded into the current receive descriptor start address. The value of this register will not be updated during any hardware operation. The system would ignore the least 2 significant bits to fit word alignment.

DMA Receive Frame Control Register (DMARFC_0, DMARFC_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DMARFC_0	0xFFF0.30A4	R/W	DMA Receive Frame Control Register	0x0000.0800
DMARFC_1	0xFFF0.38A4	R/W	DMA Receive Frame Control Register	0x0000.0800

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
RXMS							
7	6	5	4	3	2	1	0
RXMS							

RXMS [15:0]: DMA receive frame maximum size

Default value: 0800h

This value controls the maximum bytes for a received frame can be saved to memory. If the received frame size exceeds the value stored in this location and the **EnDFO** is set, an error interrupt is reported. The default maximum size is 2K bytes.

Transmit Start Demand Register (TSDR_0, TSDR_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
TSDR_0	0xFFF0.30A8	W	Transmit Start Demand Register	Undefined
TSDR_1	0xFFF0.38A8	W	Transmit Start Demand Register	Undefined

31	30	29	28	27	26	25	24
TSDR							
23	22	21	20	19	18	17	16
TSDR							
15	14	13	12	11	10	9	8
TSDR							
7	6	5	4	3	2	1	0
TSDR							

TSDR [31:0]: Transmit Start Demand Register

Default value: Undefined

While the transmit descriptor is unavailable, the Tx state machine will enter Halt state. The user has to issue a write command with any data to Transmit Start Demand register to restart the Tx operation. Only while Tx state machine stay at Halt state, the write command to Transmit Start Demand register can affect the Tx operation.

Receive Start Demand Register (TSDR_0, TSDR_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
RSDR_0	0xFFF0.30AC	W	Receive Start Demand Register	Undefined
RSDR_1	0xFFF0.38AC	W	Receive Start Demand Register	Undefined

31	30	29	28	27	26	25	24
RSDR							
23	22	21	20	19	18	17	16
RSDR							
15	14	13	12	11	10	9	8
RSDR							
7	6	5	4	3	2	1	0
RSDR							

RSDR [31:0]: Receive Start Demand Register

Default value: Undefined

While the receive descriptor is unavailable, the Rx state machine will enter Halt state. The user has to issue a write command with any data to Receive Start Demand register to restart the Rx operation.

Only while Rx state machine stay at Halt state, the write command to Receive Start Demand register can affect the Rx operation.

FIFO Threshold Adjustment Register (FIFOTHD_0, FIFOTHD_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
FIFOTHD_0	0xFFF0.30B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101
FIFOTHD_1	0xFFF0.38B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		Blength		Reserved			SWR
15	14	13	12	11	10	9	8
Reserved						TxTHD	
7	6	5	4	3	2	1	0
Reserved						RxTHD	

Blength [21:20]: DMA burst length

Default value: 0h

Value setting:

00b: 4 beats
01b: 8 beats
10b: 16 beats
11b: 16 beats

SWR [16]: software reset

Default value: 0h

Software reset. After a reset is complete, the MAC controller will clear the SWR reset bit.

TxTHD [9:8]: Transmit FIFO Lower threshold Register

Default value: 1h

Value setting:

00b: forbidden
01b: 32 bytes (i.e. high threshold 64 bytes)
10b: 64 bytes (i.e. high threshold 128 bytes)
11b: 96 bytes (i.e. high threshold 192 bytes)

This value controls the transmit FIFO low threshold. If transmitting packet number is less than the setting value, Tx DMA will request the arbiter to get data from memory.

RxTHD [1:0]: Receive FIFO Upper threshold Register

Default value: 1h

Value setting:

00b: Depend on the burst length setting

01b: 64 bytes (i.e. low threshold 32 bytes)

10b: 128 bytes (i.e. low threshold 64 bytes)

11b: 192 bytes (i.e. low threshold 96 bytes)

This value controls the receive FIFO high threshold. If receiving packet number is greater than the setting value, Rx DMA will request the arbiter to send data into memory.

MAC Interrupt Status Register (MISTA_0, MISTA_1)

The MAC event register is used as the Ethernet event register to generate interrupts and report events recognized by MAC controller. When an event is recognized, the MAC controller sets the corresponding MISTA bit. Interrupts are enabled by setting, and masked by clearing, the equivalent bits in the MAC Interrupt Enable Register (MIEN). The MISTA bits are cleared by write ones; writing zeros has no effect.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MISTA_0	0xFFF0.30B4	R/W	MAC Interrupt Status Register	0x0000.0000
MISTA_1	0xFFF0.38B4	R/W	MAC Interrupt Status Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							TxBErr
23	22	21	20	19	18	17	16
TDU	LC	TXABT	NCS	EXDEF	TXCP	TXEMP	TXINTR
15	14	13	12	11	10	9	8
Reserved	CFR	NATErr	NATOK	RxBErr	RDU	DENI	DFOI
7	6	5	4	3	2	1	0
MMP	RP	ALIE	RXGD	PTLE	RXOV	CRCE	RXINTR

TxBErr [24]: Transmit Bus Error interrupt

Default value: 0

This field will be set if access error from EMC to memory (for example, address undefined in system) is occurred. If the status and **EnTxBErr** in **MIEN** are both set, the EMC_TxINT will be triggered. If the status is set, the Tx operation will be ceased and the software reset to reset the EMC is recommended.

TDU [23]: Transmit Descriptor Unavailable interrupt

Default value: 0

This field will be set if the transmit descriptors owned to the TxDMA is unavailable. If the status and **EnTDU** in **MIEN** are both set, the EMC_TxINT will be triggered. When it is set, the TxDMA operation will be ceased till the user issues a write command to Transmit Start Demand register to restart the Tx operation.

LC [22]: Late Collision

Default value: 0

This bit will be set if a collision occurs after 512 bit times.

TXABT [21]: Transmit Abort

Default value: 0

The bit is set to indicate 16 collisions occur while transmitting the same packet.

NCS [20]: No Carrier Sense

Default value: 0

Set to indicate no carrier sense is presented during transmission.

EXDEF [19]: Defer

Default value: 0

This bit is set to indicate that defer time exceeding 0.32768ms operated at 100Mbs/s and 3.2768ms operated at 10Mbs/s. When the **EnEXDEF** in **MIEN** is set, the internal 15-bit counter will automatically count the deferred bit time and generate interrupt when the counter overflows.

TXCP [18]: Transmit Completion

Default value: 0

This bit is set when the MAC transmits, or discards one packet.

TXEMP [17]: Transmit FIFO Empty

Default value: 0

Set when MAC transmitting FIFO becomes empty (underflow) during a packet transmission.

TXINTR [16]: Interrupt on Transmit

Default value: 0

This bit is set if transmission of a packet caused an interrupt condition.

CFR [14]: Control Frame Receive

Default value: 0

This field will be set if the incoming frame is a MAC control frame (type==8808h).

NATErr [13]: NAT Processing Error

Default value: 0

This field will be set if there is any error during NATA do the NAT processing. If the status and EnNATErr in MIEN are both set, the EMC_RxINT will be triggered.

NATOK [12]: NAT Processing OK

Default value: 0

This field will be set if there is no error during NATA do the NAT processing. If the status and EnNATOK in MIEN are both set, the EMC_RxINT will be triggered.

RxBErr [11]: Receive Bus Error interrupt

Default value: 0

This field will be set if the access error from EMC to memory (for example, address undefined in system) is occurred. If the status and **EnBErr** in **MIEN** are both set, the EMC_RxINT will be triggered. If the status is set, the Rx operation will be ceased and software reset to reset the EMC is recommended.

RDU [10]: Receive Descriptor Unavailable interrupt

Default value: 0

This field will be set if the receive descriptors owned to the RxDMA is unavailable. If the status and **ENRDU** in **MIEN** are both set, the EMC_RxINT will be triggered. When the status is set, the RxDMA operation will be ceased till the user issues a write command to Receive Start Demand register to restart Rx operation.

DENI [9]: DMA early notification interrupt

Default value: 0

If **EnDEN** is reset, an interrupt will be generated when the length field of the current frame is received.

DFOI [8]: DMA receive frame over maximum size interrupt

Default value: 0

If **ENDFO** is set, an interrupt will be generated when the received frame size is larger than the value stored in **RXMS**.

MMP [7]: More Missed Packets than miss rolling over counter flag

Default value: 0

This bit is automatically set when the missed error counter rolls over.

RP [6]: Runt Packet

Default value: 0

This bits is set, it indicates that the received packet length is less than 64 bytes (unless ARP in MCMDR is set).

ALIE [5]: Alignment Error

Default value: 0

This bit is set if the frame length in bits was not a multiple of eight.

RXGD [4]: Receive Good

Default value: 0

This bit is set if a packet was successfully received with no errors.

PTLE [3]: Packet Too Long Error

Default value: 0

This bit is set if the MAC received a frame longer than 1518 bytes (unless ALP in MCMDR is set).

RXOV [2]: Receive FIFO Overflow error

Default value: 0

This bit is set if the MAC receives FIFO was overflow when receiving a frame.

CRCE [1]: CRC Error

Default value: 0

This bit is set if the CRC at the end of a packet is not correct, or else the PHY asserted Rx_er during packet reception.

RXINTR [0]: Interrupt on Receive

Default value: 0

This bit is set if the reception of a packet caused an interrupt to be generated. This includes a good received interrupt, if the EnRXGD bit in MIEN is set.

MAC General Status Register (MGSTA_0, MGSTA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MGSTA_0	0xFFF0.30B8	R/W	MAC General Status Register	0x0000.0000
MGSTA_1	0xFFF0.38B8	R/W	MAC General Status Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				TXHA	SQE	PAU	DEF
7	6	5	4	3	2	1	0
CCNT				Reserved		RXHA	CFR

All the MGSTA bits are write ones clear.

TXHA [11]: Transmission Halted

Default value: 0

Set to indicate that the transmission is halt by clearing the TXON bit.

SQE [10]: Signal Quality Error

Default value: 0

Set to indicate a SQE.

PAU [9]: Pause Bit

Default value: 0

Set when transmission was delayed due to a remote Pause command.

DEF [8]: Deferred transmission

Default value: 0

This bit is set to indicate the network is busy.

CCNT [7:4]: Collision Count

Default value: 0

Four bits counter to indicate the number of collisions occurred before the frame is transmitted.

RXHA [1]: Reception Halted

Default value: 0

This bit is set if reception is halted by clearing RXON bit in the MAC Command Register (MCMDR).

CFR [0]: Control Frame Received

Default value: 0

This bit is set if (1) the packet received is a MAC control frame (type = 8808H), (2) if the CAM recognizes the packet address, and (3) if the frame length is 64 bytes.

MAC Received Pause Count Register (MRPC_0, MRPC_1)

The received pause count register, **MRPC**, stores the value of the 16-bit received pause counter. It is read only.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MRPC_0	0xFFF0.30BC	R	MAC Receive Pause count register	0x0000.0000
MRPC_1	0xFFF0.38BC	R	MAC Receive Pause count register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MRPC							
7	6	5	4	3	2	1	0
MRPC							

MRPC [15:0]: MAC Received Pause Count Register

Default value: 0

The count value indicates the number of time slots the transmitter was paused due to the receipt of control pause operation packets from the MAC.

MAC Received Pause Current Count Register (MRPCC_0, MRPCC_1)

The received pause current count register, **MRPCC**, stores the current value of the 16-bit received pause counter. It is read only.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MRPCC_0	0xFFF0.30C0	R	MAC Receive Pause Current Count register	0x0000.0000
MRPCC_1	0xFFF0.38C0	R	MAC Receive Pause Current Count register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MRPC							
7	6	5	4	3	2	1	0
MRPC							

MRPC [15:0]: MAC Received Pause Count Register

Default value: 0

The count value indicates the number of time slots the transmitter was paused due to the receipt of control pause operation packets from the MAC.

MAC Remote Pause Count Register (MREPC_0, MREPC_1)

The remote pause count register, MREPC, stores the current value of the remote pause counter. It is read only.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MREPC_0	0xFFF0.30C4	R	MAC Remote pause count register	0x0000.0000
MREPC_1	0xFFF0.38C4	R	MAC Remote pause count register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
MREPC							
7	6	5	4	3	2	1	0
MREPC							

MREPC [15:0]: MAC Remote Pause Count Register

Default value: 0

The count value indicates the number of time slots that a remote MAC was paused as a result of its sending control pause operation packets.

DMA Receive Frame Status Register (DMARFS_0, DMARFS_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DMARFS_0	0xFFF0.30C8	R/W	DMA Receive Frame Status Register	0x0000.0000
DMARFS_1	0xFFF0.38C8	R/W	DMA Receive Frame Status Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
RXFS							
7	6	5	4	3	2	1	0
RXFS							

RXFS [15:0]: DMA receive frame length

Default value: 0000h

When an early notification interrupt occurs, the frame length/type field contains the size of the frame that is currently being received, and stores in **RXFS**.

To save space in the frame memory buffer, users can determine the current frame length by :

1. Enable the early notification interrupt (set **EnDEN** bit in **MIEN**)
2. Read the RXFS field when the interrupt occurs

Note: all the DMARFS bits are cleared by write ones; writing zeros has no effect.

Current Transmit Descriptor Start Address Register (CTXDSA_0, CTXDSA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CTXDSA_0	0xFFF0.30CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000
CTXDSA_1	0xFFF0.38CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CTXDSA							
23	22	21	20	19	18	17	16
CTXDSA							
15	14	13	12	11	10	9	8
CTXDSA							
7	6	5	4	3	2	1	0
CTXDSA							

CTXDSA [31:0]: Current Transmit Descriptor Start Address

Default value: 0000h

This register reports the start address of the current transmit descriptor used by EMC.

Current Transmit Buffer Start Address Register (CTXBSA_0, CTXBSA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CTXBSA_0	0xFFF0.30D0	R	Current Transmit Buffer Start Address Register	0x0000.0000
CTXBSA_1	0xFFF0.38D0	R	Current Transmit Buffer Start Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CTXBSA							
23	22	21	20	19	18	17	16
CTXBSA							
15	14	13	12	11	10	9	8
CTXBSA							
7	6	5	4	3	2	1	0
CTXBSA							

CTXBSA [31:0]: Current Transmit Buffer Start Address

Default value: 0000h

This register reports the start address of the current transmit buffer used by EMC.

Current Receive Descriptor Start Address Register (CRXDSA_0, CRXDSA_1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CRXDSA_0	0xFFF0.30D4	R	Current Receive Descriptor Start Address Register	0x0000.0000
CRXDSA_1	0xFFF0.38D4	R	Current Receive Descriptor Start Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CRXDSA							
23	22	21	20	19	18	17	16
CRXDSA							
15	14	13	12	11	10	9	8
CRXDSA							
7	6	5	4	3	2	1	0
CRXDSA							

CRXDSA [31:0]: Current Receive Descriptor Start Address

Default value: 0000h

This register reports the start address of the current receive descriptor used by EMC.

Current Receive Buffer Start Address Register (CRXBSA_0, CRXBSA_1)

Register	Address	R/W	Description	Reset Value
CRXBSA_0	0xFFF0.30D8	R	Current Receive Buffer Start Address Register	0x0000.0000
CRXBSA_1	0xFFF0.38D8	R	Current Receive Buffer Start Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CRXBSA							
23	22	21	20	19	18	17	16
CRXBSA							
15	14	13	12	11	10	9	8
CRXBSA							
7	6	5	4	3	2	1	0
CRXBSA							

CRXBSA [31:0]: Current Receive Buffer Start Address

Default value: 0000h

This register reports the start address of the current receive buffer used by EMC.

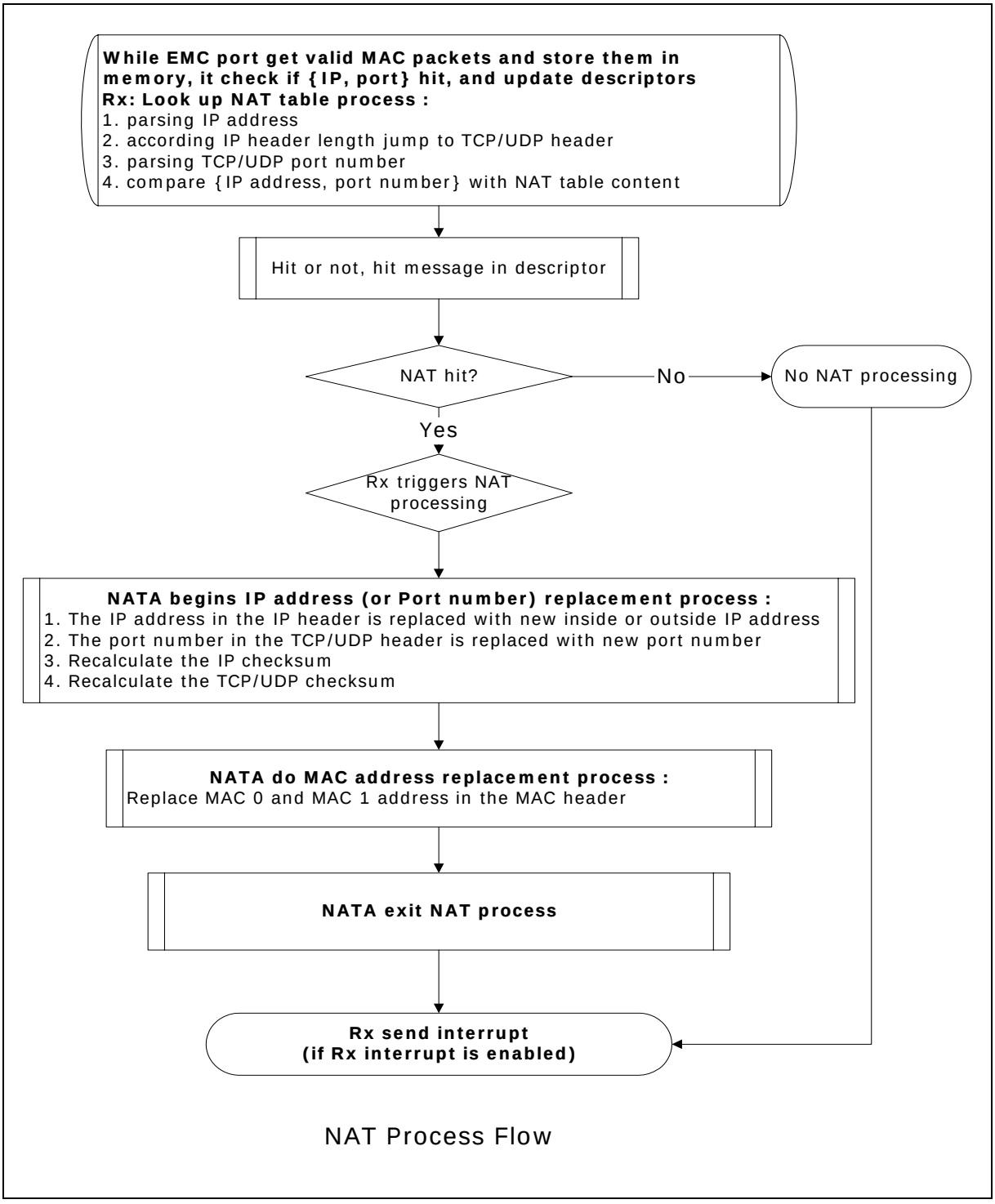
6.6 Network Address Translation Accelerator (NATA)

The Network Address Translation Accelerator (NATA) provides hardware acceleration function to enhance the IP address and port number translation. An inside (local/LAN) IP address is mapped to an outside (global/WAN) IP address, meaning that an inside IP address is replaced by the appropriate outside IP address, and vice versa. When the network is connected and SW Users can use NATA on W90N740 to speed up fixed (static) address translation and reduce software loading on processing layer-3 IP replacement. The NATA has 64 entries for users to initial replacement IP content and cooperate the 2 EMC ports to do NAT.

The Features of the NATA：

- Hardware acceleration on IP address / port number look up and replacement for network address
- Translation, including MAC address translation
- Provide 64 entries of translation table
- Support TCP / UDP packets

6.6.1 NAT Process Flow



NAT Process Flow

6.6.2 NATA Registers Map

This set of registers is used to convey status/control information to/from the NAT engine. These registers are used for loading commands generated by user, indicating network translation status, and providing interrupt control.

The registers used by W90N740 NATA controller are divided into two groups:

- **NATA Control and Status Registers**
- **Address Look Up and Replacement Entry Registers**

REGISTER	OFFSET	R/W	DESCRIPTION	RESET VALUE
NATA Control and Status Registers				
NATCMD	0xFFF0.6000	R/W	NAT Command Register	0x0000.0000
NATCCLR0	0xFFF0.6010	W	NAT Counter 0 Clear Register	0x0000.0000
NATCCLR1	0xFFF0.6014	W	NAT Counter 1 Clear Register	0x0000.0000
NATCCLR2	0xFFF0.6018	W	NAT Counter 2 Clear Register	0x0000.0000
NATCCLR3	0xFFF0.601C	W	NAT Counter 3 Clear Register	0x0000.0000
NATCFG0	0xFFF0.6100	R/W	NAT Entry 0 Configuration Register	0x0000.0000
NATCFG1	0xFFF0.6104	R/W	NAT Entry 1 Configuration Register	0x0000.0000
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
NATCFG63	0xFFF0.61FC	R/W	NAT Entry 63 Configuration Register	0x0000.0000
EXMACM	0xFFF0.6200	R/W	External MAC Address Most Significant Word Register	0x0000.0000
EXMACL	0xFFF0.6204	R/W	External MAC Address Least Significant Word Register	0x0000.0000
INMACM	0xFFF0.6208	R/W	Internal MAC Address Most Significant Word Register	0x0000.0000
INMACL	0xFFF0.620C	R/W	Internal MAC Address Least Significant Word Register	0x0000.0000

REGISTER	OFFSET	R/W	DESCRIPTION	RESET VALUE
Address Lookup and Replacement Registers				
MASAD0	0xFFF0.6800	R/W	NAT Masquerading IP Address Entry 0	0x0000.0000
MASPN0	0xFFF0.6804	R/W	NAT Masquerading Port Number Entry 0	0x0000.0000
LSAD0	0xFFF0.6808	R/W	Local Station IP Address Entry 0	0x0000.0000
LSPN0	0xFFF0.680C	R/W	Local Station Port Number Entry 0	0x0000.0000
LSMAC0M	0xFFF0.6810	R/W	Local Station MAC Address Most Significant Word Register for Entry 0	0x0000.0000
LSMAC0L	0xFFF0.6814	R/W	Local Station MAC Address Least Significant Word Register for Entry 0	0x0000.0000
RSMAC0M	0xFFF0.6818	R/W	Remote Station MAC Address Most Significant Word Register for Entry 0	0x0000.0000
RSMAC0L	0xFFF0.681C	R/W	Remote Station MAC Address Least Significant Word Register for Entry 0	0x0000.0000
MASAD1	0xFFF0.6820	R/W	NAT Masquerading IP Address Entry 1	0x0000.0000
MASPN1	0xFFF0.6824	R/W	NAT Masquerading Port Number Entry 1	0x0000.0000
LSAD1	0xFFF0.6828	R/W	Local Station IP Address Entry 1	0x0000.0000
LSPN1	0xFFF0.682C	R/W	Local Station Port Number Entry 1	0x0000.0000
LSMAC1M	0xFFF0.6830	R/W	Local Station MAC Address Most Significant Word Register for Entry 1	0x0000.0000
LSMAC1L	0xFFF0.6834	R/W	Local Station MAC Address Least Significant Word Register for Entry 1	0x0000.0000
RSMAC1M	0xFFF0.6838	R/W	Remote Station MAC Address Most Significant Word Register for Entry 1	0x0000.0000
RSMAC1L	0xFFF0.683C	R/W	Remote Station MAC Address Least Significant Word Register for Entry 1	0x0000.0000
. . . .	. . . .	. . . .	. . . .	. . . .
MASAD63	0xFFF0.6FE0	R/W	NAT Masquerading IP Address Entry 63	0x0000.0000
MASPN63	0xFFF0.6FE4	R/W	NAT Masquerading Port Number Entry 63	0x0000.0000
LSAD63	0xFFF0.6FE8	R/W	Local Station IP Address Entry 63	0x0000.0000
LSPN63	0xFFF0.6FEC	R/W	Local Station Port Number Entry 63	0x0000.0000
LSMAC63M	0xFFF0.6FF0	R/W	Local Station MAC Address Most Significant Word Register for Entry 63	0x0000.0000
LSMAC63L	0xFFF0.6FF4	R/W	Local Station MAC Address Least Significant Word Register for Entry 63	0x0000.0000
RSMAC63M	0xFFF0.6FF8	R/W	Remote Station MAC Address Most Significant Word Register for Entry 63	0x0000.0000
RSMAC63L	0xFFF0.6FFC	R/W	Remote Station MAC Address Least Significant Word Register for Entry 63	0x0000.0000

NAT Command Register (NATCMD)

The NAT function is enabled by software setting NATEN, and auto triggered by EMC Rx if current packet is hit. S/W will get hit status from Rx descriptors when current packet is receiving, and processed by NATA, if it is hit. Writing ones in NATCMD can start NAT function, or clear entry counters.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
NATCMD	0x7FF06000	R/W	NAT Command Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							NATEN

NATEN [0]: NAT enable bit

Default value: 0

Set this bit to start NAT function. The EMC Rx will begin packet parsing and lookup procedure if this bit is set. Clear this bit will stop all NAT operations.

NAT Counter x Clear Register (NATCCLRx)(x: 3 ~ 0)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
NATCCLR0	0x7FF06010		NAT Counter 0 Clear Register	0x0000.0000
|	|	W	|	|
NATCCLR3	0x7FF0601C		NAT Counter 3 Clear Register	0x0000.0000

6.6.2.1. NATCCLR0

31	30	29	28	27	26	25	24
CLREH15	CLREH14	CLREH13	CLREH12	CLREH11	CLREH10	CLREH 9	CLREH 8
23	22	21	20	19	18	17	16
CLREH 7	CLREH 6	CLREH 5	CLREH 4	CLREH 3	CLREH 2	CLREH 1	CLREH 0
15	14	13	12	11	10	9	8
CLRCNT15	CLRCNT14	CLRCNT13	CLRCNT12	CLRCNT11	CLRCNT10	CLRCNT9	CLRCNT8
7	6	5	4	3	2	1	0
CLRCNT7	CLRCNT6	CLRCNT5	CLRCNT4	CLRCNT3	CLRCNT2	CLRCNT1	CLRCNT0

6.6.2.2. NATCCLR1

31	30	29	28	27	26	25	24
CLREH31	CLREH30	CLREH29	CLREH28	CLREH27	CLREH26	CLREH25	CLREH24
23	22	21	20	19	18	17	16
CLREH23	CLREH22	CLREH21	CLREH20	CLREH19	CLREH18	CLREH17	CLREH16
15	14	13	12	11	10	9	8
CLRCNT31	CLRCNT30	CLRCNT29	CLRCNT28	CLRCNT27	CLRCNT26	CLRCNT25	CLRCNT24
7	6	5	4	3	2	1	0
CLRCNT23	CLRCNT22	CLRCNT21	CLRCNT20	CLRCNT19	CLRCNT18	CLRCNT17	CLRCNT16

6.6.2.3. NATCCLR2

31	30	29	28	27	26	25	24
CLREH47	CLREH46	CLREH45	CLREH44	CLREH43	CLREH42	CLREH41	CLREH40
23	22	21	20	19	18	17	16
CLREH39	CLREH38	CLREH37	CLREH36	CLREH35	CLREH34	CLREH33	CLREH32
15	14	13	12	11	10	9	8
CLRCNT47	CLRCNT46	CLRCNT45	CLRCNT44	CLRCNT43	CLRCNT42	CLRCNT41	CLRCNT40
7	6	5	4	3	2	1	0
CLRCNT39	CLRCNT38	CLRCNT37	CLRCNT36	CLRCNT35	CLRCNT34	CLRCNT33	CLRCNT32

6.6.2.4. NATCCLR3

31	30	29	28	27	26	25	24
CLREH63	CLREH62	CLREH61	CLREH60	CLREH59	CLREH58	CLREH57	CLREH56
23	22	21	20	19	18	17	16
CLREH55	CLREH54	CLREH53	CLREH52	CLREH51	CLREH50	CLREH49	CLREH48
15	14	13	12	11	10	9	8
CLRCNT63	CLRCNT62	CLRCNT61	CLRCNT60	CLRCNT59	CLRCNT58	CLRCNT57	CLRCNT56
7	6	5	4	3	2	1	0
CLRCNT55	CLRCNT54	CLRCNT53	CLRCNT52	CLRCNT51	CLRCNT50	CLRCNT49	CLRCNT48

CLREHx (x: 63 ~ 0) [31:16]: Entry x hit counter clear bit

Default value: 0

Set the appropriate bit to clear the corresponding entry x hit counter (EHCNTx); writing zero to the bit has no effect. About the usage of EHCNTx, please see details in NATCFGx.

CLRCNTx (x: 63 ~ 0) [15:0]: NATA Entry x counter clear bit

Default value: 0

Set the appropriate bit to clear the corresponding entry counter (CNTx); writing zero to the bit has no effect. About the usage of CNTx, please see details in NATCFGx.

NAT Entry x Configuration Registers (NATCFGx)(x: 63 ~ 0)

All NAT Configuration registers, NATCFGx, include enable switches to control IP address and port number comparison, or replacement. Further, additional inverse (I) bit to control source address (SA) or destination address (DA) comparison. The NAT function is enabled if either of entry enable bits is set, else the NAT function is disabled.

For some special applications, the user can reset the port comparison enable bits to ignore port comparison and do only IP address comparison.

The entry count field, CNTx, is read by S/W to determine when to change either entry data without miss hit packet processing. If S/W program wants to change some entry data, S/W program has to disable the selected entry and monitor corresponding CNTx till the value is 0, then it is acceptable to change new entry data. Otherwise there may be an error condition occurred, for example, when S/W program has changed entry data, but the previous hit packet is being processed, and cannot find replacement data.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
NATCFG0	0x7FF06100	R/W	NAT Entry 0 Configuration Register	0x0000.0000
|	|	|	|	|
NATCFG63	0x7FF061FC	R/W	NAT Entry 63 Configuration Register	0x0000.0000

31	30	29	28	27	26	25	24
EHCNTx							
23	22	21	20	19	18	17	16
EHCNTx							
15	14	13	12	11	10	9	8
Reserved					CNTx		
7	6	5	4	3	2	1	0
Nop	Discard	Inverse	PxRE	AxRE	PxCE	AxCE	ExEN

6.6.2.5. EHCNTx [31:16]: Counter of Packets Hit with Entry x

Default value: 0

The register is read-only, to indicate that how many packets are hit with entry x. When a new packet is hit with entry x, the corresponding EHCNTx, will increase. The value can be reset to zero by writing one to corresponding CLREHx in NATCCLR register.

6.6.2.6. CNTx [10:8]: Number of Entry x Hit Packets to be processed

Default value: 0x0

The register is read-only, to indicate that how many packet is hit with entry x and still not processed by NAT. When a new packet is hit with entry x, the corresponding entry counter, CNTx, will increase. On the other hand, when a packet hit with entry x is process, the corresponding CNTx will be decrease.

Nop [7]: Packet Nop bit

Default value: 0

Set this bit to receive current hit packet as usual. The Rx descriptor will be updated for this packet and set the Nop bit in descriptor. This bit will be valid while Discard[6]=0.

Discard [6]: Packet Discard bit

Default value: 0

Set this bit to automatically discard current hit packet. The Rx descriptor will not be updated for this packet. It is applicable for IP filter.

Inverse [5]: Inverse Comparison and Replacement bit

Default value: 0

Set this bit to change comparison and replacement field in packets. For example, at the WAN port, destination address and port {DA, DP} is compared for inverse bit (I bit) clear. If I bit is set, source address and port {SA, SP} is compared instead of {DA, DP}. It is applicable for IP filter.

PxRE [4]: Port Number Replacement Enable at Entry x

Default value: 0

Set the bits to selectively enable port number replacement at the entry location. This bit is valid when ExEN is set.

AxRE [3]: IP Address Replacement Enable at Entry x

Default value: 0

Set the bits to selectively enable IP address replacement at the entry location. This bit is valid when ExEN is set.

PxCE [2]: Port Number Comparison Enable at Entry x

Default value: 0

Set the bits to selectively enable port number comparison at the entry location. This bit is valid when ExEN is set.

AxCE [1]: IP Address Comparison Enable at Entry x

Default value: 0

Set the bits to selectively enable IP address comparison at the entry location. This bit is valid when ExEN is set.

ExEN [0]: Entry x Comparison Enable bit

Default value: 0

Set the bits to selectively enable entry location comparison. To disable an entry location, clear the appropriate bit. If S/W wants to change some entry data, it has to disable the selected entry and monitor corresponding CNTx till the value is 0, then it is acceptable to change new entry data.

NAT Entry Configuration Register (NATCFGx) Application Note:

MA: masquerading IP address

MP: masquerading port number

LA: local mapping IP address

LP: local mapping port number

SA: (IP) address at source field

SP: port number at source field

DA: (IP) address at destination field

DP: port number at destination field

Data Content in the NATA table

	Field 0	**Field 1**	**Field 2**	**Field 3**
Entry 0	*MA 0*	*MP 0*	*LA 0*	*LP 0*
Entry 1	*MA 0*	*MP 0*	*LA 0*	*LP 0*
....	....	....	....	....
Entry 15	*MA 15*	*MP 15*	*LA 15*	*LP 15*

NATA comparison and replacement table at different port

	INVERSE BIT IS RESET		INVERSE BIT IS SET	
	COMPARISON	**REPLACEMENT**	**COMPARISON**	**REPLACEMENT**
WAN port (for receiving external packets)	**DA with *MA*** (if AxCE set)	**DA with *LA*** (if AxRE set)	**SA with *MA*** (if AxCE set)	**SA with *LA*** (if AxRE set)
	DP with *MP* (if PxCE set)	**DP with *LP*** (if PxRE set)	**SP with *MP*** (if PxCE set)	**SP with *LP*** (if PxRE set)
LAN port (for receiving local station packets)	**SA with *LA*** (if AxCE set)	**SA with *MA*** (if AxRE set)	**DA with *LA*** (if AxCE set)	**DA with *MA*** (if AxRE set)
	SP with *LP* (if PxCE set)	**SP with *MP*** (if PxRE set)	**DP with *LP*** (if PxCE set)	**DP with *MP*** (if PxRE set)

6.6.2.7. Possible Settings for Different Applications, only for reference

	AxCE	PxCE	AxRE	PxRE	I bit	Description
NAT with port comparison	1	1	1	1	0	Comparison IP address and port number
NAT without port comparison	1	0	1	0	0	Comparison IP address
IP filter	1	1	0	0	1	The S/W program can discard the hit packets for filtering

There are still some restrictions of configuration table above. It cannot be replaced the Address or Port without compare them first.

MAC Address Registers (EXMACM, EXMACL, INMACM, INMACL, LSMACxM, LSMACxL, RSMACxM, RSMACxL)

The MAC address registers are to store the MAC address of each EMC port. When the NATA is enabled and corresponding entry is hit, the MAC address translation from one port to another port must be done by hardwire, instead of by software. Thus the user must set the MAC address of each port for NAT to translate.

{EXMACM, EXMACL (INMACM, INMACL)}: MAC address (6 bytes), with 2 bytes in EXMACL (INMACL) and 4 bytes in EXMACM (INMACM)

{LSMACxM, LSMACxL (RSMACxM, RSMACxL)}: MAC address (6 bytes), with 2 bytes in LSMACxL (RSMACxL) and 4 bytes in LSMACxM (RSMACxM)

For example, if the External MAC address is desired to store 12-34-56-78-90-13, then the content of EXMACM is 12-34-56-78, and the content of EXMACL is 90-13-00-00.

6.6.2.8. EXMACM, INMACM, LSMACxM, RSMACxM

31	30	29	28	27	26	25	24
Address Byte 6 (Most Significant Byte)							
23	22	21	20	19	18	17	16
Address Byte 5							
15	14	13	12	11	10	9	8
Address Byte 4							
7	6	5	4	3	2	1	0
Address Byte 3							

EXMACL, INMACL, LSMACxL, RSMACxL

31	30	29	28	27	26	25	24
Destination Address Byte 2							
23	22	21	20	19	18	17	16
Destination Address Byte 1							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

NAT Masquerading IP Address Registers (MASADx) (x : 15 ~ 0)

NAT Masquerading Port Number Registers (MASPNx) (x : 15 ~ 0)

Local Station IP Address Registers (LSADx) (x : 15 ~ 0)

Local Station Port Number Registers (LSPNx) (x : 15 ~ 0)

The **{MASADx, MASPNx}** is represented for the outside IP address and the port number.

The **{LSADx, LSPNx}** is represented for the internal IP address and the port number.

A private network is set up with its own public IP address (MASADx) and port number (MASPNx) for external access. It means that when a local station wants to sent a packet outside via the NAT module, the packet is transmitted to external MAC port with its source address and source port number replaced by MASADx and MASPNx.

On the other hand, when the external MAC receive packet, its destination address and destination port number is compared. If the result is hit, then its destination address and destination port number are be replaced by LSADx and LSPNx, and the packet is transmitted to local MAC.

6.6.2.9. MASADx, LSADx

31	30	29	28	27	26	25	24
IP Address Byte 4 (Most Significant Byte)							
23	22	21	20	19	18	17	16
IP Address Byte 3							
15	14	13	12	11	10	9	8
IP Address Byte 2							
7	6	5	4	3	2	1	0
IP Address Byte 1							

MASPNx, LSPNx

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Port Number							
7	6	5	4	3	2	1	0
Port Number							

For example, if the masquerading address is 140.112.2.100 and the masquerading port number is 7500, then the value in MASAD is 8C-70-02-64, and the value in MASPN is 00-00-1D-4C.

6.7 GDMA Controller

The GDMA Controller of W90N740 is a two-channel general DMA controller. The two-channel GDMA performs the following data transfers without the CPU intervention:

- Memory-to-memory (memory to/from memory)
- Memory –to – IO
- IO- to -memory

The GDMA can be started by the software or external DMA request nXDREQ1/2/3. Software can also be used to restart the GDMA operation after it has been stopped. The CPU can recognize the completion of a GDMA operation by software polling or when it receives an internal GDMA interrupt. The W90N740 GDMA controller can increase source or destination address, decrease them as well, and conduct 8-bit (byte), 16-bit (half-word), or 32-bit (word) data transfers.

The Features of the GDMA ：

- 2 Channel GDMA for memory-to-memory data transfers without CPU intervention
- Increase or decrease source / destination address in 8-bit, 16-bit, or 32-bit data transfers
- Supports 4-data burst mode to boost performance
- Support external GDMA request by through bank 3

6.7.1 GDMA Function Description

The GDMA directly transfers data between source and destination. The GDMA starts to transfer data after it receives service requests from nXDREQ1/2/3 signal or software. When the entire data have been transferred completely, the GDMA becomes idle. Nevertheless, if another transfer is needed, then the GDMA must be programmed again.

There are three transfer modes:

- **Single Mode**

  Single mode requires a GDMA request for each data transfer. A GDMA request (nXDREQ1/2/3 or software) causes one byte, one half-word, or one word to transfer if the 4-data burst mode is disabled, or four times of transfer width is the 4-data burst mode is enabled.

- **Block Mode**

  The assertion of a single GDMA request causes all of the data to be transferred in a single operation. The GDMA transfer is completed when the current transfer count register reaches zero.

- **Demand Mode**

  The GDMA continues transferring data until the GDMA request input nXDREQ1/2/3 becomes inactive.

6.7.2 GDMA Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CTL0	0xFFF0.4000	R/W	Channel 0 Control Register	0x0000.0000
GDMA_SRCB0	0xFFF0.4004	R/W	Channel 0 Source Base Address Register	0x0000.0000
GDMA_DSTB0	0xFFF0.4008	R/W	Channel 0 Destination Base Address Register	0x0000.0000
GDMA_TCNT0	0xFFF0.400C	R/W	Channel 0 Transfer Count Register	0x0000.0000
GDMA_CSRC0	0xFFF0.4010	R	Channel 0 Current Source Address Register	0x0000.0000
GDMA_CDST0	0xFFF0.4014	R	Channel 0 Current Destination Address Register	0x0000.0000
GDMA_CTCNT0	0xFFF0.4018	R	Channel 0 Current Transfer Count Register	0x0000.0000
GDMA_CTL1	0xFFF0.4020	R/W	Channel 1 Control Register	0x0000.0000
GDMA_SRCB1	0xFFF0.4024	R/W	Channel 1 Source Base Address Register	0x0000.0000
GDMA_DSTB1	0xFFF0.4028	R/W	Channel 1 Destination Base Address Register	0x0000.0000
GDMA_TCNT1	0xFFF0.402C	R/W	Channel 1 Transfer Count Register	0x0000.0000
GDMA_CSRC1	0xFFF0.4030	R	Channel 1 Current Source Address Register	0x0000.0000
GDMA_CDST1	0xFFF0.4034	R	Channel 1 Current Destination Address Register	0x0000.0000
GDMA_CTCNT1	0xFFF0.4038	R	Channel 1 Current Transfer Count Register	0x0000.0000

R: read only ; W: write only ; R/W: both read and write

Channel 0/1 Control Register (GDMA_CTL0, GDMA_CTL1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CTL0	0xFFF0.4000	R/W	Channel 0 Control Register	0x0000.0000
GDMA_CTL1	0xFFF0.4020	R/W	Channel 1 Control Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED				REQ_SEL		REQ_ATV	ACK_ATV
23	22	21	20	19	18	17	16
RESERVED	SABNDERR	DABNDERR	GDMAERR	AUTOIEN	TC	BLOCK	SOFTREQ
15	14	13	12	11	10	9	8
DM	RESERVED	TWS		SBMS	RESERVED	BME	SIEN
7	6	5	4	3	2	1	0
SAFIX	DAFIX	SADIR	DADIR	GDMAMS		RESERVED	GDMAEN

REQ_SEL [27:26]: External request pin selection, if GDMAMS [3:2]=00, REQ_SEL doesn't care.

If REQ_SEL [27:26]=00, external request doesn't use.

If REQ_SEL [27:26]=01, use nXDREQ1.

If REQ_SEL [27:26]=10, use nXDREQ2.

If REQ_SEL [27:26]=11, use nXDREQ3.

REQ_ATV [25]: nXDREQ High/Low active selection

If REQ_ATV [25]=0, nXDREQ1/2/3 is **LOW** active.

If REQ_ATV [25]=1, nXDREQ1/2/3 is **HIGH** active.

ACK_ATV [24]: nXDACK High/Low active selection

If ACK_ATV [24]=0, nXDACK is **LOW** active.

If ACK_ATV [24]=1, nXDACK is **HIGH** active.

SABNDERR [22]: Source address Boundary alignment Error flag

If TWS [13:12]=10, GDMA_SRCB [1:0] should be 00

If TWS [13:12]=01, GDMA_SRCB [0] should be 0

The address boundary alignment should be depended on TWS [13:12].

0 = the GDMA_SRCB is on the boundary alignment.

1 = the GDMA_SRCB not on the boundary alignment

The SABNDERR register bits just can be read only.

DABNDERR [21]: Destination address Boundary alignment Error flag

If TWS [13:12]=10, GDMA_DSTB [1:0] should be 00

If TWS [13:12]=01, GDMA_DSTB [0] should be 0

The address boundary alignment should be depended on TWS [13:12].

0 = the GDMA_DSTB is on the boundary alignment.

1 = the GDMA_DSTB not on the boundary alignment

The DABNDERR register bits just can be read only.

GDMATERR [20]: GDMA Transfer Error

O = No error occurs

1 = Hardware sets this bit on a GDMA transfer failure

Transfer error will generate GDMA interrupt

AUTOIEN [19]: Auto initialization Enable

0 = Disables auto initialization

1 = Enables auto initialization, the GDMA_CSRC0/1,GDMA_CDST0/1,and GDMA_CTCNT0/1 registers are updated by the GDMA_SRC0/1,GDMA_DST0/1,and GDMA_TCNT0/1 registers automatically when transfer is complete.

TC [18]: Terminal Count

0 = Channel does not expire

1 = Channel expires; this bit is set only by GDMA hardware, and clear by software to write logic 0.

TC [18] is the GDMA interrupt flag. TC [18] or GDMATERR[20] will generate interrupt

BLOCK [17]: Bus Lock

0 = Unlocks the bus during the period of transfer

1 = locks the bus during the period of transfer

SOFTREQ [16]: Software Triggered GDMA Request

Software can request the GDMA transfer service by setting this bit to 1. This bit is automatically cleared by hardware when the transfer is completed. This bit is available only while GDMAMS [3:2] register bits are set on software mode (memory to memory).

DM [15]: Demand Mode

0 = Normal external GDMA mode

1 = When this bit is set to 1, the external GDMA operation is speeded up. When external GDMA device is operating in the demand mode, the GDMA transfers data as long as the external GDMA request signal nXDREQ1/2/3 is active. The amount of data transferred depends on how long the nXDREQ1/2/3 is active. When the nXDREQ1/2/3 is active and GDMA gets the bus in Demand mode, DMA holds the system bus until the nXDREQ1/2/3 signal becomes non-active. Therefore, the period of the active nXDREQ1/2/3 signal should be carefully tuned such that the entire operation does not exceed an acceptable interval (for example, in a DRAM refresh operation).

TWS [13:12]: Transfer Width Select

00 = One byte (8 bits) is transferred for every GDMA operation

01 = One half-word (16 bits) is transferred for every GDMA operation

10 = One word (32 bits) is transferred for every GDMA operation

11 = Reserved

The GDMA_SCRB and GDMA_DSTB should be alignment under the TWS selection

SBMS [11]: Single/Block Mode Select

0 = Selects single mode. It requires an external GDMA request for every incurring GDMA operation.

1 = Selects block mode. It requires a single external GDMA request during the atomic GDMA operation. An atomic GDMA operation is defined as the sequence of GDMA operations until the transfer count register reaches zero.

6.7.2.1. BME [9]: Burst Mode Enable

0 = Disables the 4-data burst mode

1 = Enables the 4-data burst mode

Ff there are 16 words to be transferred, and BME [9]=1, the GDMA_TCNT should be 0x04;

However, if BME [9]=0, the GDMA_TCNT should be 0x10.

SIEN [8]: Stop Interrupt Enable

0 = Do not generate an interrupt when the GDMA operation is stopped

1 = interrupt is generated when the GDMA operation is stopped

SAFIX [7]: Source Address Fixed

0 = Source address is changed during the GDMA operation

1 = Do not change the destination address during the GDMA operation. This feature can be used when data were transferred from a single source to multiple destinations.

DAFIX [6]: Destination Address Fixed

0 = Destination address is changed during the GDMA operation

1 = Do not change the destination address during the GDMA operation. This feature can be used when data were transferred from multiple sources to a single destination.

DADIR [5]: Source Address Direction

0 = Source address is incremented successively

1 = Source address is decremented successively

DADIR [4]: Destination Address Direction

0 = Destination address is incremented successively

1 = Destination address is decremented successively

GDMAMS [3:2]: GDMA Mode Select

00 = Software mode (memory-to-memory)

01 = External nXDREQ1/2/3 mode for external device

10 = Reserved

11 = Reserved

GDMAEN [0]: GDMA Enable

0 = Disables the GDMA operation

1 = Enables the GDMA operation; this bit will be clear automatically when the transfer is complete on AUTOIEN [19] register bit is on Disable mode.

Channel 0/1 Source Base Address Register (GDMA_SRCB0, GDMA_SRCB1)

The GDMA channel starts reading its data from the source address as defined in this source base address register.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_SRCB0	0xFFF0.4004	R/W	Channel 0 Source Base Address Register	0x0000.0000
GDMA_SRCB1	0xFFF0.4024	R/W	Channel 1 Source Base Address Register	0x0000.0000

31	30	29	28	27	26	25	24
SRC_BASE_ADDR [31:24]							
23	22	21	20	19	18	17	16
SRC_BASE_ADDR [23:16]							
15	14	13	12	11	10	9	8
SRC_BASE_ADDR [15:8]							
7	6	5	4	3	2	1	0
SRC_BASE_ADDR [7:0]							

SRC_BASE_ADDR [31:0]: 32-bit Source Base Address

Channel 0/1 Destination Base Address Register (GDMA_DSTB0, GDMA_DSTB1)

The GDMA channel starts writing its data to the destination address as defined in this destination base address register. During a block transfer, the GDMA determines successive destination addresses by adding to or subtracting from the destination base address.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_DSTB0	0xFFF0.4008	R/W	Channel 0 Destination Base Address Register	0x0000.0000
GDMA_DSTB1	0xFFF0.4028	R/W	Channel 1 Destination Base Address Register	0x0000.0000

31	30	29	28	27	26	25	24
DST_BASE_ADDR [31:24]							
23	22	21	20	19	18	17	16
DST_BASE_ADDR [23:16]							
15	14	13	12	11	10	9	8
DST_BASE_ADDR [15:8]							
7	6	5	4	3	2	1	0
DST_BASE_ADDR [7:0]							

DST_BASE_ADDR [31:0]: 32-bit Destination Base Address

Channel 0/1 Transfer Count Register (GDMA_TCNT0, GDMA_TCNT1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_TCNT0	0xFFF0.400C	R/W	Channel 0 Transfer Count Register	0x0000.0000
GDMA_TCNT1	0xFFF0.402C	R/W	Channel 1 Transfer Count Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
TFR_CNT [23:16]							
15	14	13	12	11	10	9	8
TFR_CNT [15:8]							
7	6	5	4	3	2	1	0
TFR_CNT [7:0]							

TFR_CNT [23:0]: 24-bit Transfer Count

The TFR_CNT represents the required number of GDMA transfers. The maximum transfer count is 16M –1.

Channel 0/1 Current Source Register (GDMA_CSRC0, GDMA_CSRC1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CSRC0	0xFFF0.4010	R	Channel 0 Current Source Address Register	0x0000.0000
GDMA_CSRC1	0xFFF0.4030	R	Channel 1 Current Source Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CURRENT_SRC_ADDR [31:24]							
23	22	21	20	19	18	17	16
CURRENT_SRC_ADDR [23:16]							
15	14	13	12	11	10	9	8
CURRENT_SRC_ADDR [15:8]							
7	6	5	4	3	2	1	0
CURRENT_SRC_ADDR [7:0]							

CURRENT_SRC_ADDR [31:0]: 32-bit Current Source Address

The CURRENT_SRC_ADDR indicates the source address where the GDMA transfer is just occurring. During a block transfer, the GDMA determines the successive source addresses by adding to or subtracting from the source base address. Depending on the settings you make to the control register, the current source address will remain the same or will be incremented or decremented.

Channel 0/1 Current Destination Register (GDMA_CDST0, GDMA_CDST1)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CDST0	0xFFF0.4014	R	Channel 0 Current Destination Address Register	0x0000.0000
GDMA_CDST1	0xFFF0.4034	R	Channel 1 Current Destination Address Register	0x0000.0000

31	30	29	28	27	26	25	24
CURRENT_DST_ADDR [31:24]							
23	22	21	20	19	18	17	16
CURRENT_DST_ADDR [23:16]							
15	14	13	12	11	10	9	8
CURRENT_DST_ADDR [15:8]							
7	6	5	4	3	2	1	0
CURRENT_DST_ADDR [7:0]							

CURRENT_DST_ADDR [31:0]: 32-bit Current Destination Address

The CURRENT_DST_ADDR indicates the destination address where the GDMA transfer is just occurring. During a block transfer, the GDMA determines the successive destination addresses by adding to or subtracting from the destination base address. Depending on the settings you make to the control register, the current destination address will remain the same or will be incremented or decremented.

Channel 0/1 Current Transfer Count Register (GDMA_CTCNT0, GDMA_CTCNT1)

The Current transfer count register indicates the number of transfer being performed.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CTCNT0	0xFFF0.4018	R	Channel 0 Current Transfer Count Register	0x0000.0000
GDMA_CTCNT1	0xFFF0.4038	R	Channel 1 Current Transfer Count Register	0x0000.0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURENT_TFR_CNT [23:16]							
15	14	13	12	11	10	9	8
CURRENT_TFR_CNT [15:8]							
7	6	5	4	3	2	1	0
CURRENT_TFR_CNT [7:0]							

CURRENT_TFR_CNT [23:0]: Current Transfer Count

6.8 USB Host Controller

The **Universal Serial Bus (USB)** is a low-cost, low-to-middle speed peripheral interface standard intended for modem, printer, scanner, PDA, keyboard, mouse, and other devices that do not require a high-bandwidth parallel interface. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and a peripheral device. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

It allows user to setup a flexible, plug-and-play networks of USB devices. And in the USB network, there is only one USB host, but there can be many USB devices and USB hubs.

The Features of the USB Host Controller:

- USB 1.1 compatible
- Open Host Controller Interface (OHCI) 1.1 compatible.
- Supports both low-speed (1.5 Mbps) and full-speed (12Mbps) USB devices.
- Built-in DMA for real-time data transfer
- Option for on-chip USB transceiver or external USB transceiver

6.8.1 USB Host Controller Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
OpenHCI Registers				
HcRevision	0xFFF0.5000	R	Host Controller Revision Register	0x0000.0010
HcControl	0xFFF0.5004	R/W	Host Controller Control Register	0x0000.0000
HcCommandStatus	0xFFF0.5008	R/W	Host Controller Command Status Register	0x0000.0000
HcInterruptStatus	0xFFF0.500C	R/W	Host Controller Interrupt Status Register	0x0000.0000
HcInterruptEnable	0xFFF0.5010	R/W	Host Controller Interrupt Enable Register	0x0000.0000
HclnterruptDisable	0xFFF0.5014	R/W	Host Controller Interrupt Disable Register	0x0000.0000
HcHCCA	0xFFF0.5018	R/W	Host Controller Communication Area Register	0x0000.0000
HcPeriodCurrentED	0xFFF0.501C	R/W	Host Controller Period Current ED Register	0x0000.0000
HcControlHeadED	0xFFF0.5020	R/W	Host Controller Control Head ED Register	0x0000.0000
HcControlCurrentED	0xFFF0.5024	R/W	Host Controller Control Current ED Register	0x0000.0000
HcBulkHeadED	0xFFF0.5028	R/W	Host Controller Bulk Head ED Register	0x0000.0000
HcBulkCurrentED	0xFFF0.502C	R/W	Host Controller Bulk Current ED Register	0x0000.0000
HcDoneHead	0xFFF0.5030	R/W	Host Controller Done Head Register	0x0000.0000
HcFmInterval	0xFFF0.5034	R/W	Host Controller Frame Interval Register	0x0000.2EDF
HcFrameRemaining	0xFFF0.5038	R	Host Controller Frame Remaining Register	0x0000.0000
HcFmNumber	0xFFF0.503C	R	Host Controller Frame Number Register	0x0000.0000
HcPeriodicStart	0xFFF0.5040	R/W	Host Controller Periodic Start Register	0x0000.0000
HcLSThreshold	0xFFF0.5044	R/W	Host Controller Low Speed Threshold Register	0x0000.0628
HcRhDescriptorA	0xFFF0.5048	R/W	Host Controller Root Hub Descriptor A Register	0x0100.0002
HcRhDescriptorB	0xFFF0.504C	R/W	Host Controller Root Hub Descriptor B Register	0x0000.0000
HcRhStatus	0xFFF0.5050	R/W	Host Controller Root Hub Status Register	0x0000.0000
HcRhPortStatus [1]	0xFFF0.5054	R/W	Host Controller Root Hub Port Status [1]	0x0000.0000
HcRhPortStatus [2]	0xFFF0.5058	R/W	Host Controller Root Hub Port Status [2]	0x0000.0000

Host Controller Revision Register (HcRevision)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcRevision	0xFFF0.5000	R	Host Controller Revision Register	0x0000.0010

Register: *HcRevision*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	10h	R	**Revision** Indicates the Open HCI Specification revision number implemented by the Hardware. Host Controller supports 1.1 specification. (X.Y = XYh)
31-8	0h	-	Reserved. Read/Write 0's

Host Controller Control Register (HcControl)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcControl	0xFFF0.5004	R/W	Host Controller Control Register	0x0000.0000

Register: *HcControl*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
1-0	00b	R/W	**ControlBulkServiceRatio** Specifies the number of Control Endpoints serviced for every Bulk Endpoint. Encoding is N-1 where N is the number of Control Endpoints (i.e. '00' = 1 Control Endpoint; '11' = 3 Control Endpoints)
2	0b	R/W	**PeriodicListEnable** When set, this bit enables processing of the Periodic (interrupt and isochronous) list. The Host Controller checks this bit prior to attempting any periodic transfers in a frame.
3	0b	R/W	**IsochronousEnable** When clear, this bit disables the Isochronous List when the Periodic List is enabled (so Interrupt EDs may be serviced). While processing the Periodic List, the Host Controller will check this bit when it finds an isochronous ED.
4	0b	R/W	**ControlListEnable** When set this bit enables processing of the Control list.
5	0b	R/W	**BulkListEnable** When set this bit enables processing of the Bulk list.

Continued.

Register: *HcControl*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-6	00b	R/W	**HostControllerFunctionalState** This field sets the Host Controller state. The Controller may force a state change from USBSUSPEND to USBRESUME after detecting resume signaling from a downstream port. States are: 00: USBRESET 01: USBRESUME 10: USBOPERATIONAL 11: USBSUSPEND
8	0b	R/W	**InterruptRouting** This bit is used for interrupt routing: 0: Interrupts routed to normal interrupt mechanism (INT). 1: Interrupts routed to SMI.
9	0b	R	**RemoteWakeupConnected** This bit indicated whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hard-coded to '0.'
10	0b	R/W	**RemoteWakeupConnectedEnable** If a remote wakeup signal is supported, this bit enables that operation. Since there is no remote wakeup signal supported, this bit is ignored.
31-11	0h	-	Reserved. Read/Write 0's

Host Controller Command Status Register (HcCommandStatus)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcCommandStatus	0xFFF0.5008	R/W	Host Controller Command Status Register	0x0000.0000

Register: *HcCommandStatus*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**HostControllerReset** This bit is set to initiate the software reset. This bit is cleared by the Host Controller, upon completed of the reset operation.
1	0b	R/W	**ControlListFilled** Set to indicate there is an active ED on the Control List. It may be set by either software or the Host Controller and cleared by the Host Controller each time it begins processing the head of the Control List.
2	0b	R/W	**BulkListFilled** Set to indicate there is an active ED on the Bulk List. The bit may be set by either software or the Host Controller and cleared by the Host Controller each time it begins processing the head of the Bulk List.
3	0b	R/W	**OwnershipChangeRequest** When set by software, this bit sets the **OwnershipChange** field in *HcInterruptStatus*. The bit is cleared by software.
15-4	0h	-	Reserved. Read/Write 0's
17-16	00b		**ScheduleOverrunCount** This field is increment every time the **SchedulingOverrun** bit in *HcInterruptStatus* is set. The count wraps from '11' to '00.'
31-18	0h	-	Reserved. Read/Write 0's

Host Controller Interrupt Status Register (HcInterruptStatus)

All bits are set by hardware and cleared by software.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcInterruptStatus	0xFFF0.500C	R/W	Host Controller Interrupt Status Register	0x0000.0000

Register: *HcInterruptStatus*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrun** Set when the List Processor determines a Schedule Overrun has occurred.
1	0b	R/W	**WritebackDoneHead** Set after the Host Controller has written *HcDoneHead* to *HccaDoneHead*.
2	0b	R/W	**StartOfFrame** Set when the Frame Management block signals a 'Start of Frame' event.
3	0b	R/W	**ResumeDetected** Set when Host Controller detects resume signaling on a downstream port.
4	0b	R	**UnrecoverableError** This event is not implemented and is hard-coded to '0.' Writes are ignored.
5	0b	R/W	**FrameNumberOverflow** Set when bit 15 of **FrameNumber** changes value.
6	0b	R/W	**RootHubStatusChange** This bit is set when the content of *HcRhStatus* or the content of any *HcRhPortStatus* register has changed.
29-7	0h	-	Reserved. Read/Write 0's
30	0b	R/W	**OwnershipChange** This bit is set when the **OwnershipChangeRequest** bit of *HcCommandStatus* is set.
31	0h	-	Reserved. Read/Write 0's

Host Controller Interrupt Enable Register (HcInterruptEnable)

Writing a '1' to a bit in this register sets the corresponding bit, while writing a '0' leaves the bit unchanged.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcInterruptEnable	0xFFF0.5010	R/W	Host Controller Interrupt Enable Register	0x0000.0000

Register: *HcInterruptEnable*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrunEnable** 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun.
1	0b	R/W	**WritebackDoneHeadEnable** 0: Ignore 1: Enable interrupt generation due to Write-back Done Head.
2	0b	R/W	**StartOfFrameEnable** 0: Ignore 1: Enable interrupt generation due to Start of Frame.
3	0b	R/W	**ResumeDetectedEnable** 0: Ignore 1: Enable interrupt generation due to Resume Detected.
4	0b	R/W	**UnrecoverableErrorEnable** This event is not implemented. All writes to this bit are ignored.
5	0b	R/W	**FrameNumberOverflowEnable** 0: Ignore 1: Enable interrupt generation due to Frame Number Overflow.
6	0b	R/W	**RootHubStatusChangeEnable** 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change.
29-7	0h	-	Reserved. Read/Write 0's
30	0b	R/W	**OwnershipChangeEnable** 0: Ignore 1: Enable interrupt generation due to Ownership Change.
31	0b	R/W	**MasterInterruptEnable** This bit is a global interrupt enable. A write of '1' allows interrupts to be enabled via the specific enable bits listed above.

Host Controller Interrupt Disable Register (HcInterruptDisable)

Writing a ‘1’ to a bit in this register clears the corresponding bit, while writing a ‘0’ to a bit leaves the bit nchanged.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcInterrputDisable	0xFFF0.5014	R/W	Host Controller Interrupt Disable Register	0x0000.0000

Register: *HcInterruptStatus*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
0	0b	R/W	**SchedulingOverrunEnable** 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun.
1	0b	R/W	**WritebackDoneHeadEnable** 0: Ignore 1: Disable interrupt generation due to Write-back Done Head.
2	0b	R/W	**StartOfFrameEnable** 0: Ignore 1: Disable interrupt generation due to Start of Frame.
3	0b	R/W	**ResumeDetectedEnable** 0: Ignore 1: Disable interrupt generation due to Resume Detected.
4	0b	R/W	**UnrecoverableErrorEnable** This event is not implemented. All writes to this bit will be ignored.
5	0b	R/W	**FrameNumberOverflowEnable** 0: Ignore 1: Disable interrupt generation due to Frame Number Overflow.
6	0b	R/W	**RootHubStatusChangeEnable** 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change.
29-7	0h	-	Reserved. Read/Write 0's
30	0b	R/W	**OwnershipChangeEnable** 0: Ignore 1: Disable interrupt generation due to Ownership Change.
31	0b	R/W	**MasterInterruptEnable** Global interrupt disable. A write of ‘1’ disables all interrupts.

Host Controller Communication Area Register (HcHCCA)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcHCCA	0xFFF0.5018	R/W	Host Controller Communication Area Register	0x0000.0000

Register: *HcHCCA*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
31-8	0h	R/W	**HCCA** Pointer to HCCA base address.

Host Controller Period Current ED Register (HcPeriodCurrentED)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcPeriodCurrentED	0xFFF0.501C	R/W	Host Controller Period Current ED Register	0x0000.0000

Register: *HcPeriodCurrentED*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**PeriodCurrentED** Pointer to the current Periodic List ED.

Host Controller Control Head ED Register (HcControlHeadED)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcControlHeadED	0xFFF0.5020	R/W	Host Controller Control Head ED Register	0x0000.0000

Register: *HcControlHeadED*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**ControlHeadED** Pointer to the Control List Head ED.

Host Controller Control Current ED Register (HcControlCurrentED)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcControlCurrentED	0xFFF0.5024	R/W	Host Controller Control Current ED Register	0x0000.0000

Register: *HcControlCurrentED*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**ControlCurrentED** Pointer to the current Control List ED.

Host Controller Bulk Head ED Register (HcBulkHeadED)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcBulkHeadED	0xFFF0.5028	R/W	Host Controller Bulk Head ED Register	0x0000.0000

Register: *HcBulkHeadED*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**BulkHeadED** Pointer to the Bulk List Head ED.

Host Controller Bulk Current ED Register (HcBulkCurrentED)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcBulkCurrentED	0xFFF0.502C	R/W	Host Controller Bulk Current ED Register	0x0000.0000

Register: *HcBulkCurrentED*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**BulkCurrentED** Pointer to the current Bulk List ED.

Host Controller Done Head Register (HcDoneHead)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcDoneHead	0xFFF0.5030	R/W	Host Controller Done Head Register	0x0000.0000

Register: *HcDoneHead*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
3-0	0h	-	Reserved. Read/Write 0's
31-4	0h	R/W	**DoneHead** Pointer to the current Done List Head ED.

Host Controller Frame Interval Register (HcFmInterval)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcFmInterval	0xFFF0.5034	R/W	Host Controller Frame Interval Register	0x0000.2EDF

Register: *HcFmInterval*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
13-0	2EDFh	R/W	**FrameInterval** This field specifies the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.
15-14	0h	-	Reserved. Read/Write 0's
30-16			**FSLargestDataPacket** This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame.
31			**FrameIntervalToggle** This bit is toggled by HCD when it loads a new value into **FrameInterval**.

Host Controller Frame Remaining Register (HcFrameRemaining)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcFrameRemaining	0xFFF0.5038	R	Host Controller Frame Remaining Register	0x0000.0000

Register: *HcFrameRemaining*			
BITS	**RESET**	**R/W+**	**DESCRIPTION**
13-0	0b	R	**FrameRemaining** When the Host Controller is in the USBOPERATIONAL state, this 14-bit field decrements each 12 MHz clock period. When the count reaches 0, (end of frame) the counter reloads with **FrameInterval**. In addition, the counter loads when the Host Controller transitions into USBOPERATIONAL.
30-14	0h	-	Reserved. Read/Write 0's
31	0b	R	**FrameRemainingToggle** Loaded with **FrameIntervalToggle** when **FrameRemaining** is loaded.

Host Controller Frame Number Register (HcFmNumber)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcFmNumber	0xFFF0.503C	R	Host Controller Frame Number Register	0x0000.0000

Register: *HcFmNumber*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
15-0	0b	R	**FrameNumber** This 16-bit incrementing counter field is incremented coincident with the loading of **FrameRemaining**. The count rolls over from 'FFFFh' to '0h.'
31-16	0h	-	Reserved. Read/Write 0's

Host Controller Periodic Start Register (HcPeriodicStart)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcPeriodicStart	0xFFF0.5040	R/W	Host Controller Periodic Start Register	0x0000.0000

Register: *HcPeriodicStart*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
13-0	0b	R/W	**PeriodicStart** This field contains a value used by the List Processor to determine where in a frame the Periodic List processing must begin.
31-14	0h	-	Reserved. Read/Write 0's

Host Controller Low Speed Threshold Register (HcLSThreshold)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcLSThreshold	0xFFF0.5044	R/W	Host Controller Low Speed Threshold Register	0x0000.0628

Register: *HcLSThreshold*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
11-0	628h	R/W	**LSThreshold** This field contains a value used by the Frame Management block to determine whether or not a low speed transaction can be started in the current frame.
31-12	0h	-	Reserved. Read/Write 0's

Host Controller Root Hub Descriptor A Register (HcRhDescriptorA)

This register is only reset by a power-on reset. It is written during system initialization to configure the Root Hub. This bit should not be written during normal operation.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
HcRhDescriptorA	0xFFF0.5048	R/W	Host Controller Root Hub Descriptor A Register	0x0100.0002

Register: *HcRhDescriptorA*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-0	02h	R	**NumberDownstreamPorts** table of none-4 supports two downstream ports.
8	0	R/W	**PowerSwitchingMode** Global power switching mode implemented in HYDRA-2. This bit is only valid when **NoPowerSwitching** is cleared. This bit should be written '0'. 0 = Global Switching 1 = Individual Switching
9	0	R/W	**NoPowerSwitching** Global power switching implemented in HYDRA-2. This bit should be written to support the external system port power switching implementation. 0 = Ports are power switched. 1 = Ports are always powered on.
10	0	R	**DeviceType** table of none-4is not a compound device.
11	0	R/W	**OverCurrentProtectionMode** Global over-current reporting implemented in HYDRA-2. This bit should be written 0 and is only valid when **NoOverCurrentProtection** is cleared. 0 = Global Over-Current 1 = Individual Over-Current
12	0	R/W	**NoOverCurrentProtection** Global over-current reporting implemented in HYDRA-2. This bit should be written to support the external system port over-current implementation. 0 = Over-current status is reported 1 = Over-current status is not reported
23-13	0h	-	Reserved. Read/Write 0's
31-24	01h	R/W	**PowerOnToPowerGoodTime** This field value is represented as the number of 2 ms intervals, which ensuring that the power switching is effective within 2 ms. Only bits [25:24] are implemented as R/W. The remaining bits are read only as '0'. It is not expected that these bits be written to anything other than 1h, but limited adjustment is provided. This field should be written to support system implementation. This field should always be written to a non-zero value.

Host Controller Root Hub Descriptor B Register (HcRhDescriptorB)

This register is only reset by a power-on reset. It is written during system initialization to configure the Root Hub. These bits should not be written during normal operation.

Register	Address	R/W	Description	Reset Value
HcRhDescriptorB	0xFFF0.504C	R/W	Host Controller Root Hub Descriptor B Register	0x0000.0000

Register: *HcRhDescriptorB*			
Bits	**Reset**	**R/W**	**Description**
15-0	0000h	R/W	**DeviceRemoveable** table of none-4 ports default to removable devices. 0 = Device not removable 1 = Device removable Port Bit relationship 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15 Unimplemented ports are reserved, read/write '0'.
31-16	0000h	R/W	**PortPowerControlMask** Global-power switching. This field is only valid if **NoPowerSwitching** is cleared and **PowerSwitchingMode** is set (individual port switching). When set, the port only responds to individual port power switching commands (**Set/ClearPortPower**). When cleared, the port only responds to global power switching commands (**Set/ClearGlobalPower**). 0 = Device not removable 1 = Global-power mask Port Bit relationship - Unimplemented ports are reserved, read/write '0'. 0 : Reserved 1 : Port 1 2 : Port 2 ... 15 : Port 15

Host Controller Root Hub Status Register (HcRhStatus)

This register is reset by the USBRESET state.

Register	Address	R/W	Description	Reset Value
HcRhStatus	0xFFF0.5050	R/W	Host Controller Root Hub Status Register	0x0000.0000

Register: *HcRhStatus*			
Bits	**Reset**	**R/W**	**Description**
0	0	R/W	(Read) **LocalPowerStatus** Not Supported. Always read '0'. (Write) **ClearGlobalPower** Writing a '1' issues a **ClearGlobalPower** command to the ports. Writing a '0' has no effect.
1	-	R	**OverCurrentIndicator** This bit reflects the state of the OVRCUR pin. This field is only valid if **NoOverCurrentProtection** and **OverCurrentProtectionMode** are cleared. 0 = No over-current condition 1 = Over-current condition
14-2	0h	-	Reserved. Read/Write 0's
15	0	R/W	(Read) **DeviceRemoteWakeupEnable** This bit enables ports' **ConnectStatusChange** as a remote wakeup event. 0 = disabled 1 = enabled (Write) **SetRemoteWakeupEnable** Writing a '1' sets **DeviceRemoteWakeupEnable**. Writing a '0' has no effect.
16	0	R/W	(Read) **LocalPowerStatusChange** Not supported. Always read '0'. (Write) **SetGlobalPower** Write a '1' issues a **SetGlobalPower** command to the ports. Writing a '0' has no effect.
17	0	R/W	**OverCurrentIndicatorChange** This bit is set when **OverCurrentIndicator** changes. Writing a '1' clears this bit. Writing a '0' has no effect.
30-18	0h	-	Reserved. Read/Write 0's
31	0	W	(Write) **ClearRemoteWakeupEnable** Writing a '1' to this bit clears **DeviceRemoteWakeupEnable**. Writing a '1' has no effect.

Host Controller Root Hub Port Status (HcRhPortStatus [1:2])

This register is reset by the USBRESET state.

Register	Address	R/W	Description	Reset Value
HcRhPortStatus [1]	0xFFF0.5054	R/W	Host Controller Root Hub Port Status [1]	0x0000.0000
HcRhPortStatus [2]	0xFFF0.5058	R/W	Host Controller Root Hub Port Status [2]	0x0000.0000

Register: *HcRhPortStatus[1:2]*			
Bits	**Reset**	**R/W**	**Description**
0	0	R/W	(Read) **CurrentConnectStatus** 0 = No device connected. 1 = Device connected. NOTE: If **DeviceRemoveable** is set (not removable) this bit is always '1'. (Write) **ClearPortEnable** Writing '1' a clears **PortEnableStatus**. Writing a '0' has no effect.
1	0	R/W	(Read) **PortEnableStatus** 0 = Port disabled. 1 = Port enabled. (Write) **SetPortEnable** Writing a '1' sets **PortEnableStatus**. Writing a '0' has no effect.
2	0	R/W	(Read) **PortSuspendStatus** 0 = Port is not suspended 1 = Port is selectively suspended (Write) **SetPortSuspend** Writing a '1' sets **PortSuspendStatus**. Writing a '0' has no effect.
3	0	R/W	(Read) **PortOverCurrentIndicator** table of none-2 supports global over-current reporting. This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if **NoOverCurrentProtection** is cleared and **OverCurrentProtectionMode** is set. 0 = No over-current condition 1 = Over-current condition (Write) **ClearPortSuspend** Writing a '1' initiates the selective resume sequence for the port. Writing a '0' has no effect.
4	0	R/W	(Read) **PortResetStatus** 0 = Port reset signal is not active. 1 = Port reset signal is active. (Write) **SetPortReset** Writing a '1' sets **PortResetStatus**. Writing a '0' has no effect.

Continued.

Register: *HcRhPortStatus[1:2]*			
BITS	**RESET**	**R/W**	**DESCRIPTION**
7-5	0h	-	Reserved. Read/Write 0's
8	0	R/W	(Read) **PortPowerStatus** This bit reflects the power state of the port regardless of the power switching mode. 0 = Port power is off. 1 = Port power is on. Note: If **NoPowerSwitching** is set, this bit is always read as '1'. (Write) **SetPortPower** Writing a '1' sets **PortPowerStatus**. Writing a '0' has no effect.
9	0	R/W	(Read) **LowSpeedDeviceAttached** This bit defines the speed (and bud idle) of the attached device. It is only valid when **CurrentConnectStatus** is set. 0 = Full Speed device 1 = Low Speed device (Write) **ClearPortPower** Writing a '1' clears **PortPowerStatus**. Writing a '0' has no effect
15-10	0h	-	Reserved. Read/Write 0's
16	0	R/W	**ConnectStatusChange** This bit indicates a connect or disconnect event has been detected. Writing a '1' clears this bit. Writing a '0' has no effect. 0 = No connect/disconnect event. 1 = Hardware detection of connect/disconnect event. Note: If DeviceRemoveable is set, this bit resets to '1'.
17	0	R/W	**PortEnableStatusChange** This bit indicates that the port has been disabled due to a hardware event (cleared **PortEnableStatus**). 0 = Port has not been disabled. 1 = PortEnableStatus has been cleared.
18	0	R/W	**PortSuspendStatusChange** This bit indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed. 1 = Port resume is complete.
19	0	R/W	**PortOverCurrentIndicatorChange** This bit is set when **OverCurrentIndicator** changes. Writing a '1' clears this bit. Writing a '0' has no effect.
20	0	R/W	**PortResetStatusChange** This bit indicates that the port reset signal has completed. 0 = Port reset is not complete. 1 = Port reset is complete.
31-21	0h	-	Reserved. Read/Write 0's

6.9 UART Controller

The **Universal Asynchronous Receiver/Transmitter (UART)** performs a serial-to-parallel conversion on data characters received from the peripheral such as MODEM, and a parallel-to-serial conversion on data characters received from the CPU.

There are five types of interrupts, i.e., **line status interrupt, transmitter FIFO empty interrupt, receiver threshold level reaching interrupt, time out interrupt, and MODEM status interrupt.** One 16-byte transmitter FIFO **(TX_FIFO)** and one 16-byte (plus 3-bit of error data per byte) receiver FIFO **(RX_FIFO)** has been built in to reduce the number of interrupts presented to the CPU. The CPU can completely read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt) found. The UART includes a programmable baud rate generator that is capable of dividing crystal clock input by divisors to produce the clock that transmitter and receiver needed. The equation is

BaudOut = crystal clock / 16 * [Divisor + 2].

The Features of the UART:

- Transmitter and receiver are buffered with a 16-byte FIFO each to reduce the number of interrupts.
- Full set of MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  - -- 5-, 6-, 7-, or 8-bit character
  - -- Even, odd, or no-parity bit generation and detection
  - -- 1-, 1&1/2, or 2-stop bit generation
  - -- Baud rate generation
- Break generation and detection
- False start bit detection
- Parity, overrun, and framing error detection
- Full prioritized interrupt system controls

6.9.1 UART Control Registers Map

R: read only, **W**: write only, **R/W**: both read and write, **C**: Only value 0 can be written

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
RBR	0xFFF8.0000	R	Receive Buffer Register (DLAB = 0)	Undefined
THR	0xFFF8.0000	W	Transmit Holding Register (DLAB = 0)	Undefined
IER	0xFFF8.0004	R/W	Interrupt Enable Register (DLAB = 0)	0x0000.0000
DLL	0xFFF8.0000	R/W	Divisor Latch Register (LS) (DLAB = 1)	0x0000.0000
DLM	0xFFF8.0004	R/W	Divisor Latch Register (MS) (DLAB = 1)	0x0000.0000
IIR	0xFFF8.0008	R	Interrupt Identification Register	0x8181.8181
FCR	0xFFF8.0008	W	FIFO Control Register	Undefined
LCR	0xFFF8.000C	R/W	Line Control Register	0x0000.0000
MCR	0xFFF8.0010	R/W	Modem Control Register	0x0000.0000
LSR	0xFFF8.0014	R	Line Status Register	0x6060.6060
MSR	0xFFF8.0018	R	MODEM Status Register	0x0000.0000
TOR	0xFFF8.001C	R/W	Time Out Register	0x0000.0000

Receive Buffer Register (RBR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
RBR	0xFFF8.0000	R	Receive Buffer Register (DLAB = 0)	Undefined

7	6	5	4	3	2	1	0
8-bit Received Data							

8-bit Received Data [7:0]

By reading this register, the UART will return an 8-bit data received from SIN pin (LSB first).

Transmit Holding Register (THR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
THR	0xFFF8.0000	W	Transmit Holding Register (DLAB = 0)	Undefined

7	6	5	4	3	2	1	0
8-bit Transmitted Data							

8-bit Transmitted Data [7:0]

By writing to this register, the UART will send out an 8-bit data through the SOUT pin (LSB first).

Interrupt Enable Register (IER)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
IER	0xFFF8.0004	R/W	Interrupt Enable Register (DLAB = 0)	0x0000.0000

7	6	5	4	3	2	1	0
RESERVED			nDBGACK_EN	**MSIE**	**RLSIE**	**THREIE**	**RDAIE**

nDBGACK_EN [4]: ICE debug mode acknowledge enable

0 = When DBGACK is high, the UART receiver time-out clock will be held

1 = No matter what DBGACK is high or not, the UART receiver timer-out clock will not be held

MSIE [3]: MODEM Status Interrupt (Irpt_MOS) Enable

0 = Mask off Irpt_MOS

1 = Enable Irpt_MOS

RLSIE [2]: Receive Line Status Interrupt (Irpt_RLS) Enable

0 = Mask off Irpt_RLS

1 = Enable Irpt_RLS

THREIE [1]: Transmit Holding Register Empty Interrupt (Irpt_THRE) Enable

0 = Mask off Irpt_THRE

1 = Enable Irpt_THRE

RDAIE [0]: Receive **D**ata **A**vailable **I**nterrupt **(Irpt_RDA) E**nable and Time-out Interrupt **(Irpt_TOUT)** Enable

0 = Mask off Irpt_RDA and Irpt_TOUT

1 = Enable Irpt_RDA and Irpt_TOUT

Divider Latch (Low Byte) Register (DLL)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DLL	0xFFF8.0000	R/W	Divisor Latch Register (LS) (DLAB = 1)	0x0000.0000

7	6	5	4	3	2	1	0
Baud Rate Divider (Low Byte)							

Baud Rate Divisor (Low Byte) [7:0]

The low byte of the baud rate divider

Divisor Latch (High Byte) Register (DLM)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DLM	0xFFF8.0004	R/W	Divisor Latch Register (MS) (DLAB = 1)	0x0000.0000

7	6	5	4	3	2	1	0
Baud Rate Divider (High Byte)							

Baud Rate Divisor (High Byte) [7:0]

The high byte of the baud rate divider

This 16-bit divider {DLM, DLL} is used to determine the baud rate as follows

Baud Rate = Crystal Clock / {16 * [Divisor + 2]}

Note: This definition is different from 16550

Interrupt Identification Register (IIR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
IIR	0xFFF8.0008	R	Interrupt Identification Register	0x8181.8181

7	6	5	4	3	2	1	0
FMES	RFTLS		DMS	IID			NIP

FMES [7]: FIFO Mode Enable Status

This bit indicates whether the FIFO mode is enabled or not. Since the FIFO mode is always enable, this bit always shows the logical 1 when CPU is reading this register.

RFTLS [6:5]: RX FIFO Threshold Level Status

These bits show the current setting of receiver FIFO threshold level (RTHO). The meaning of RTHO is defined in the following FCR description.

DMS [4]: DMA Mode Select

The DMA function is not implemented in this version. When reading IIR, the DMS is always returned 0.

IID [3:1]: Interrupt Identification

The IID together with NIP indicates the current interrupt request from UART.

NIP [0]: No Interrupt Pending

There is no pending interrupt.

Table 6.9.1 Interrupt Control Functions

IIR [3:0]	PRIORITY	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
- - - 1	--	None	None	--
0110	Highest	Receiver Line Status (Irpt_RLS)	Overrun error, parity error, framing error, or break interrupt	Reading the LSR
0100	Second	Received Data Available (Irpt_RDA)	Receiver FIFO threshold level is reached	Receiver FIFO drops below the threshold level
1100	Second	Receiver FIFO Time-out (Irpt_TOUT)	Receiver FIFO is non-empty and no activities are occurred in the receiver FIFO during the TOR defined time duration	Reading the RBR
0010	Third	Transmitter Holing Register Empty (Irpt_THRE)	Transmitter holding register empty	Reading the IIR (if source of interrupt is Irpt_THRE) or writing into the THR
0000	Fourth	MODEM Status (Irpt_MOS)	The CTS, DSR, or DCD bits are changing state or the RI bit is changing from high to low.	Reading the MSR

Note: These definitions of bit 7, bit 6, bit 5, bit 4 are different from the 16550.

FIFO Control Register (FCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
FCR	0xFFF8.0008	W	FIFO Control Register	Undefined

7	6	5	4	3	2	1	0
RFITL		RESERVED		DMS	TFR	RFR	FME

RFITL [7:6]: RX FIFO Interrupt (Irpt_RDA) Trigger Level

RFITL [7:6]	IRPT_RDA TRIGGER LEVEL (BYTES)
00	01
01	04
10	08
11	14

DMS [3]: DMA Mode Select

The DMA function is not implemented in this version.

TFR [2]: TX FIFO Reset

Setting this bit will generate an OSC cycle reset pulse to reset TX FIFO. The TX FIFO becomes empty (TX pointer is reset to 0) after such reset. This bit is returned to 0 automatically after the reset pulse is generated.

RFR [1]: RX FIFO Reset

Setting this bit will generate an OSC cycle reset pulse to reset RX FIFO. The RX FIFO becomes empty (RX pointer is reset to 0) after such reset. This bit is returned to 0 automatically after the reset pulse is generated.

FME [0]: FIFO Mode Enable

Because UART is always operating in the FIFO mode, writing this bit has no effect while reading always gets logical one. This bit must be 1 when other FCR bits are written to; otherwise, they will not be programmed.

Line Control Register (LCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
LCR	0xFFF8.000C	R/W	Line Control Register	0x0000.0000

7	6	5	4	3	2	1	0
DLAB	BCB	SPE	EPE	PBE	NSB	WLS	

DLAB [7]: Divider Latch Access Bit

0 = It is used to access RBR, THR or IER.

1 = It is used to access Divisor Latch Registers {DLL, DLM}.

BCB [6]: Break Control Bit

When this bit is set to logic 1, the serial data output (SOUT) is forced to the Spacing State (logic 0). This bit acts only on SOUT and has no effect on the transmitter logic.

SPE [5]: Stick Parity Enable

0 = Disable stick parity

1 = Parity bit is transmitted and checked as a logic 1 if bit 4 is 0 (odd parity), or as a logic 0 if bit 4 is 1 (even parity). This bit has effect only when bit 3 (parity bit enable) is set.

EPE [4]: Even Parity Enable

0 = Odd number of logic 1's are transmitted or checked in the data word and parity bits.

1 = Even number of logic 1's are transmitted or checked in the data word and parity bits.

This bit has effect only when bit 3 (parity bit enable) is set.

PBE [3]: Parity Bit Enable

0 = Parity bit is not generated (transmit data) or checked (receive data) during transfer.

1 = Parity bit is generated or checked between the "last data word bit" and "stop bit" of the serial data.

NSB [2]: Number of "STOP bit"

0 = One " STOP bit" is generated in the transmitted data

1 = One and a half " STOP bit" is generated in the transmitted data when 5-bit word length is selected;

Two " STOP bit" is generated when 6-, 7- and 8-bit word length is selected.

WLS [1:0]: Word Length Select

WLS[1:0]	Character length
00	5 bits
01	6 bits
10	7 bits
11	8 bits

Modem Control Register (MCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MCR	0xFFF8.0010	R/W	Modem Control Register	0x0000.0000

7	6	5	4	3	2	1	0
RESERVED			**LBME**	**OUT2#**	**OUT1#**	**RTS#**	**DTR#**

LBME [4]: Loop-back Mode Enable

0 = Disable

1 = When the loop-back mode is enabled, the following signals are connected internally:

SOUT connected to SIN and SOUT pin fixed at logic 1

DTR# connected to DSR# and DTR# pin fixed at logic 1

RTS# connected to CTS# and RTS# pin fixed at logic 1

OUT1# connected to RI# and OUT1# pin fixed at logic 1

OUT2# connected to DCD# and OUT2# pin fixed logic 1

OUT2#[3]: Complement version of OUT2# (user-designated output) signal

OUT1#[2]: Complement version of OUT1# (user-designated output) signal

RTS#[1]: Complement version of RTS# (Request-To-Send) signal

DTR#[0]: Complement version of DTR# (Data-Terminal-Ready) signal

Writing 0x00 to MCR, the DTR#, RTS#, nOUT1# and OUT2# bit are set to logic 1's;

Writing 0x0f to MCR, the DTR#, RTS#, nOUT1# and OUT2# bit are reset to logic 0's.

Line Status Control Register (LSR)

Register	Address	R/W	Description	Reset Value
LSR	0xFFF8.0014	R	Line Status Register	0x6060.6060

7	6	5	4	3	2	1	0
ERR_RX	**TE**	**THRE**	**BII**	**FEI**	**PEI**	**OEI**	**RFDR**

ERR_RX [7]: RX FIFO Error

0 = RX FIFO works normally

1 = There is at least one parity error (PE), framing error (FE), or break indication (BI) in the FIFO. ERR_RX is cleared when CPU reads the LSR and if there are no subsequent errors in the RX FIFO.

TE [6]: Transmitter Empty

0 = Either Transmitter Holding Register (**THR** - TX FIFO) or Transmitter Shift Register (**TSR**) are not empty.

1 = Both THR and TSR are empty.

THRE [5]: Transmitter Holding Register Empty

0 = THRE is not empty.

1 = THRE is empty.

THRE is set when the last data word of TX FIFO is transferred to Transmitter Shift Register (TSR). The CPU resets this bit when the THR (or TX FIFO) is loaded. This bit also causes the UART to issue an interrupt (Irpt_THRE) to the CPU when IER [1]=1.

BII [4]: Break Interrupt Indicator

This bit is set to a logic 1 whenever the received data input is held in the "spacing state" (logic 0) for longer than a full word transmission time (that is, the total time of "start bit" + data bits + parity + stop bits) and is reset whenever the CPU reads the contents of the LSR**.**

FEI [3]: Framing Error Indicator

This bit is set to logic 1 whenever the received character does not have a valid "stop bit" (that is, the stop bit following the last data bit or parity bit is detected as a logic 0), and is reset whenever the CPU reads the contents of the LSR**.**

PEI [2]: Parity Error Indicator

This bit is set to logic 1 whenever the received character does not have a valid "parity bit", and is reset whenever the CPU reads the contents of the LSR**.**

OEI [1]: Overrun Error Indicator

An overrun error will occur only after the RX FIFO is full and the next character has been completely received in the shift register. The character in the shift register is overwritten, but it is not transferred to the RX FIFO. OE is indicated to the CPU as soon as it happens and is reset whenever the CPU reads the contents of the LSR.

RFDR [0]: RX FIFO Data Ready

0 = RX FIFO is empty

1 = RX FIFO contains at least 1 received data word.

LSR [4:2] (BII, FEI, PEI) are revealed to the CPU when its associated character is at the top of the RX FIFO. These three error indicators are reset whenever the CPU reads the contents of the LSR.

LSR [4:1] (BII, FEI, PEI, OEI) are the error conditions that produce a "receiver line status interrupt" (Irpt_RLS) when IER [2]=1. Reading LSR clears Irpt_RLS. Writing LSR is a null operation (not suggested).

Modem Status Register (MSR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MSR	0xFFF8.0018	R	MODEM Status Register	0x0000.0000

7	6	5	4	3	2	1	0
DCD#	**RI#**	**DSR#**	**CTS#**	**DDCD**	**TERI**	**DDSR**	**DCTS**

DCD#[7]: **Complement version of Data Carrier Detect (nDCD#) input**

RI#[6]: **Complement version of ring indicator (RI#) input**

DSR#[5]: **Complement version of data set ready (DSR#) input**

CTS#[4]: **Complement version of clear to send (CTS#) input**

DDCD [3]: **DCD# State Change**

This bit is set whenever DCD# input has changed state, and it will be reset if the CPU reads the MSR.

TERI [2]: Tailing Edge of RI#

This bit is set whenever RI# input has changed from high to low, and it will be reset if the CPU reads the MSR.

DDSR [1]: DSR# State Change

This bit is set whenever DSR# input has changed state, and it will be reset if the CPU reads the MSR.

DCTS [0]: CTS# State Change

This bit is set whenever CTS# input has changed state, and it will be reset if the CPU reads the MSR.

Whenever any of MSR [3:0] is set to logic 1, a Modem Status Interrupt is generated if IER[3]=1. Writing MSR is a null operation (not suggested).

Time Out Register (TOR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
TOR	0xFFF8.001C	R/W	Time Out Register	0x0000.0000

7	6	5	4	3	2	1	0
TOIE	TOIC						

TOIE [7]: Time Out Interrupt Enable

The feature of receiver time out interrupt is enabled only when TOR [7] = IER[0] = 1.

TOIC [6:0]: Time Out Interrupt Comparator

The time out counter resets and starts counting (the counting clock = baud rate) whenever the RX FIFO receives a new data word. Once the content of time out counter (TOUT_CNT) is equal to that of time out interrupt comparator (TOIC), a receiver time out interrupt (Irpt_TOUT) is generated if TOR [7] = IER [0] = 1. A new incoming data word or RX FIFO empty clears Irpt_TOUT.

6.10 TIMER Controller

6.10.1 General Timer Controller

The timer module has two channels, TIMER0 and TIMER1, which allow you to easily implement a counting scheme for use. The timer can perform functions like frequency measurement, event counting, interval measurement, pulse generation, delay timing, and so on. The timer possesses features such as adjustable resolution, programmable counting period, and detailed information. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

The Features of the TIMER Controller：

- Two programmable 24-bit timers with 8-bit pre-scalar
- One programmable 24-bit Watch-Dog timer
- Independent clock source for each channel
- One-short mode, period mode or toggle mode operation
- Maximum uninterrupted time = (1 / 15 MHz) * (255) * (2^24 - 1), if TCLK = 15 MHz

6.10.2 Watch Dog Timer

The purpose of watchdog timer is to perform a system restart after the software running into a problem. This prevents system from hanging for an indefinite period of time. It is a free running timer with programmable time-out intervals. When the specified time internal expires, a system reset can be generated. If the watchdog timer reset function is enabled and the watchdog timer is not being reset before timing out, then the watchdog rest is activated after 512 WDT clocks. Setting WTE in the register WTCR enables the watchdog timer.

The WTR should be set before making use of watchdog timer. This ensures that the watchdog timer restarts from a know state. The watchdog timer will start counting and time-out after a specified period of time. The time-out interval is selected by two bits, WTIS1 and WTIS0. The WTR is self-clearing, i.e., after setting it, the hardware will automatically reset it. When time-out occurs, the watchdog timer interrupt flag is set. The watchdog timer waits for an additional 512 clocks before issuing a reset signal, if the WTRE is set. The reset signal will last for two clocks long and the WTRF will be set. When used as a simple timer, the interrupt and reset functions are disabled. The watchdog timer will set the WTIF each time a time-out occurs. The WTIF can be polled to check the status, and software can restart the timer by setting the WTR.

6.10.3 Timer Control Registers Map

R: read only, **W**: write only, **R/W**: both read and write, **C**: Only value 0 can be written

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
TCR0	0xFFF8.1000	R/W	Timer Control Register 0	0x0000.0005
TCR1	0xFFF8.1004	R/W	Timer Control Register 1	0x0000.0005
TICR0	0xFFF8.1008	R/W	Timer Initial Control Register 0	0x0000.00FF
TICR1	0xFFF8.100C	R/W	Timer Initial Control Register 1	0x0000.00FF
TDR0	0xFFF8.1010	R	Timer Data Register 0	0x0000.00FF
TDR1	0xFFF8.1014	R	Timer Data Register 1	0x0000.00FF
TISR	0xFFF8.1018	R/C	Timer Interrupt Status Register	0x0000.0000
WTCR	0xFFF8.101C	R/W	Watchdog Timer Control Register	0x0000.0000

Timer Control Register 0 (TCR0)

Timer Control Register 1 (TCR1)

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
TCR0	0xFFF8.1000	R/W	Timer Control Register 0	0x0000.0005
TCR1	0xFFF8.1004	R/W	Timer Control Register 1	0x0000.0005

31	30	29	28	27	26	25	24
nDBGACK_EN	**CE**	**IE**	**MODE**		RESERVED		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRESCALE							

nDBGACK_EN [31]: ICE debug mode acknowledge enable

0 = When DBGACK is high, the timer clock will be held

1 = No matter what DBGACK is high or not, the timer clock will not be held

CE [30]: Counter Enable

0 = Stops counting

1 = Starts counting

IE [29]: Interrupt Enable

0 = Disables timer interrupt

1 = Enables timer interrupt. If timer interrupt is enabled, the timer asserts its interrupt signal when the associated counter decrements to zero.

MODE [28:27]: Timer Operating Mode

MODE [28:27]	TIMER OPERATING MODE
00	The timer is operating in the one-shot mode. The associated interrupt signal is generated once (if IE is enabled) and CE is automatically cleared then.
01	The timer is operating in the periodic mode. The associated interrupt signal is generated periodically (if IE is enabled).
10	The timer is operating in the toggle mode. The associated interrupt signal is changing back and forth (if IE is enabled) with 50% duty cycle.
11	Reserved for further use

PRESCALE [7:0]

Clock input is divided by PRESCALE + 1 before it is fed to the counter (here PRESCALE is considered as a decimal number). If PRESCALE = 0, then there is no scaling.

Timer Initial Count Register 0 (TICR0)

Timer Initial Count Register 1 (TICR1)

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
TICR0	0xFFF8.1008	R/W	Timer Initial Control Register 0	0x0000.00FF
TICR1	0xFFF8.100C	R/W	Timer Initial Control Register 1	0x0000.00FF

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TIC [23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TIC [15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TIC [7:0]							

TIC [23:0]: Timer Initial Count

This is a 24-bit value representing the initial count. Timer will reload this value whenever the counter is decremented to zero.

Timer Data Register 0 (TDR0)

Timer Data Register 1 (TDR1)

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
TDR0	0xFFF8.1010	R	Timer Data Register 0	0x0000.00FF
TDR1	0xFFF8.1014	R	Timer Data Register 1	0x0000.00FF

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
TDR [23:16]							
15	14	13	12	11	10	9	8
TDR [15:8]							
7	6	5	4	3	2	1	0
TDR [7:0]							

TDR [23:0]: Timer Data Register

The current count is registered in this 24-bit value.

Timer Interrupt Status Register (TISR)

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
TISR	0xFFF8.1018	R/C	Timer Interrupt Status Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						TIF1	TIF0

TIF1 [1]: Timer Interrupt Flag 1

It indicates the interrupt status of the timer 1.

0 = It indicates that the timer 1 does not count down to zero yet. Software can reset this bit after the timer interrupt 1 had occurred.

1 = It indicates that the counter of timer 1 is decremented to zero; the timer interrupt 1 is generated if it was enabled.

TIF1 [0]: Timer Interrupt Flag 0

It indicates the interrupt status of the timer 0.

0 = It indicates that the timer 0 does not count down to zero yet. Software can reset this bit after the timer interrupt 0 had occurred.

1 = It indicates that the counter of timer 0 is decremented to zero; the timer interrupt 0 is generated if it was enabled.

Watchdog Timer Control Register (WTCR)

REGISTER	ADDRESS	R/W/C	DESCRIPTION	RESET VALUE
WTCR	0xFFF8.101C	R/W	Watchdog Timer Control Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						**nDBGACK_EN**	RESERVED
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WTE	**WTIE**	**WTIS**		**WTIF**	**WTRF**	**WTRE**	**WTR**

nDBGACK_EN [9]: ICE debug mode acknowledge enable

0 = When DBGACK is high, the timer clock will be held

1 = No matter what DBGACK is high or not, the timer clock will not be held

RESERVED **[8]:**

0 = Put the watchdog time in the normal operating mode

WTE [7]: Watchdog Timer Enable

0 = Disable the watchdog timer

1 = Enable the watchdog timer

WTIE [6]: Watchdog Timer Interrupt Enable

0 = Disable the watchdog timer interrupt

1 = Enable the watchdog timer interrupt

WTIS [5:4]: Watchdog **T**imer **I**nterval **S**elect

These two bits select the interval for the watchdog timer. No matter which interval is chosen, the reset time-out is always occurred 512 clocks later than the interrupt time-out.

WTIS [5:4]	INTERRUPT TIME-OUT	RESET TIME-OUT
00	2^{21} clocks	2^{21} + 512 clocks
01	2^{22} clocks	2^{22} + 512 clocks
10	2^{23} clocks	2^{23} + 512 clocks
11	2^{24} clocks	2^{24} + 512 clocks

WTIF [3]: Watchdog Timer Interrupt Flag

If the watchdog interrupt is enabled, then the hardware will set this bit to indicate that the watchdog interrupt has occurred. If the watchdog interrupt is not enabled, then this bit indicates that a time-out period has elapsed.

0 = Watchdog timer interrupt does not occur

1 = Watchdog timer interrupt occurs

WTRF [2]: Watchdog Timer Reset Flag

When the watchdog timer initiates a reset, the hardware will set this bit. This flag can be read by software to determine the source of reset. Software is responsible to clear it up manually. If **WTRE** is disabled, then the watchdog timer has no effect on this bit.

0 = Watchdog timer reset does not occur

1 = Watchdog timer reset occurs

WTRE [1]: Watchdog Timer Reset Enable

Setting this bit will enable the watchdog timer reset function.

0 = Disable watchdog timer reset function

1 = Enable watchdog timer reset function

WTR [0]: Watchdog Timer Reset

This bit brings the watchdog timer into a known state. It helps reset the watchdog timer before a time-out situation occurring. Failing to set **WTR** before time-out will initiates an interrupt if **WTIE** is set. If **WTRE** is set, a watchdog timer reset will occur 512 clocks after time-out. This bit is self-clearing.

1 = Reset the contents of the watchdog timer

0 = Do not reset the contents of the watchdog timer

6.11 Advanced Interrupt Controller (AIC)

An interrupt temporarily changes the sequence of program execution to react to a particular event such as power failure, watchdog timer timeout, transmit/receive request from Ethernet MAC Controller, and so on. The ARM7TDMI processor provides two modes of interrupt, the **Fast Interrupt (FIQ)** mode for critical session and the **Interrupt (IRQ)** mode for general purpose. The IRQ exception is occurred when the nIRQ input is asserted. Similarly, the FIQ exception is occurred when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F and I bits in the **current program status register (CPSR)**.

The W90N740 incorporates the **advanced interrupt controller (AIC)** that is capable of dealing with the interrupt requests from a total of 32 different sources. Currently, only 18 interrupt sources are defined. Each interrupt source is uniquely assigned to an interrupt channel. For example, the watchdog timer interrupt is assigned to channel 1 and the general-purpose direct-access memory access (GDMA) interrupt 0 to channel 17. The AIC implements a proprietary eight-level priority scheme that differentiates the available 18 interrupt sources into eight priority levels. Interrupt sources within the priority level 0 have the highest priority and the priority level 7 has the lowest. To work this scheme properly, you must specify a certain priority level to each interrupt source during power-on initialization; otherwise, the system shall behave unexpectedly. Within each priority level, interrupt source that is positioned in a lower channel has a higher priority. Interrupt source that is active, enabled, and positioned in the lowest channel within the priority level 0 is promoted to the FIQ. Interrupt sources within the priority levels other than 0 can petition for the IRQ. The IRQ can be preempted by the occurrence of the FIQ. Interrupt nesting is performed automatically by the AIC.

Though interrupt sources originated from the W90N740 itself are intrinsically high-level sensitive, the AIC can be configured as either low-level sensitive, high-level sensitive, negative-edge triggered, or positive-edge triggered to each interrupt source.

The Features of the AIC (advanced interrupt controller):

- 18 interrupt sources, including 4 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 4 external interrupt sources
- Programmable as either low-active or high-active for 4 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting
- Automatically clear the interrupt flag when the interrupt source is programmed to be edge-triggered

6.11.1 Interrupt Sources

The table as shown below lists all the interrupt sources originated from internal peripherals and external devices. Please be careful that interrupt channel 0 and all that beyond 18 are undefined in this implementation.

Table 6.11.1 W90N740 Interrupt Sources

CHANNEL	NAME	PRIORITY	MODE	SOURCE
		HIGHEST		
1	WDTINT		Positive Level	Watch Dog Timer Interrupt
2	nIRQ0		Programmable	External Interrupt 0
3	nIRQ1		Programmable	External Interrupt 1
4	nIRQ2		Programmable	External Interrupt 2
5	nIRQ3		Programmable	External Interrupt 3
6	UARTINT		Positive Level	UART Interrupt
7	TINT0		Positive Level	Timer Interrupt 0
8	TINT1		Positive Level	Timer Interrupt 1
9	USBINT0		Positive Level	USB Interrupt 0
10	USBINT1		Positive Level	USB Interrupt 1
11	Reserved		Reserved	Reserved
12	Reserved		Reserved	Reserved
13	EMCTXINT0		Positive Level	EMC TX Interrupt 0
14	EMCTXINT1		Positive Level	EMC TX Interrupt 1
15	EMCRXINT0		Positive Level	EMC RX Interrupt 0
16	EMCRXINT1		Positive Level	EMC RX Interrupt 1
17	GDMAINT0		Positive Level	GDMA Channel Interrupt 0
18	GDMAINT1		Positive Level	GDMA Channel Interrupt 1
19 ~ 31	-	Lowest	-	Reserved for further use

6.11.2 AIC Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_SCR1	0xFFF8.2004	R/W	Source Control Register 1	0x0000.0047
AIC_SCR2	0xFFF8.2008	R/W	Source Control Register 2	0x0000.0047
AIC_SCR3	0xFFF8.200C	R/W	Source Control Register 3	0x0000.0047
AIC_SCR4	0xFFF8.2010	R/W	Source Control Register 4	0x0000.0047
AIC_SCR5	0xFFF8.2014	R/W	Source Control Register 5	0x0000.0047
AIC_SCR6	0xFFF8.2018	R/W	Source Control Register 6	0x0000.0047
AIC_SCR7	0xFFF8.201C	R/W	Source Control Register 7	0x0000.0047
AIC_SCR8	0xFFF8.2020	R/W	Source Control Register 8	0x0000.0047
AIC_SCR9	0xFFF8.2024	R/W	Source Control Register 9	0x0000.0047
AIC_SCR10	0xFFF8.2028	R/W	Source Control Register 10	0x0000.0047
AIC_SCR11	0xFFF8.202C	R/W	Source Control Register 11	0x0000.0047
AIC_SCR12	0xFFF8.2030	R/W	Source Control Register 12	0x0000.0047
AIC_SCR13	0xFFF8.2034	R/W	Source Control Register 13	0x0000.0047
AIC_SCR14	0xFFF8.2038	R/W	Source Control Register 14	0x0000.0047
AIC_SCR15	0xFFF8.203C	R/W	Source Control Register 15	0x0000.0047
AIC_SCR16	0xFFF8.2040	R/W	Source Control Register 16	0x0000.0000
AIC_SCR17	0xFFF8.2044	R/W	Source Control Register 17	0x0000.0000
AIC_SCR18	0xFFF8.2048	R/W	Source Control Register 18	0x0000.0000
AIC_IRSR	0xFFF8.2100	R	Interrupt Raw Status Register	0x0000.0000
AIC_IASR	0xFFF8.2104	R	Interrupt Active Status Register	0x0000.0000
AIC_ISR	0xFFF8.2108	R	Interrupt Status Register	0x0000.0000
AIC_IPER	0xFFF8.210C	R	Interrupt Priority Encoding Register	0x0000.0000
AIC_ISNR	0xFFF8.2110	R	Interrupt Source Number Register	0x0000.0000
AIC_IMR	0xFFF8.2114	R	Interrupt Mask Register	0x0000.0000
AIC_OISR	0xFFF8.2118	R	Output Interrupt Status Register	0x0000.0000
AIC_MECR	0xFFF8.2120	W	Mask Enable Command Register	Undefined
AIC_MDCR	0xFFF8.2124	W	Mask Disable Command Register	Undefined
AIC_SSCR	0xFFF8.2128	W	Source Set Command Register	Undefined
AIC_SCCR	0xFFF8.212C	W	Source Clear Command Register	Undefined
AIC_EOSCR	0xFFF8.2130	W	End of Service Command Register	Undefined

AIC Source Control Registers (AIC_SCR1 ~ AIC_SCR18)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_SCR1	0xFFF8.2004	R/W	Source Control Register 1	0x0000.0047
AIC_SCR2	0xFFF8.2008	R/W	Source Control Register 2	0x0000.0047
• • •	• • •	• • •	• • •	• • •
AIC_SCR17	0xFFF8.2044	R/W	Source Control Register 17	0x0000.0047
AIC_SCR18	0xFFF8.2048	R/W	Source Control Register 18	0x0000.0047

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SRCTYPE			RESERVED		**PRIORITY**		

SRCTYPE[7:6]: Interrupt Source Type

Whether an interrupt source is considered active or not by the AIC is subject to the settings of this field.

SRCTYPE [7:6]		Interrupt Source Type
0	0	Low-level Sensitive
0	1	High-level Sensitive
1	0	Negative-edge Triggered
1	1	Positive-edge Triggered

PRIORITY [2:0]: Priority Level

Every interrupt source must be assigned a priority level during initiation. Among them, priority level 0 has the highest priority and priority level 7 the lowest. Interrupt sources with priority level 0 are promoted to FIQ. Interrupt sources with priority level other than 0 belong to IRQ. For interrupt sources of the same priority level, that located in the lower channel number has higher priority.

AIC Interrupt Raw Status Register (AIC_IRSR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_IRSR	0xFFF8.2100	R	Interrupt Raw Status Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					IRS18	IRS17	IRS16
15	14	13	12	11	10	9	8
IRS15	IRS14	IRS13	IRS12	IRS11	IRS10	IRS9	IRS8
7	6	5	4	3	2	1	0
IRS7	IRS6	IRS5	IRS4	IRS3	IRS2	IRS1	RESERVED

This register records the intrinsic state within each interrupt channel.

IRS*x*: Interrupt Status

Indicate the intrinsic status of the corresponding interrupt source

0 = Interrupt channel is in the voltage level 0

1 = Interrupt channel is in the voltage level 1

AIC Interrupt Active Status Register (AIC_IASR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_IASR	0xFFF8.2104	R	Interrupt Active Status Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					IAS18	IAS17	IAS16
15	14	13	12	11	10	9	8
IAS15	IAS14	IAS13	IAS12	IAS11	IAS10	IAS9	IAS8
7	6	5	4	3	2	1	0
IAS7	IAS6	IAS5	IAS4	IAS3	IAS2	IAS1	RESERVED

This register indicates the status of each interrupt channel in consideration of the interrupt source type as defined in the corresponding Source Control Register, but regardless of its mask setting.

IAS*x*: Interrupt Active Status

Indicate the status of the corresponding interrupt source

0 = Corresponding interrupt channel is inactive

1 = Corresponding interrupt channel is active

AIC Interrupt Status Register (AIC_ISR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_ISR	0xFFF8.2108	R	Interrupt Status Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					**IS18**	**IS17**	**IS16**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IS15	**IS14**	**IS13**	**IS12**	**IS11**	**IS10**	**IS9**	**IS8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IS7	**IS6**	**IS5**	**IS4**	**IS3**	**IS2**	**IS1**	RESERVED

This register identifies those interrupt channels whose are both active and enabled.

IS*x*: Interrupt Status

Indicates the status of corresponding interrupt channel

0 = Two possibilities:

(1) The corresponding interrupt channel is inactive no matter whether it is enabled or disabled;

(2) It is active but not enabled

1 = Corresponding interrupt channel is both active and enabled (can assert an interrupt)

AIC IRQ Priority Encoding Register (AIC_IPER)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_IPER	0xFFF8.210C	R	Interrupt Priority Encoding Register	0x0000.0000

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	**VECTOR**					0	0

When the AIC generates the interrupt, **VECTOR** represents the interrupt channel number that is active, enabled, and has the highest priority. If the representing interrupt channel possesses a priority level 0, then the interrupt asserted is FIQ; otherwise, it is IRQ. The value of **VECTOR** is copied to the register AIC_ISNR thereafter by the AIC. *This register was restored a value 0 after it was read by the interrupt handler*. This register can help indexing into a branch table to quickly jump to the corresponding interrupt service routine.

VECTOR [6:2]: Interrupt Vector

0 = no interrupt occurs

1 ~ 31 = representing the interrupt channel that is active, enabled, and having the highest priority

AIC Interrupt Source Number Register (AIC_ISNR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_ISNR	0xFFF8.2110	R	Interrupt Source Number Register	0x0000.0000

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	**IRQID**				

The purpose of this register is to record the interrupt channel number that is active, enabled, and has the highest priority.

IRQID [4:0]: IRQ Identification

Stands for the interrupt channel number

AIC Interrupt Mask Register (AIC_IMR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_IMR	0xFFF8.2114	R	Interrupt Mask Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					**IM18**	**IM17**	**IM16**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IM15	**IM14**	**IM13**	**IM12**	**IM11**	**IM10**	**IM9**	**IM8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IM7	**IM6**	**IM5**	**IM4**	**IM3**	**IM2**	**IM1**	RESERVED

IM*x*: Interrupt Mask

This bit determines whether the corresponding interrupt channel is enabled or disabled. Every interrupt channel can be active no matter whether it is enabled or disabled. If an interrupt channel is enabled, it does not definitely mean it is active. Every interrupt channel can be authorized by the AIC only when it is both active and enabled.

0 = Corresponding interrupt channel is disabled

1 = Corresponding interrupt channel is enabled

AIC Output Interrupt Status Register (AIC_OISR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_OISR	0xFFF8.2118	R	Output Interrupt Status Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						**IRQ**	**FIQ**

The AIC classifies the interrupt into FIQ and IRQ. This register indicates whether the asserted interrupt is FIQ or IRQ. If both IRQ and FIQ are equal to 0, it means there is no interrupt occurred.

IRQ [1]: Interrupt Request

0 = nIRQ line is inactive.

1 = nIRQ line is active.

FIQ [0]: Fast Interrupt Request

0 = nFIQ line is inactive.

1 = nFIQ line is active

AIC Mask Enable Command Register (AIC_MECR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_MECR	0xFFF8.2120	W	Mask Enable Command Register	Undefined

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					MEC18	MEC17	MEC16
15	14	13	12	11	10	9	8
MEC15	MEC14	MEC13	MEC12	MEC11	MEC10	MEC9	MEC8
7	6	5	4	3	2	1	0
MEC7	MEC6	MEC5	MEC4	MEC3	MEC2	MEC1	RESERVED

MEC*x*: Mask Enable Command

0 = No effect

1 = Enables the corresponding interrupt channel

AIC Mask Disable Command Register (AIC_MDCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_MDCR	0xFFF8.2124	W	Mask Disable Command Register	Undefined

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					MDC18	MDC17	MDC16
15	14	13	12	11	10	9	8
MDC15	MDC14	MDC13	MDC12	MDC11	MDC10	MDC9	MDC8
7	6	5	4	3	2	1	0
MDC7	MDC6	MDC5	MDC4	MDC3	MDC2	MDC1	RESERVED

MDC*x*: Mask Disable Command

0 = No effect

1 = Disables the corresponding interrupt channel

AIC Source Set Command Register (AIC_SSCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_SSCR	0xFFF8.2128	W	Source Set Command Register	Undefined

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					SSC18	SSC17	SSC16
15	14	13	12	11	10	9	8
SSC15	SSC14	SSC13	SSC12	SSC11	SSC10	SSC9	SSC8
7	6	5	4	3	2	1	0
SSC7	SSC7	SSC6	SSC4	SSC3	SSC2	SSC1	RESERVED

When the W90N740 is under debugging or verification, software can activate any interrupt channel by setting the corresponding bit in this register. This feature is useful in hardware verification or software debugging.

SSC*x*: Source Set Command

0 = No effect.

1 = Activates the corresponding interrupt channel

AIC Source Clear Command Register (AIC_SCCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_SCCR	0xFFF8.212C	W	Source Clear Command Register	Undefined

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					SCC18	SCC17	SCC16
15	14	13	12	11	10	9	8
SCC15	SCC14	SCC13	SCC12	SCC11	SCC10	SCC9	SCC8
7	6	5	4	3	2	1	0
SCC7	SCC7	SCC6	SCC4	SCC3	SCC2	SCC1	RESERVED

When the W90N740 is under debugging or verification, software can deactivate any interrupt channel by setting the corresponding bit in this register. This feature is useful in hardware verification or software debugging.

SCC*x*: Source Clear Command

0 = No effect.

1 = Deactivates the corresponding interrupt channels

AIC End of Service Command Register (AIC_EOSCR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_EOSCR	0xFFF8.2130	W	End of Service Command Register	Undefined

31	30	29	28	27	26	25	24
---	---	---	---	---	---	---	---
23	22	21	20	19	18	17	16
---	---	---	---	---	---	---	---
15	14	13	12	11	10	9	8
---	---	---	---	---	---	---	---
7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

This register is used by the interrupt service routine to indicate that it is completely served. Thus, the interrupt handler can write any value to this register to indicate the end of its interrupt service.

6.12 General-Purpose Input/Output Controller (GPIO)

The General-Purpose Input/Output (GPIO) module possesses 21 pins and serves multiple purposes.

The Features of the GPIO Controller:

- Programmable as an input or output pin
- Includes de-bouncer circuits on GPIO20, GPIO19, GPIO18, and GPIO17 which can be turned off if not requir

For example, GPIO20 ~ GPIO17 can be programmed as external interrupt input pins, GPIO16 ~ GPIO15 for external DMA function, GPIO14 ~ GPIO13 for TIMER tone output, GPIO12 as the watchdog timeout flag, GPIO11 ~ GPIO10 used for UART console monitor, GPIO9 ~ GPIO4 for modem. The table as shown below is a summary.

Table 6.12.1 GPIO Pin Assignment of Multi-Function

GPIO	GENERAL-PURPOSE I/O		MULTI-FUNCTION 1		MULTI-FUNCTION 2 (USB IO PORT)	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
GPIO20	GP20	IO	nIRQ3	I	-	-
GPIO19	GP19	IO	nIRQ2	I	-	-
GPIO18	GP18	IO	nIRQ1	I	OVRCUR	I
GPIO17	GP17	IO	nIRQ0	I	-	-
GPIO16	GP16	IO	NXDREQ3	I	-	-
GPIO15	GP15	IO	nXDACK	O	-	-
GPIO14	GP14	IO	TIMER1	O	SPEED	O
GPIO13	GP13	IO	TIMER0	O	STDBY	O
GPIO12	GP12	IO	nWDOG	O	PWRENX	O
GPIO11	GP11	IO	RxD	I	-	-
GPIO10	GP10	IO	TxD	O	-	-
GPIO9	GP9	IOU	nDSR	IU	nTOE	O
GPIO8	GP8	IOU	nDTR	O	FSE0	O
GPIO7	GP7	IOU	nCD	IU	VO	O
GPIO6	GP6	IOU	nCTS	IU	VM	IU
GPIO5	GP5	IOU	nRTS	O	VP	IU
GPIO4	GP4	IOU	nRI	IU	RCV	IU
GPIO3	GP3	IOU	NXDREQ2	IU	-	-
GPIO2	GP2	IOU	NXDREQ1	IU	-	-
GPIO1	GP1	IOU	NWTC	O	-	-
GPIO0	GP0	IOU	NRTC	O	-	-

Note: U means internal weak pull-up.

6.12.1 GPIO Controller Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_CFG	0xFFF8.3000	R/W	GPIO Configuration Register	0x0000.0000
GPIO_DIR	0xFFF8.3004	R/W	GPIO Direction Register	0x0000.0000
GPIO_DATAOUT	0xFFF8.3008	R/W	GPIO Data Output Register	0x0000.0000
GPIO_DATAIN	0xFFF8.300C	R	GPIO Data Input Register	Undefined
DEBNCE_CTRL	0xFFF8.3010	R/W	De-bounce Control Register	0x0000.0000

GPIO Configuration Register (GPIO_CFG)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_CFG	0xFFF8.3000	R/W	GPIO Configuration Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
		GPIOCFG20		GPIOCFG19		GPIOCFG18	
15	14	13	12	11	10	9	8
GPIOCFG17		GPIOCFG16_15		GPIOCFG14		GPIOCFG13	
7	6	5	4	3	2	1	0
GPIOCFG12		GPIOCFG11_10		GPIOCFG9_4		GPIOCFG3_0	

GPIOCFG20 [21:20]: Operating mode for GPIO20

GPIOCFG20	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO20	RESERVED	I	RESERVED		nIRQ3	I	GP20	IO

nIRQ3 is one of the external interrupt input pins.

GPIOCFG19 [19:18]: Operating mode for GPIO19

GPIOCFG19	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO19	RESERVED	I	RESERVED		nIRQ2	I	GP19	IO

nIRQ2 is one of the external interrupt input pins.

GPIOCFG18 [17:16]: Operating mode for GPIO18

GPIOCFG18	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO18	RESERVED	I	OVRCUR	I	nIRQ1	I	GP18	IO

OVRCUR is used as over current indicator if this field set to **10.**

nIRQ1 is one of the external interrupt input pins.

GPIOCFG17 [15:14]: Operating mode for GPIO17

GPIOCFG17	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO17	RESERVED		RESERVED		nIRQ0	I	GP17	IO

nIRQ0 is one of the external interrupt input pins.

GPIOCFG16_15 [13:12]: Operating mode for GPIO16 and GPIO15

GPIOCFG16_15	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO16	RESERVED	O	RESERVED		NXDREQ3	I	GP16	I/O
GPIO15	RESERVED	O	RESERVED		nXDACK	O	GP15	I/O

NXDREQ3 is the external DMA request signal pin.

nXDACK is the external DMA granted signal pin.

GPIOCFG14 [11:10]: Operating mode for GPIO14

GPIOCFG14	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO14	RESERVED	O	SPEED	O	TIMER1	O	GP14	IO

SPEED is a USB IO port, which controls the external USB transceiver speed mode.

TIMER1 is the tone output of TIMER1.

GPIOCFG13 [9:8]: Operating mode for GPIO13

GPIOCFG13	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO13	RESERVED	O	STDBY	O	TIMER0	O	GP13	IO

STDBY is a USB IO port, which controls the external USB transceiver power-down mode.

TIMER0 is the tone output of TIMER0.

GPIOCFG12 [7:6]: Operating mode for GPIO12

GPIOCFG12	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO12	RESERVED	IO	PWREN	IO	nWDOG	O	GP12	IO

nWDOG is the timeout output of Watch-Dog Timer.

GPIOCFG11_10 [5:4]: Operating mode for GPIO11 and GPIO10

GPIOCFG11_10	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO11	RESERVED	O	RESERVED		RxD	I	GP11	IO
GPIO10		O			TxD	O	GP10	IO

RxD and **TxD** are used for the UART console.

GPIOCFG9_4 [3:2]: Operating mode for GPIO9, GPIO8, GPIO7, GPIO6, GPIO5, and GPIO4

GPIOCFG9_4	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO9	RESERVED		nTOE	O	nDSR	IU	GP9	IOU
GPIO8			FSE0	O	nDTR	O	GP8	IOU
GPIO7			VO	O	nCD	IU	GP7	IOU
GPIO6			VM	IU	nCTS	IU	GP6	IOU
GPIO5			VP	IU	nRTS	O	GP5	IOU
GPIO4			RCV	IU	nRI	IU	GP4	IOU

nTOE, FSE0, VO, VM, VP, and RCV are the USB IO signal pins, which connected to the external USB transceiver to control the data in/out.

nDSR, nDTR, nCD, nCTS, nRTS and nRI are the UART modem signal pins.

GPIOCFG3_0 [1:0]: Operating mode for GPIO3, GPIO2, GPIO1, and GPIO0

GPIOCFG3_0	11		10		01		00	
	Name	Type	Name	Type	Name	Type	Name	Type
GPIO3	RESERVED		RESERVED		NXDREQ2	IU	GP3	I/O
GPIO2					NXDREQ1	IU	GP2	I/O
GPIO1					NWTC	O	GP1	I/O
GPIO0					NRTC	O	GP0	I/O

GPIO Direction Register (GPIO_DIR)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_DIR	0xFFF8.3004	R/W	GPIO Direction Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED			GPIOD20	GPIOD19	GPIOD18	GPIOD17	GPIOD16
15	14	13	12	11	10	9	8
GPIOD15	GPIOD14	GPIOD13	GPIOD12	GPIOD11	GPIOD10	GPIOD9	GPIOD8
7	6	5	4	3	2	1	0
GPIOD7	GPIOD6	GPIOD5	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOD0

GPIOD*x*: GPIOx direction

The GPIOD*x* is used to set the direction of GPIO*x* if it is used as a regular input/output pin (**GPx**).

0 = GPIO*x* is an input pin

1 = GPIO*x* is an output pin

GPIO Data Output Register (GPIO_DATAOUT)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_DATAOUT	0xFFF8.3008	R/W	GPIO Data Output Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED			GPIODO20	GPIODO19	GPIODO18	GPIODO17	GPIODO16
15	14	13	12	11	10	9	8
GPIODO15	GPIODO14	GPIODO13	GPIODO12	GPIODO11	GPIODO10	GPIODO9	GPIODO8
7	6	5	4	3	2	1	0
GPIODO7	GPIODO6	GPIODO5	GPIODO4	GPIODO3	GPIODO2	GPIODO1	GPIODO0

GPIODO*x*: GPIO output corresponding to bit *x*

If the GPIO*x* is used as a general-purpose output pin, then the corresponding GPIODO*x* specifies the value to output from this pin.

GPIO Data Input Register (GPIO_DATAIN)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_DATAIN	0xFFF8.3008	R	GPIO Data Input Register	Undefined

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED			GPIODI20	GPIODI19	GPIODI18	GPIODI17	GPIODI16
15	14	13	12	11	10	9	8
GPIODI15	GPIODI14	GPIODI13	GPIODI12	GPIODI11	GPIODI10	GPIODI9	GPIODI8
7	6	5	4	3	2	1	0
GPIODI7	GPIODI6	GPIODI5	GPIODI4	GPIODI3	GPIODI2	GPIODI1	GPIODI0

GPIODI*x*: GPIO status corresponding to bit *x*

The GPIODI*x* indicates the status of each GPIO pin regardless of its operation mode.

Debounce Control Register (DEBNCE_CTRL)

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
DEBNCE_CTRL	0xFFF8.3010	R/W	De-bounce Control Register	0x0000.0000

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	DBCLKSEL			DBE3	DBE2	DBE1	DBE0

DBCLKSEL [6:4]: De-bounce Clock Rate Selector

These three bits are used to select the clock rate for de-bouncer circuit. The relationship between the system clock HCLK and the de-bounce clock TCLK_BUN is as follows:

$$TCLK\_BUN = HCLK / 2^{DBCLKSEL}$$

DBE3 [3]: De-bouncer Circuit Enable for GPIO20

0 = De-bounce function is disabled

1 = De-bounce function is enabled

DBE2 [2]: De-bouncer Circuit Enable for GPIO19

0 = De-bounce function is disabled

1 = De-bounce function is enabled

DBE1 [1]: De-bouncer Circuit Enable for GPIO18

0 = De-bounce function is disabled

1 = De-bounce function is enabled

DBE0 [0]: De-bouncer Circuit Enable for GPIO17

0 = De-bounce function is disabled

1 = De-bounce function is enabled

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Ambient Temperature	0 °C ~ 70 °C
Storage Temperature	-40 °C ~ 125°C
Voltage on Any Pin	-0.5V ~ 6V
Power Supply Voltage (Core logic)	1.62V ~ 1.96V
Power Supply Voltage (IO Buffer)	3.0V ~ 3.6V
Injection Current (latch-up testing)	100 mA
Crystal Frequency	3 MHz ~ 30 MHz

7.2 DC Characteristics

(Normal test conditions: VDD33/USBVDD = 3.3V+/- 0.3V, VDD18/DVDD18/AVDD18 = 1.8V+/- 0.18V

T_A = 0 °C ~ 70 °C unless otherwise specified)

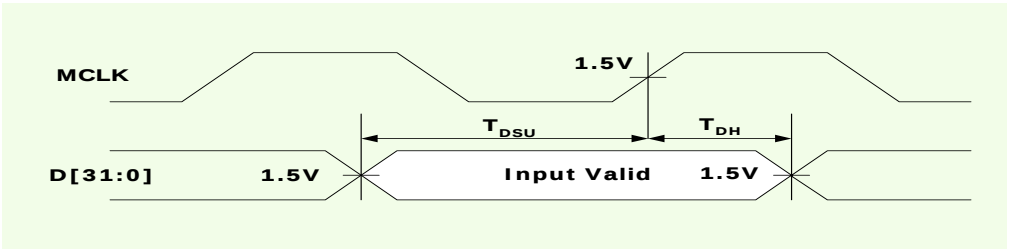
SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
VDD33/ USBVDD	Power Supply		3.00	3.60	V
VDD18/ DVDD18/ AVDD18	Power Supply		1.62	1.98	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	5.5	V
VT+	Schmitt Trigger positive-going threshold		1.47	1.5	V
VT-	Schmitt trigger negative-going threshold		0.89	0.95	V
V_{OL}	Output Low Voltage	Depend on driving		0.4	V
V_{OH}	Output High Voltage	Depend on driving	2.4		V
I_{CC1}	Supply Current (VDD33)	F_{cpu} = 80MHz		90	mA
I_{CC2}	Supply Current (VDD18)	F_{cpu} = 80MHz		40	mA
I_{IH}	Input High Current	V_{IN} = 2.4 V	-1	1	µA
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-1	1	µA
I_{IHP}	Input High Current (pull-up)	V_{IN} = 2.4 V	-15	-10	µA
I_{ILP}	Input Low Current (pull-up)	V_{IN} = 0.4 V	-55	-25	µA
I_{IHD}	Input High Current (pull-down)	V_{IN} = 2.4 V	25	60	µA
I_{ILD}	Input Low Current (pull-down)	V_{IN} = 0.4 V	5	10	µA

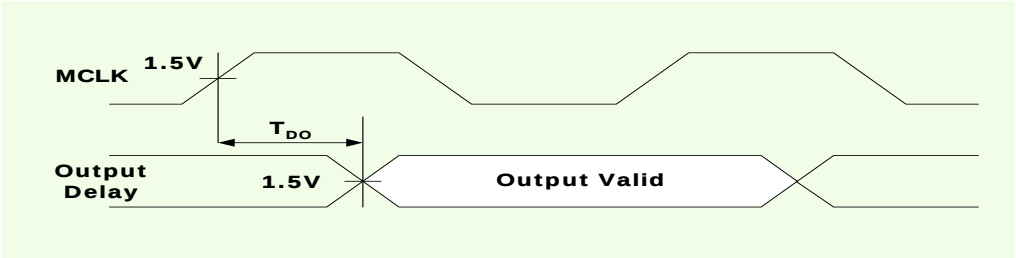
7.2.1 USB Transceiver DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DI}	DIFFERENTIAL INPUT SENSITIVITY	|DP – DM|	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	2.0	V
V_{OL}	Static Output Low Voltage	RL of 1.5 KΩ to 3.6 V		0.3	V
V_{OH}	Static Output High Voltage	RL of 15 KΩ to V_{SS}	2.8	3.6	V
V_{CRS}	Output Signal Crossover Voltage		1.3	2.0	V
Z_{DRV}	Driver Output Resistance	Steady state drive	28	43	Ω

7.3 AC Characteristics

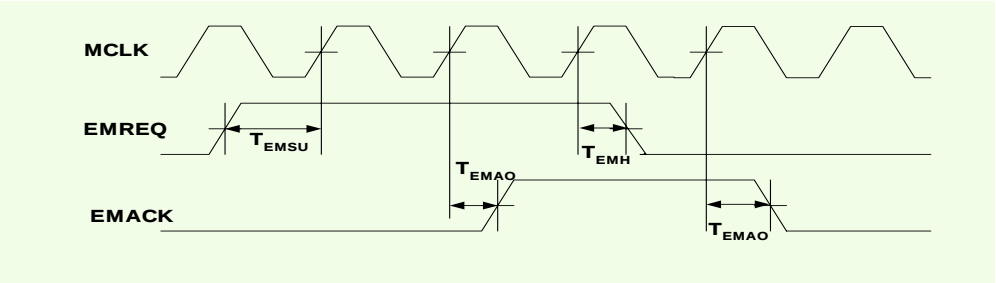
7.3.1 EBI/SDRAM Interface AC Characteristics





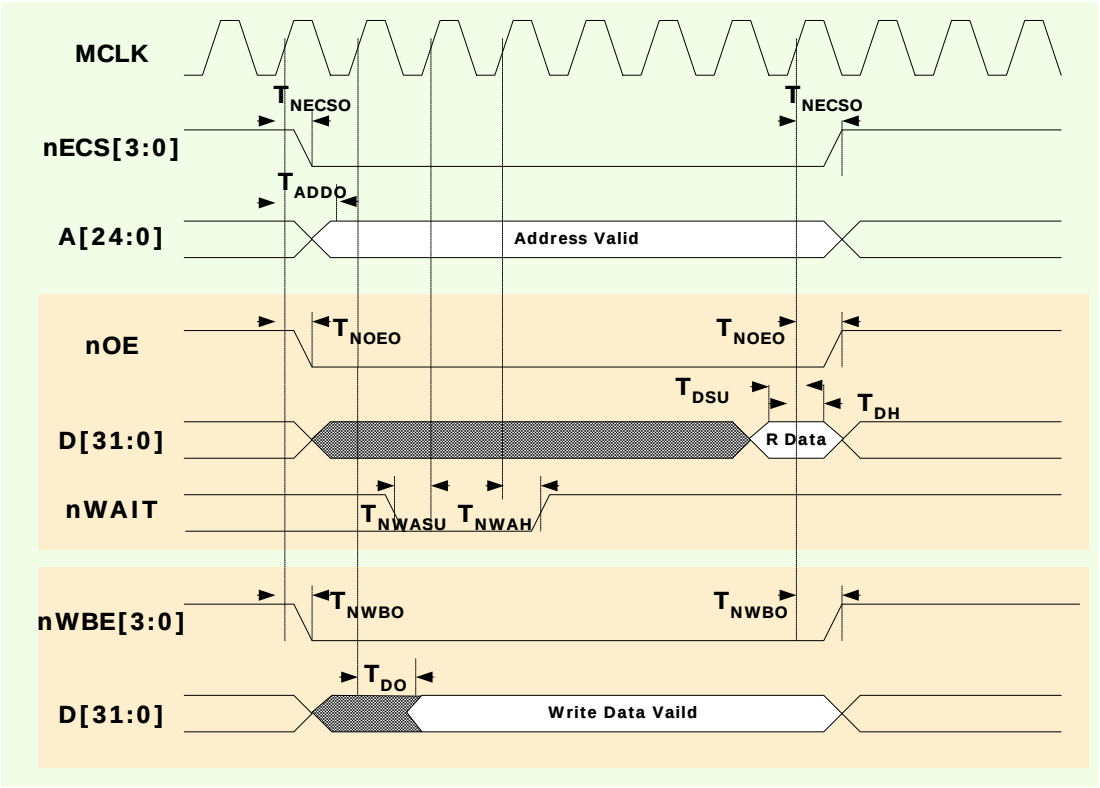
SYM.	PARAMETER	MIN.	MAX.	UNIT
T_{DSU}	D [31:0] Setup Time	2		nS
T_{DH}	D [31:0] Hold Time	3		nS
T_{DO}	D [31:0], A [24:0], nSCS [1:0], SDQM [3:0], CKE, nSWE, nSRAS, nSCAS	2	7	nS

7.3.2 EBI/External Master Interface AC Characteristics



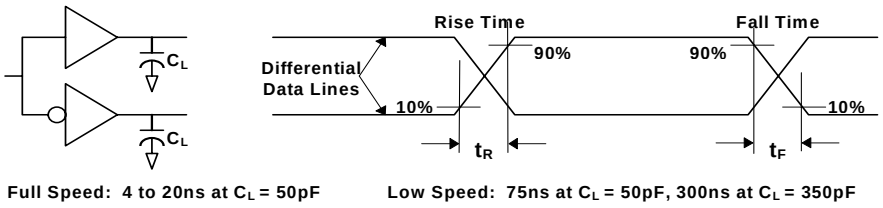
SYM.	DESCRIPTION	MIN.	MAX.	UNIT
T_{EMSU}	EMREQ Setup Time	2		nS
T_{EMH}	EMREQ Hold Time	3		nS
T_{EMAO}	EMACK Output Delay Time	4	7	nS

7.3.3 EBI/(ROM/SRAM/External I/O) AC Characteristics



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T_{ADDO}	Address Output Delay Time	2	7	nS
T_{NCSO}	ROM/SRAM/Flash or External I/O Chip Select Delay Time	2	7	nS
T_{NOEO}	ROM/SRAM or External I/O Bank Output Enable Delay	2	7	nS
T_{NWBO}	ROM/SRAM or External I/O Bank Write Byte Enable Delay	2	7	nS
T_{DH}	Read Data Hold Time	7		nS
T_{DSU}	Read Data Setup Time	0		nS
T_{DO}	Write Data Output Delay Time (SRAM or External I/O)	2	7	nS
T_{NWASU}	External Wait Setup Time	3		nS
T_{NWAH}	External Wait Hold Time	1		nS

7.3.4 USB Transceiver AC Characteristics



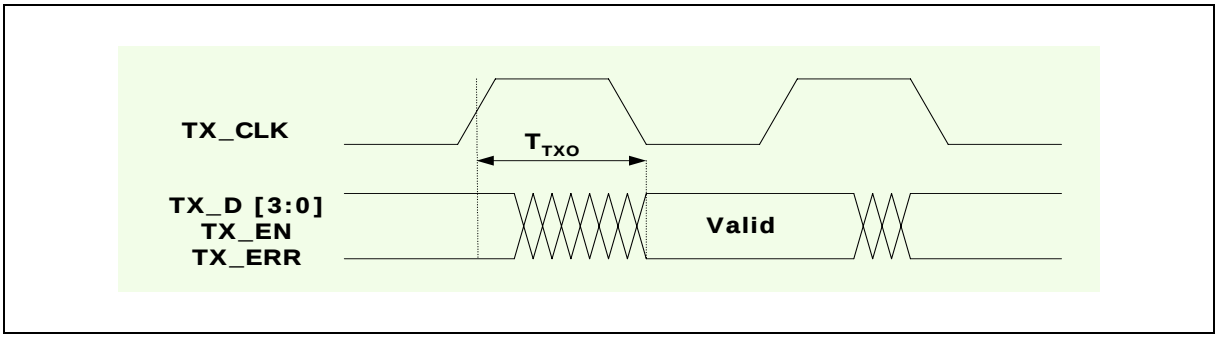
Data Signal Rise and Fall Time

USB Transceiver AC Characteristics

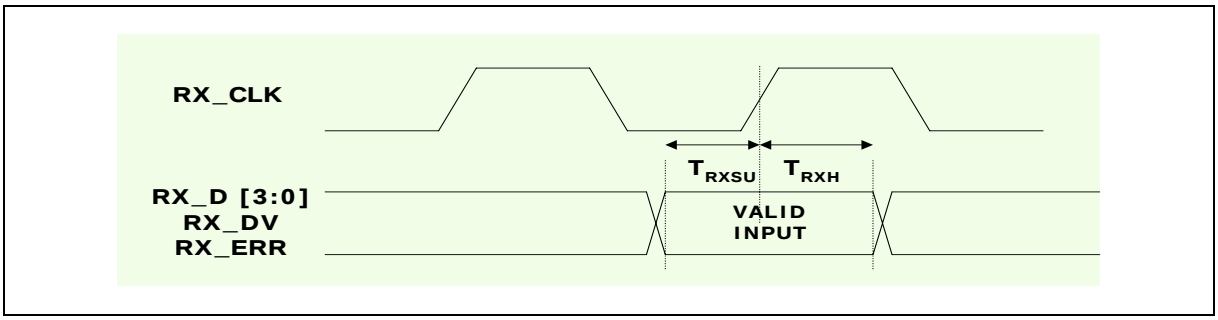
SYM.	DESCRIPTION	CONDITIONS	MIN.	MAX.	UNIT
T_R	Rise Time (Full Speed)	CL = 50 pF	4	20	nS
T_F	Fall Time (Full Speed	CL = 50 pF	4	20	nS
T_{RFM}	Rise/Fall Time Matching (Full Speed)		90	112	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ±0.25%)	11.97	12.03	Mbps

7.3.5 EMC MII AC Characteristics

The signal timing characteristics conforms to the guidelines specified in IEEE Std. 802.3.

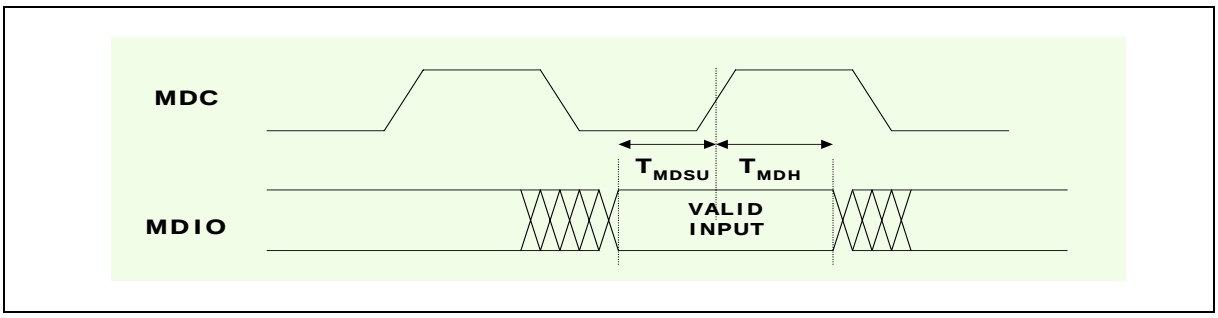


Transmit Signal Timing Relationships at MII

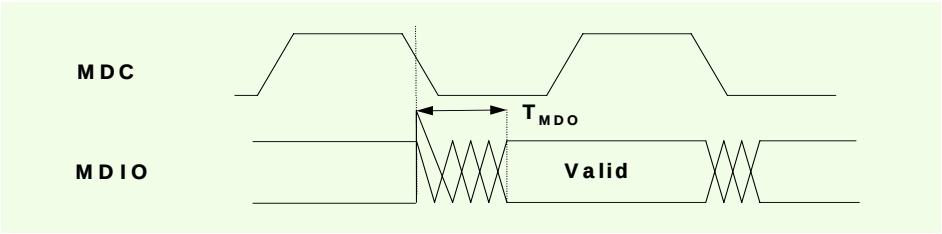


Receive Signal Timing Relationships at MII

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T_{TXO}	Transmit Output Delay Time	3	15	nS
T_{RXSU}	Receive Setup Time	5		nS
T_{RXH}	Receive Hold Time	5		nS



MDIO Read From PHY Timing

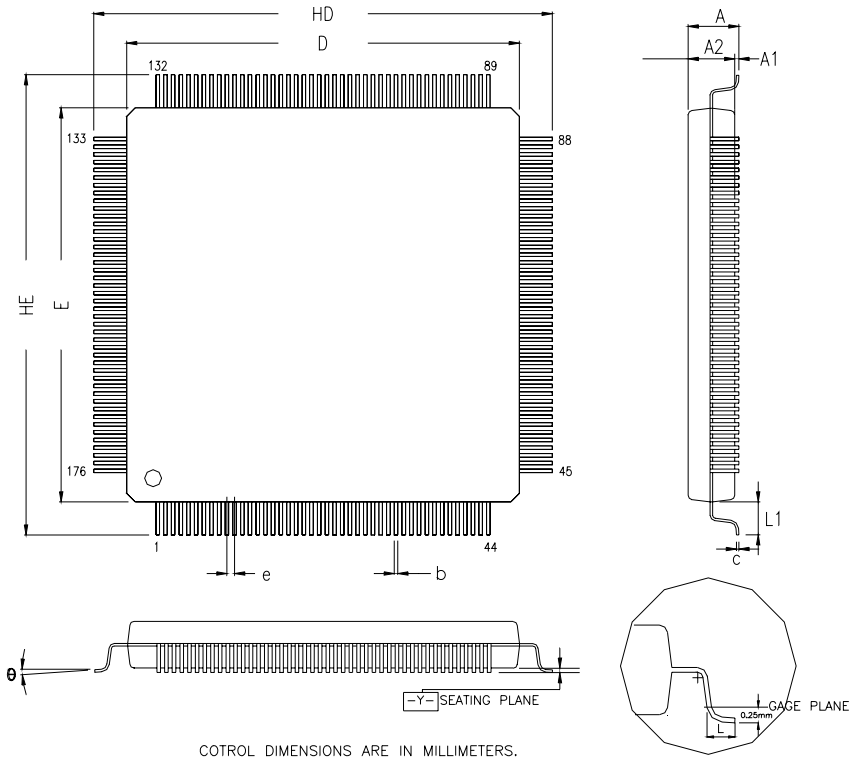


MDIO Write to PHY Timing

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T_{MDO}	MDIO Output Delay Time	0	5	nS
T_{MDSU}	MDIO Setup Time	5		nS
T_{MDH}	MDIO Hold Time	5		nS

8. PACKAGE DIMENSIONS

176-Pin LQFP (note that the value in inches may have some inaccuracy as it is translated from the value in millimeter)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	22.00 BSC.			0.866 BSC.		
D	20.00 BSC.			0.787 BSC.		
HE	22.00 BSC.			0.866 BSC.		
E	20.00 BSC.			0.787 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
c	0.09	—	0.20	0.004	—	0.008
Y	—	—	0.10	—	—	0.004

9. W90N740 REGISTERS MAPPING TABLE

R: read only, **W**: write only, **R/W**: both read and write, **C**: Only value 0 can be written

System Manager Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
PDID	0xFFF0.0000	R	Product Identifier Register	0xX090.0740
ARBCON	0xFFF0.0004	R/W	Arbitration Control Register	0x0000.0000
PLLCON	0xFFF0.0008	R/W	PLL Control Register	0x0000.2F01
CLKSEL	0xFFF0.000C	R/W	Clock Select Register	0x0000.3FX8

EBI Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
EBICON	0xFFF0.1000	R/W	EBI control register	0x0001.0000
ROMCON	0xFFF0.1004	R/W	ROM/FLASH control register	0x0000.0XFC
SDCONF0	0xFFF0.1008	R/W	SDRAM bank 0 configuration register	0x0000.0800
SDCONF1	0xFFF0.100C	R/W	SDRAM bank 1 configuration register	0x0000.0800
SDTIME0	0xFFF0.1010	R/W	SDRAM bank 0 timing control register	0x0000.0000
SDTIME1	0xFFF0.1014	R/W	SDRAM bank 1 timing control register	0x0000.0000
EXT0CON	0xFFF0.1018	R/W	External I/O 0 control register	0x0000.0000
EXT1CON	0xFFF0.101C	R/W	External I/O 1 control register	0x0000.0000
EXT2CON	0xFFF0.1020	R/W	External I/O 2 control register	0x0000.0000
EXT3CON	0xFFF0.1024	R/W	External I/O 3 control register	0x0000.0000
CKSKEW	0xFFF0.1F00	R/W	Clock skew control register	0xXXXX.0038

Cache Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAHCNF	0xFFF0.2000	R/W	Cache configuration register	0x0000.0000
CAHCON	0xFFF0.2004	R/W	Cache control register	0x0000.0000
CAHADR	0xFFF0.2008	R/W	Cache address register	0x0000.0000

EMC 0 Control registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAMCMR_0	0xFFF0.3000	R/W	CAM Command Register	0x0000.0000
CAMEN_0	0xFFF0.3004	R/W	CAM enable register	0x0000.0000
CAM1M_0	0xFFF0.3008	R/W	CAM1 Most Significant Word Register	0x0000.0000
CAM1L_0	0xFFF0.300C	R/W	CAM1 Least Significant Word Register	0x0000.0000
CAM2M_0	0xFFF0.3010	R/W	CAM2 Most Significant Word Register	0x0000.0000
CAM2L_0	0xFFF0.3014	R/W	CAM2 Least Significant Word Register	0x0000.0000
CAM3M_0	0xFFF0.3018	R/W	CAM3 Most Significant Word Register	0x0000.0000
CAM3L_0	0xFFF0.301C	R/W	CAM3 Least Significant Word Register	0x0000.0000
CAM4M_0	0xFFF0.3020	R/W	CAM4 Most Significant Word Register	0x0000.0000
CAM4L_0	0xFFF0.3024	R/W	CAM4 Least Significant Word Register	0x0000.0000
CAM5M_0	0xFFF0.3028	R/W	CAM5 Most Significant Word Register	0x0000.0000
CAM5L_0	0xFFF0.302C	R/W	CAM5 Least Significant Word Register	0x0000.0000
CAM6M_0	0xFFF0.3030	R/W	CAM6 Most Significant Word Register	0x0000.0000
CAM6L_0	0xFFF0.3034	R/W	CAM6 Least Significant Word Register	0x0000.0000
CAM7M_0	0xFFF0.3038	R/W	CAM7 Most Significant Word Register	0x0000.0000
CAM7L_0	0xFFF0.303C	R/W	CAM7 Least Significant Word Register	0x0000.0000
CAM8M_0	0xFFF0.3040	R/W	CAM8 Most Significant Word Register	0x0000.0000
CAM8L_0	0xFFF0.3044	R/W	CAM8 Least Significant Word Register	0x0000.0000
CAM9M_0	0xFFF0.3048	R/W	CAM9 Most Significant Word Register	0x0000.0000
CAM9L_0	0xFFF0.304C	R/W	CAM9 Least Significant Word Register	0x0000.0000
CAM10M_0	0xFFF0.3050	R/W	CAM10 Most Significant Word Register	0x0000.0000
CAM10L_0	0xFFF0.3054	R/W	CAM10 Least Significant Word Register	0x0000.0000
CAM11M_0	0xFFF0.3058	R/W	CAM11 Most Significant Word Register	0x0000.0000
CAM11L_0	0xFFF0.305C	R/W	CAM11 Least Significant Word Register	0x0000.0000
CAM12M_0	0xFFF0.3060	R/W	CAM12 Most Significant Word Register	0x0000.0000
CAM12L_0	0xFFF0.3064	R/W	CAM12 Least Significant Word Register	0x0000.0000
CAM13M_0	0xFFF0.3068	R/W	CAM13 Most Significant Word Register	0x0000.0000
CAM13L_0	0xFFF0.306C	R/W	CAM13 Least Significant Word Register	0x0000.0000
CAM14M_0	0xFFF0.3070	R/W	CAM14 Most Significant Word Register	0x0000.0000
CAM14L_0	0xFFF0.3074	R/W	CAM14 Least Significant Word Register	0x0000.0000

EMC 0 Control registers Map, continued

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAM15M_0	0xFFF0.3078	R/W	CAM15 Most Significant Word Register	0x0000.0000
CAM15L_0	0xFFF0.307C	R/W	CAM15 Least Significant Word Register	0x0000.0000
CAM16M_0	0xFFF0.3080	R/W	CAM16 Most Significant Word Register	0x0000.0000
CAM16L_0	0xFFF0.3084	R/W	CAM16 Least Significant Word Register	0x0000.0000
MAC REGISTERS				
MIEN_0	0xFFF0.3088	R/W	MAC Interrupt Enable Register	0x0000.0000
MCMDR_0	0xFFF0.308C	R/W	MAC Command Register	0x0000.0000
MIID_0	0xFFF0.3090	R/W	MII Management Data Register	0x0000.0000
MIIDA_0	0xFFF0.3094	R/W	MII Management Data Control and Address Register	0x0090.0000
MPCNT_0	0xFFF0.3098	R/W	Missed Packet counter register	0x0000.7FFF
DMA REGISTERS				
TXDLSA_0	0xFFF0.309C	R/W	Transmit Descriptor Link List Start Address register	0xFFFF.FFFC
RXDLSA_0	0xFFF0.30A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC
DMARFC_0	0xFFF0.30A4	R/W	DMA Receive Frame Control Register	0x0000.0800
TSDR_0	0xFFF0.30A8	W	Transmit Start Demand Register	Undefined
RSDR_0	0xFFF0.30AC	W	Receive Start Demand Register	Undefined
FIFOTHD_0	0xFFF0.30B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101

EMC 0 Status Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MAC REGISTERS				
MISTA_0	0xFFF0.30B4	R/W	MAC Interrupt Status Register	0x0000.0000
MGSTA_0	0xFFF0.30B8	R/W	MAC General Status Register	0x0000.0000
MRPC_0	0xFFF0.30BC	R	MAC Receive Pause count register	0x0000.0000
MRPCC_0	0xFFF0.30C0	R	MAC Receive Pause Current Count Register	0x0000.0000
MREPC_0	0xFFF0.30C4	R	MAC Remote pause count register	0x0000.0000
DMA REGISTERS				
DMARFS_0	0xFFF0.30C8	R/W	DMA Receive Frame Status Register	0x0000.0000
CTXDSA_0	0xFFF0.30CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000
CTXBSA_0	0xFFF0.30D0	R	Current Transmit Buffer Start Address Register	0x0000.0000
CRXDSA_0	0xFFF0.30D4	R	Current Receive Descriptor Start Address Register	0x0000.0000
CRXBSA_0	0xFFF0.30D8	R	Current Receive Buffer Start Address Register	0x0000.0000

EMC 1 Control Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAMCMR_1	0xFFF0.3800	R/W	CAM Command Register	0x0000.0000
CAMEN_1	0xFFF0.3804	R/W	CAM enable register	0x0000.0000
CAM1M_1	0xFFF0.3808	R/W	CAM1 Most Significant Word Register	0x0000.0000
CAM1L_1	0xFFF0.380C	R/W	CAM1 Least Significant Word Register	0x0000.0000
CAM2M_1	0xFFF0.3810	R/W	CAM2 Most Significant Word Register	0x0000.0000
CAM2L_1	0xFFF0.3814	R/W	CAM2 Least Significant Word Register	0x0000.0000
CAM3M_1	0xFFF0.3818	R/W	CAM3 Most Significant Word Register	0x0000.0000
CAM3L_1	0xFFF0.381C	R/W	CAM3 Least Significant Word Register	0x0000.0000
CAM4M_1	0xFFF0.3820	R/W	CAM4 Most Significant Word Register	0x0000.0000
CAM4L_1	0xFFF0.3824	R/W	CAM4 Least Significant Word Register	0x0000.0000
CAM5M_1	0xFFF0.3828	R/W	CAM5 Most Significant Word Register	0x0000.0000
CAM5L_1	0xFFF0.382C	R/W	CAM5 Least Significant Word Register	0x0000.0000
CAM6M_1	0xFFF0.3830	R/W	CAM6 Most Significant Word Register	0x0000.0000
CAM6L_1	0xFFF0.3834	R/W	CAM6 Least Significant Word Register	0x0000.0000
CAM7M_1	0xFFF0.3838	R/W	CAM7 Most Significant Word Register	0x0000.0000
CAM7L_1	0xFFF0.383C	R/W	CAM7 Least Significant Word Register	0x0000.0000
CAM8M_1	0xFFF0.3840	R/W	CAM8 Most Significant Word Register	0x0000.0000
CAM8L_1	0xFFF0.3844	R/W	CAM8 Least Significant Word Register	0x0000.0000
CAM9M_1	0xFFF0.3848	R/W	CAM9 Most Significant Word Register	0x0000.0000
CAM9L_1	0xFFF0.384C	R/W	CAM9 Least Significant Word Register	0x0000.0000
CAM10M_1	0xFFF0.3850	R/W	CAM10 Most Significant Word Register	0x0000.0000
CAM10L_1	0xFFF0.3854	R/W	CAM10 Least Significant Word Register	0x0000.0000
CAM11M_1	0xFFF0.3858	R/W	CAM11 Most Significant Word Register	0x0000.0000
CAM11L_1	0xFFF0.385C	R/W	CAM11 Least Significant Word Register	0x0000.0000
CAM12M_1	0xFFF0.3860	R/W	CAM12 Most Significant Word Register	0x0000.0000
CAM12L_1	0xFFF0.3864	R/W	CAM12 Least Significant Word Register	0x0000.0000
CAM13M_1	0xFFF0.3868	R/W	CAM13 Most Significant Word Register	0x0000.0000
CAM13L_1	0xFFF0.386C	R/W	CAM13 Least Significant Word Register	0x0000.0000

EMC 1 Control Registers, continued.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
CAM REGISTERS				
CAM14M_1	0xFFF0.3870	R/W	CAM14 Most Significant Word Register	0x0000.0000
CAM14L_1	0xFFF0.3874	R/W	CAM14 Least Significant Word Register	0x0000.0000
CAM15M_1	0xFFF0.3878	R/W	CAM15 Most Significant Word Register	0x0000.0000
CAM15L_1	0xFFF0.387C	R/W	CAM15 Least Significant Word Register	0x0000.0000
CAM16M_1	0xFFF0.3880	R/W	CAM16 Most Significant Word Register	0x0000.0000
CAM16L_1	0xFFF0.3884	R/W	CAM16 Least Significant Word Register	0x0000.0000
MAC REGISTERS				
MIEN_1	0xFFF0.3888	R/W	MAC Interrupt Enable Register	0x0000.0000
MCMDR_1	0xFFF0.388C	R/W	MAC Command Register	0x0000.0000
MIID_1	0xFFF0.3890	R/W	MII Management Data Register	0x0000.0000
MIIDA_1	0xFFF0.3894	R/W	MII Management Data Control and Address Register	0x0090.0000
MPCNT_1	0xFFF0.3898	R/W	Missed Packet counter register	0x0000.7FFF
DMA REGISTERS				
TXDLSA_1	0xFFF0.389C	R/W	Transmit Descriptor Link List Start Address register	0xFFFF.FFFC
RXDLSA_1	0xFFF0.38A0	R/W	Receive Descriptor Link List Start Address register	0xFFFF.FFFC
DMARFC_1	0xFFF0.38A4	R/W	DMA Receive Frame Control Register	0x0000.0800
TSDR_1	0xFFF0.38A8	W	Transmit Start Demand Register	Undefined
RSDR_1	0xFFF0.38AC	W	Receive Start Demand Register	Undefined
FIFOTHD_1	0xFFF0.38B0	R/W	FIFO Threshold Adjustment Register	0x0000.0101

EMC 1 Status Registers

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MAC REGISTERS				
MISTA_1	0xFFF0.38B4	R/W	MAC Interrupt Status Register	0x0000.0000
MGSTA_1	0xFFF0.38B8	R/W	MAC General Status Register	0x0000.0000
MRPC_1	0xFFF0.38BC	R	MAC Receive Pause count register	0x0000.0000
MRPCC_1	0xFFF0.38C0	R	MAC Receive Pause Current Count Register	0x0000.0000
MREPC_1	0xFFF0.38C4	R	MAC Remote pause count register	0x0000.0000
DMA REGISTERS				
DMARFS_1	0xFFF0.38C8	R/W	DMA Receive Frame Status Register	0x0000.0000
CTXDSA_1	0xFFF0.38CC	R	Current Transmit Descriptor Start Address Register	0x0000.0000
CTXBSA_1	0xFFF0.38D0	R	Current Transmit Buffer Start Address Register	0x0000.0000
CRXDSA_1	0xFFF0.38D4	R	Current Receive Descriptor Start Address Register	0x0000.0000
CRXBSA_1	0xFFF0.38D8	R	Current Receive Buffer Start Address Register	0x0000.0000

GDMA Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GDMA_CTL0	0xFFF0.4000	R/W	Channel 0 Control Register	0x0000.0000
GDMA_SRCB0	0xFFF0.4004	R/W	Channel 0 Source Base Address Register	0x0000.0000
GDMA_DSTB0	0xFFF0.4008	R/W	Channel 0 Destination Base Address Register	0x0000.0000
GDMA_TCNT0	0xFFF0.400C	R/W	Channel 0 Transfer Count Register	0x0000.0000
GDMA_CSRC0	0xFFF0.4010	R	Channel 0 Current Source Address Register	0x0000.0000
GDMA_CDST0	0xFFF0.4014	R	Channel 0 Current Destination Address Register	0x0000.0000
GDMA_CTCNT0	0xFFF0.4018	R	Channel 0 Current Transfer Count Register	0x0000.0000
GDMA_CTL1	0xFFF0.4020	R/W	Channel 1 Control Register	0x0000.0000
GDMA_SRCB1	0xFFF0.4024	R/W	Channel 1 Source Base Address Register	0x0000.0000
GDMA_DSTB1	0xFFF0.4028	R/W	Channel 1 Destination Base Address Register	0x0000.0000
GDMA_TCNT1	0xFFF0.402C	R/W	Channel 1 Transfer Count Register	0x0000.0000
GDMA_CSRC1	0xFFF0.4030	R	Channel 1 Current Source Address Register	0x0000.0000
GDMA_CDST1	0xFFF0.4034	R	Channel 1 Current Destination Address Register	0x0000.0000
GDMA_CTCNT1	0xFFF0.4038	R	Channel 1 Current Transfer Count Register	0x0000.0000

USB Host Controller Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
OpenHCI Registers				
HcRevision	0xFFF0.5000	R	Host Controller Revision Register	0x0000.0010
HcControl	0xFFF0.5004	R/W	Host Controller Control Register	0x0000.0000
HcCommandStatus	0xFFF0.5008	R/W	Host Controller Command Status Register	0x0000.0000
HcInterruptStatus	0xFFF0.500C	R/W	Host Controller Interrupt Status Register	0x0000.0000
HcInterruptEnable	0xFFF0.5010	R/W	Host Controller Interrupt Enable Register	0x0000.0000
HcInterruptDisable	0xFFF0.5014	R/W	Host Controller Interrupt Disable Register	0x0000.0000
HcHCCA	0xFFF0.5018	R/W	Host Controller Communication Area Register	0x0000.0000
HcPeriodCurrentED	0xFFF0.501C	R/W	Host Controller Period Current ED Register	0x0000.0000
HcControlHeadED	0xFFF0.5020	R/W	Host Controller Control Head ED Register	0x0000.0000
HcControlCurrentED	0xFFF0.5024	R/W	Host Controller Control Current ED Register	0x0000.0000
HcBulkHeadED	0xFFF0.5028	R/W	Host Controller Bulk Head ED Register	0x0000.0000
HcBulkCurrentED	0xFFF0.502C	R/W	Host Controller Bulk Current ED Register	0x0000.0000
HcDoneHead	0xFFF0.5030	R/W	Host Controller Done Head Register	0x0000.0000
HcFmInterval	0xFFF0.5034	R/W	Host Controller Frame Interval Register	0x0000.2EDF
HcFrameRemaining	0xFFF0.5038	R	Host Controller Frame Remaining Register	0x0000.0000
HcFmNumber	0xFFF0.503C	R	Host Controller Frame Number Register	0x0000.0000
HcPeriodicStart	0xFFF0.5040	R/W	Host Controller Periodic Start Register	0x0000.0000
HcLSThreshold	0xFFF0.5044	R/W	Host Controller Low Speed Threshold Register	0x0000.0628
HcRhDescriptorA	0xFFF0.5048	R/W	Host Controller Root Hub Descriptor A Register	0x0100.0002
HcRhDescriptorB	0xFFF0.504C	R/W	Host Controller Root Hub Descriptor B Register	0x0000.0000
HcRhStatus	0xFFF0.5050	R/W	Host Controller Root Hub Status Register	0x0000.0000
HcRhPortStatus [1]	0xFFF0.5054	R/W	Host Controller Root Hub Port Status [1]	0x0000.0000
HcRhPortStatus [2]	0xFFF0.5058	R/W	Host Controller Root Hub Port Status [2]	0x0000.0000

NATA Registers Map

REGISTER	OFFSET	R/W	DESCRIPTION	RESET VALUE
NATA Control and Status Registers				
NATCMD	0xFFF0.6000	R/W	NAT Command Register	0x0000.0000
NATCCLR0	0xFFF0.6010	W	NAT Counter 0 Clear Register	0x0000.0000
NATCCLR1	0xFFF0.6014	W	NAT Counter 1 Clear Register	0x0000.0000
NATCCLR2	0xFFF0.6018	W	NAT Counter 2 Clear Register	0x0000.0000
NATCCLR3	0xFFF0.601C	W	NAT Counter 3 Clear Register	0x0000.0000
NATCFG0	0xFFF0.6100	R/W	NAT Entry 0 Configuration Register	0x0000.0000
NATCFG1	0xFFF0.6104	R/W	NAT Entry 1 Configuration Register	0x0000.0000
. . .	. . .	. . .	. . .	. . .
NATCFG63	0xFFF0.61FC	R/W	NAT Entry 63 Configuration Register	0x0000.0000
EXMACM	0xFFF0.6200	R/W	External MAC Address Most Significant Word Register	0x0000.0000
EXMACL	0xFFF0.6204	R/W	External MAC Address Least Significant Word Register	0x0000.0000
INMACM	0xFFF0.6208	R/W	Internal MAC Address Most Significant Word Register	0x0000.0000
INMACL	0xFFF0.620C	R/W	Internal MAC Address Least Significant Word Register	0x0000.0000

REGISTER	OFFSET	R/W	DESCRIPTION	RESET VALUE
Address Lookup and Replacement Registers				
MASAD0	0xFFF0.6800	R/W	NAT Masquerading IP Address Entry 0	0x0000.0000
MASPN0	0xFFF0.6804	R/W	NAT Masquerading Port Number Entry 0	0x0000.0000
LSAD0	0xFFF0.6808	R/W	Local Station IP Address Entry 0	0x0000.0000
LSPN0	0xFFF0.680C	R/W	Local Station Port Number Entry 0	0x0000.0000
LSMAC0M	0xFFF0.6810	R/W	Local Station MAC Address Most Significant Word Register for Entry 0	0x0000.0000
LSMAC0L	0xFFF0.6814	R/W	Local Station MAC Address Least Significant Word Register for Entry 0	0x0000.0000
RSMAC0M	0xFFF0.6818	R/W	Remote Station MAC Address Most Significant Word Register for Entry 0	0x0000.0000
RSMAC0L	0xFFF0.681C	R/W	Remote Station MAC Address Least Significant Word Register for Entry 0	0x0000.0000
MASAD1	0xFFF0.6820	R/W	NAT Masquerading IP Address Entry 1	0x0000.0000
MASPN1	0xFFF0.6824	R/W	NAT Masquerading Port Number Entry 1	0x0000.0000
LSAD1	0xFFF0.6828	R/W	Local Station IP Address Entry 1	0x0000.0000
LSPN1	0xFFF0.682C	R/W	Local Station Port Number Entry 1	0x0000.0000
LSMAC1M	0xFFF0.6830	R/W	Local Station MAC Address Most Significant Word Register for Entry 1	0x0000.0000
LSMAC1L	0xFFF0.6834	R/W	Local Station MAC Address Least Significant Word Register for Entry 1	0x0000.0000
RSMAC1M	0xFFF0.6838	R/W	Remote Station MAC Address Most Significant Word Register for Entry 1	0x0000.0000
RSMAC1L	0xFFF0.683C	R/W	Remote Station MAC Address Least Significant Word Register for Entry 1	0x0000.0000
…	…	…	…	…
MASAD63	0xFFF0.6FE0	R/W	NAT Masquerading IP Address Entry 63	0x0000.0000
MASPN63	0xFFF0.6FE4	R/W	NAT Masquerading Port Number Entry 63	0x0000.0000
LSAD63	0xFFF0.6FE8	R/W	Local Station IP Address Entry 63	0x0000.0000
LSPN63	0xFFF0.6FEC	R/W	Local Station Port Number Entry 63	0x0000.0000
LSMAC63M	0xFFF0.6FF0	R/W	Local Station MAC Address Most Significant Word Register for Entry 63	0x0000.0000
LSMAC63L	0xFFF0.6FF4	R/W	Local Station MAC Address Least Significant Word Register for Entry 63	0x0000.0000
RSMAC63M	0xFFF0.6FF8	R/W	Remote Station MAC Address Most Significant Word Register for Entry 63	0x0000.0000
RSMAC63L	0xFFF0.6FFC	R/W	Remote Station MAC Address Least Significant Word Register for Entry 63	0x0000.0000

UART Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
RBR	0xFFF8.0000	R	Receive Buffer Register (DLAB = 0)	Undefined
THR	0xFFF8.0000	W	Transmit Holding Register (DLAB = 0)	Undefined
IER	0xFFF8.0004	R/W	Interrupt Enable Register (DLAB = 0)	0x0000.0000
DLL	0xFFF8.0000	R/W	Divisor Latch Register (LS) (DLAB = 1)	0x0000.0000
DLM	0xFFF8.0004	R/W	Divisor Latch Register (MS) (DLAB = 1)	0x0000.0000
IIR	0xFFF8.0008	R	Interrupt Identification Register	0x8181.8181
FCR	0xFFF8.0008	W	FIFO Control Register	Undefined
LCR	0xFFF8.000C	R/W	Line Control Register	0x0000.0000
MCR	0xFFF8.0010	R/W	Modem Control Register	0x0000.0000
LSR	0xFFF8.0014	R	Line Status Register	0x6060.6060
MSR	0xFFF8.0018	R	MODEM Status Register	0x0000.0000
TOR	0xFFF8.001C	R	Time Out Register	0x0000.0000

Timer Control Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
TCR0	0xFFF8.1000	R/W	Timer Control Register 0	0x0000.0005
TCR1	0xFFF8.1004	R/W	Timer Control Register 1	0x0000.0005
TICR0	0xFFF8.1008	R/W	Timer Initial Control Register 0	0x0000.00FF
TICR1	0xFFF8.100C	R/W	Timer Initial Control Register 1	0x0000.00FF
TDR0	0xFFF8.1010	R	Timer Data Register 0	0x0000.0000
TDR1	0xFFF8.1014	R	Timer Data Register 1	0x0000.0000
TISR	0xFFF8.1018	R/C	Timer Interrupt Status Register	0x0000.0000
WTCR	0xFFF8.101C	R/W	Watchdog Timer Control Register	0x0000.0000

GPIO Controller Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
GPIO_CFG	0xFFF8.3000	R/W	GPIO Configuration Register	0x0000.0000
GPIO_DIR	0xFFF8.3004	R/W	GPIO Direction Register	0x0000.0000
GPIO_DATAOUT	0xFFF8.3008	R/W	GPIO Data Output Register	0x0000.0000
GPIO_DATAIN	0xFFF8.300C	R	GPIO Data Input Register	Undefined
DEBNCE_CTRL	0xFFF8.3010	R/W	De-bounce Control Register	0x0000.0000

AIC Registers Map

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
AIC_SCR1	0xFFF8.2004	R/W	Source Control Register 1	0x0000.0047
AIC_SCR2	0xFFF8.2008	R/W	Source Control Register 2	0x0000.0047
AIC_SCR3	0xFFF8.200C	R/W	Source Control Register 3	0x0000.0047
AIC_SCR4	0xFFF8.2010	R/W	Source Control Register 4	0x0000.0047
AIC_SCR5	0xFFF8.2014	R/W	Source Control Register 5	0x0000.0047
AIC_SCR6	0xFFF8.2018	R/W	Source Control Register 6	0x0000.0047
AIC_SCR7	0xFFF8.201C	R/W	Source Control Register 7	0x0000.0047
AIC_SCR8	0xFFF8.2020	R/W	Source Control Register 8	0x0000.0047
AIC_SCR9	0xFFF8.2024	R/W	Source Control Register 9	0x0000.0047
AIC_SCR10	0xFFF8.2028	R/W	Source Control Register 10	0x0000.0047
AIC_SCR11	0xFFF8.202C	R/W	Source Control Register 11	0x0000.0047
AIC_SCR12	0xFFF8.2030	R/W	Source Control Register 12	0x0000.0047
AIC_SCR13	0xFFF8.2034	R/W	Source Control Register 13	0x0000.0047
AIC_SCR14	0xFFF8.2038	R/W	Source Control Register 14	0x0000.0047
AIC_SCR15	0xFFF8.203C	R/W	Source Control Register 15	0x0000.0047
AIC_SCR16	0xFFF8.2040	R/W	Source Control Register 16	0x0000.0000
AIC_SCR17	0xFFF8.2044	R/W	Source Control Register 17	0x0000.0000
AIC_SCR18	0xFFF8.2048	R/W	Source Control Register 18	0x0000.0000
AIC_IRSR	0xFFF8.2100	R	Interrupt Raw Status Register	0x0000.0000
AIC_IASR	0xFFF8.2104	R	Interrupt Active Status Register	0x0000.0000
AIC_ISR	0xFFF8.2108	R	Interrupt Status Register	0x0000.0000
AIC_IPER	0xFFF8.210C	R	Interrupt Priority Encoding Register	0x0000.0000
AIC_ISNR	0xFFF8.2110	R	Interrupt Source Number Register	0x0000.0000
AIC_IMR	0xFFF8.2114	R	Interrupt Mask Register	0x0000.0000
AIC_OISR	0xFFF8.2118	R	Output Interrupt Status Register	0x0000.0000
AIC_MECR	0xFFF8.2120	W	Mask Enable Command Register	Undefined
AIC_MDCR	0xFFF8.2124	W	Mask Disable Command Register	Undefined
AIC_SSCR	0xFFF8.2128	W	Source Set Command Register	Undefined
AIC_SCCR	0xFFF8.212C	W	Source Clear Command Register	Undefined
AIC_EOSCR	0xFFF8.2130	W	End of Service Command Register	Undefined

10. ORDERING INFORMATION

PART NUMBER	NAME	PACKAGE DESCRIPTION
W90N740CD	LQFP176	176 Leads, body 22 x 22 x 1.4 mm
W90N740CDG	LQFP176	176 Leads, body 22 x 22 x 1.4 mm, Lead free package

11. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan 15, 2003	-	Initial Issued
A2	May 27, 2003	-	Add DC specifications in 8.2
A3	Sep. 3, 2004		Change Pin Description
A4	Nov. 26, 2004	Page 54	Change tCOH description
		Page 56	Remove Fig. 7.3.7
		Page 57	Address change from 0x7ff71f00 to 0xfff71f00
		Page 127	Add description in external GDMA
		Page 215	Add lead free package item
A5	April 19, 2005	Page 216	Add Important Notice
A6	Aug. 18, 2005	Page 155	Change the clock order
		Page 3	Change OHCI 1.0 to OHCI 1.1
		Page 121	Section 7.8 Change OHCI 1.0 to OHCI 1.1
		Page 123	Change OHCI 1.0 to OHCI 1.1
		Page 114	Section 7.7.2 Change the GDMA_CTL0 describe and content
A7	Sep. 19, 2006	Page 5	Section 3
		Page 113	Section 6.7.2 Change the GDMA_CTL0/ GDMA_CTL1 describe and content

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