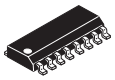
1:6 PCI Clock Generator/ Fanout Buffer

The MPC905 is a six output clock generation device targeted to provide the clocks required in a 3.3 V or 5.0 V PCI environment. The device operates from a 3.3 V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0 V when the V_{CC} is at 3.3 V. The outputs of the MPC905 meet all of the specifications of the PCI standard.

**1:6 PCI
CLOCK GENERATOR/
FANOUT BUFFER**



**D SUFFIX
EF SUFFIX (PB-FREE PACKAGE)
PLASTIC SOIC PACKAGE
CASE 751B-05**

Features

- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0 V Tolerant Enable Inputs

Functional Description

The MPC905 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC905 can drive two series terminated 50Ω transmission lines. This capability effectively makes the MPC905 a 1:12 fanout buffer.

The MPC905 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic ‘0’ on the ENABLE1 will pull outputs 0 to 4 into the logic ‘0’ state. A logic ‘1’ on the ENABLE1 input will result in outputs 0 to 4 to be toggling. A logic ‘0’ on ENABLE2 will cause output BLK5 to a logic ‘0’ state, whereas a logic ‘1’ on ENABLE2 will cause output BLK5 to toggle. The oscillator remains on.

The ENABLE2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling.

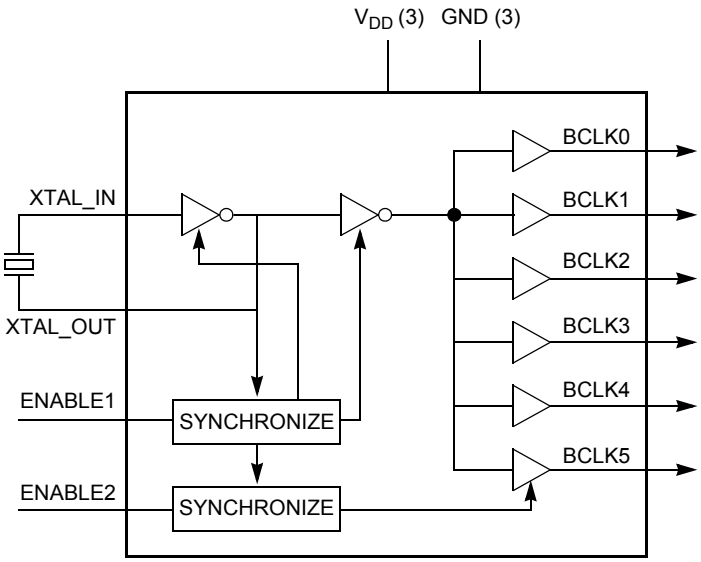


Figure 1. Block Diagram

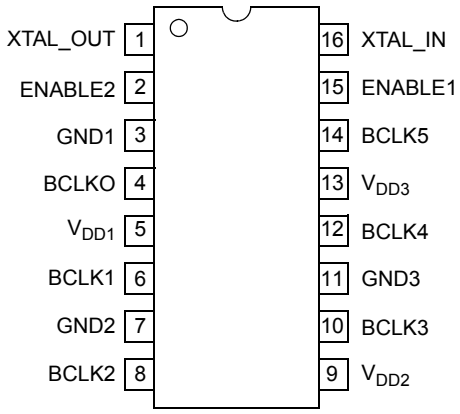


Figure 2. Pinout: 16-Lead Plastic Package
(Top View)

Table 1. Pin Configurations

Pin	I/O	Type	Function
XTAL_IN, XTAL_OUT	Input	Analog	Crystal Oscillator Terminals
ENABLE1, ENABLE2	Input	LVCMOS	Output Enable
BCLK0–BCLK5	Output	LVCMOS	Clock Outputs
V_{DD}		Supply	Positive Power Supply
GND		Supply	Negative Power Supply

Table 2. Function Table

ENABLE1	ENABLE2	Outputs 0 to 4	Output 5	OSC (On/Off)
0	0	Low	Low	ON
0	1	Low	Toggling	ON
1	0	Toggling	Low	ON
1	1	Toggling	Toggling	ON

Table 3. Absolute Maximum Ratings(1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	4.6	V
V_{IN}	Input Voltage	–0.5	V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0	+70	°C
T_{stg}	Storage Temperature Range	–65	+150	°C
T_{sol}	Soldering Temperature Range (10 Sec)		+260	°C
T_j	Junction Temperature Range		+125	°C
ESD	Static Discharge Voltage	1500		V
I_{Latch}	Latch Up Current	50		mA

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature Range	0	70	°C
V_{CC}	Positive Supply Voltage (Functional Range)	3.0	3.6	V
t_{DC}in	T_{high} (at XTAL_IN Input) T_{low} (at XTAL_IN Input)	0.44T(1) 0.44T(1)	0.56T(1) 0.56T(1)	T = Period

1. When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

Table 5. DC Characteristics (T_A = 0–70°C; V_{DD} = 3.3 V ± 0.3 V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	High Level Input Voltage		2.0		5.5(2)	V	
V_{IL}	Low Level Input Voltage				0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –36 mA(1)
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 36 mA(1)
I_{IH}	Input High Current				2.5(2)	µA	
I_{IL}	Input Low Current				2.5	µA	
I_{CC}	Power Supply Current	DC 33 MHz 66 MHz		20 37 78	 45 95	µA mA mA	
C_{IN}	Input Capacitance	XTAL_IN Others			9.0 4.5	pF	

1. The MPC905 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to V_{TT} = V_{CC}/2. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
2. XTAL_IN input will sink up to 10mA when driven to 5.5 V. There are no reliability concerns associated with the condition. Note that the ENABLE1 input must be a logic HIGH. Do not take the ENABLE1 input to a logic LOW with >V_{CC} volts on the XTAL_IN input.

Table 6. AC Characteristics (T_A = 0–70°C; V_{DD} = 3.3 V ± 0.3 V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Operating Frequency	Using External Crystal Using External Clock Source	— DC		50 100	MHz	
t_{pw}	Output Pulse Width	HIGH (Above 2.0 V) LOW (Below 0.8 V) HIGH (Above 2.0 V) LOW (Below 0.8 V)	0.40T(1) 0.40T(1) 0.45T(2) 0.45T(2)		0.60T(1) 0.60T(1) 0.55T(2) 0.55T(2)		T = Periods
t_{per}	Output Period		T - 400 ps				T = Desired Period
t_{os}	Output-to-Output Skew	Rising Edges Falling Edges			400 500	ps	
t_r, t_f	Rise/Fall Times (Slew Rate)		1.0		4.0	V/ns	Series Terminated Transmission Lines
t_{EN}	Enable Time	ENABLE1 ENABLE2			5.0 4.0	ms Cycles	
t_{DIS}	Disable Time	ENABLE1 ENABLE2			4.0 4.0	Cycles	
A_{osc}	XTAL_IN to XTAL_OUT Oscillator Gain		6.0			dB	
Phase	Loop Phase Shift Modulo 360° +		30			Degrees	

1. Assuming input duty cycle specs from Recommended Operating Conditions table are met.
2. Assuming external crystal or 50% duty cycle external reference is used.

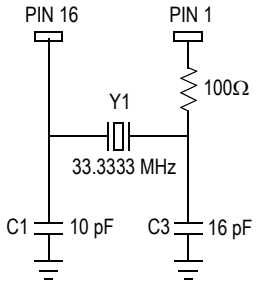


Figure 3. Crystal Oscillator Interface
(Fundamental)

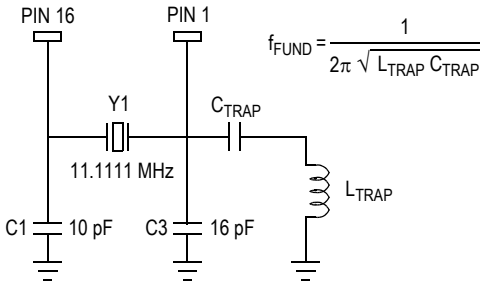


Figure 4. Crystal Oscillator Interface
(3rd Overtone)

Table 7. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7 pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100 µW
Aging	5 ppm/Yr (First 3 Years)

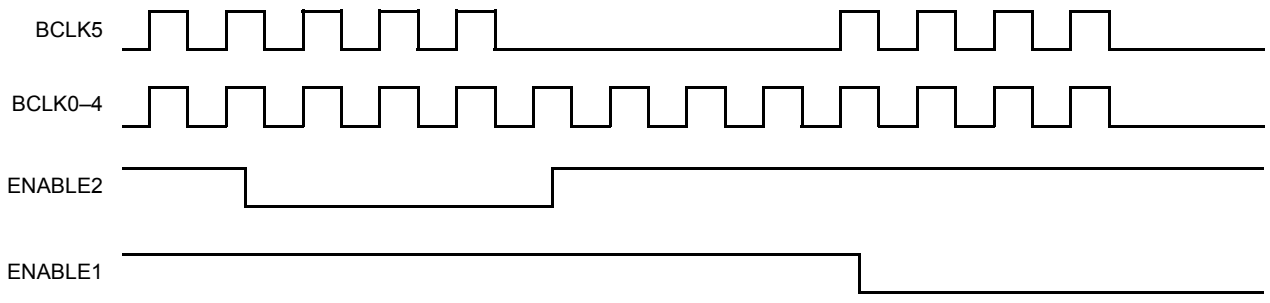


Figure 5. Enable Timing Diagram

APPLICATIONS INFORMATION

DRIVING TRANSMISSION LINES

The MPC905 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC905 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC905 clock driver is effectively doubled due to its capability to drive multiple lines.

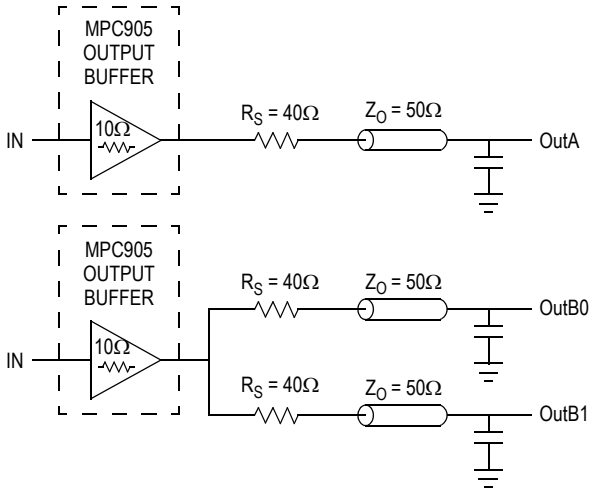


Figure 6. Single versus Dual Transmission Lines

The waveform plots of Figure 7 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC905 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge.

Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 40Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/55) = 1.36 V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.73 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

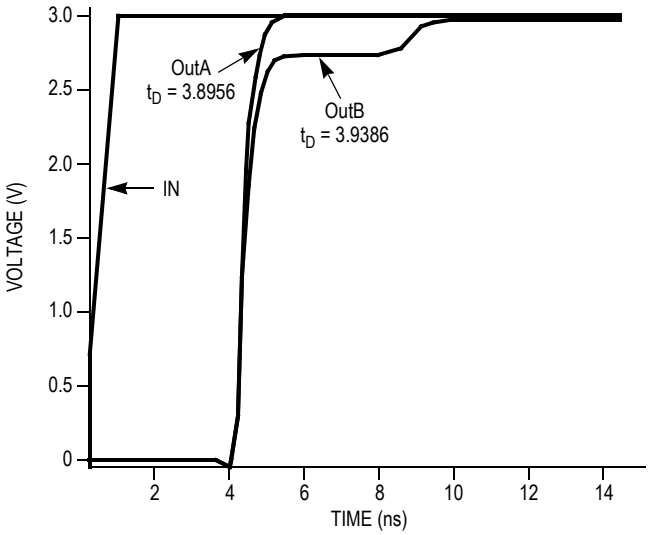
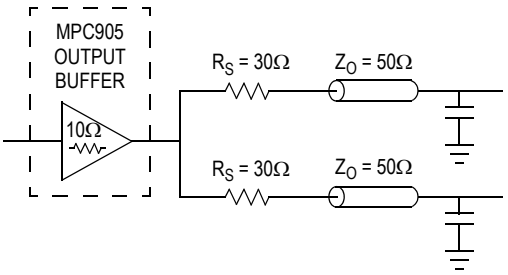


Figure 7. Single versus Dual Waveforms

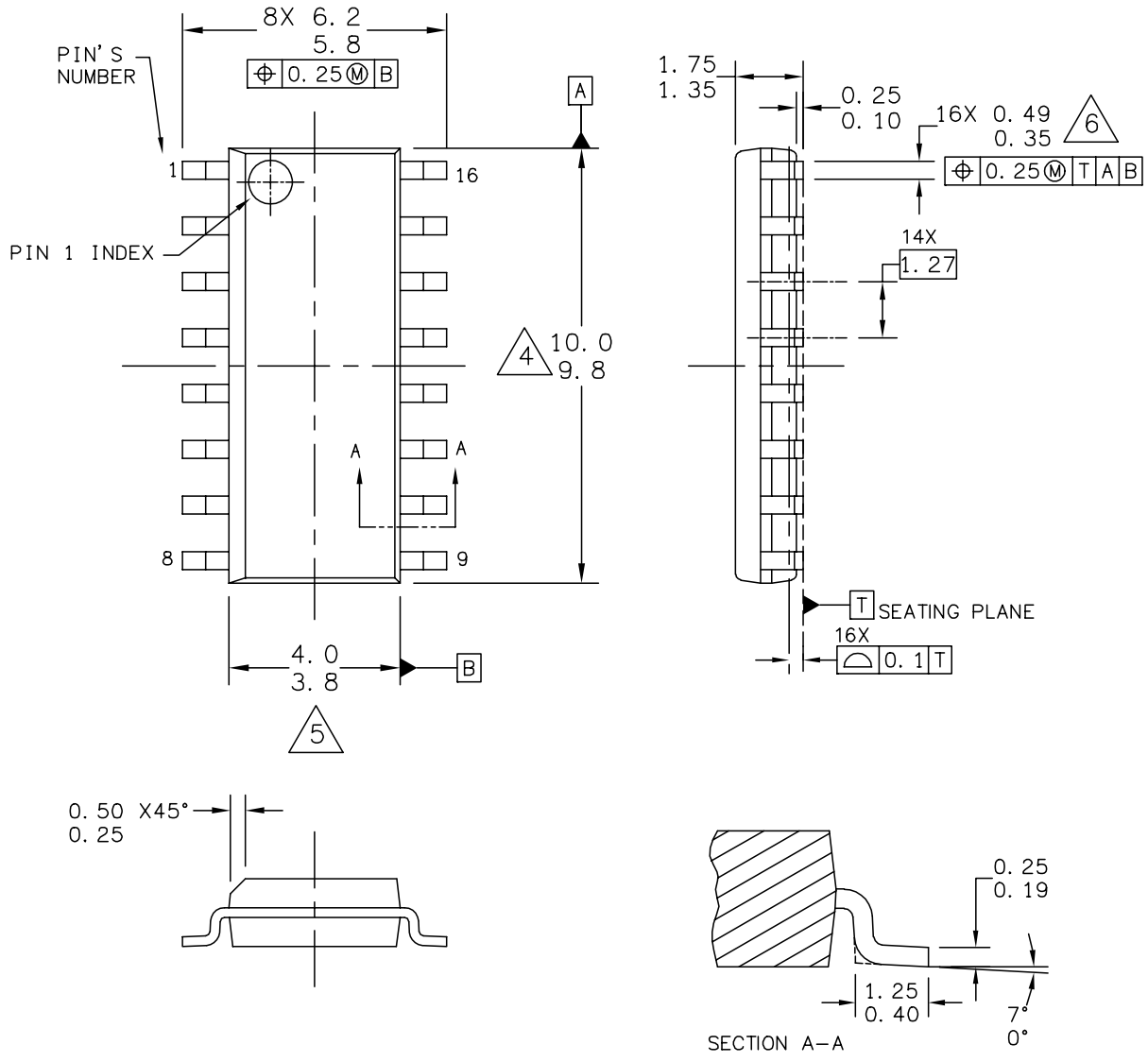
Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



10Ω + 30Ω || 30Ω = 50Ω ||50Ω
25Ω = 25Ω

Figure 8. Optimized Dual Line Termination

PACKAGE DIMENSIONS



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CASE 751B-05
ISSUE L
PLASTIC SOIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
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CASE 751B-05
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PLASTIC SOIC PACKAGE

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