LOW-COST, 3.3V ZERO DELAY BUFFER

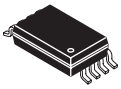
MPC962305

MPC962305
MPC962309

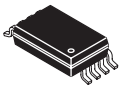
The MPC962309 is a zero delay buffer designed to distribute high-speed clocks. Available in a 16-pin SOIC or TSSOP package, the device accepts one reference input and drives nine low-skew clocks. The MPC962305 is the 8-pin version of the MPC962309 which drives five outputs with one reference input. The -1H versions of these devices have higher drive than the -1 devices and can operate up to 100/-133 MHz frequencies. These parts have on-chip PLLs which lock to an input clock presented on the REF pin. The PLL feedback is on-chip and is obtained from the CLOCKOUT pad.

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

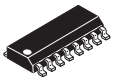
EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-06



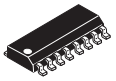
DT SUFFIX
8-LEAD TSSOP PACKAGE
CASE 948J-01



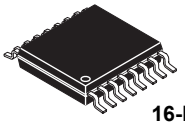
EJ SUFFIX
8-LEAD TSSOP PACKAGE
Pb-FREE PACKAGE
CASE 948J-01



D SUFFIX
16-LEAD SOIC PACKAGE
CASE 751B-05



EF SUFFIX
16-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751B-05



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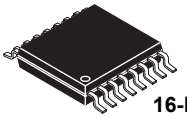
16-LEAD TSSOP PACKAGE
CASE 948F-01



EJ SUFFIX
16-LEAD TSSOP PACKAGE
Pb-FREE PACKAGE
CASE 948F-01

Features

- 1:5 LVCMOS zero-delay buffer (MPC962305)
- 1:9 LVCMOS zero-delay buffer (MPC962309)
- Zero input-output propagation delay
- Multiple low-skew outputs
- 250 ps max output-output skew
- 700 ps max device-device skew
- Supports a clock I/O frequency range of 10 MHz to 133 MHz, compatible with CPU and PCI bus frequencies
- Low jitter, 200 ps max cycle-cycle, and compatible with Pentium® based systems
- Test Mode to bypass PLL (MPC962309 only. See Table 3)
- 8-pin SOIC or 8-pin TSSOP package (MPC962305);16-pin SOIC or 16-pin TSSOP package (MPC962309)
- Single 3.3 V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2305, CY23S05, CY2309, CY23S09
- Spread spectrum compatible
- Pb-free packages available

Functional Description

The MPC962309 has two banks of four outputs each, which can be controlled by the Select Inputs as shown in Table 3. Bank B can be tri-stated if all of the outputs are not required. Select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The MPC962305 and MPC962309 PLLs enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate, the PLL is turned off, and there is less than 25.0 μA of current draw for the device. The PLL shuts down in one additional case as shown in Table 3.

Multiple MPC962305 and MPC962309 devices can accept the same input clock and distribute it throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

All outputs have less than 200 ps of cycle-cycle jitter. The input-to-output propagation delay on both devices is guaranteed to be less than 350 ps and the output-to-output skew is guaranteed to be less than 250 ps.

The MPC962305 and MPC962309 are available in two/three different configurations, as shown on the ordering information page. The MPC962305-1/MPC962309-1 are the base parts. High drive versions of those devices, MPC962305-1H and MPC962309-1H, are available to provide faster rise and fall times of the base device.

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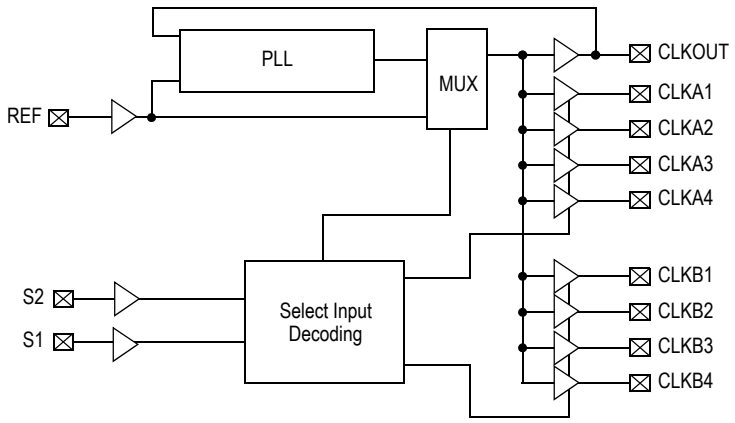
Block Diagram



Pin Configuration

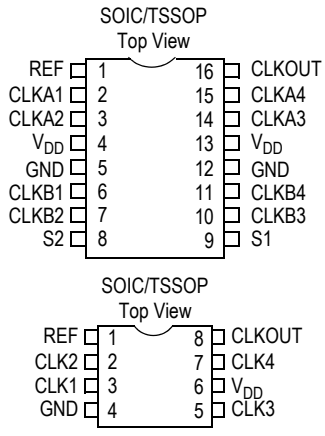


Table 1. Pin Description for MPC962309

Pin	Signal	Description
1	REF(1)	Input reference frequency, 5 V-tolerant input
2	CLKA1(2)	Buffered clock output, Bank A
3	CLKA2(2)	Buffered clock output, Bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1(2)	Buffered clock output, Bank B
7	CLKB2(2)	Buffered clock output, Bank B
8	S2(3)	Select input, bit 2
9	S1(3)	Select input, bit 1
10	CLKB3(2)	Buffered clock output, Bank B
11	CLKB4(2)	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3(2)	Buffered clock output, Bank A
15	CLKA4(2)	Buffered clock output, Bank A
16	CLKOUT(2)	Buffered output, internal feedback on this pin

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

Table 2. Pin Description for MPC962305

Pin	Signal	Description
1	REF(1)	Input reference frequency, 5 V-tolerant input
2	CLK2(2)	Buffered clock output
3	CLK1(2)	Buffered clock output
4	GND	Ground
5	CLK3(2)	Buffered clock output
6	V_{DD}	3.3 V supply
7	CLK4(2)	Buffered clock output
8	CLKOUT(2)	Buffered clock output, internal feedback on this pin

1. Weak pull-down.
2. Weak pull-down on all outputs.

Table 3. Select Input Decoding for MPC962309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[1]	Output Source	PLL Shutdown
0	0	Three-State	Three-State	Driven	PLL	N
0	1	Driven	Three-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Table 4. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +3.9	V
DC Input Voltage (Except Ref)	–0.5 to V_{DD}+0.5	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction Temperature	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 5. Operating Conditions for MPC962305-X and MPC962309-X Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Table 6. Electrical Characteristics for MPC962305-X and MPC962309-X Industrial Temperature Devices[1]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage[2]			0.8	V
V_{IH}	Input HIGH Voltage[2]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[3]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)		0.4	V
V_{OH}	Output HIGH Voltage[3]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		35.0	mA

1. All parameters are specified with loaded outputs.
2. REF input has a threshold voltage of V_{PP}/2.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. Switching Characteristics for MPC962305-1 and MPC962309-1 Industrial Temperature Devices(1)

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle(2) = $t_2 \div t_1$	Measured at 1.4 V, F_{OUT} = 66.67 MHz	40.0	50.0	60.0	%
t_3	Rise Time(2)	Measured between 0.8 V and 2.0 V			2.50	ns
t_4	Fall Time(2)	Measured between 0.8 V and 2.0 V			2.50	ns
t_5	Output to Output Skew(2)	All outputs equally loaded			250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$		0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, MPC962309 device only	1	5	8.7	ns
t_7	Device to Device Skew(2)	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
t_J	Cycle to Cycle Jitter(2)	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time(2)	Stable power supply, valid clock presented on REF pin			1.0	ms

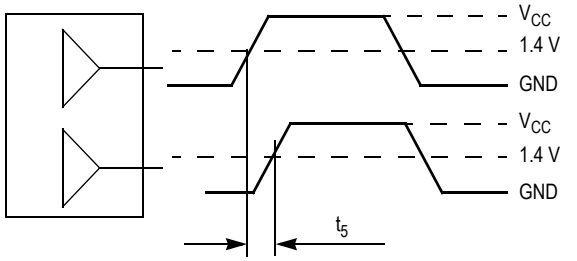
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 8. Switching Characteristics for MPC962305-1H and MPC962309-1H Industrial Temperature Devices(1)

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle(2) = t2 ÷ t1	Measured at 1.4 V, F_{OUT} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle(2) = t2 ÷ t1	Measured at 1.4 V, F_{OUT} < 50 MHz	45.0	55.0	55.0	%
t_3	Rise Time(2)	Measured between 0.8 V and 2.0 V			1.50	ns
t_4	Fall Time(2)	Measured between 0.8 V and 2.0 V			1.50	ns
t_5	Output to Output Skew(2)	All outputs equally loaded			250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$		0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, MPC962309 device only	1	5	8.7	ns
t_7	Device to Device Skew(2)	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
t_8	Output Slew Rate(2)	Measured between 0.8 V and 2.0 V using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter(2)	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time(2)	Stable power supply, valid clock presented on REF pin			1.0	ms

1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew $t_{SK(O)}$

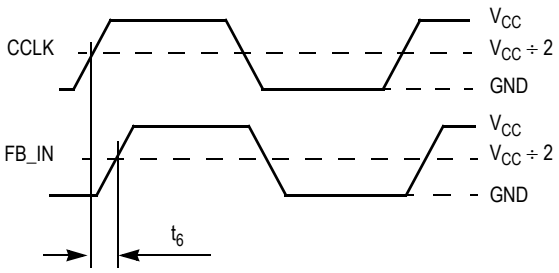
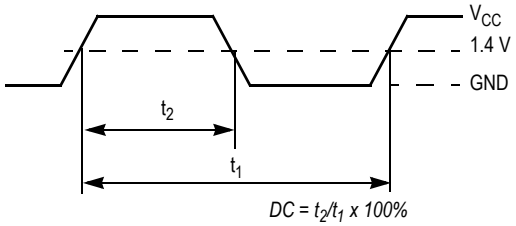


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

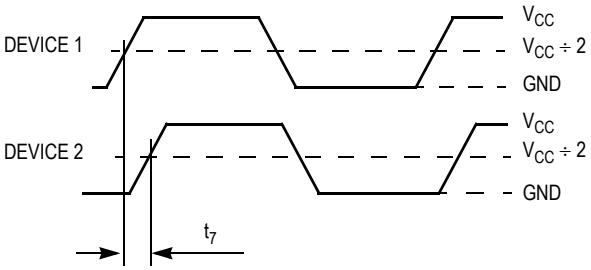
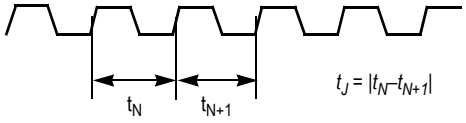


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

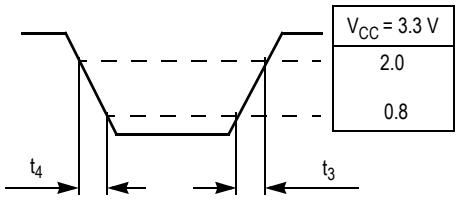
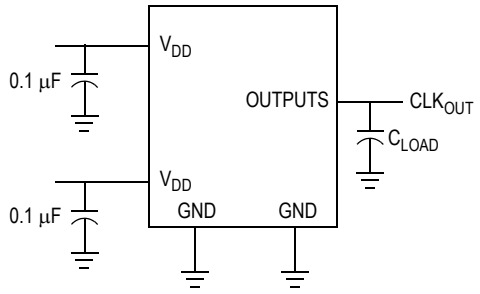


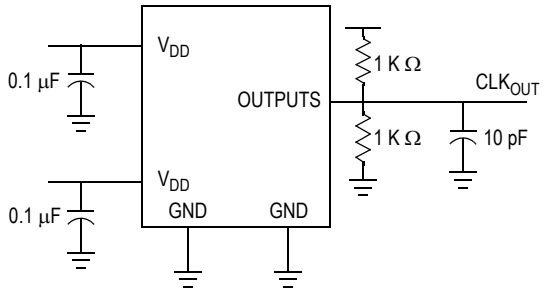
Figure 6. Output Transition Time Test Reference

Test Circuit #1



Test Circuit for all parameters except t_8

Test Circuit #2

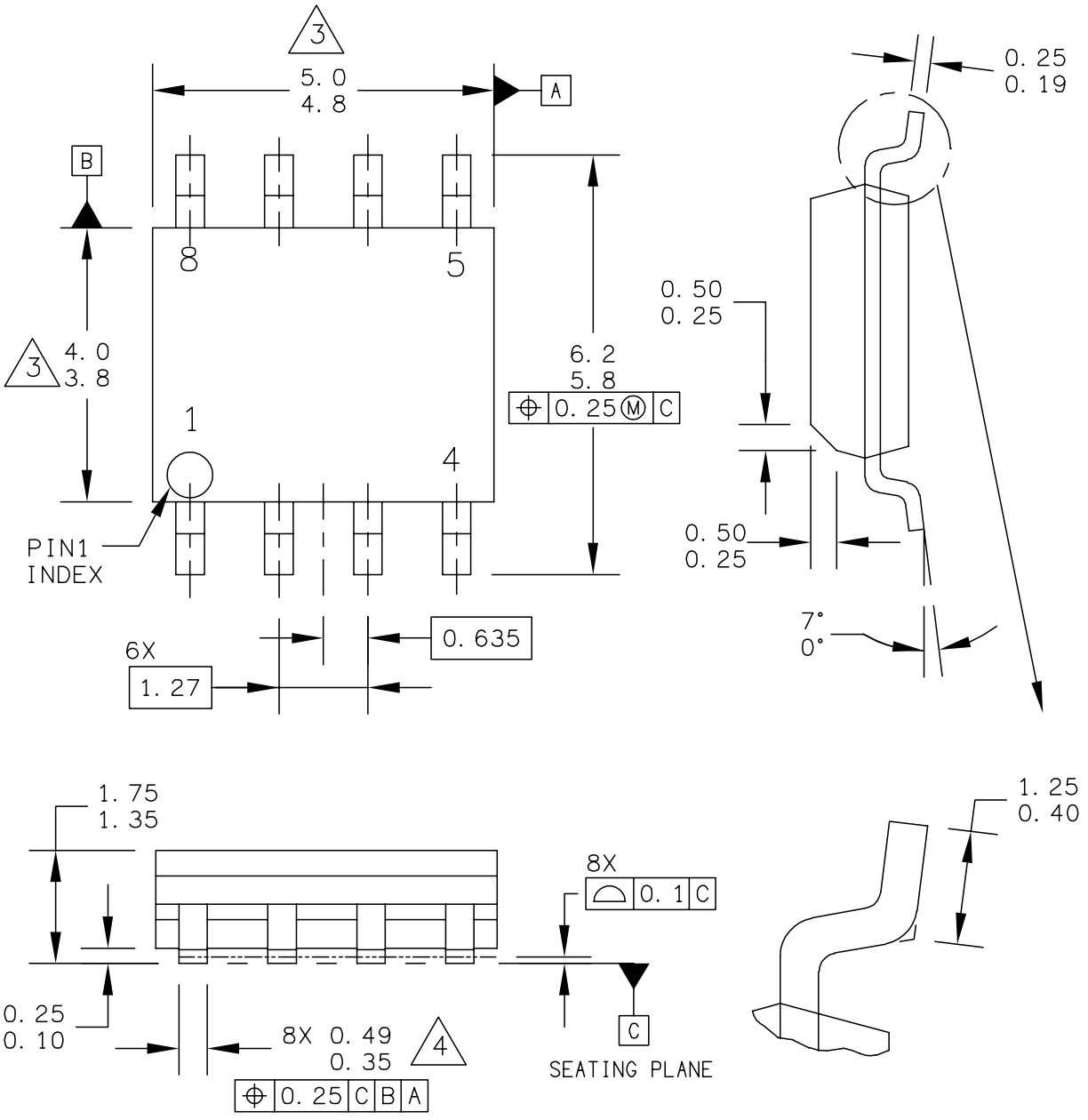


Test Circuit for t_8, Output slew rate on –1H, –5 device

Table 9. Ordering Information

Ordering Code	Package Type
MPC962305D-1	8-pin 150-mil SOIC
MPC962305D-1R2	8-pin 150-mil SOIC - Tape and Reel
MPC962305EF-1	8-pin 150-mil SOIC (Pb-free)
MPC962305EF-1R2	8-pin 150-mil SOIC (Pb-free) - Tape and Reel
MPC962305D-1H	8-pin 150-mil SOIC
MPC962305D-1HR2	8-pin 150-mil SOIC - Tape and Reel
MPC962305EF-1H	8-pin 150-mil SOIC (Pb-free)
MPC962305EF-1HR2	8-pin 150-mil SOIC (Pb-free) - Tape and Reel
MPC962305DT-1H	8-pin 150-mil TSSOP
MPC962305DT-1HR2	8-pin 150-mil TSSOP - Tape and Reel
MPC962305EJ-1H	8-pin 150-mil TSSOP (Pb-free)
MPC962305EJ-1HR2	8-pin 150-mil TSSOP (Pb-free) - Tape and Reel
MPC962309D-1	16-pin 150-mil SOIC
MPC962309D-1R2	16-pin 150-mil SOIC - Tape and Reel
MPC962309EF-1	16-pin 150-mil SOIC (Pb-free)
MPC962309EF-1R2	16-pin 150-mil SOIC (Pb-free) - Tape and Reel
MPC962309D-1H	16-pin 150-mil SOIC
MPC962309D-1HR2	16-pin 150-mil SOIC - Tape and Reel
MPC962309EF-1H	16-pin 150-mil SOIC (Pb-free)
MPC962309EF-1HR2	16-pin 150-mil SOIC (Pb-free) - Tape and Reel
MPC962309DT-1H	16-pin 4.4-mm TSSOP
MPC962309DT-1HR2	16-pin 4.4-mm TSSOP - Tape and Reel
MPC962309EJ-1H	16-pin 4.4-mm TSSOP (Pb-free)
MPC962309EJ-1HR2	16-pin 4.4-mm TSSOP (Pb-free) - Tape and Reel

PACKAGE DIMENSIONS



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U
	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

PAGE 1 OF 2

CASE 751-07
ISSUE U
8-LEAD SOIC PLASTIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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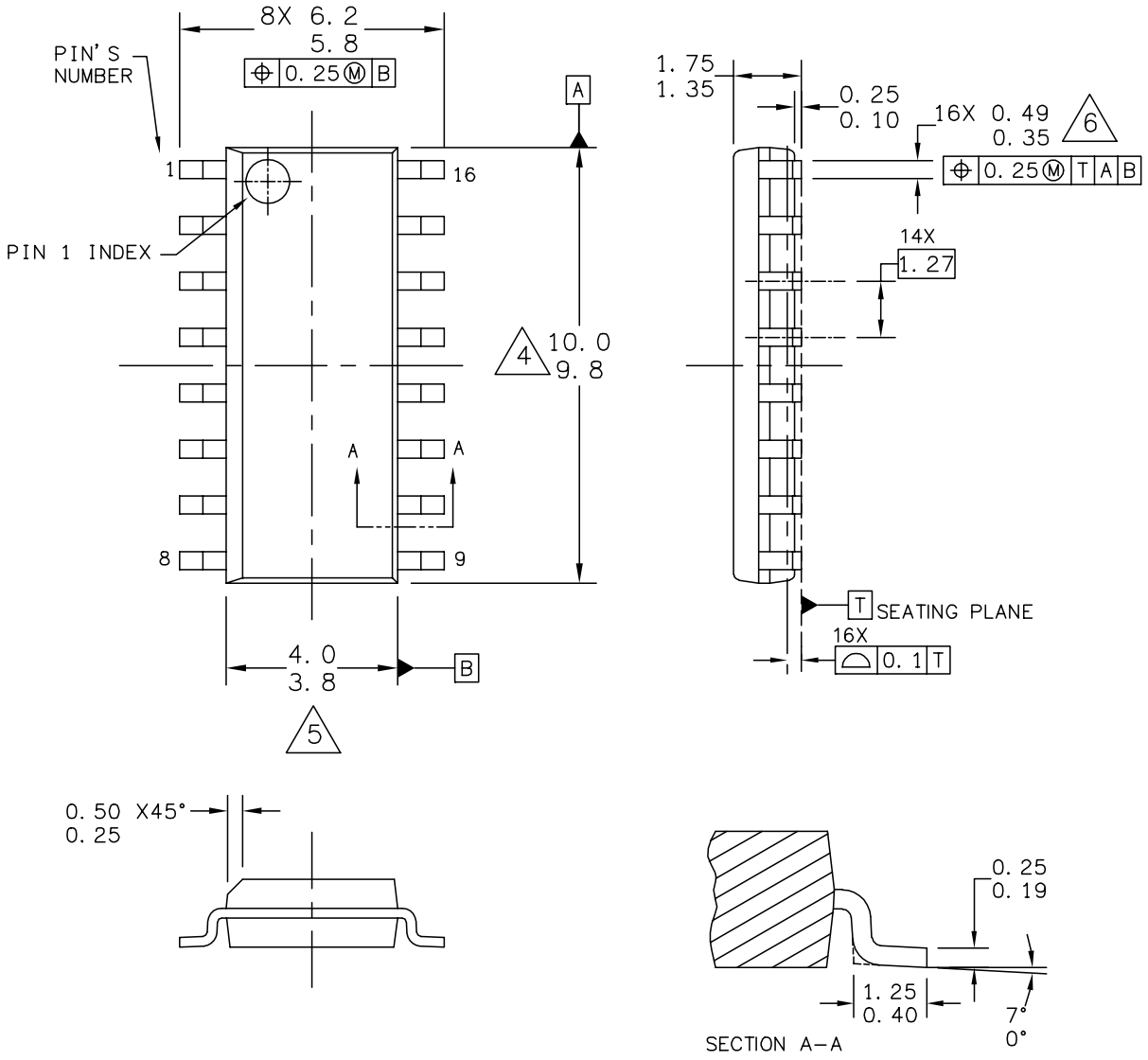
TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U
	CASE NUMBER: 751–07	07 APR 2005
	STANDARD: JEDEC MS–012AA	

PAGE 2 OF 2

CASE 751-07
ISSUE U
8-LEAD SOIC PLASTIC PACKAGE

PACKAGE DIMENSIONS



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	CASE NUMBER: 751B-05	11 APR 2005
	STANDARD: JECDEC MS-012AC	

PAGE 1 OF 2

CASE 751B-05
ISSUE L
16-LEAD SOIC PLASTIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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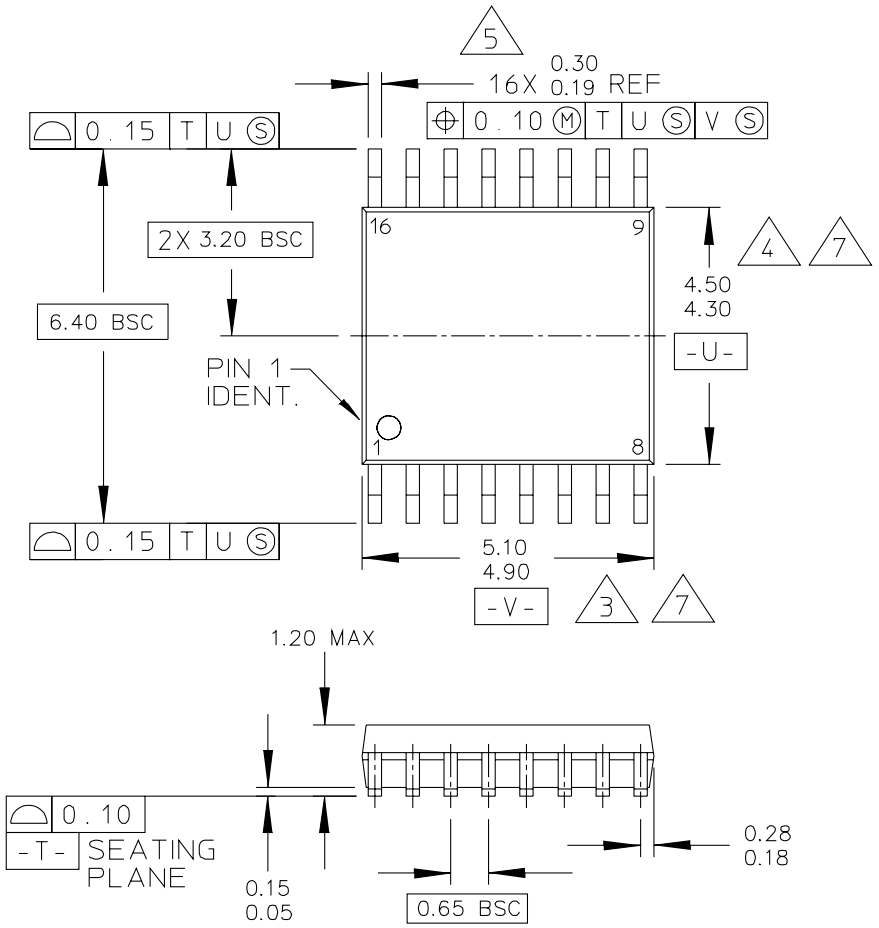
16LD SOIC N/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751B–05	11 APR 2005
	STANDARD: JEDEC MS–012AC	

PAGE 2 OF 2

CASE 751B-05
ISSUE L
16-LEAD SOIC PLASTIC PACKAGE

PACKAGE DIMENSIONS



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TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 1 OF 3

CASE 948F-01
ISSUE B
16-LEAD TSSOP PLASTIC PACKAGE

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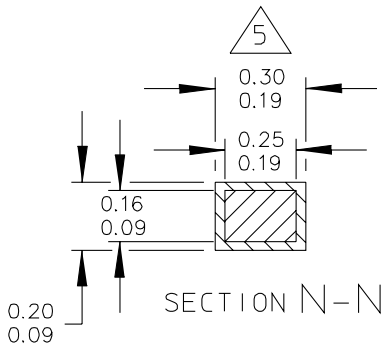

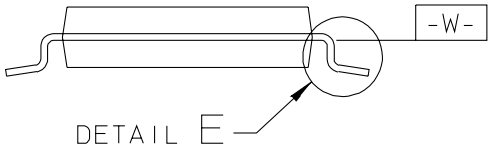

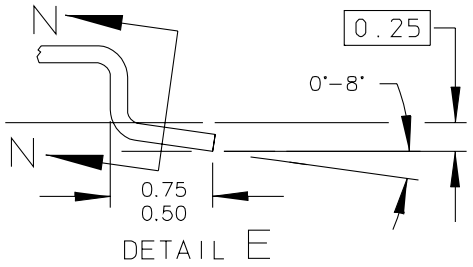

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TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 2 OF 3

CASE 948F-01
ISSUE B
16-LEAD TSSOP PLASTIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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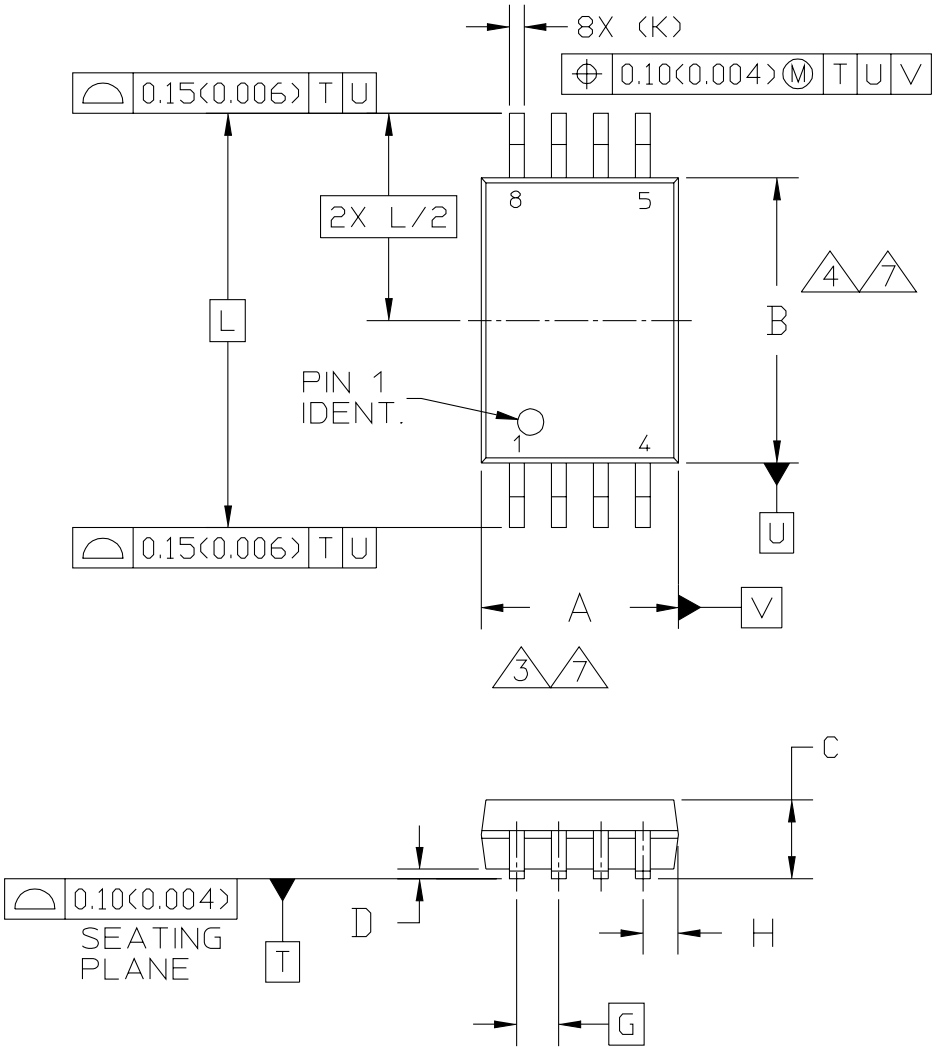
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 3 OF 3

CASE 948F-01
ISSUE B
16-LEAD TSSOP PLASTIC PACKAGE

PACKAGE DIMENSIONS



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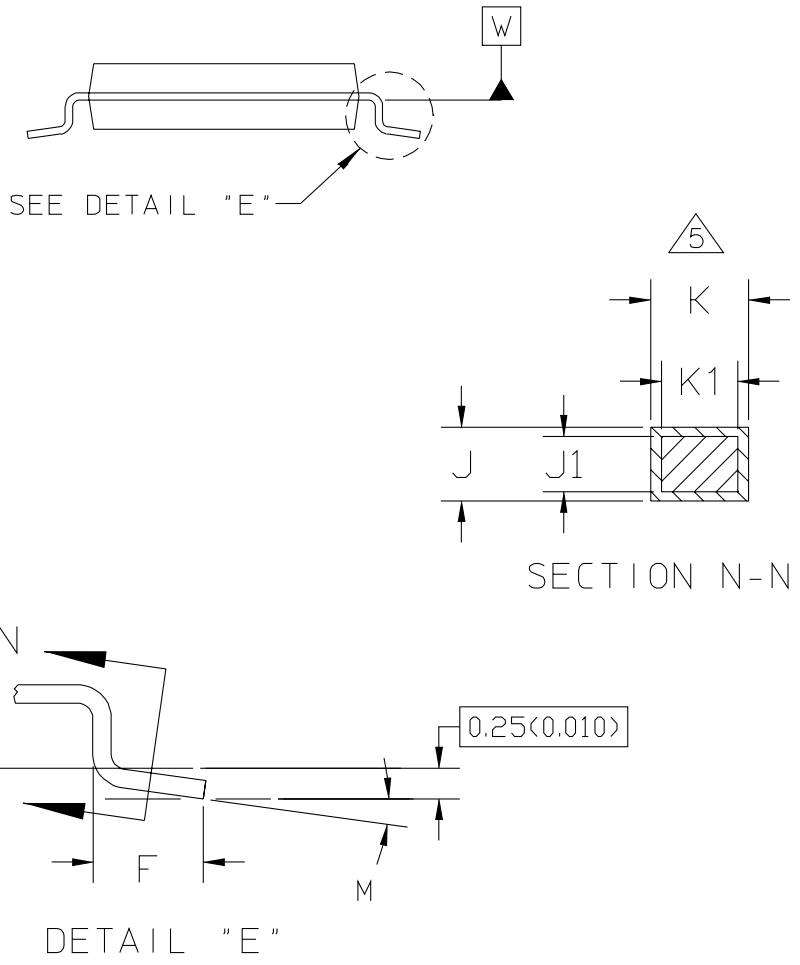
TITLE: 8 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70382A	REV: B
	CASE NUMBER: 948J-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 1 OF 3

CASE 948J-01
ISSUE B
8-LEAD TSSOP PLASTIC PACKAGE

PACKAGE DIMENSIONS



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TITLE: 8 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70382A	REV: B
	CASE NUMBER: 948J-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 2 OF 3

CASE 948J-01
ISSUE B
8-LEAD TSSOP PLASTIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (.006) PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (.010) PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (.003) TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE –W–.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10					
B	0.169	0.177	4.30	4.50					
C	–	0.047	–	1.20					
D	0.002	0.006	0.05	0.15					
F	0.020	0.030	0.50	0.75					
G	0.026 BSC		0.65 BSC						
H	0.020	0.024	0.50	0.60					
J	0.004	0.008	0.09	0.20					
J1	0.004	0.006	0.09	0.16					
K	0.007	0.012	0.19	0.30					
K1	0.007	0.010	0.19	0.25					
L	0.252 BSC		6.40 BSC						
M	0°	8°	0°	8°					

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TITLE:	DOCUMENT NO: 98ASH70382A	REV: B
8 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948J-01	19 MAY 2005
	STANDARD: JEDEC	

PAGE 3 OF 3

CASE 948J-01
ISSUE B
8-LEAD TSSOP PLASTIC PACKAGE

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