

8Gb NAND FLASH HY27UG088G(5/D)B

Document Title
8Gbit (1Gx8bit) NAND Flash Memory

Revision History

| Revision No. | History | Draft Date | Remark |
|--------------|---|---------------|-------------|
| 0.0 | Initial Draft. | Jun. 22. 2007 | Preliminary |
| 0.1 | 1) Correct Read Cache figure 2) Add ULGA package 3) Correct Block erase | Jun. 27. 2007 | Preliminary |
| 0.2 | 1) Delete Preliminary | Jan. 15. 2008 | |

FEATURES SUMMARY**HIGH DENSITY NAND FLASH MEMORIES**

- Cost effective solutions for mass storage applications

MULTIPLANE ARCHITECTURE

- Array is split into two independent planes. Parallel Operations on both planes are available, halving Program and erase time.

NAND INTERFACE

- x8 bus width.
- Address/ Data Multiplexing
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- 3.3V device : $V_{cc} = 2.7 V \sim 3.6 V$

MEMORY CELL ARRAY

- x8 : (2K + 64) bytes x 64 pages x 8192 blocks

PAGE SIZE

- (2K + 64 spare) Bytes

BLOCK SIZE

- (128K + 4Kspare) Bytes

PAGE READ / PROGRAM

- Random access : 25us (max.)
- Sequential access : 25ns (min.)
- Page program time : 200us (typ.)
- Multi-page program time (2 pages) : 200us (Typ)

COPY BACK PROGRAM

- Automatic block download without latency time

FAST BLOCK ERASE

- Block erase time: 1.5ms (Typ)
- Multi-block erase time (2 blocks) : 1.5ms (Typ)

STATUS REGISTER

- Normal Status Register (Read/Program/Erase)
- Extended Status Register (EDC)

ELECTRONIC SIGNATURE

- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle : Page size, Block size, Organization, Spare size
- 5th cycle : Multiplane information

CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions.

DATA RETENTION

- 100,000 Program/Erase cycles (with 1bit/528byte ECC)
- 10 years Data Retention

PACKAGE

- HY27UG088G5B-T(P)
 - : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
 - HY27UG088G5B-T (Lead)
 - HY27UG088G5B-TP (Lead Free)
- HY27UG088GDB-UP
 - : 52-ULGA (12 x 17 x 0.65 mm)
 - HY27UG088GDB-UP (Lead Free)

1. SUMMARY DESCRIPTION

Hynix NAND HY27UG088G(5/D)B Series have 1024Mx8bit with spare 32Mx8 bit capacity. The device is offered in 3.3 Vcc Power Supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 8192 blocks, composed by 64 pages. A program operation allows to write the 2112-byte page in typical 200us and an erase operation can be performed in typical 1.5ms on a 128K-byte block.

Data in the page can be read out at 25ns cycle time per byte(x8). The I/O pins serve as the ports for address and data input/output as well as command input.

This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using \overline{CE} , \overline{WE} , \overline{RE} , ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the \overline{WP} input. The output pin R/\overline{B} (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/\overline{B} pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management. when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation: 1 bit error every 528byte (x8) can be detected. Due to this feature, it is no more nor necessary nor recommended to use external 2-bit ECC to detect copy back operation errors. Data read out after copy back read (both for single and multiplane cases) is allowed.

Even the write-intensive systems can take advantage of the HY27UG088G(5/D)B Series extended reliability of 100K program/erase cycles by supporting ECC (Error Correcting Code) with real time mapping-out algorithm. The chip supports \overline{CE} don't care function. This function allows the direct download of the code from the NAND Flash memory device by a micro-controller, since the \overline{CE} transitions do not stop the read operation.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The HY27UG088G(5/D)B Series are available in 48-TSOP1 12 x 20 mm, 52-ULGA 12 x 17mm.

1.1 Product List

| PART NUMBER | ORGANIZATION | Vcc RANGE | PACKAGE |
|--------------|--------------|-------------|----------|
| HY27UG088G5B | x8 | 2.7V ~ 3.6V | 48-TSOP1 |
| HY27UG088GDB | | | 52-ULGA |

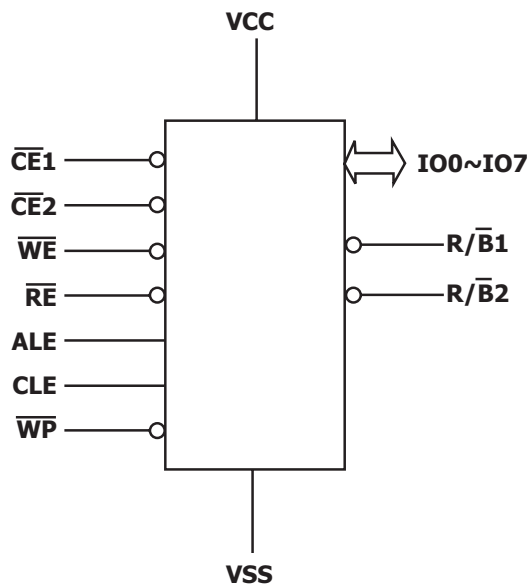


Figure1: Logic Diagram

| | |
|---|----------------------|
| IO7 - IO0 | Data Input / Outputs |
| CLE | Command latch enable |
| ALE | Address latch enable |
| $\overline{CE1}$, $\overline{CE2}$ | Chip Enable |
| \overline{RE} | Read Enable |
| \overline{WE} | Write Enable |
| \overline{WP} | Write Protect |
| R/ $\overline{B1}$, R/ $\overline{B2}$ | Ready / Busy |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

Table 1: Signal Names

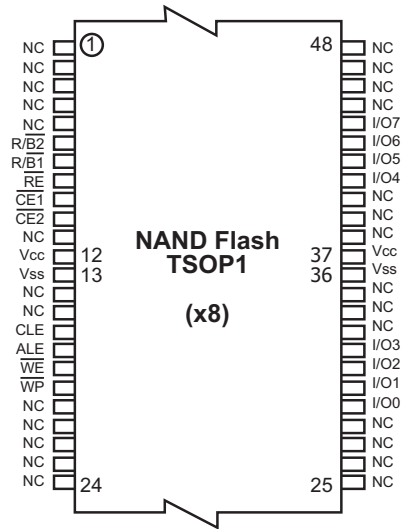
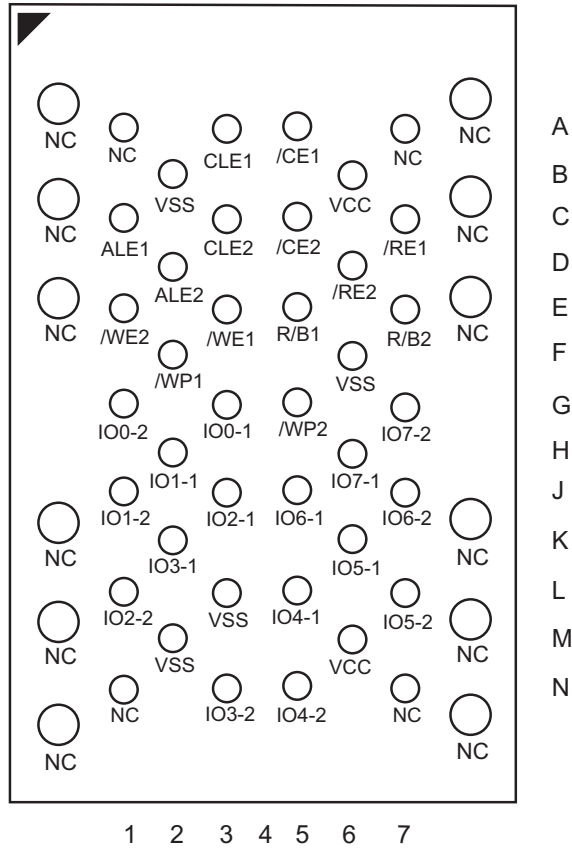


Figure 2. 48TSOP1 Contact, x8 Device



**Figure 3: 52-ULGA Contactions, x8 Device, Dual interface
(Top view through package)**

1.2 PIN DESCRIPTION

| Pin Name | Description |
|---|--|
| I00-I07 | DATA INPUTS/OUTPUTS The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (\overline{WE}). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled. |
| CLE | COMMAND LATCH ENABLE This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable (\overline{WE}). |
| ALE | ADDRESS LATCH ENABLE This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable (\overline{WE}). |
| $\overline{CE1}$, $\overline{CE2}$ | CHIP ENABLE This input controls the selection of the device. When the device is busy $\overline{CE1}$, $\overline{CE2}$ low does not deselect the memory. |
| \overline{WE} | WRITE ENABLE This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of \overline{WE} . |
| \overline{RE} | READ ENABLE The \overline{RE} input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t _{REA} after the falling edge of \overline{RE} which also increments the internal column address counter by one. |
| \overline{WP} | WRITE PROTECT The \overline{WP} pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. |
| R/ $\overline{B1}$, R/ $\overline{B2}$ | READY BUSY The Ready/Busy output is an Open Drain pin that signals the state of the memory. |
| V _{cc} | SUPPLY VOLTAGE The V _{cc} supplies the power for all the operations (Read, Write, Erase). |
| V _{ss} | GROUND |
| NC | NO CONNECTION |

Table 2: Pin Description
NOTE:

1. A 0.1uF capacitor should be connected between the V_{cc} Supply Voltage pin and the V_{ss} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever V_{CC} is below 1.8V (3.3V version) or 1.1V (1.8V) version to protect the device from any involuntary program/erase during power transitions.

| | IO0 | IO1 | IO2 | IO3 | IO4 | IO5 | IO6 | IO7 |
|------------------|------------|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 1st Cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| 2nd Cycle | A8 | A9 | A10 | A11 | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ |
| 3rd Cycle | A12 | A13 | A14 | A15 | A16 | A17 | A18 | A19 |
| 4th Cycle | A20 | A21 | A22 | A23 | A24 | A25 | A26 | A27 |
| 5th Cycle | A28 | A29 | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ | L ⁽¹⁾ |

Table 3: Address Cycle Map(x8)
NOTE:

1. L must be set to Low.

| FUNCTION | 1st CYCLE | 2nd CYCLE | 3rd CYCLE | 4th CYCLE | Acceptable command during busy |
|-------------------------------------|------------------|------------------|------------------|------------------|---------------------------------------|
| READ1 | 00h | 30h | - | - | |
| READ FOR COPY-BACK | 00h | 35h | - | - | |
| READ ID | 90h | - | - | - | |
| RESET | FFh | - | - | - | Yes |
| PAGE PROGRAM | 80h | 10h | - | - | |
| COPY BACK PGM | 85h | 10h | - | - | |
| MULTI PLANE PROGRAM | 80h | 11h | 81h | 10h | |
| MULTI PLANE COPYBACK PROGRAM | 85h | 11h | 81h | 10h | |
| BLOCK ERASE | 60h | D0h | - | - | |
| MULTI PLANE BLOCK ERASE | 60h | 60h | D0h | - | |
| READ STATUS REGISTER | 70h | - | - | - | Yes |
| RANDOM DATA INPUT | 85h | - | - | - | |
| RANDOM DATA OUTPUT | 05h | E0h | - | - | |
| READ CACHE (RANDOM) | 00h | 31h | - | - | |
| READ CACHE (SEQUENTIAL) | 31h | - | - | - | |
| READ CACHE END | 3Fh | - | - | - | |
| READ EDC STATUS REGISTER | 7Bh | - | - | - | |

Table 4: Command Set

| CLE | ALE | $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{RE}}$ | $\overline{\text{WP}}$ | MODE | |
|-----|-----|------------------------|------------------------|------------------------|------------------------|---------------------------------|-------------------------|
| H | L | L | Rising | H | X | Read Mode | Command Input |
| L | H | L | Rising | H | X | | Address Input(5 cycles) |
| H | L | L | Rising | H | H | Write Mode | Command Input |
| L | H | L | Rising | H | H | | Address Input(5 cycles) |
| L | L | L | Rising | H | H | Data Input | |
| L | L | L ⁽¹⁾ | H | Falling | X | Sequential Read and Data Output | |
| L | L | L | H | H | X | During Read (Busy) | |
| X | X | X | X | X | H | During Program (Busy) | |
| X | X | X | X | X | H | During Erase (Busy) | |
| X | X | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/Vcc | Stand By | |

Table 5: Mode Selection
NOTE:

1. With the $\overline{\text{CE}}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 3ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 12 for details of the timings requirements. Command codes are always applied on IO7:0 regardless of the bus configuration. (x8)

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses for the 8Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 12 for details of the timings requirements. Addresses are always applied on IO7:0 regardless of the bus configuration (x8).

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 7 and Table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 8,9,11,12,13 and Table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modifying operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read.

This operation is operated by writing 00h and 30h to the command register along with five address cycles.

Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes (x8) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Page Program.

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8 times. The addressing should be done on each pages in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The bytes other than those to be programmed do not need to be loaded. The device supports random data input in a page.

The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.

The command register remains in Read Status command mode until another valid command is written to the command register. Figure 15 details the sequence.

3.3 Multi Plane Program.

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.

A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane ($A<18>=0$). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (t_{DDBSY}). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane ($A<18>=1$). The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by $\overline{R/B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (t_{DDBSY}). In case of fail in 1st or 2nd page program, fail bit of status register will be set: Device supports pass/fail status of each plane. Figure 20 details the sequence.

3.4 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in there cycles initiated by an Erase Setup command (60h). Only address A18 to A29 is valid while A12 to A17 is ignored (x8). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of an erase by monitoring the $\overline{R/B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 19 details the sequence.

3.5 Multi Plane Erase.

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.

Block erase setup command (60h) must be repeated two times, each time followed by 1st block and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multiplane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion. Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program. Figure 21 details the sequence

3.6 Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register.

When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 17 & Figure 18). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure18.

Copy-back program operation is allowed only within same plane.

3.7 Multi-Plane Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also need to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling \overline{RE} (See Figure 21), or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 22.

Most NAND devices require 2 bit external ECC only due to copy back operation while 1 bit ECC can be enough for all other operation. Reason is that during read for copy back + copy back program sequence a bit error due to charge loss is not checked by external error detection/correction scheme. On the contrary, 8Gbit NAND includes automatic Error Detection Code during copy back operation: thanks to this, 2 bit external ECC is no more required, with significant advantage for customers that can always use single bit ECC. More details on EDC operation are available in section 3.8.

3.8 EDC Operation

Error Detection Code check automatically starts immediately after device becomes busy for a copy back program operation (both single and multiple plane). In the x8 version EDC allows detection of 1 single bit error every 528 bytes, where each 528byte group is composed by 512 bytes of main array and 16 bytes of spare area (see Table 20) So described 528byte area is called "EDC unit".

To Properly use EDC, some limitations apply:

- Random data input can be used only once in copy back program or page program or multiple page program, unless user inputs data for a whole EDC unit (or more whole EDC units).
- Any page program operation must be done on whole page basis, or on whole EDC unit (s).

EDC result can be checked only during copy back program through 7Bh (specific Read EDC register command, Table 21)

3.9 Read Status Register.

The device contains a Status Register which may be read to find out whether, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/\overline{B} pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random data output, the read command (00h) should be given before starting read cycles.

3.10 Read EDC Status Register

The operation is available only in copy back program and it allows the detection of errors occurred during read for copy back. In case of multiple plane copy back, it is not possible to know which of the two read operation caused the error. After writing 7Bh command to the command register, a read cycle outputs the content of the EDC Register to the I/O pins on the falling edge of CE or RE, whichever occurs last.

Operation is same read status register command. Refer to below Table 21 for specific EDC Register definitions.

3.11 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 23 shows the operation sequence, while tables 14 explain the byte meaning.

3.12 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/\overline{B} pin goes low for tRST after the Reset command is written. Refer to Figure 26.

3.13 Cache Read

Cache read operation allows automatic download of consecutive pages. Immediately after 1st latency end, while user can start reading out data, device internally starts reading following page.

Start address of 1st page is at page start (A<10:0>=00h), after 1st latency time (tr), automatic data download will be uninterrupted. In fact latency time is 25us, while download of a page require at least 100us for x8 device. (50us for x16device).

The Cache Read function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read function. Issuing an additional Cache Read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.

Refer to Figure 14.

Cache Read operation must be done only block by block if system needs to avoid reading also reading from invalid blocks.

4. OTHER FEATURES

4.1 Data Protection & Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{cc} is below about 2.0V(3.3V device). \overline{WP} pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10 μ s is required before internal circuit gets ready for any command sequences as shown in Figure 26. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/\overline{B} pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/\overline{B} outputs to be Or-tied.

Because pull-up resistor value is related to $t_{R(\overline{B})}$ and current drain during busy (I_{busy}), an appropriate value can be obtained with the following reference chart (Fig 27). Its value can be determined by the following guidance.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------|--------|------|-----|------|--------|
| Valid Block Number | NVB | 8032 | - | 8192 | Blocks |

Table 6 : Valid Blocks Numbers

NOTE:

1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. The number of valid blocks is for single plane & multi-plane operations.
3. Each chip has maximum 80 invalid blocks.

| Symbol | Parameter | Value | Unit |
|----------------|--|-------------|------|
| T_A | Ambient Operating Temperature (Commercial Temperature Range) | 0 to 70 | °C |
| | Ambient Operating Temperature (Industrial Temperature Range) | -40 to 85 | °C |
| T_{BIAS} | Temperature Under Bias | -50 to 125 | °C |
| T_{STG} | Storage Temperature | -65 to 150 | V |
| $V_{IO}^{(2)}$ | Input or Output Voltage | -0.6 to 4.6 | V |
| V_{CC} | Supply Voltage | -0.6 to 4.6 | V |

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

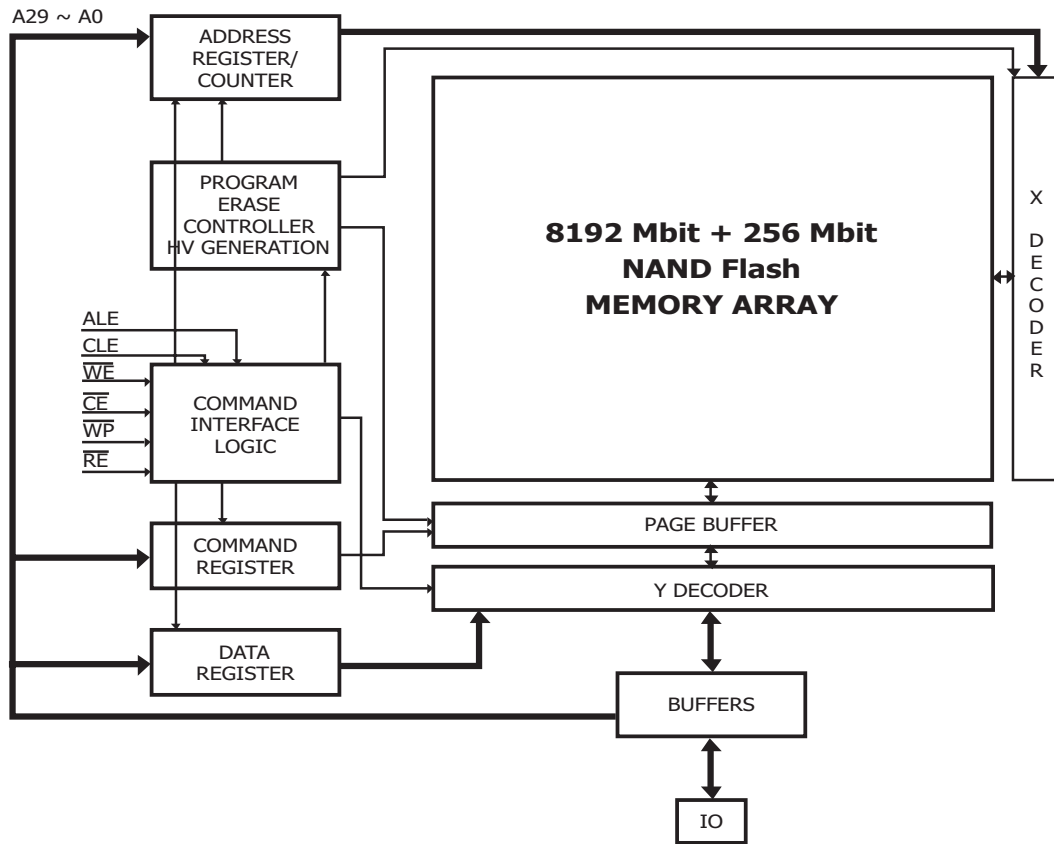


Figure 4: Block Diagram

| Parameter | | Symbol | Test Conditions | 3.3Volt | | | Unit |
|---------------------------|-----------------|--------------------------|---|---------------------|-----|----------------------|------|
| | | | | Min | Typ | Max | |
| Operating Current | Sequential Read | I _{CC1} | t _{RC} =25ns CE=V _{IL} , I _{OUT} =0mA | - | 15 | 30 | mA |
| | Program | I _{CC2} | - | - | 15 | 30 | mA |
| | Erase | I _{CC3} | - | - | 15 | 30 | mA |
| Stand-by Current (TTL) | | I _{CC4} | CE=V _{IH} , WP=0V/V _{CC} | - | | 1 | mA |
| Stand-by Current (CMOS) | | I _{CC5} | CE=V _{CC} -0.2, WP=0V/V _{CC} | - | 20 | 100 | uA |
| Input Leakage Current | | I _{LI} | V _{IN} =0 to V _{CC} (max) | - | - | ± 20 | uA |
| Output Leakage Current | | I _{LO} | V _{OUT} =0 to V _{CC} (max) | - | - | ± 20 | uA |
| Input High Voltage | | V _{IH} | - | 0.8xV _{CC} | - | V _{CC} +0.3 | V |
| Input Low Voltage | | V _{IL} | - | -0.3 | - | 0.2xV _{CC} | V |
| Output High Voltage Level | | V _{OH} | I _{OH} =-400uA | 2.4 | - | - | V |
| Output Low Voltage Level | | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | V |
| Output Low Current (R/B) | | I _{OL} (R/B) | V _{OL} =0.4V | 8 | 10 | - | mA |

Table 8: DC and Operating Characteristics

| Parameter | Value |
|--------------------------------|------------------------|
| | 3.3Volt |
| Input Pulse Levels | 0V to VCC |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | VCC/2 |
| Output Load (2.7V - 3.6V) | 1 TTL GATE and CL=50pF |

Table 9: AC Conditions

| Item | Symbol | Test Condition | Min | Max | Unit |
|----------------------------|------------------|---------------------|-----|-----|------|
| Input / Output Capacitance | C _{I/O} | V _{IL} =0V | - | 20 | pF |
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 20 | pF |

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------------------|-----|-----|----------------|--------|
| Program Time / Multi-Plane Program Time | t _{PROG} | - | 200 | 700 | us |
| Dummy Busy Time for Two Plane Program | t _{DBSY} | - | 0.5 | 1 | us |
| Number of partial Program Cycles in the same page | NOP | - | - | 8 | Cycles |
| Block Erase Time / Multi-Plane Block Erase Time | t _{BERS} | - | 1.5 | 2 | ms |
| Read Cache Busy Time | t _{RCBSY} | - | 3 | t _R | us |

Table 11: Program / Erase Characteristics

| Parameter | Symbol | 3.3V | | Unit |
|--|--------------------|------|-------------------------|------|
| | | Min | Max | |
| CLE Setup time | tCLS | 12 | | ns |
| CLE Hold time | tCLH | 5 | | ns |
| \overline{CE} setup time | tCS | 20 | | ns |
| \overline{CE} hold time | tCH | 5 | | ns |
| \overline{WE} pulse width | tWP | 12 | | ns |
| ALE setup time | tALS | 12 | | ns |
| ALE hold time | tALH | 5 | | ns |
| Data setup time | tDS | 12 | | ns |
| Data hold time | tDH | 5 | | ns |
| Write Cycle time | tWC | 25 | | ns |
| \overline{WE} High hold time | tWH | 10 | | ns |
| Data Transfer from Cell to register | tr | | 25 | us |
| ALE to \overline{RE} Delay | tAR | 10 | | ns |
| CLE to \overline{RE} Delay | tCLR | 10 | | ns |
| Ready to \overline{RE} Low | tRR | 20 | | ns |
| \overline{RE} Pulse Width | tRP | 12 | | ns |
| \overline{WE} High to Busy | tWB | | 100 | ns |
| Read Cycle Time | tRC | 25 | | ns |
| \overline{RE} Access Time | tREA | | 20 | ns |
| \overline{RE} High to Output High Z | tRHZ | | 100 | ns |
| \overline{CE} High to Output High Z | tCHZ | | 50 | ns |
| \overline{CE} High to Output hold | tCOH | 15 | | ns |
| \overline{RE} High to Output Hold | tRHOH | 15 | | ns |
| \overline{RE} Low to Output Hold | tRLOH | 5 | | ns |
| \overline{RE} High Hold Time | tREH | 10 | | ns |
| Output High Z to \overline{RE} low | tIR | 0 | | ns |
| \overline{CE} Low to \overline{RE} Low | tCR | 10 | | ns |
| Address to data loading time | tADL | 70 | | ns |
| \overline{WE} High to \overline{RE} low | tWHR | 80 | | ns |
| \overline{RE} High to \overline{WE} low | tRHW | 100 | | ns |
| Device Resetting Time (Read / Program / Erase) | tRST | | 5/10/500 ⁽¹⁾ | us |
| Write Protection time | tww ⁽²⁾ | 100 | | ns |

Table 12: AC Timing Characteristics
NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. Program / Erase Enable Operation : \overline{WP} high to \overline{WE} High.
Program / Erase Disable Operation : \overline{WP} Low to \overline{WE} High.

| IO | Page Program | Block Erase | Read | Cache Read | CODING |
|----|---------------|---------------|---------------|----------------------|--------------------------------------|
| 0 | Pass / Fail | Pass / Fail | NA | NA | Pass: '0' Fail: '1' |
| 1 | NA | NA | NA | NA | - |
| 2 | NA | NA | NA | NA | - |
| 3 | NA | NA | NA | NA | - |
| 4 | NA | NA | NA | NA | - |
| 5 | Ready / Busy | Ready / Busy | Ready / Busy | P/E/R Controller Bit | Active: '0' Idle:'1' |
| 6 | Ready / Busy | Ready / Busy | Ready / Busy | Ready/Busy | Busy: '0' Ready:'1' |
| 7 | Write Protect | Write Protect | Write Protect | NA | Protected: '0' Not Protected: '1' |

Table 13 : Status Register Coding

| DEVICE IDENTIFIER CYCLE | DESCRIPTION |
|-------------------------|---|
| 1st | Manufacturer Code |
| 2nd | Device Identifier |
| 3rd | Internal chip number, cell Type, etc. |
| 4th | Page Size, Block Size, Spare Size, Organization |
| 5th | Multiplane information |

Table 14: Device Identifier Coding

| Part Number | Voltage | Bus Width | 1st cycle (Manufacture Code) | 2nd cycle (Device Code) | 3rd cycle | 4th cycle | 5th cycle |
|------------------|---------|-----------|------------------------------|-------------------------|-----------|-----------|-----------|
| HY27UG088G(5/D)B | 3.3V | x8 | ADh | DCh | 10h | 95h | 54h |

Table 15: Read ID Data Table

| | Description | IO7 | IO6 | IO5 IO4 | IO3 IO2 | IO1 IO0 |
|---|---------------|-----|-----|---------|---------|---------|
| Die / Package | 1 | | | | | 0 0 |
| | 2 | | | | | 0 1 |
| | 4 | | | | | 1 0 |
| | 8 | | | | | 1 1 |
| Cell Type | 2 Level Cell | | | | 0 0 | |
| | 4 Level Cell | | | | 0 1 | |
| | 8 Level Cell | | | | 1 0 | |
| | 16 Level Cell | | | | 1 1 | |
| Number of Simultaneously Programmed Pages | 1 | | | 0 0 | | |
| | 2 | | | 0 1 | | |
| | 4 | | | 1 0 | | |
| | 8 | | | 1 1 | | |
| Interleave Program Between Multiple chips | Not Supported | | 0 | | | |
| | Supported | | 1 | | | |
| Write Cache | Not Supported | 0 | | | | |
| | Supported | 1 | | | | |

Table 16: 3rd Byte of Device Identifier Description

| | Description | IO7 | IO6 | IO5-4 | IO3 | IO2 | IO1-0 |
|----------------------------------|-------------|-----|-----|-------|-----|-----|-------|
| Page Size (Without Spare Area) | 1KB | | | | | | 0 0 |
| | 2KB | | | | | | 0 1 |
| | 4KB | | | | | | 1 0 |
| | 8KB | | | | | | 1 1 |
| Spare Area Size (Byte / 512Byte) | 8 | | | | | 0 | |
| | 16 | | | | | 1 | |
| Serial Access Time | 50ns | 0 | | | 0 | | |
| | 30ns | 0 | | | 1 | | |
| | 25ns | 1 | | | 0 | | |
| | Reserved | 1 | | | 1 | | |
| Block Size (Without Spare Area) | 64K | | | 0 0 | | | |
| | 128K | | | 0 1 | | | |
| | 256K | | | 1 0 | | | |
| | 512KB | | | 1 1 | | | |
| Organization | X8 | | 0 | | | | |
| | X16 | | 1 | | | | |

Table 17: 4th Byte of Device Identifier Description

| | Description | I07 | I06 | I05 | I04 | I03 | I02 | I01 | I00 |
|------------------------------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Plane Number | 1 | | | | | 0 | 0 | | |
| | 2 | | | | | 0 | 1 | | |
| | 4 | | | | | 1 | 0 | | |
| | 8 | | | | | 1 | 1 | | |
| Plane Size (w/o redundant Area) | 64Mb | | 0 | 0 | 0 | | | | |
| | 128Mb | | 0 | 0 | 1 | | | | |
| | 256Mb | | 0 | 1 | 0 | | | | |
| | 512Mb | | 0 | 1 | 1 | | | | |
| | 1Gb | | 1 | 0 | 0 | | | | |
| | 2Gb | | 1 | 0 | 1 | | | | |
| | 4Gb | | 1 | 1 | 0 | | | | |
| | 8Gb | | 1 | 1 | 1 | | | | |
| Reserved | | 0 | | | | | 0 | 0 | |

Table 18: 5rd Byte of Device Identifier Description

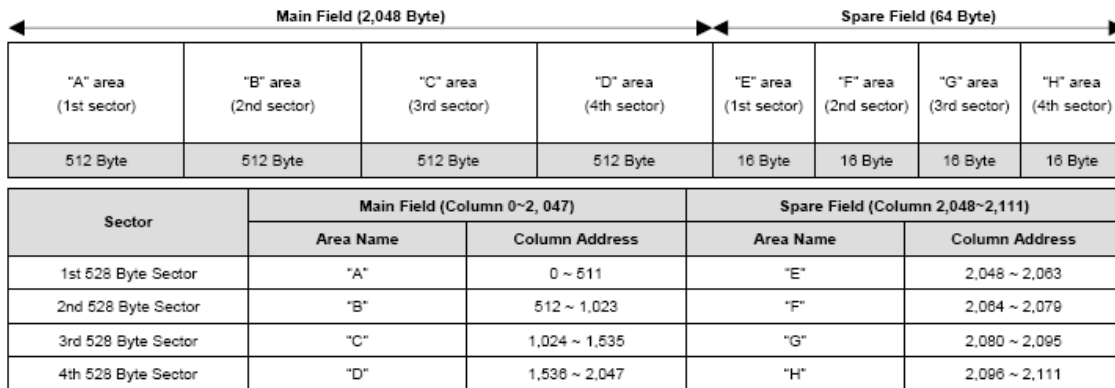


Table 19: Page organization in EDC units (x8)

| IO | Copy back Program | CODING |
|----|-------------------|-----------------------------------|
| 0 | Pass/Fail | Pass: Fail: '1' |
| 1 | EDC status | NO error: '0' |
| 2 | EDC Validity | Invalid: '0' Valid: '1' |
| 3 | NA | - |
| 4 | NA | - |
| 5 | Ready/Busy | Busy: '0' Ready: '1' |
| 6 | Ready/Busy | Busy: '0' Ready: '1' |
| 7 | Write Protect | Protected: '0' Not Protected: '1' |

Table 20: EDC Register Coding

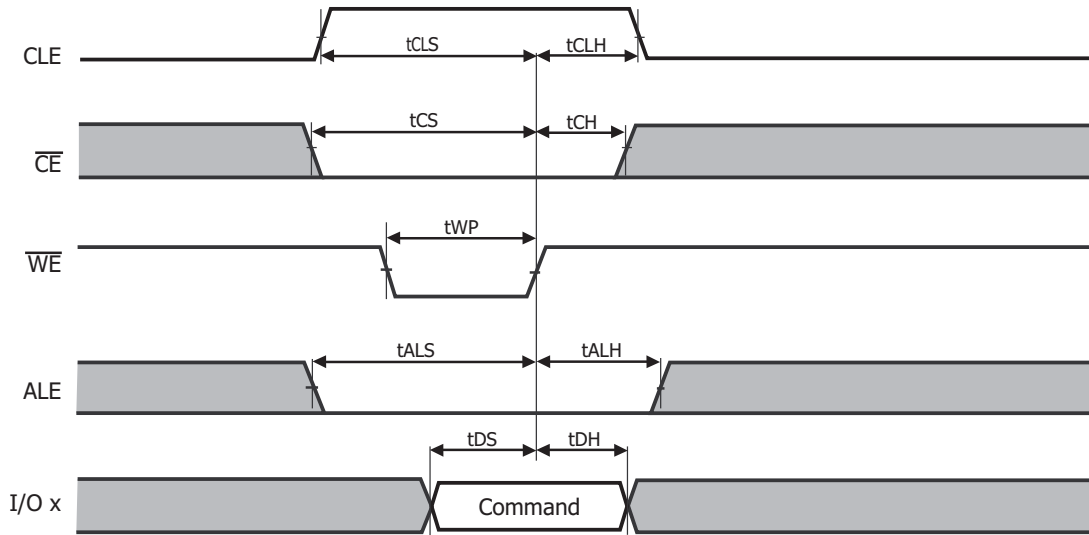


Figure 5: Command Latch Cycle

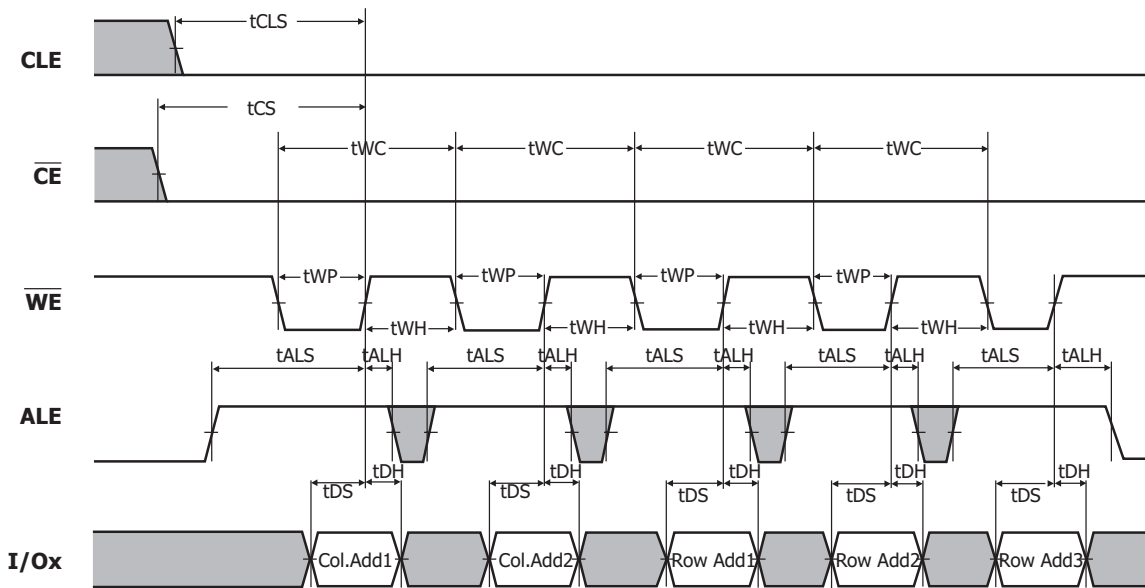


Figure 6: Address Latch Cycle

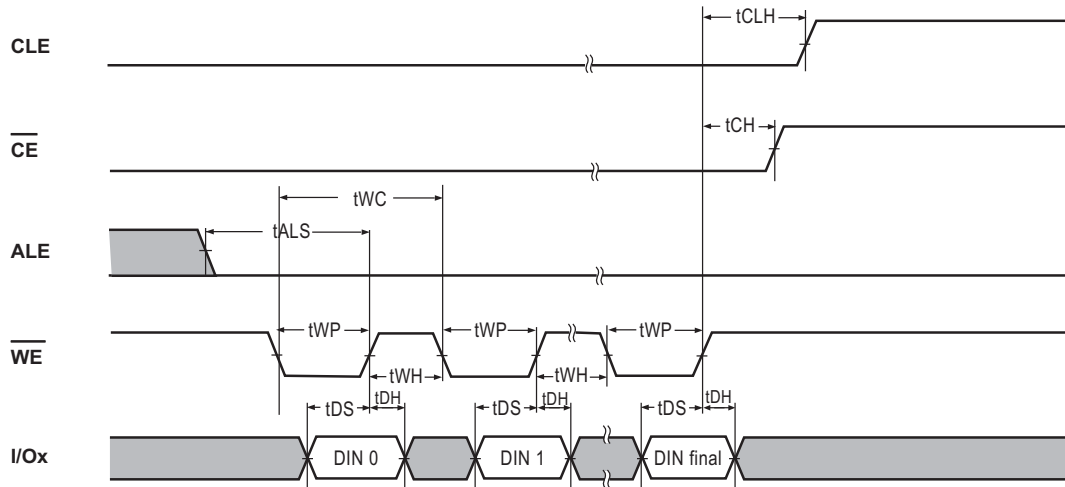
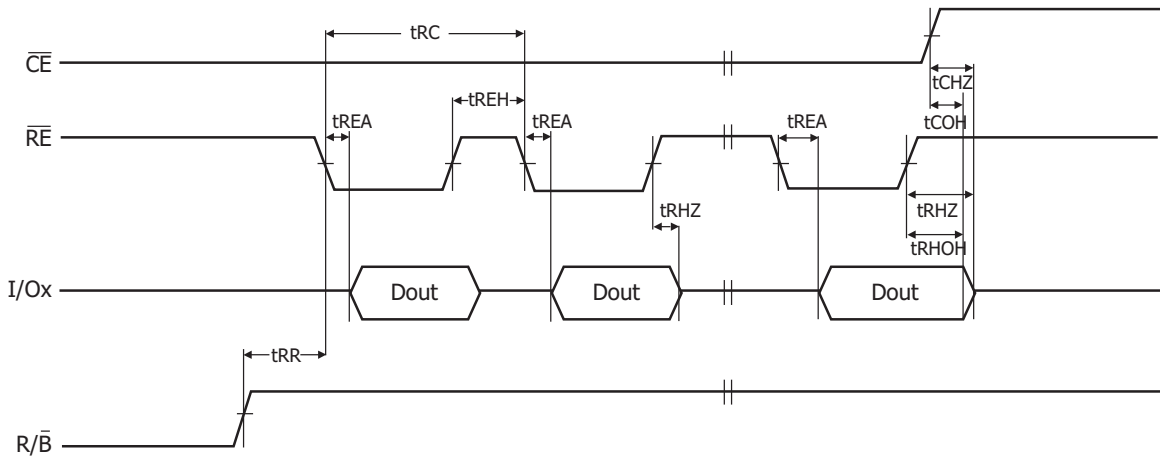
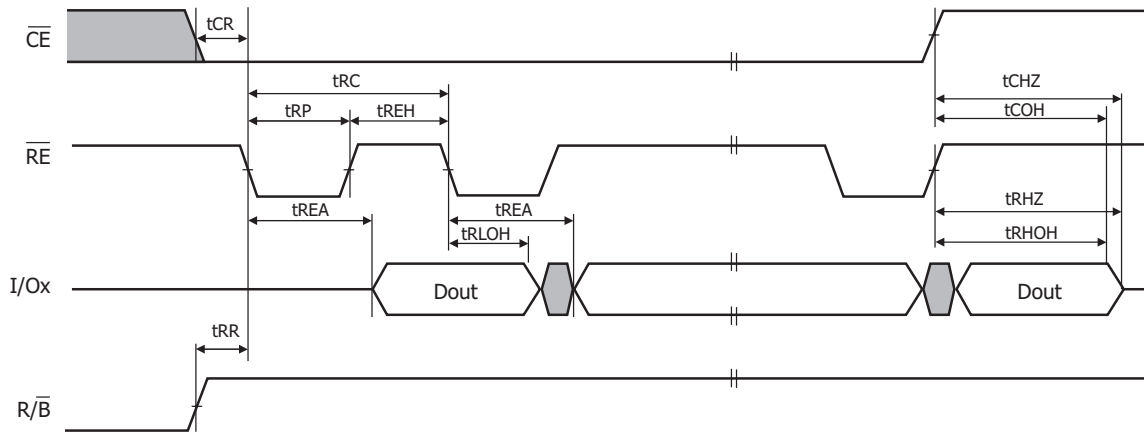


Figure 7: Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (t_{CHZ} , t_{RHZ})
 t_{RLOH} is valid when frequency is higher than 33MHz.
 t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read (CLE=L, \overline{WE} =H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (t_{CHZ} , t_{RHZ})
 t_{RLOH} is valid when frequency is higher than 33MHz.
 t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read (EDO Type CLE=L, \overline{WE} =H, ALE=L)

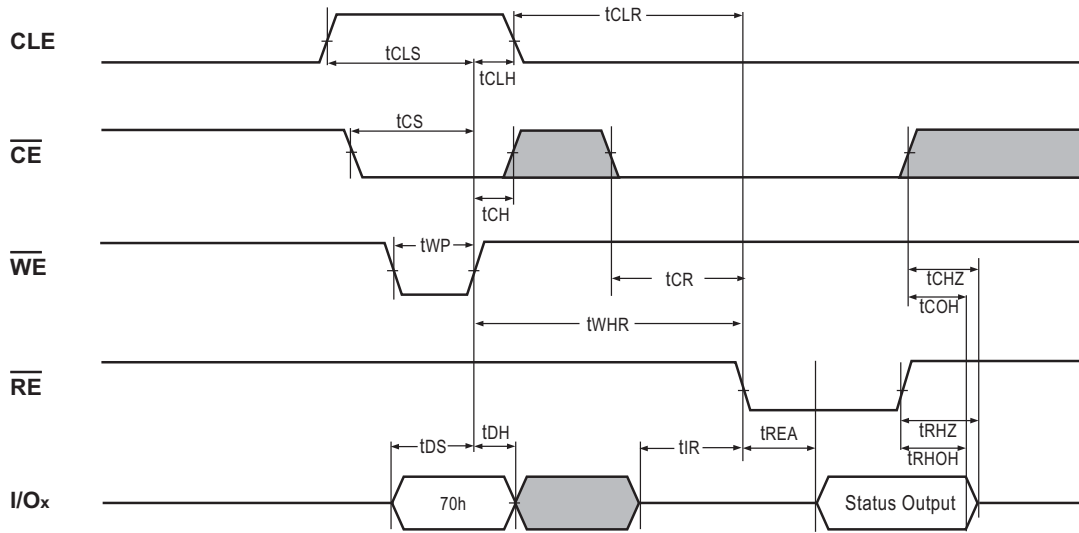


Figure 10: Status Read Cycle

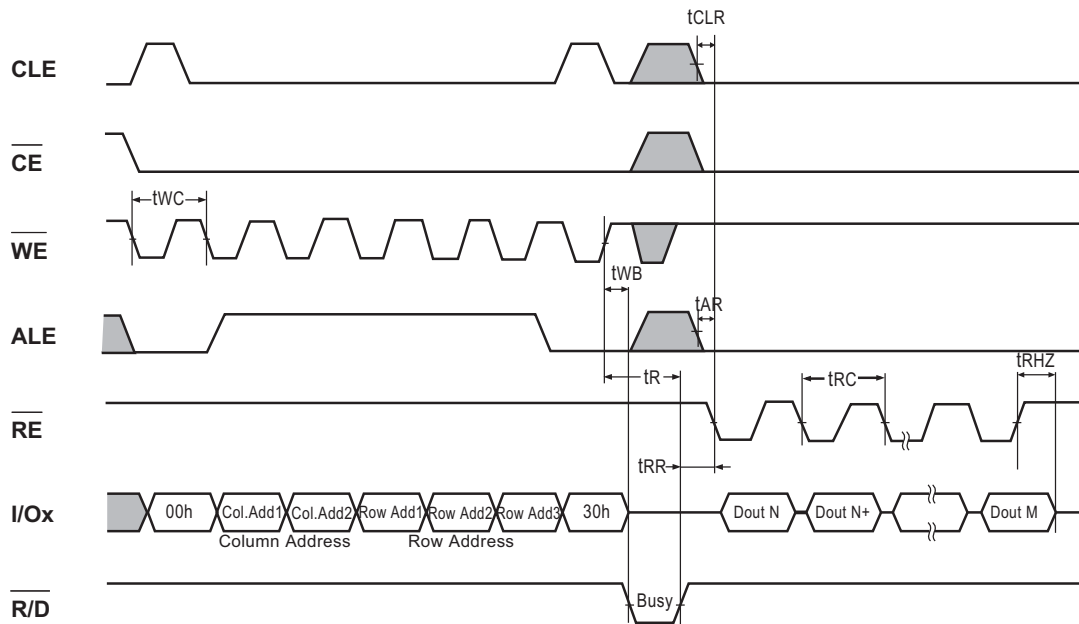


Figure 11: Read1 Operation (Read One Page)

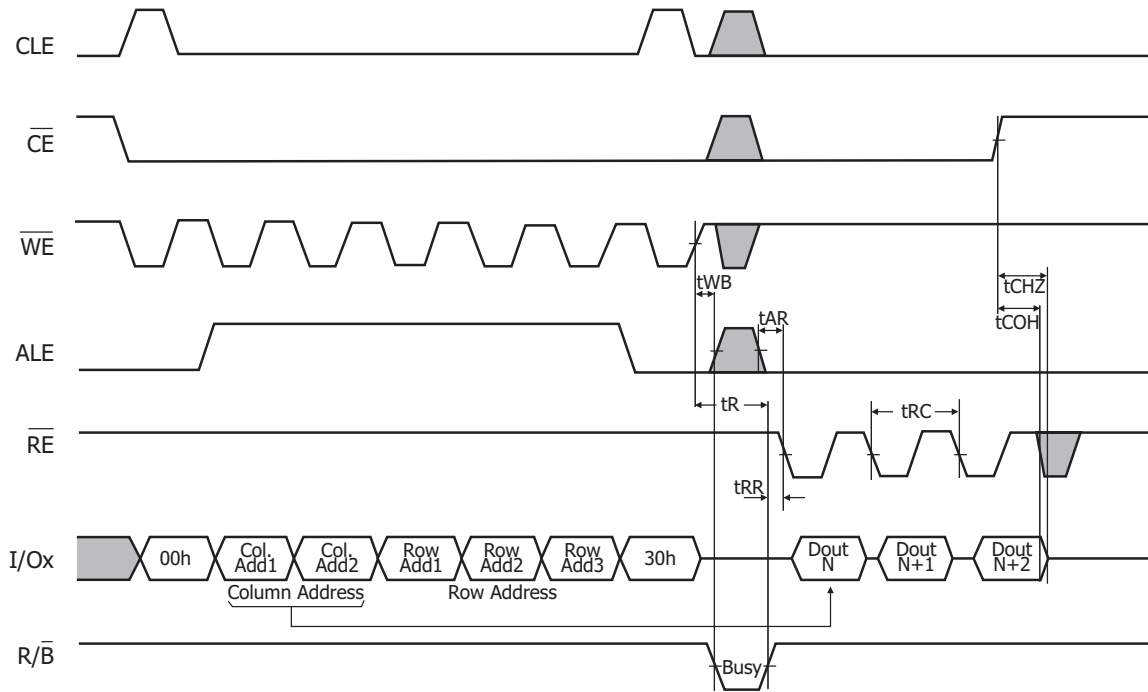


Figure 12: Read1 Operation intercepted by \overline{CE}

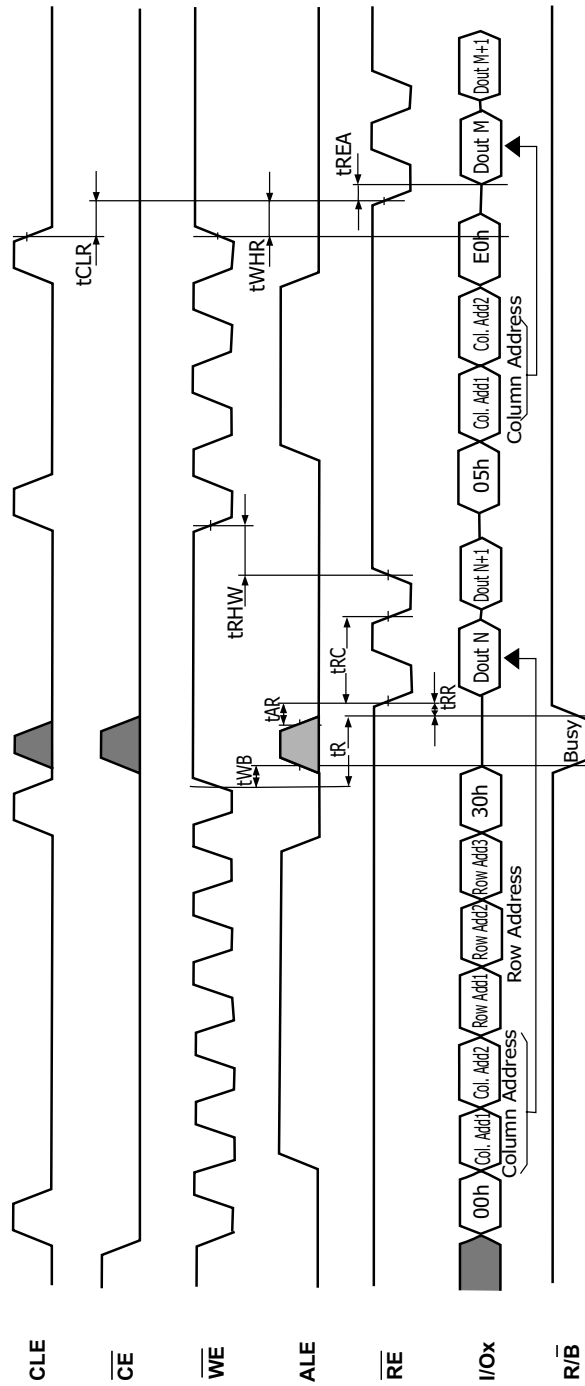


Figure 13: Random Data output

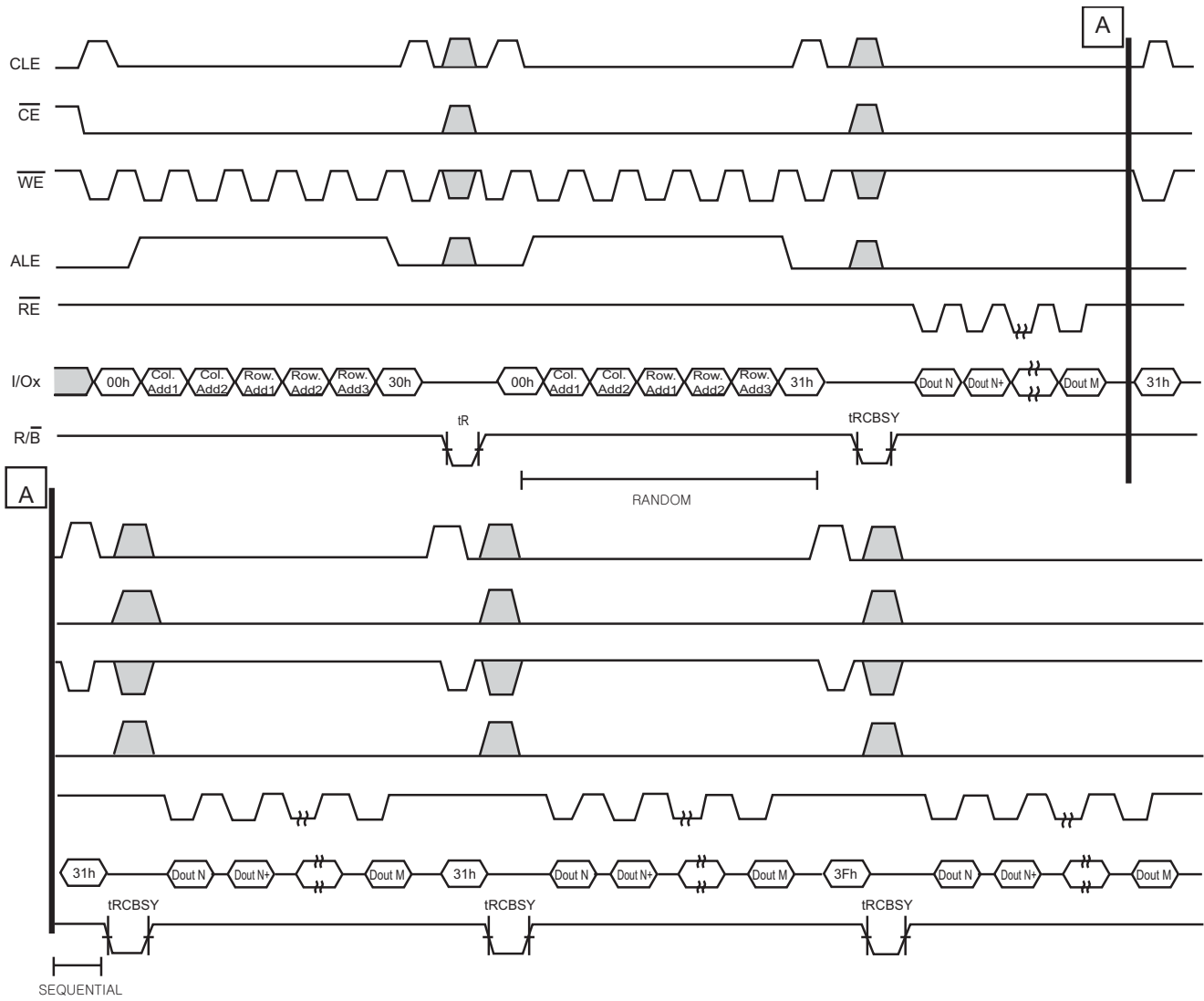


Figure 14: Read Operation with Read Cache

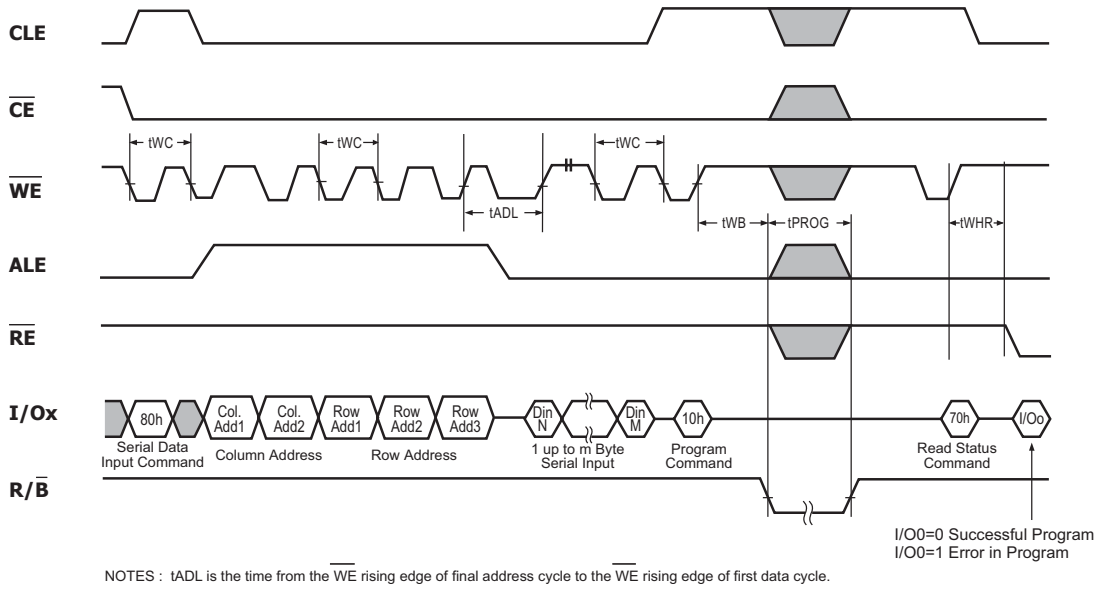
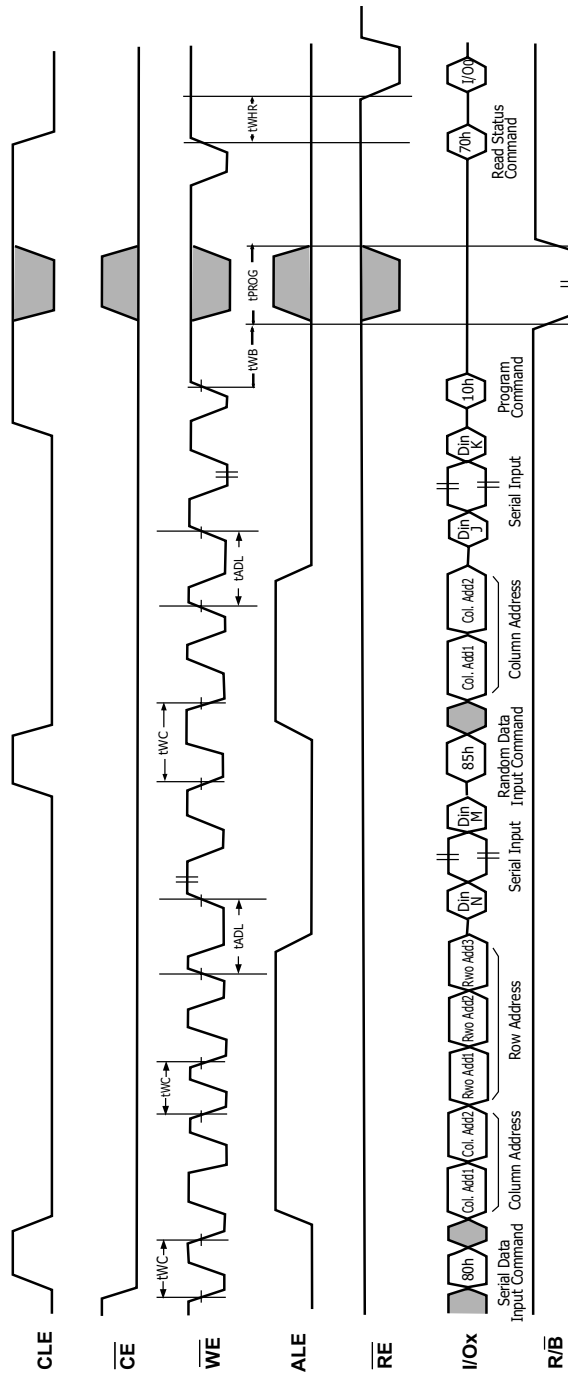


Figure 15: Page Program Operation



NOTES : 1. t_{ADL} is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.

Figure 16: Random Data In

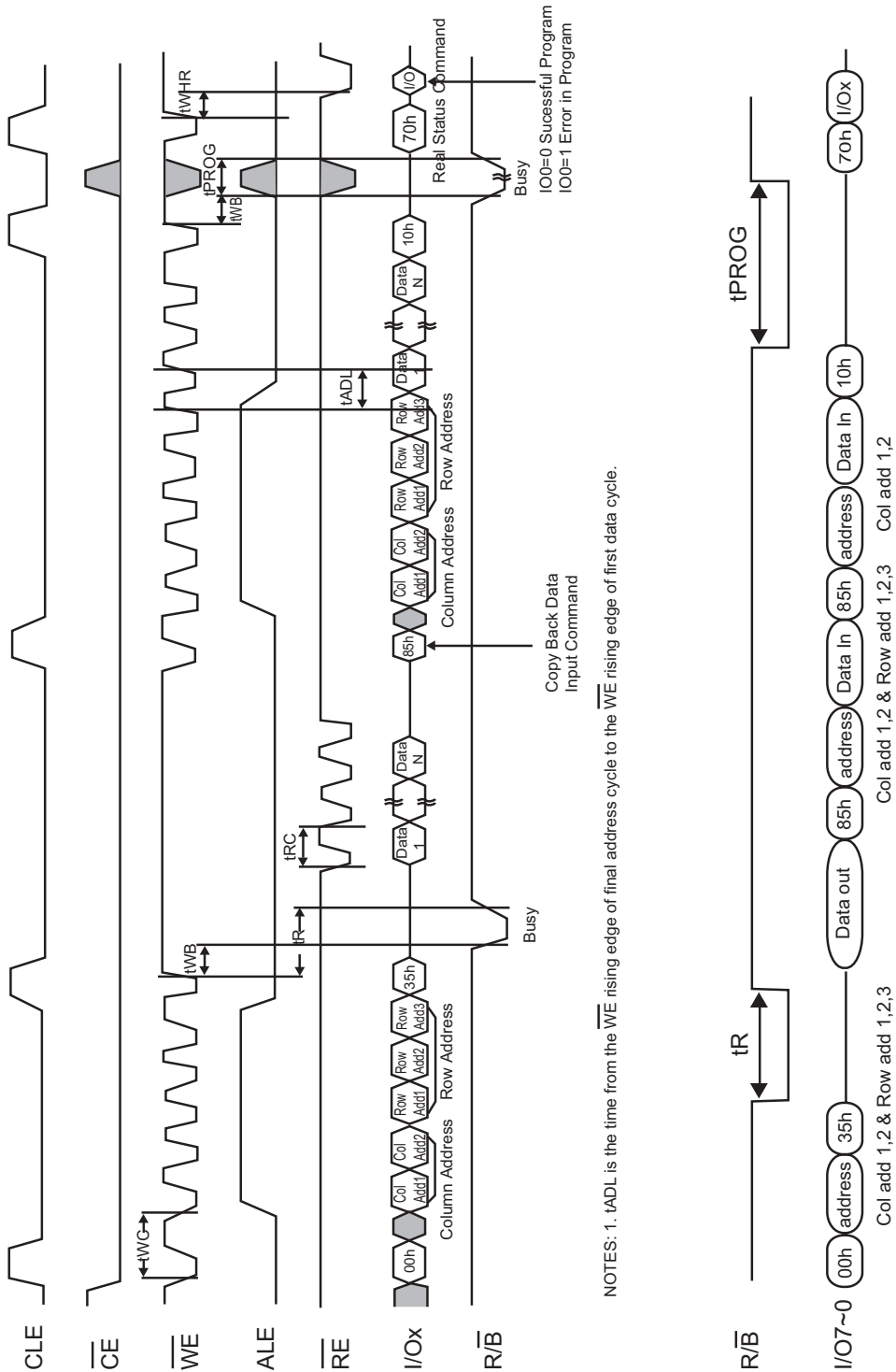


Figure 18: Copy Back Program Operation with Random Data Input

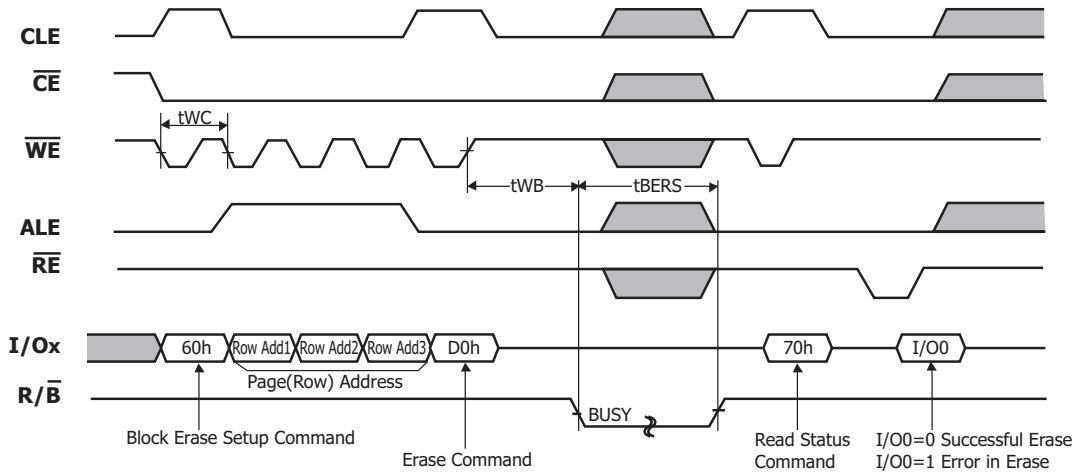


Figure 19: Block Erase Operation (Erase One Block)

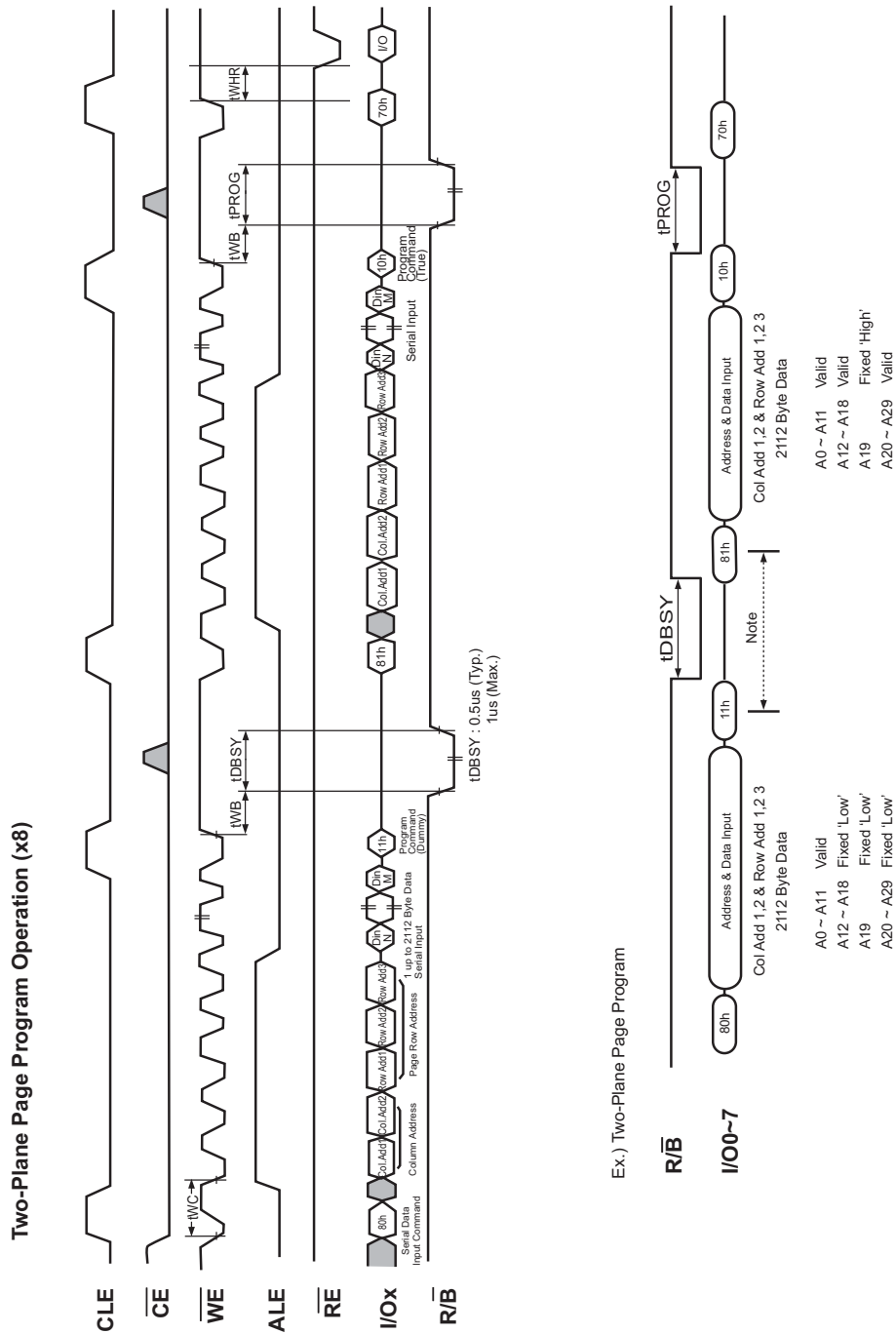
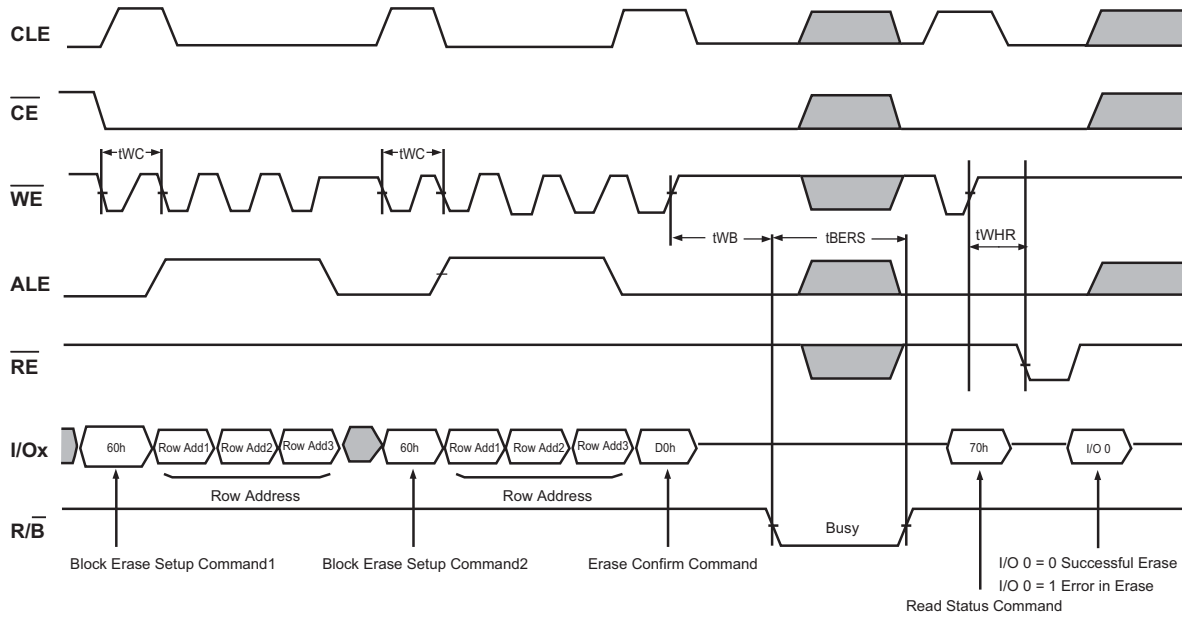


Figure 20: Multiple plane page program



Ex.) Address Restriction for Two-Plane Block Erase Operation

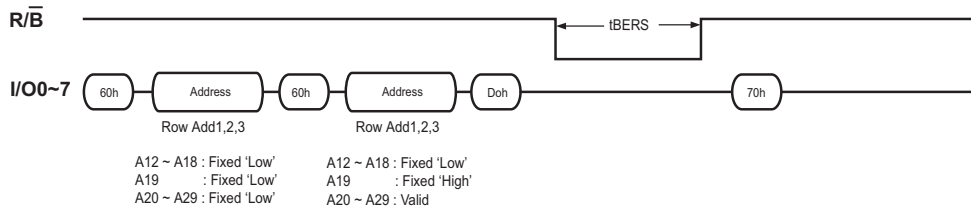


Figure 21: Multiple plane erase operation

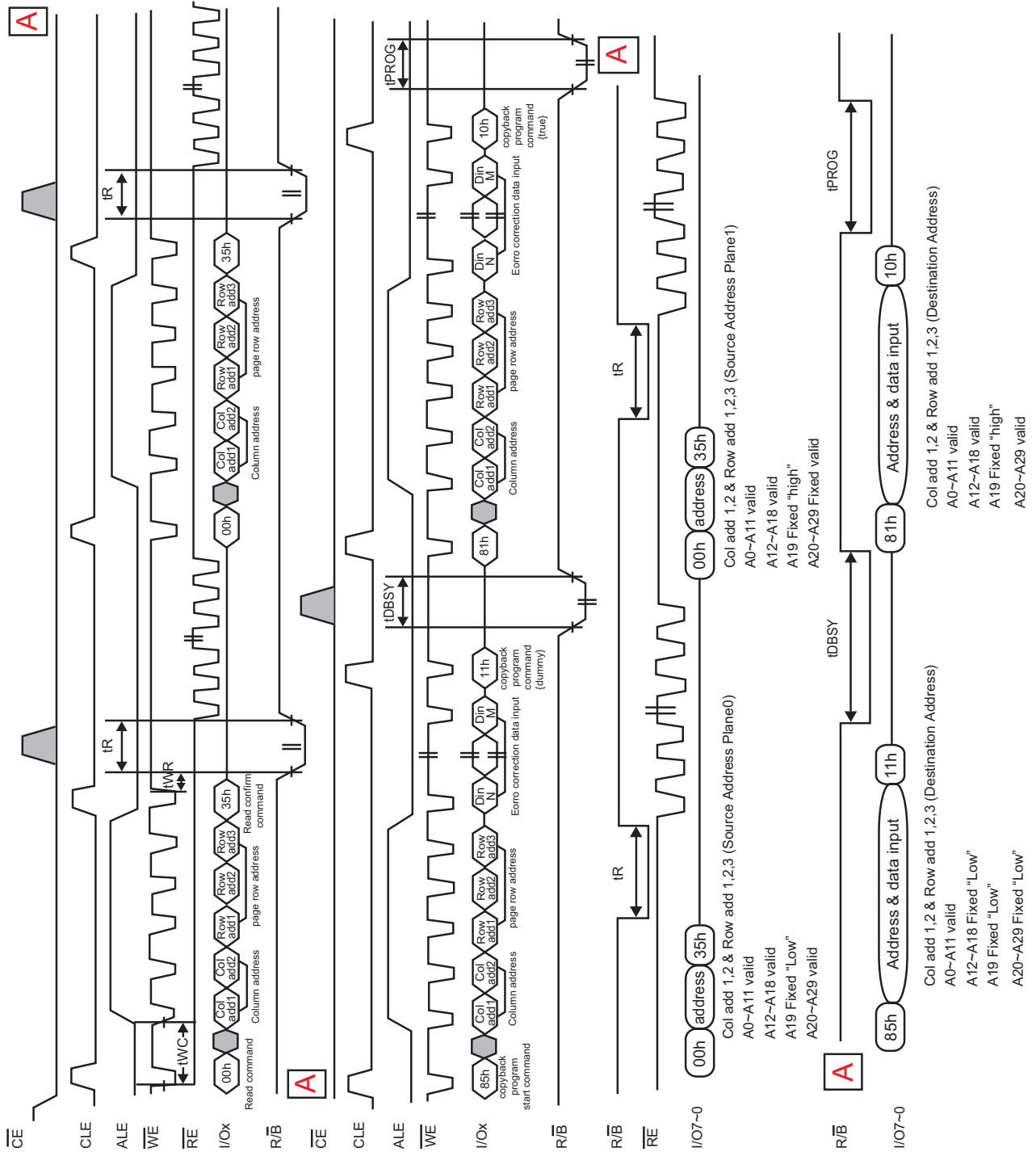


Figure 22: Multi plane copyback program Operation

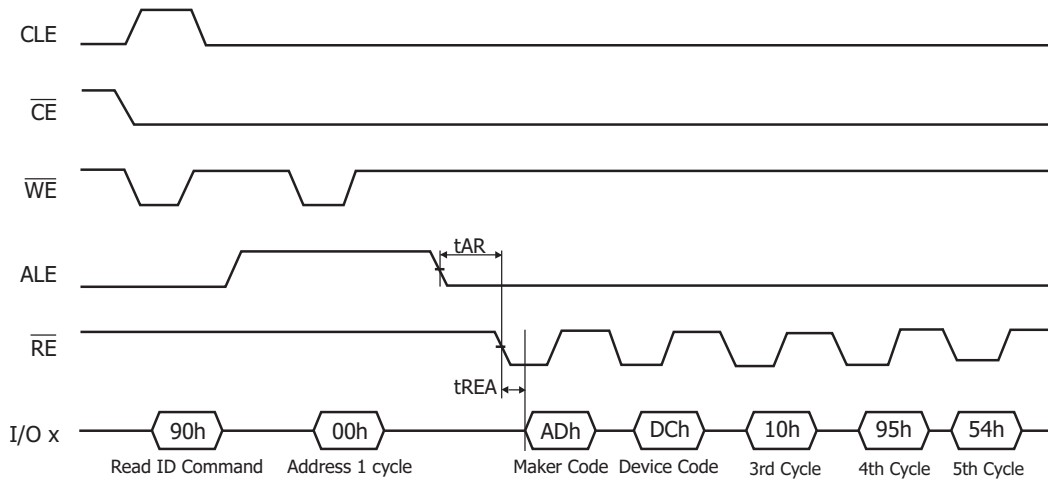


Figure 23: Read ID Operation

System Interface Using \overline{CE} don't care

To simplify system interface, \overline{CE} may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make \overline{CE} don't care read operation was disabling of the automatic sequential read function.

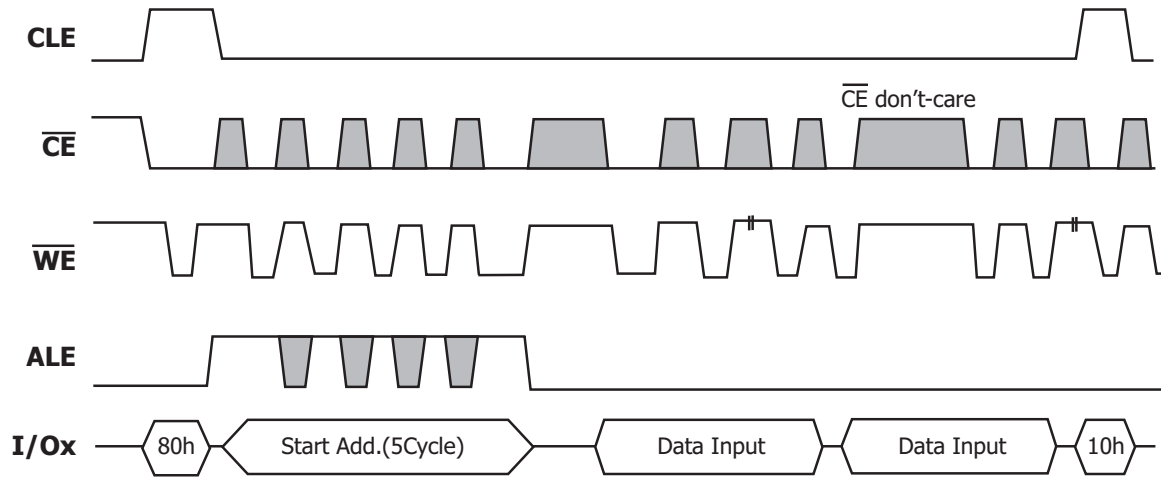


Figure 24: Program Operation with \overline{CE} don't-care.

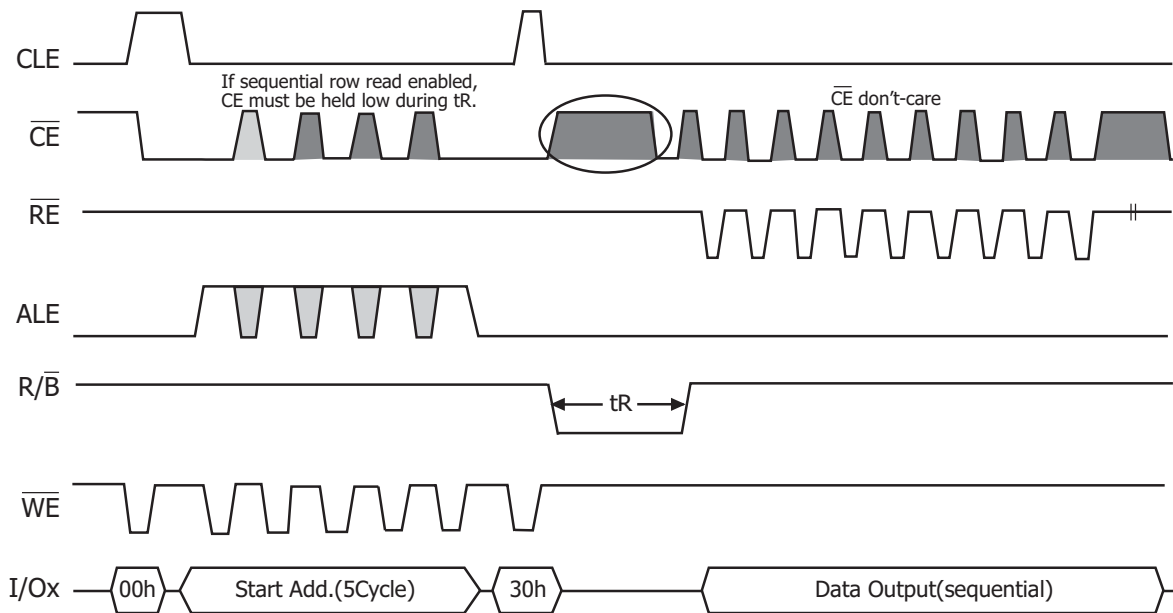


Figure 25: Read Operation with \overline{CE} don't-care.

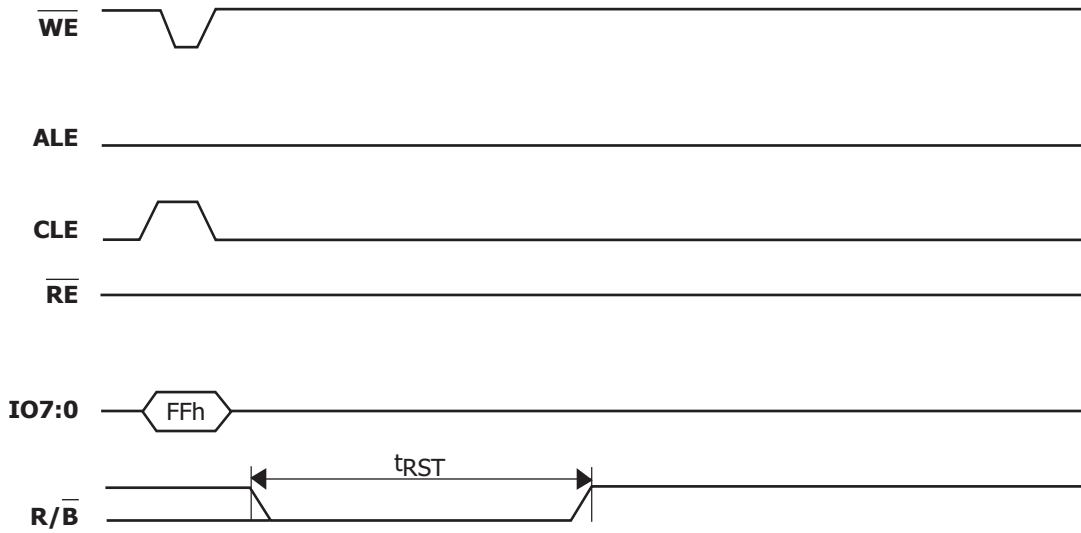


Figure 26: Reset Operation

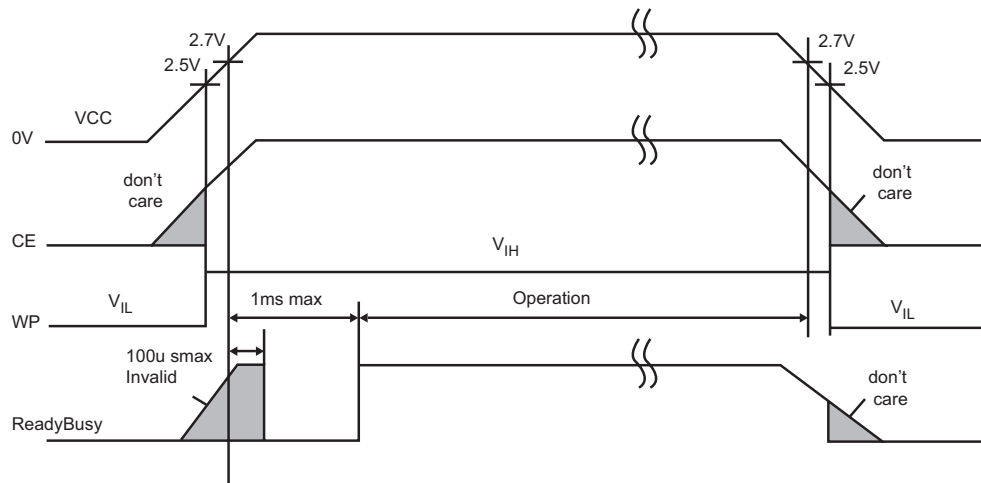


Figure 27: Power On and Data Protection Timing

$V_{TH} = 2.5$ Volt for 3.3 Volt Supply devices

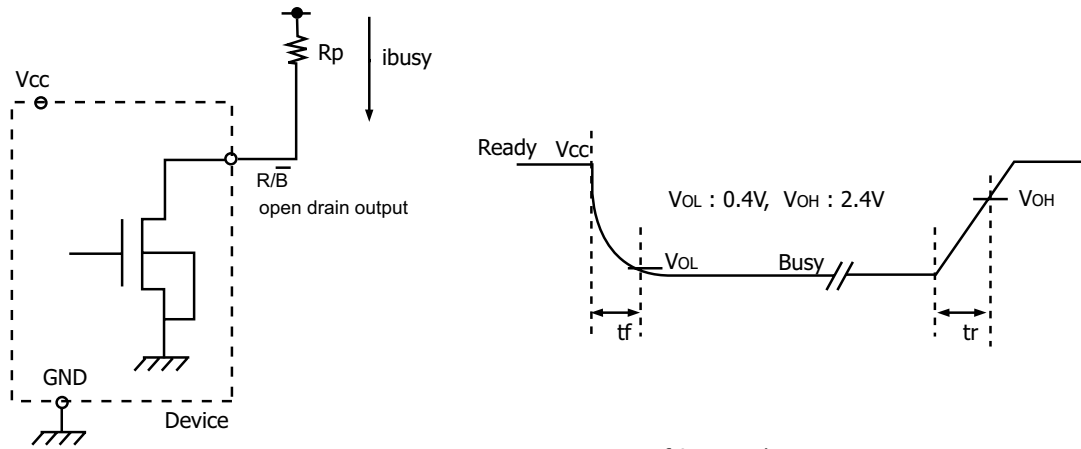
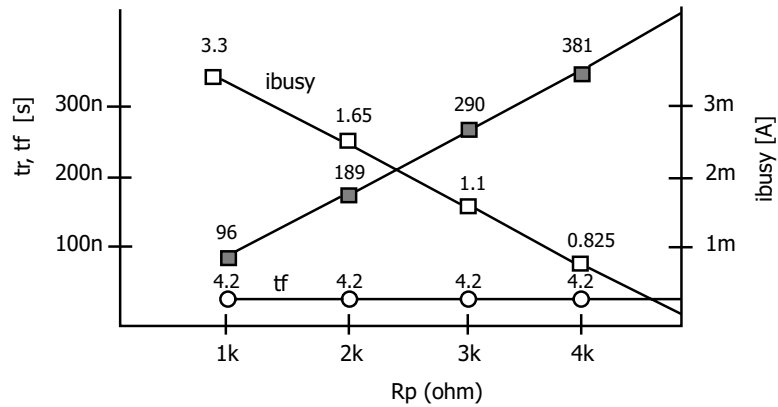


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C, CL=50pF



Rp value guidance

$$R_p (\text{min}) = \frac{V_{CC} (\text{Max.}) - V_{OL} (\text{Max.})}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 28: Ready/Busy Pin electrical specifications

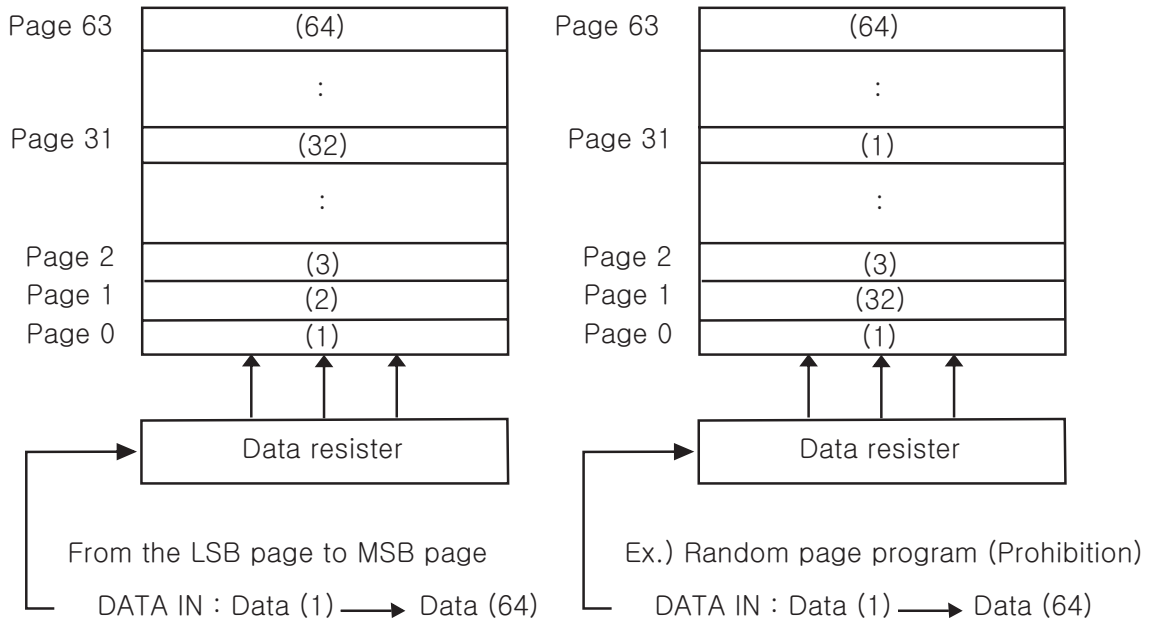


Figure 29: page programming within a block

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 30. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

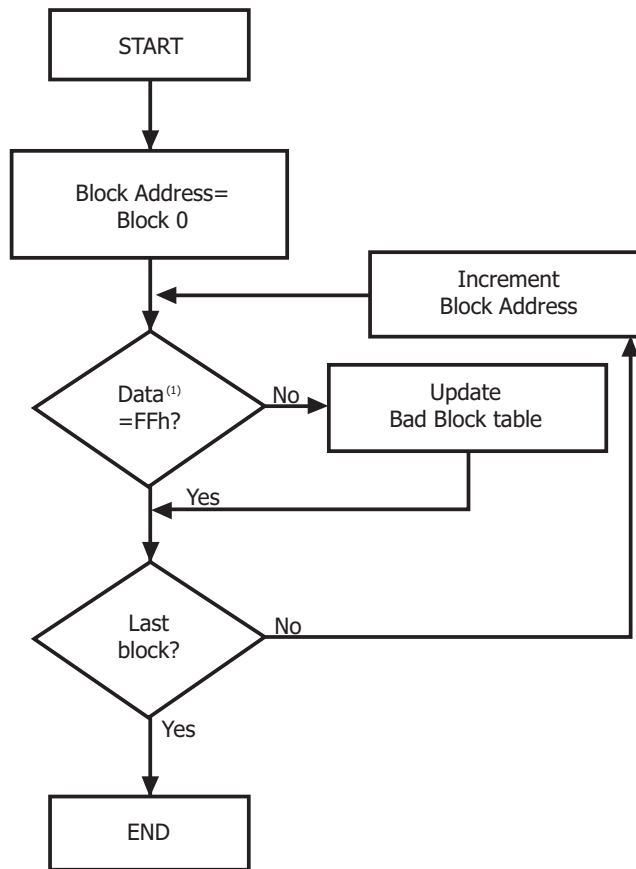


Figure 30: Bad Block Management Flowchart

NOTE :

1. Make sure that FFh at the column address 2048 of the 1st page and 2nd page.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

Unlike the case of odd page which carries a possibility of affecting previous page, the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 21 and Figure 31 for the recommended procedure to follow if an error occurs during an operation.

| Operation | Recommended Procedure |
|-----------|-------------------------|
| Erase | Block Replacement |
| Program | Block Replacement |
| Read | ECC (with 1bit/528byte) |

Table 21: Block Failure

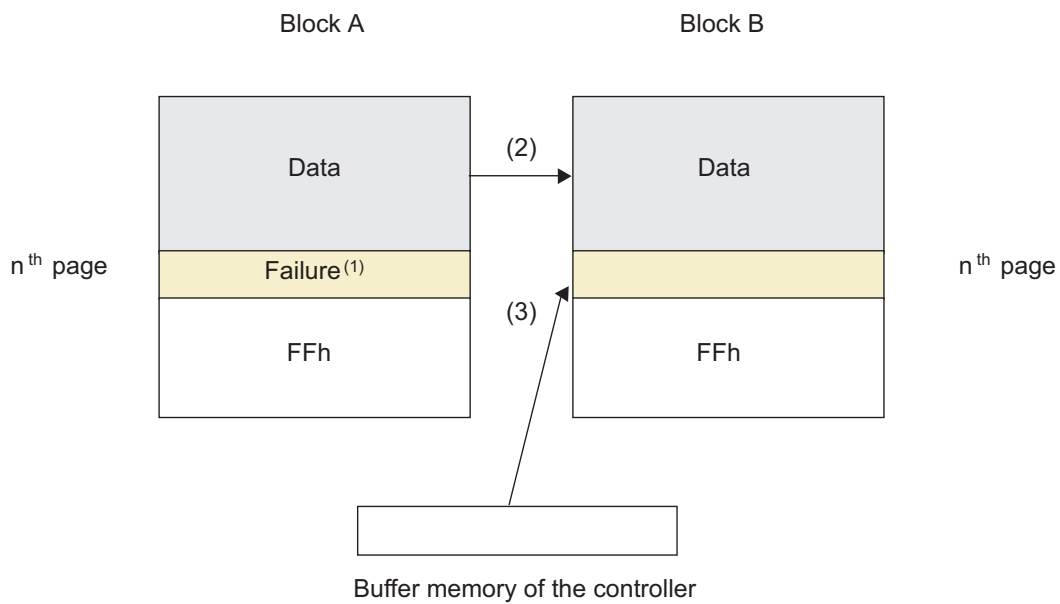


Figure 31: Bad Block Replacement

NOTE :

1. An error occurs on nth page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth data of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when \overline{WP} goes Low ($t_{WW} = 100\text{ns, min}$). The operations are enabled and disabled as follows (Figure 32~35)

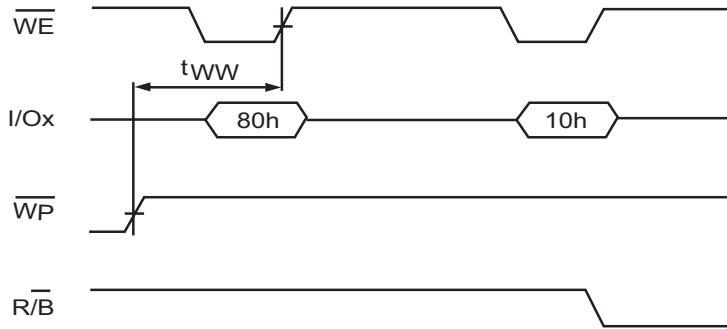


Figure 32: Enable Programming

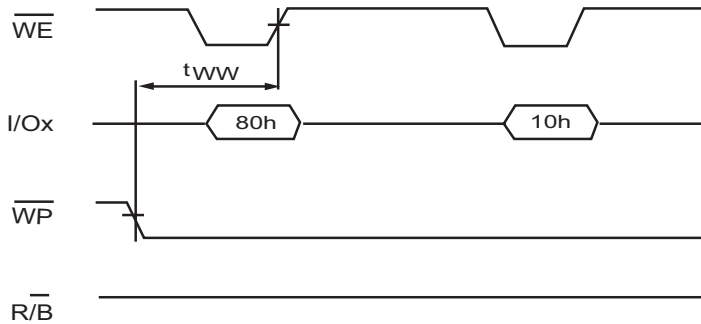


Figure 33: Disable Programming

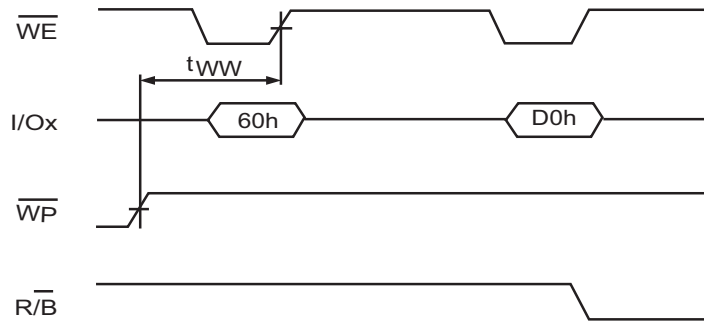


Figure 34: Enable Erasing

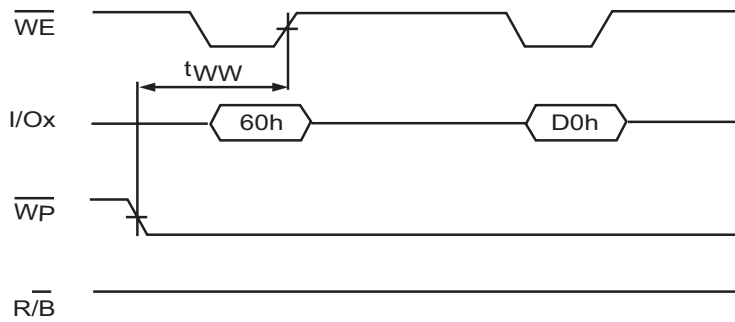


Figure 35: Disable Erasing

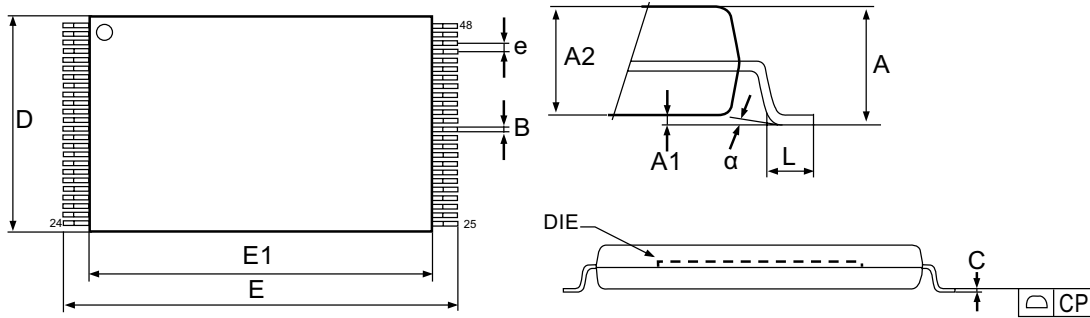
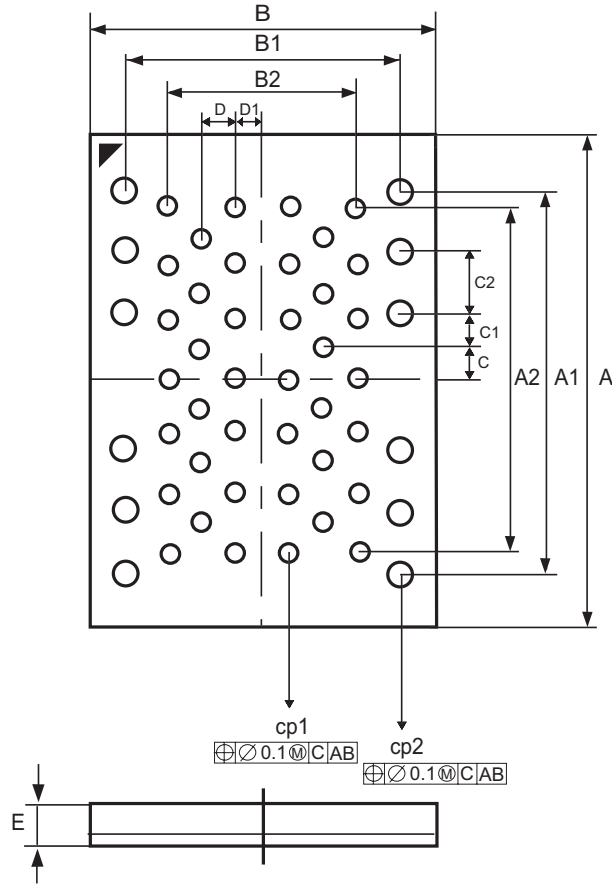


Figure 36: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

| Symbol | millimeters | | |
|--------|-------------|--------|--------|
| | Min | Typ | Max |
| A | | | 1.200 |
| A1 | 0.050 | | 0.150 |
| A2 | 0.980 | | 1.030 |
| B | 0.170 | | 0.250 |
| C | 0.100 | | 0.200 |
| CP | | | 0.100 |
| D | 11.910 | 12.000 | 12.120 |
| E | 19.900 | 20.000 | 20.100 |
| E1 | 18.300 | 18.400 | 18.500 |
| e | | 0.500 | |
| L | 0.500 | | 0.680 |
| alpha | 0 | | 5 |

**Table 22: 48-TSOP1 - 48-lead Plastic Thin Small Outline,
12 x 20mm, Package Mechanical Data**

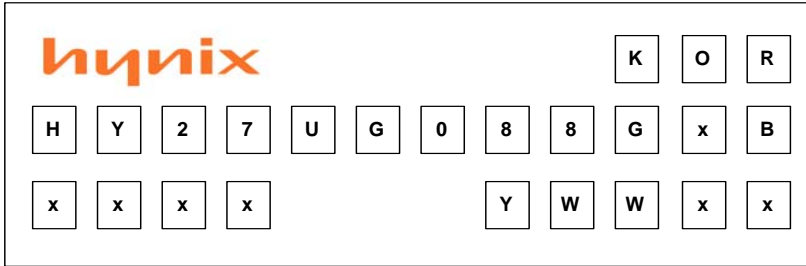


**Figure 37. 51-ULGA, 12 x 17mm, Package Outline
(Top view through package)**

| Symbol | millimeters | | |
|--------|-------------|-------|-------|
| | Min | Typ | Max |
| A | 16.90 | 17.00 | 17.10 |
| A1 | | 13.00 | |
| A2 | | 12.00 | |
| B | 11.90 | 12.00 | 12.10 |
| B1 | | 10.00 | |
| B2 | | 6.00 | |
| C | | 1.00 | |
| C1 | | 1.50 | |
| C2 | | 2.00 | |
| D | | 1.00 | |
| D1 | | 1.00 | |
| E | 0.55 | 0.60 | 0.65 |
| CP1 | 0.65 | 0.70 | 0.75 |
| CP2 | 0.95 | 1.00 | 1.05 |

Table 23: 52-ULGA, 12 x 17mm, Package Mechanical Data

MARKING INFORMATION - TSOP1 / ULGA

| Packag | Marking Example |
|---|--|
| <p style="text-align: center;">TSOP1 / ULGA</p> |  <p>The diagram shows a rectangular marking area. At the top left is the hynix logo. To its right are three boxes containing 'K', 'O', and 'R'. Below the logo is a row of boxes containing 'H', 'Y', '2', '7', 'U', 'G', '0', '8', '8', 'G', 'x', 'B'. Below that is another row of boxes containing 'x', 'x', 'x', 'x', followed by a gap, and then 'Y', 'W', 'W', 'x', 'x'.</p> |

| | |
|--|--|
| - hynix | : Hynix Symbol |
| - KOR | : Origin Country |
| - HY27UG088GxB xxxx | : Part Number |
| HY : Hynix | |
| 27 : NAND Flash | |
| U : Power Supply | : U(2.7V ~ 3.6V) |
| G : Classification | : Single Level Cell+ Double Die+ Large Block |
| 08 : Bit Organization | : 08(x8) |
| 8G : Density | : 8Gbit |
| x : Mode | : 5(2nCE & 2R/nB; Sequential Row Read Disable) : D(Dual interface; Sequential Row Read Disable) |
| B : Version | : 3rd Generation |
| x : Package Type | : T(48-TSOP1), U(52-ULGA) |
| x : Package Material | : Blank(Normal), P(Lead Free) |
| x : Operating Temperature | : C(0°C ~ 70°C), I(-40°C ~ 85°C) |
| x : Bad Block | : B(Included Bad Block), S(1~5 Bad Block), P(All Good Block) |
| - Y : Year (ex: 5= year 2005, 6= year 2006) | |
| - ww : Work Week (ex: 12= work week 12) | |
| - xx : Process Code | |
| Note | |
| - Capital Letter | : Fixed Item |
| - Small Letter | : Non-fixed Item |