WM8310

Processor Power Management Subsystem

DESCRIPTION

WM8310 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management, specifically targeted at the requirements of a range of low-power portable applications. WM8310 is specifically designed to operate as a system PMIC supporting a variety of industry standard processors and accessories in a wide range of applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP contents.

The WM8310 power management subsystem comprises of four programmable DC-DC converters, eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

WM8310 can be powered from a battery, a wall adaptor or from a USB power source. An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'always-on' processor power domains external to the WM8310.

A linear on-chip battery charger supports trickle charging and constant current / constant voltage charging of single-cell lithium-ion / lithium-polymer batteries. The charge current, termination voltage, and charger time-out are programmable. WM8310 detects and handles battery fault conditions with a minimum of system software involvement.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8310 includes a crystal oscillator, an internal RC oscillator and Frequency Locked Loop (FLL) to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8310 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <10uA, making it particularly suitable for portable applications.

The WM8310 is supplied in a 7x7mm 169-ball BGA package, ideal for use in portable systems. The WM8310 forms part of the Wolfson series of audio and power management solutions.

FEATURES

Power Management

- 2 x DC-DC synch. buck converter (0.6V - 1.8V, 1.2A, DVS)
- 1 x DC-DC synch. buck converter (0.85V - 3.4V, 1A)
- 1 x DC-DC boost converter (up to 30V, up to 170mA)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'always on' regulator (0.8V – 1.55V, up to 10mA)

Backlight LED Current Sinks

- 2 x programmable constant current sinks, suitable for multi-LED display backlight control

Battery Charger

- Programmable single-cell lithium-ion / lithium-polymer battery charger (1A max charge current)
- Battery monitoring for temperature and voltage
- Autonomous backup battery charging and switching

System Control

- I^2C or SPI compatible primary control interface
- Interrupt based feedback communication scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- Intelligent power path and power source selection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-time clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, Frequency Locked Loop, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating power state, battery charger or fault status
- Selectable USB current limiting up to 1.8A (in accordance with USB Battery Charging specification Rev 1.1)

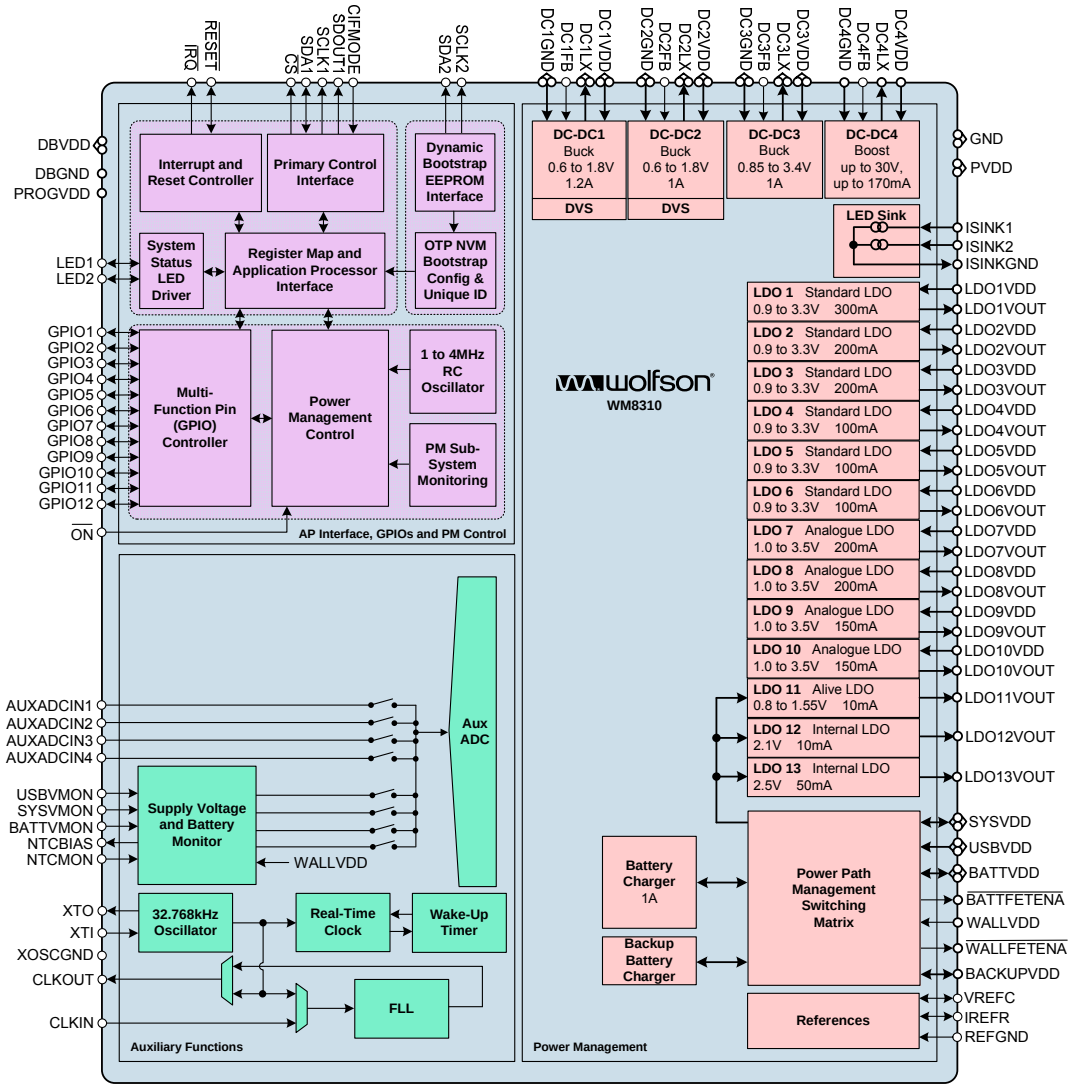
Package Options

- 7x7mm, 169-ball BGA package, 0.5mm ball pitch

APPLICATIONS

- Portable Media Players
- Portable Navigation Devices
- Cellular Handsets
- Electronic Books
- Electronic Gaming Devices

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8310 is designed as a system PMIC device that manages multiple power supply paths (wall adapter, USB, battery) and generates configurable DC supplies to power processors and associated peripherals within a system. The WM8310 provides three step-down DC-DC converters and one step-up DC-DC converter. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

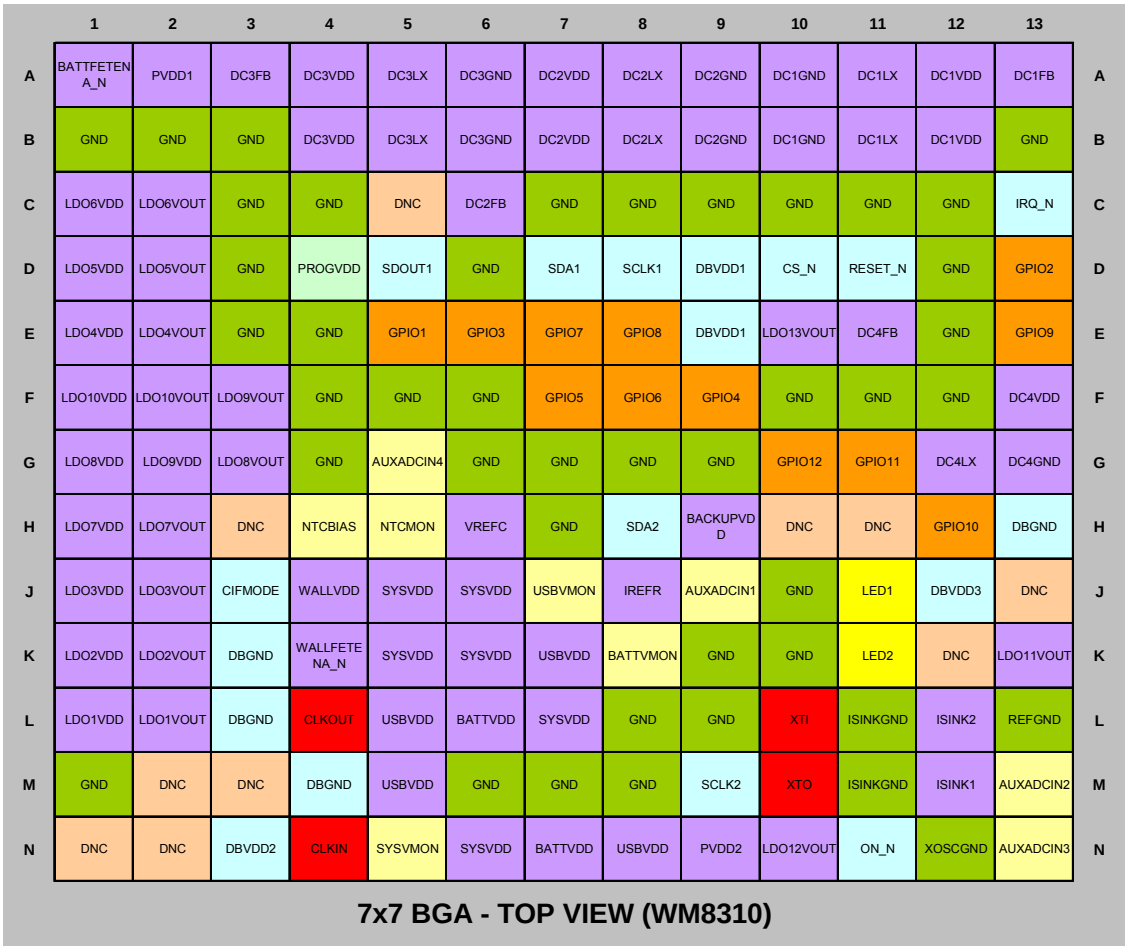
Two of the DC-DC step-down converters are specifically designed to handle rapid changes in load current, as required by modern application processors; selectable operating modes allow the converters to be optimally configured for light, heavy or transient load conditions they can also be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / cellular handset applications.

The WM8310 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-programmable OTP memory or may loaded from an external memory. The WM8310 supports the programming and verification of the integrated OTP memory.

The WM8310 provides power path management which seamlessly switches between wall adapter, USB and battery power sources according to the prevailing conditions. A backup battery supply is also supported in order to maintain the Real Time Clock (RTC) in the absence of any other supplies. The WM8310 provides a battery charger for the main battery aswell as the backup battery; these can be powered from either the wall adapter or USB supplies.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8310 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer, operating power state or battery charger.

PIN CONFIGURATION



7x7 BGA - TOP VIEW (WM8310)

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8310GEB/V	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free)	MSL3	260°C
WM8310GEB/RV	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2200

PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions; INTVDD is the domain powered by LDO13 which supplies the control circuitry for many of the power management blocks.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
Auxiliary ADC					
J7	USBVMON	Analogue Input	USBVDD	USBVDD Supply Voltage Monitor	
N5	SYSVMON	Analogue Input	SYSVDD	SYSVDD Supply Voltage Monitor	
K8	BATTVMON	Analogue Input	BATTVDD	BATTVDD Supply Voltage Monitor	
J9	AUXADCIN1	Analogue Input/Output	SYSVDD	Auxiliary Analogue Input 1 / Battery Charge Current Monitor Output	
M13	AUXADCIN2	Analogue Input		Auxiliary Analogue Input 2	
N13	AUXADCIN3	Analogue Input		Auxiliary Analogue Input 3	
G5	AUXADCIN4	Analogue Input	DBVDD3	Auxiliary Analogue Input 4	
Clocking and Real Time Clock					
M10	XTO	Analogue Output	VPMIC	Crystal Drive Output	
L10	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input	
N12	XOSCGND	Supply		Crystal Oscillator Ground	
L4	CLKOUT	Digital Output	DBVDD2	CMOS Clock Output	
N4	CLKIN	Digital Input		CMOS FLL Clock Input	
General Purpose Input / Output					
E5	GPIO1	Digital I/O	DBVDD1 or VPMIC	GPIO Pin 1	
D13	GPIO2	Digital I/O		GPIO Pin 2	
E6	GPIO3	Digital I/O		GPIO Pin 3	
F9	GPIO4	Digital I/O	DBVDD1 or SYSVDD	GPIO Pin 4	
F7	GPIO5	Digital I/O		GPIO Pin 5	
F8	GPIO6	Digital I/O		GPIO Pin 6	
E7	GPIO7	Digital I/O	DBVDD1 or VPMIC	GPIO Pin 7	
E8	GPIO8	Digital I/O		GPIO Pin 8	
E13	GPIO9	Digital I/O		GPIO Pin 9	
H12	GPIO10	Digital I/O	DBVDD1 or SYSVDD	GPIO Pin 10	
G11	GPIO11	Digital I/O		GPIO Pin 11	
G10	GPIO12	Digital I/O		GPIO Pin 12	
Processor Interface and IC Control					
N11	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
D11	$\overline{RESET}$	Digital I/O	DBVDD1	System Reset Input and Open Drain Output. (Internal pull-up)	
C13	$\overline{IRQ}$	Digital Output	DBVDD1	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
J3	CIFMODE	Digital Input	DBVDD2	Primary Control Interface Mode Select: 0 = I^2C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I^2C Compatible Control Interface Mode*
D5	SDOUT1	Digital Output	DBVDD1	Control Interface Serial Data Out	No Function

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
D8	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
D7	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. (Output can extend above DBVDD1 domain.)
D10	$\overline{CS}$	Digital Input		Control Interface Chip Select	I^2C Address Select: 0 = 34h 1 = 36h
M9	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external DBE EEPROM (Internal pull-down)	
H8	SDA2	Digital I/O		Control Interface Serial Data to/from external DBE EEPROM (Internal pull-down)	
D9, E9	DBVDD1	Supply		Digital Buffer Supply	
N3	DBVDD2	Supply		Digital Buffer Supply	
J12	DBVDD3	Supply		Digital Buffer Supply	
H13, K3, L3, M4	DBGND	Supply		Digital Buffer Ground	
OTP Memory					
D4	PROGVDD	Supply		High-voltage input for OTP programming.	
DC-DC Converters and LDO Regulators					
B1, B2, B3, B13, C3, C4, C7, C8, C9, C10, C11, C12, D3, D6, D12, E3, E4, E12, F4, F5, F6, F10, F11, F12, G4, G6, G7, G8, G9, H7, J10, K9, K10, L8, L9, M1, M6, M7, M8	GND	Supply		Ground	
A2	PVDD1	Supply		Internal VDD supply; Connect to SYSVDD	
N9	PVDD2	Supply			
A10, B10	DC1GND	Supply		DC-DC1 Power Ground	
A13	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin	
A11, B11	DC1LX	Analogue I/O		DC-DC1 Inductor Connection	
A12, B12	DC1VDD	Supply		DC-DC1 Power Input	
A9, B9	DC2GND	Supply		DC-DC2 Power Ground	
C6	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin	
A8, B8	DC2LX	Analogue I/O		DC-DC2 Inductor Connection	
A7, B7	DC2VDD	Supply		DC-DC2 Power Input	
A6, B6	DC3GND	Supply		DC-DC3 Power Ground	
A3	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
A5, B5	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
A4, B4	DC3VDD	Supply		DC-DC3 Power Input
G13	DC4GND	Supply		DC-DC4 Power Ground
E11	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Connection
G12	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
F13	DC4VDD	Supply		DC-DC4 Power Input
L1	LDO1VDD	Supply		LDO1 Power Input
L2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
K1	LDO2VDD	Supply		LDO2 Power Input
K2	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
J1	LDO3VDD	Supply		LDO3 Power Input
J2	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
E1	LDO4VDD	Supply		LDO4 Power Input
E2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
D1	LDO5VDD	Supply		LDO5 Power Input
D2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
C1	LDO6VDD	Supply		LDO6 Power Input
C2	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
H1	LDO7VDD	Supply		LDO7 Power Input
H2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
G1	LDO8VDD	Supply		LDO8 Power Input
G3	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
G2	LDO9VDD	Supply		LDO9 Power Input
F3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
F1	LDO10VDD	Supply		LDO10 Power Input
F2	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
K13	LDO11VOUT	Analogue Output		LDO11 (Alive) Power Output
N10	LDO12VOUT	Analogue I/O		LDO12 (Internal VPMIC) Output; not for general use
E10	LDO13VOUT	Analogue I/O	PVDD2	LDO13 (Internal INTVDD) Output; not for general use
Current Sinks				
M12	ISINK1	Analogue Output	SYSVDD	LED String Current Sink 1
L12	ISINK2	Analogue Output		LED String Current Sink 2
L11, M11	ISINKGND	Supply		LED String Current Sink Ground
Voltage and Current References				
H6	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
J8	IREFR	Analogue I/O		Current Reference resistor connection point
L13	REFGND	Supply		Reference Ground
Power Path Management				
J5, J6 K5, K6, L7, N6	SYSVDD	Supply		System VDD Supply
K7, L5, M5, N8	USBVDD	Supply		USB VDD Supply
L6, N7	BATTVDD	Supply		Primary Battery Supply
A1	$\overline{\text{BATTFETENA}}$	Digital Output	PVDD1	External Battery FET Driver
J4	WALLVDD	Supply		Wall VDD Supply/Sense
K4	$\overline{\text{WALLFETENA}}$	DigitalOutput	highest VDD supply	External Wall FET Driver. Power domain is the highest out of WALLVDD, USBVDD or BATTVDD.
H4	NTCBIAS	Analogue Output	VPMIC	Battery NTC Temperature Monitor Supply
H5	NTCMON	Analogue Input		Battery NTC Temperature Monitor Voltage Sense Input

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
H9	BACKUPVDD	Supply		Secondary (Backup) Battery Supply
Status LED Drivers				
J11	LED1	Digital Output	SYSVDD	Status LED Driver 1. Open Drain Output
K11	LED2	Digital Output		Status LED Driver 2. Open Drain Output
Do Not Connect				
C5, H3, H10, H11, J13, K12, M2, M3, N1, N2	DNC			Do Not Connect

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8310 has been classified as MSL3.

CONDITION	MIN	MAX
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
BATTVDD, WALLVDD and USBVDD supplies	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2, DBVDD3)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		45°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

RECOMMENDED OPERATING CONDITIONS

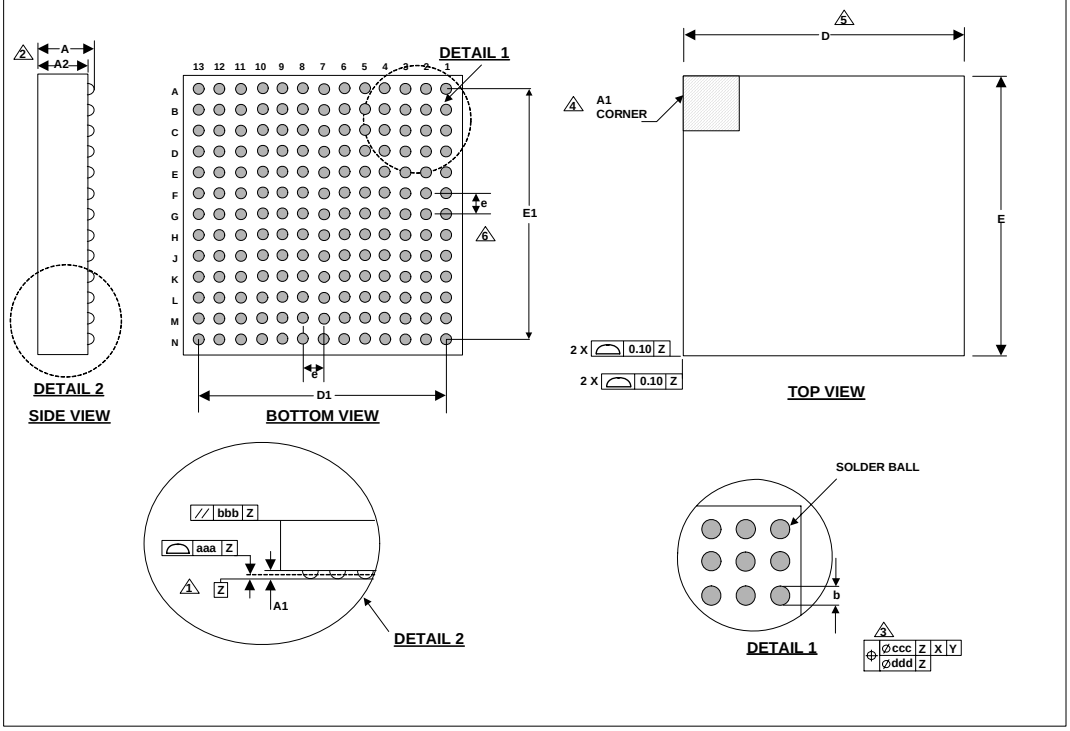
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wall Input power source	WALLVDD	4.3		5.5	V
Battery Input power source	BATTVDD	2.7		5.5	V
USB Input power source	USBVDD	4.3		5.5	V
Backup Battery power source	BACKUPVDD			3.6	V
Digital buffer supply	DBVDD1, DBVDD2, DBVDD3	1.71		3.6	V
OTP Programming Supply (see note)	PROGVDD	6.25	6.5	6.75	V
Ground	GND, DBGND, XOSCGND, REFGND		0		V

Note:

The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected.

PACKAGE DIAGRAM

B: 169 BALL BGA PLASTIC PACKAGE 7 x 7 x 1.17 mm BODY, 0.50 mm BALL PITCH **DM062.B**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A		1.17	1.27	
A1	0.17	0.21	0.26	
A2	0.91	0.96	1.01	
b	0.25	0.30	0.35	
D		7.00 BSC		
D1		6.00 BSC		
E		7.00 BSC		
E1		6.00 BSC		
e		0.50 BSC		6
Tolerances of Form and Position				
aaa		0.08		
bbb		0.10		
ccc		0.15		
ddd		0.05		
REF:		JEDEC, MO-195		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
8. FALLS WITHIN JEDEC, MO-195

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