STK4024V



AF Power Amplifier (Split Power Supply) (20 W min, THD = 0.08%)

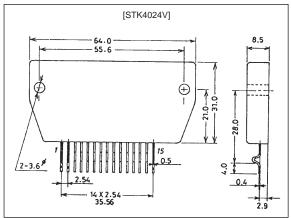
Features

- Compact packaging supports slimmer set designs (up to 70 W)
- Series designed from 20 up to 100 W (200 W) and pincompatibility (120 to 200 W have 18 pins)
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit application reduces distortion to 0.08%
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off

Package Dimensions

unit : mm

4062



Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		±37	V
Thermal resistance	өј-с		2.6	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Тс		125	°C
Storage temperature	Tstg		-30 to +125	°C
Available time for load shorted	ts *1	$V_{CC} = \pm 24.5 \text{ V}, \text{ R}_{L} = 8 \Omega, \text{ f} = 50 \text{ Hz}, \text{ P}_{O} = 20 \text{ W}$	2	s

Recommended Operational Voltage at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		±24.5	V
Load resistance	RL		8	Ω

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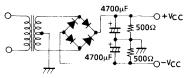
Operating Characteristics at Ta = 25°C, V_{CC} = ±24.5 V, R_L = 8 Ω , VG = 40 dB, Rg = 600 Ω , 100 k LPF ON, R_L (non-inductive)

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	Icco	V _{CC} = ±29.5 V	15		120	mA
Output power	P _O (1)	THD = 0.08%, f = 20 Hz to 20 kHz	20			W
	P _O (2)	$V_{CC} = \pm 21.5V$, THD = 0.2%, $R_L = 4 \Omega$, f = 1 kHz	20			W
Total harmonic distortion	THD	P _O = 1.0 W, f = 1 kHz			0.08	%
Frequency response	f _L , f _H	$P_{O} = 1.0 \text{ W}, \frac{+0}{-3} \text{ dB}$		20 to 50k		Hz
Input resistance	ri	P _O = 1.0 W, f = 1 kHz		55		kΩ
Output noise voltage	V _{NO} *2	$V_{CC} = \pm 29.5 \text{ V}, \text{ R}_{g} = 10 \text{ k}\Omega$			1.2	mVrms
Neutral voltage	V _N	V _{CC} = ±29.5 V	-70	0	+70	mV

Note: Use rated power supply for test unless otherwise specified.

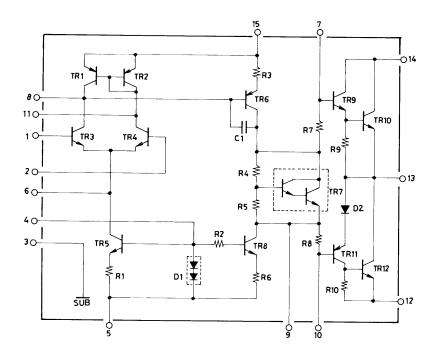
*1 When measuring permissible load short time and output noise voltage use transformer power supply indicated below.

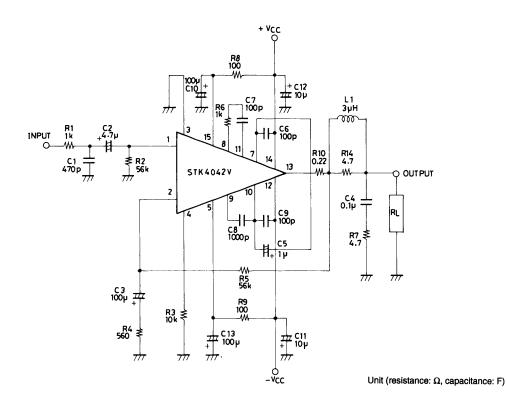
*2 Output noise voltage represents the peak value on the rms scale (VTVM). The noise voltage waveform does not include the pulse noise.



Specified Transformer Power Supply (RP-25 Equivalent)

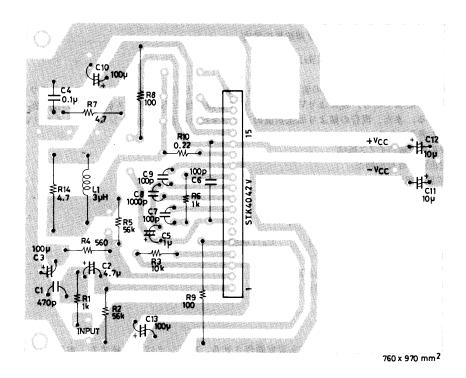
Equivalent Circuit





Application Circuit: 20W min Single Channel AF Power Amplifier

Sample Printed Circuit Pattern for Application Circuit (Copper-foiled side)



Unit (resistance: Ω, capacitance: F)

Description of External Parts

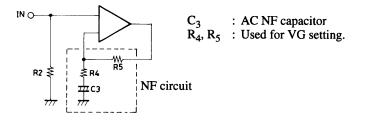
R_1, C_1 : Input filter circuit	R ₁ , C ₁	: Input filter circuit
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Reduces high-frequency noise.

C₂ : Input coupling capacitor

- DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.
- R₂ : Input bias resistor
 - Biases the input pin to zero.
 - Effects V_N stability (refer to NF circuit).
 - Due to differential input, input resistance is more or less determined by this resistance value.
- R₄, R₅ : NFB circuit (AC NF circuit). Use of resistor with 1% error is suggested.

 $C_{3}(R_{2})$



• VG settings are obtained using R₄ and R₅ according to the following equation:

 $\log 20 - \frac{R_5}{R_4}$ 40 dB is recommended.

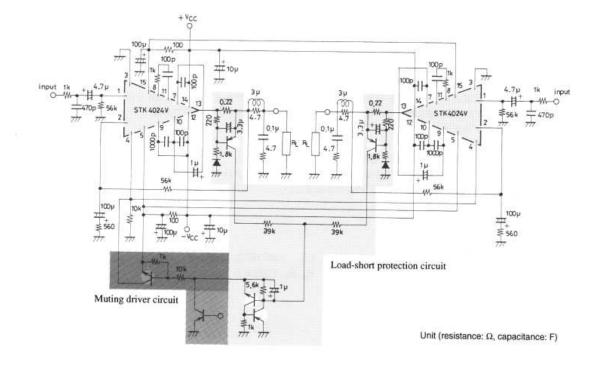
• Low-frequency cutoff frequency settings are obtained using R_4 and C_3 according to the following equation:

$$f_{L} = \frac{1}{2\pi \cdot R_{4} \cdot C_{3}} \quad [Hz]$$

When changing the VG setting, you should change R_4 which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using R_5 , the setting should ensure R_2 equals R_5 so that V_N balance stability is maintained. If the resistor value is increased more than the existing value, V_N balance may be disturbed and result in deterioration of V_N temperature characteristics.

R₃ : Differential constant-current bias resistor

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R ₆ , R ₇	: For oscillation suppression and phase compensation applications (For use with differential stage applications)
R ₇ , C ₄	: For oscillation suppression and phase compensation applications (A Mylar capacitor is recommended for C ₄ for use with output stage applications)
C ₆ , C ₉	: For oscillation suppression and phase compensation applications Power stage (Must be connected near the pin) C ₆ : Positive (+) power C ₉ : Negative (-) power
C ₈	: For oscillation suppression and phase compensation applications (Oscillation suppression before power step clip)
C ₅	: For oscillation suppression and distortion improvement applications
R ₈ , C ₁₀	: Ripple filter circuit on positive (+) side.
R ₉ , C ₁₃	: Ripple filter circuit on negative (–) side.
C ₁₁ , C ₁₂	: For oscillation suppression applications
	• Used for reducing power supply impedance to stable IC operation and should be connected near the IC pin. We recommend that you use an electrolytic capacitor.



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