Ordering number : EN 4688

Thick Film Hybrid IC

SANYO No.4688

STK392-020

Convergence Correction Circuit Three Channels in a Single Package (Maximum Output Current : 6A)

Overview

The STK392-020 is a hybrid IC for video projector convergence correction. Since this IC integrates three output amplifier circuits in a single package, the six convergence correction output circuits, i.e., the vertical and horizontal directions for each CRT of the RGB can be formed from only two ICs.

Applications

Video projectors (both standard and high definition)

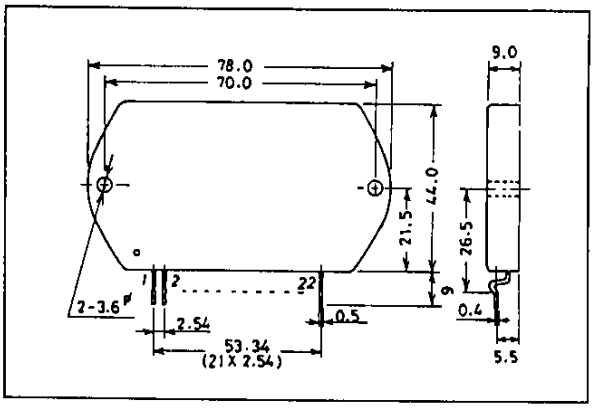
Features

- Three output amplifier circuits integrated in a single 22-pin package
- High absolute maximum supply voltage (V_{CC} max = ±44 V)
- Low thermal resistance (θj-c = 2.1 °C/W)
- High thermal stability (T_C max = 125°C)
- Isolated early stage and output stage power supplies
- Output stage power supply switching supports high efficiency designs.
- The input system, power supply system and output system pins are isolated in the pin arrangement, thus reducing the influence of the pattern layout on the characteristics and easing design.
- Since constant current circuits are used in the pre-driver stage, operation is stable with respect to the power supply switching.
- The Sanyo convergence correction circuit product lineup (the STK392-000 series) handles a wide range of end-product classes. Therefore, the same PCB can be used for end products from popularly-priced units to top-of-the-line models.

Package Dimensions

unit: mm

4086A



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±44	V
Maximum collector current	I_C	Tr8, 10, 18, 20, 28, 30	+6.0	A
Thermal resistance	θj-c	Tr8, 10, 18, 20, 28, 30 (per transistor)	2.1	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		−30 to +125	°C

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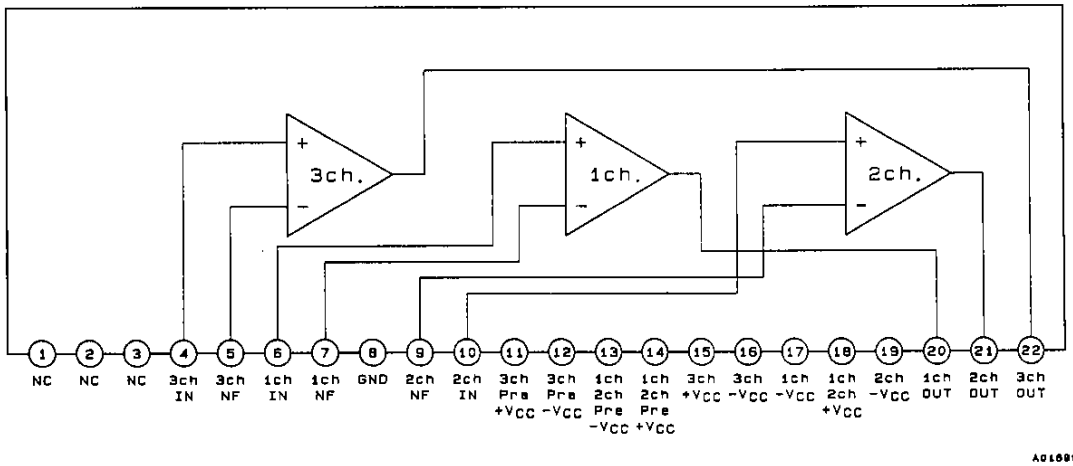
Operating Characteristics at Ta = 25°C, Rg = 50 Ω

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output noise voltage	V_{NO}	V_{CC} = ±35 V			0.2	mVrms
Quiescent current	I_{CCO}	V_{CC} = ±35 V	30	90	150	mA
Neutral voltage	V_N	V_{CC} = ±35 V	–50	0	+50	mV
Output delay time	t_D	V_{CC} = ±35 V, f = 15.75 kHz; Triangle wave input, V_{OUT} = 1.5 Vp-p			1.0	μs

Equivalent Circuit Block Diagram



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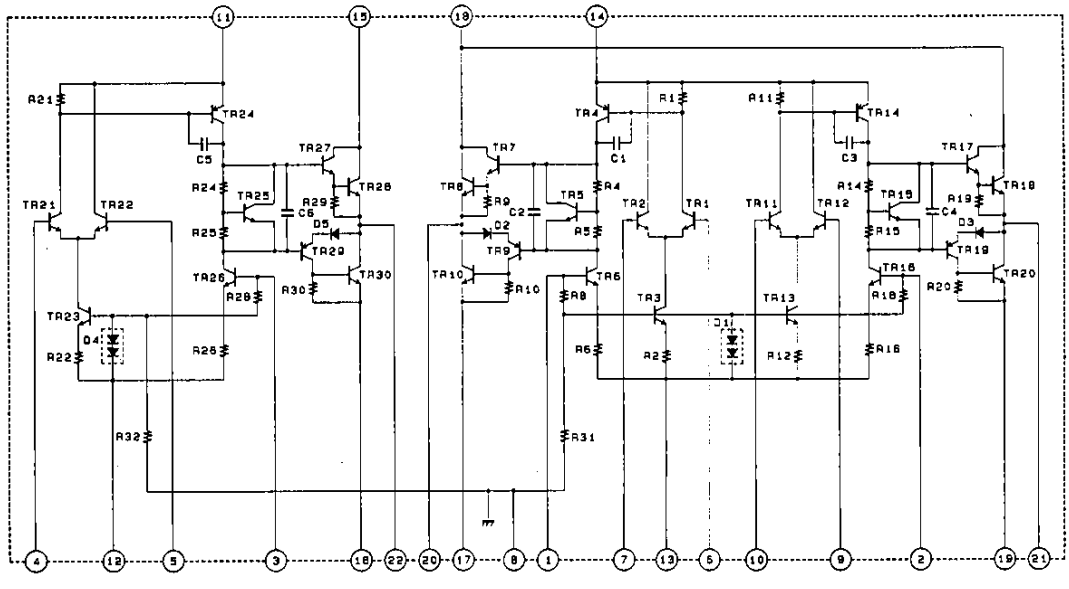
Internal Equivalent Circuit



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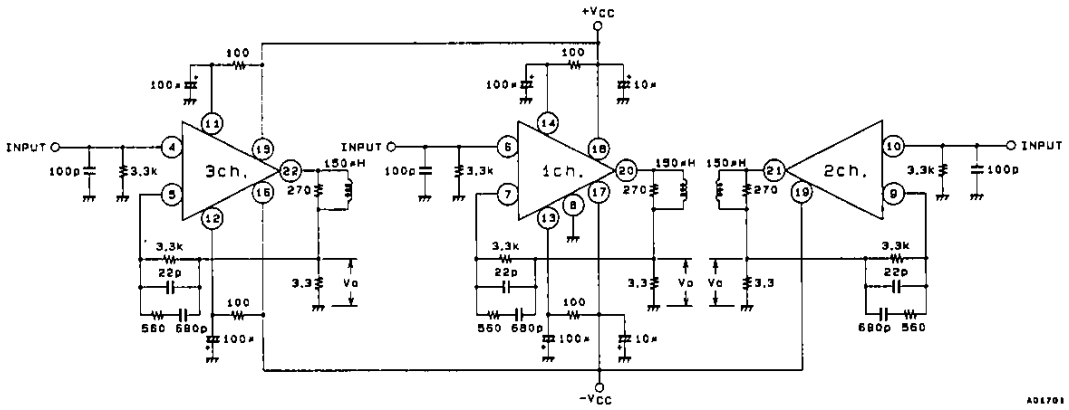
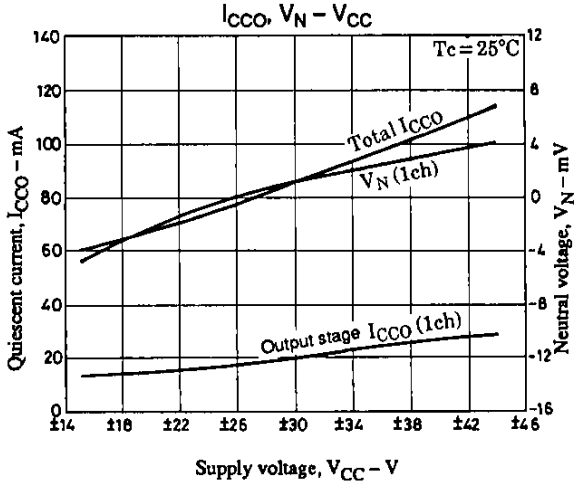
Test Circuit

Unit (Resistance: Ω, Capacitance: F)



Vo: Connect to VTVM when measuring V_{NO}
Connect to a DC volt meter when measuring V_N
Connect to the oscilloscope when measuring t_D



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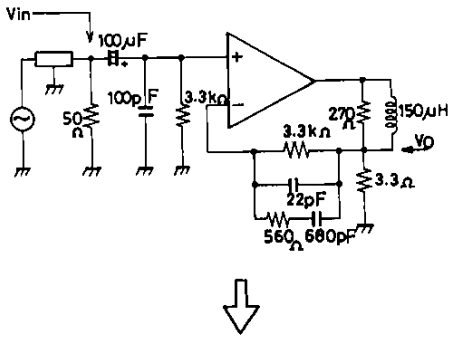
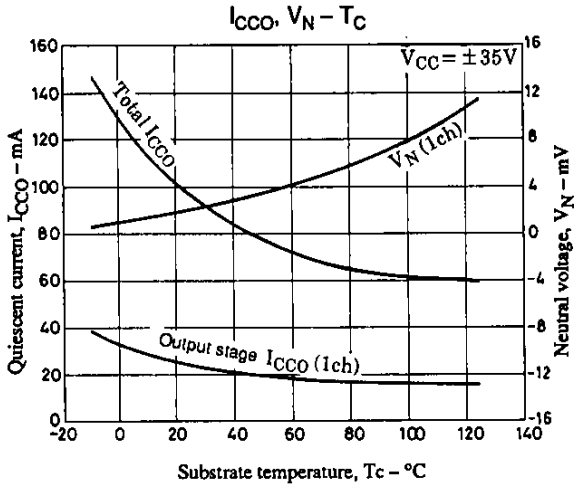
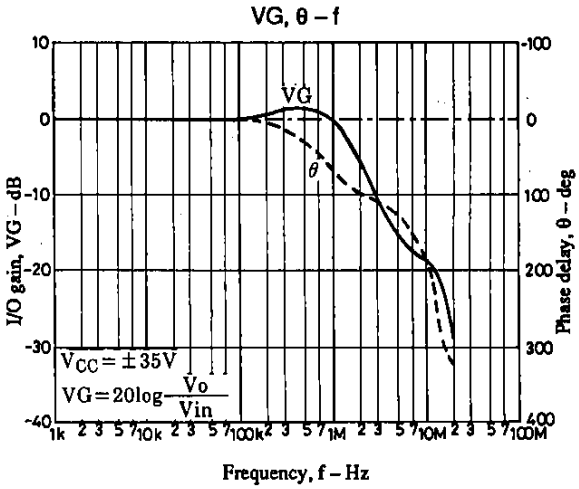
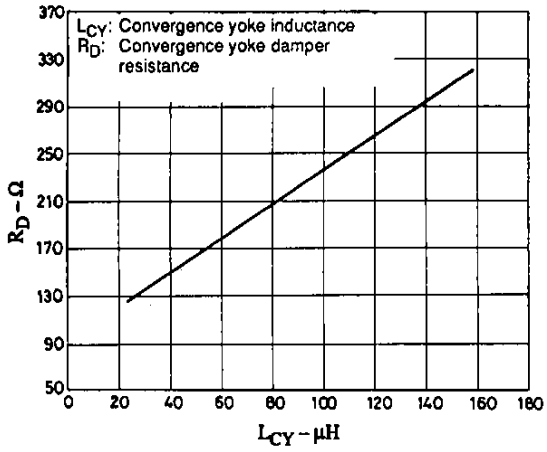




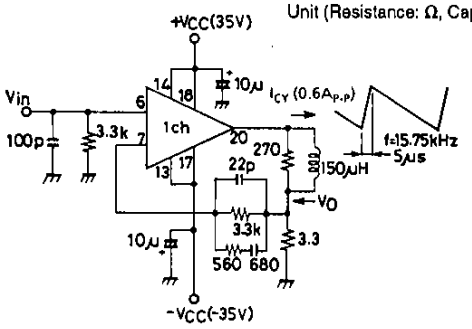


$R_D - L_{CY}$



Operating Waveforms

Unit (Resistance: Ω, Capacitance: F)



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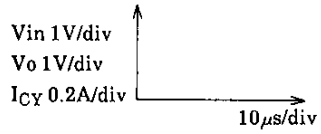
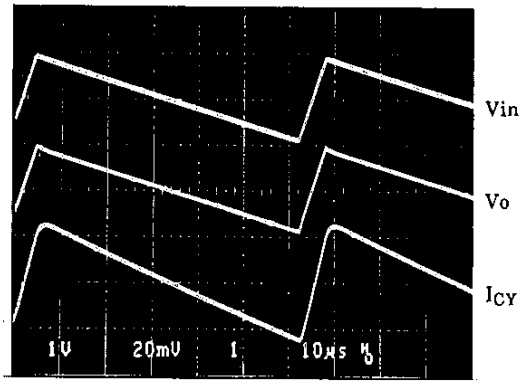
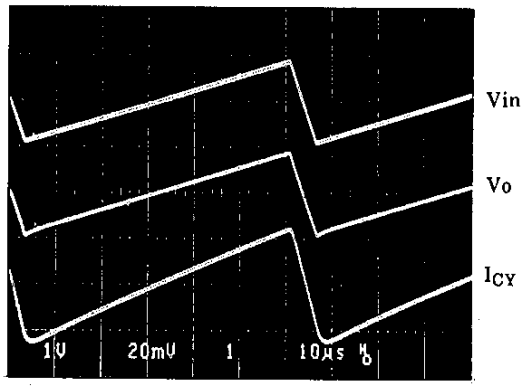
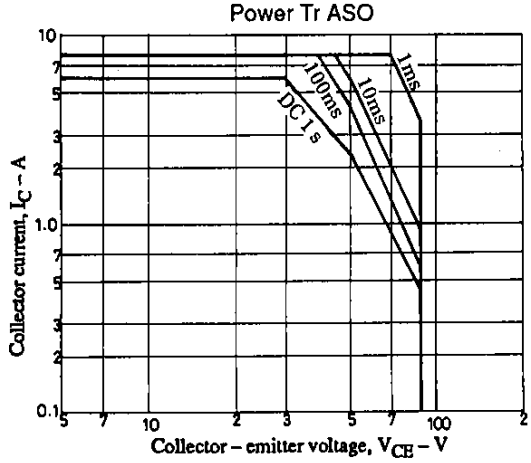






Power Tr ASO



Thermal Design

1. Tj max, Tc max, and θj-c
   Tj max, Tc max, and θj-c are stipulated in the maximum ratings as required parameters for thermal design.

   - Tj max (junction temperature)
     Tj max is a parameter that is due to the physical structure of the internal devices. Since devices will be degraded or destroyed if Tj exceeds this value, the design must not allow this value to be exceeded.

   - Tc max (operating substrate temperature)
     Tc max is a parameter that arises from the internal devices, the materials used, and the circuit design. It is determined based on comprehensive considerations, including reliability. Devices are not guaranteed if they are operated with Tc exceeding this value.

   - θj-c (thermal resistance)
     θj-c differs for each device in the design, and is stipulated in the maximum ratings since it is required to calculate Tj for the major devices in the design.

   Note that Tj and Tc are independent parameters that depend on the operating conditions, and the thermal design must fulfill the maximum ratings of both these parameters.

2. Approaches to Thermal Design
   Let Pd be the IC case internal operating power dissipation, and Pc be the power dissipation per power transistor. The required heat sink thermal resistance (θc-a) for this case internal power dissipation (Pd) can be derived as follows:

   Condition 1: Taking Ta to be the end product guaranteed ambient temperature, the IC case temperature Tc must not exceed 125°C.

   $$Pd \times \theta c\text{-}a + Ta < 125°C \text{ (Tc max)} \quad \text{.....①}$$

   Condition 2: The power transistor junction temperature must not exceed 150°C.

   $$Pd \times \theta c\text{-}a + Pc \times \theta j\text{-}c + Ta < 150°C \text{ (Tj max)} \quad \text{.....②}$$

   Where θj-c is the thermal resistance per power transistor.

   The thermal design must fulfill these above conditions.

3. Design Procedure
   The figure at right shows a model of the STK392-020 channel 1 circuit. Taking the Pd's of each channel to be Pd1 (channel 1), Pd2 (channel 2) and Pd3 (channel 3), the total Pd max can be determined as:

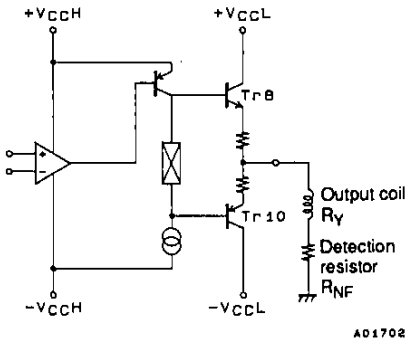
   $$Pd\ max = Pd1\ max + Pd2\ max + Pd3\ max$$

   That is, condition ① gives:

   $$\theta c\text{-}a < \frac{Tc\ max - Ta\ max}{Pd\ max} \quad \text{.....③}$$

   which allows the required heat sink thermal resistance to be derived. (Here, Tc max is taken to be 125°C.)

STK392-020 Circuit Model (channel 1)



   Also, taking the power dissipation per power transistor for each channel to be Pc, the transistor junction temperature Tj will be:

   $$Tj = Pd\ max \times \theta c\text{-}a + Ta + Pc + \theta j\text{-}c \quad \text{.....④}$$

   and this can be used to confirm that Tj does not exceed Tj max (150°C).

   At this point, if Tj exceeds 150°C in the design, Tc must be lowered by lowering the heat sink thermal resistance θc-a so that Tj does not exceed 150°C.

4. Thermal Design Example
Take the following to be the worst operating conditions for the STK392-020.

$V_{CC}H = \pm 35$ V
$V_{CC}L = \pm 25$ V
Output coil, $L_Y = 150\ \mu H$, $R_Y = 0\ \Omega$
Current detection resistor $R_{NF} = 3.3\ \Omega$
Ip-o max = 0.4 Ap-o (Ip-p = 0.8 A), Sawtooth waveform input
Io(DC) max = 0.4 A DC input
All three channels operating under the same conditions
Ta max = 60°C (unit internal temperature)

From figures 1 and 2, it can be seen that the Pd1 for channel 1 is:

(a) For a sawtooth wave input: Pd1 max = 4.8 W (AC)
(b) For a DC input: Pd1 max = 9.5 W (DC)

This shows that Pd1 max AC < Pd1 max DC, i.e. that Pd1 is larger for a DC input.

Also, considering Pc for the output transistors gives:

(a) For a sawtooth wave (AC) input: Pc = 1/2 Pd1
(b) For a DC input: Pc = Pd1 (Since the power concentrates in the transistor on one side.)

Therefore, the DC input Pc for the output transistors is larger.

Accordingly, the remainder of the thermal design is based on the DC input case.

Here we ignore the power dissipation in the early stages.

When: Pd1 max = Pd2 max = Pd3 max = 9.5 W, then the Pd max (total for three channels) will be:
Pd max = Pd1 max × 3 = 28.5 W

$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd\ max} = \frac{125 - 60}{28.5} = 2.28°C/W$$

This means that if a 2 mm thick Al plate (with an unfinished surface) is used as the heat sink, then figure 3 shows that the following area S is required.

$S = 625\ cm^2$ (25 × 25 cm)

Also, from formula ④, we see that the power transistor junction temperature Tj at this time will be:

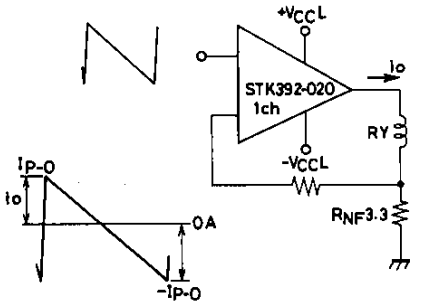
$$Tj = Pd\ max \times \theta c\text{-}a + Ta + Pc\ max \times \theta j\text{-}c$$
$$= 28.5 \times 2.28 + 60 + 9.5 \times 2.1$$
$$= 145°C$$

This is a 5°C derating from the required 150°C Tj max.

(Addendum) To be precise, the power dissipated in the early stage circuits (transistor, resistors, etc.) should also be taken into consideration.

Figure 1: Sawtooth wave input (AC) Ip-o – Pd1
Figure 2: DC input Io(DC) – Pd1
Figure 3: Aluminum plate thermal resistance characteristics

Sawtooth wave Input

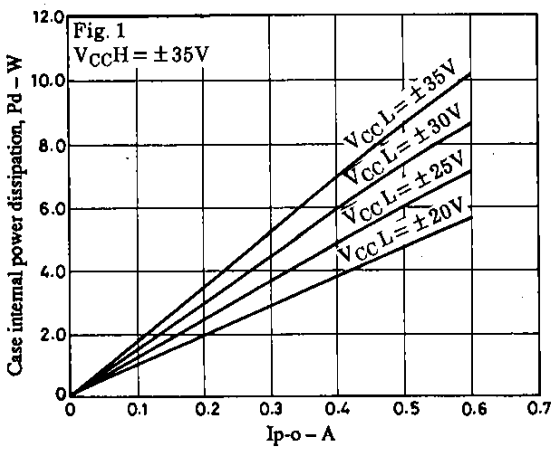


$$Pd = \frac{V_{CC}\, Ip\text{-}o}{2} = \frac{R\, Ip\text{-}o^2}{3}$$

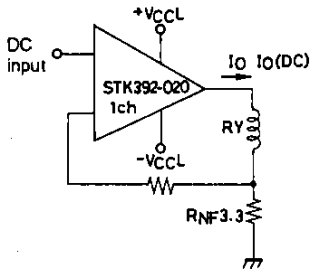
$(R = R_{NF} + R_Y \fallingdotseq R_{NF})$

⇩

Pd – Ip-o



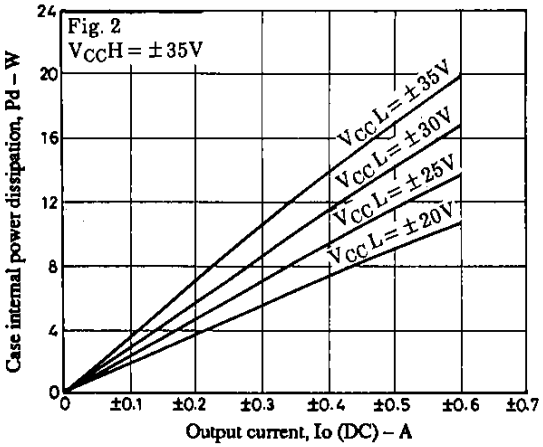
DC Input



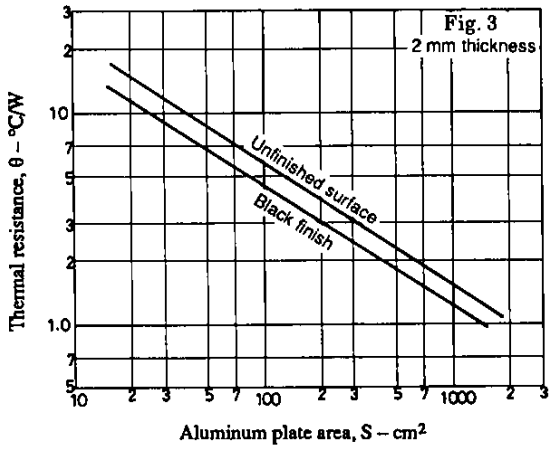
$$Pd = \{V_{CC} - (R_{NF} \times I_{DC})\} \times I_{DC}$$

⇩

Pd – Io



Aluminum plate thermal resistance



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