

## Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
-20	0.017 @ V <sub>GS</sub> = -4.5 V	-12
	0.020 @ V <sub>GS</sub> = -2.5 V	-11
	0.024 @ V <sub>GS</sub> = -1.8 V	-10.1

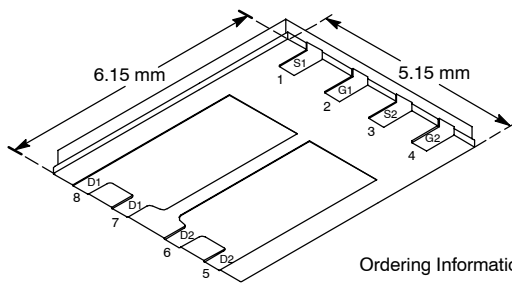
### FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

### APPLICATIONS

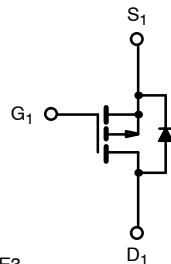
- Load Switch

PowerPAK SO-8

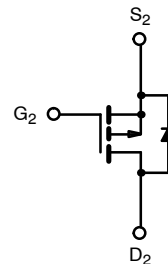


Bottom View

Ordering Information: Si7983DP-T1—E3



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	-20		V
Gate-Source Voltage		V <sub>GS</sub>	± 8		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-12	-7.7	A
	T <sub>A</sub> = 70 °C		-9.6	-6.2	
Pulsed Drain Current		I <sub>DM</sub>	-30		
continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	-2.9	-1.2	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5	1.4	W
	T <sub>A</sub> = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 sec	R <sub>thJA</sub>	26	35	°C/W
	Steady State		60	85	
Maximum Junction-to-Case (Drain)		R <sub>thJC</sub>	2.2	2.7	

Notes

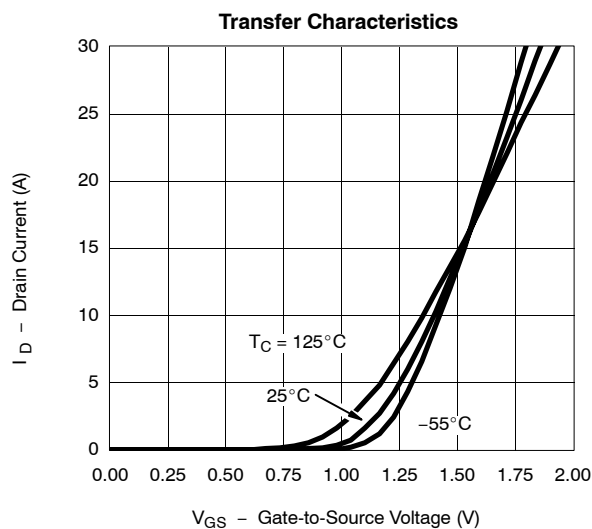
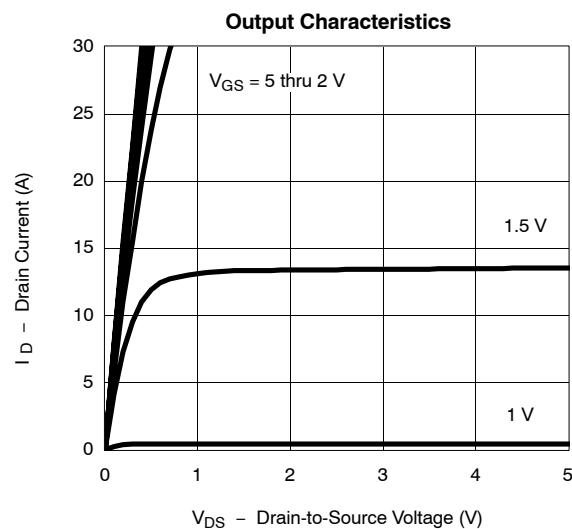
a. Surface Mounted on 1" x 1" FR4 Board.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

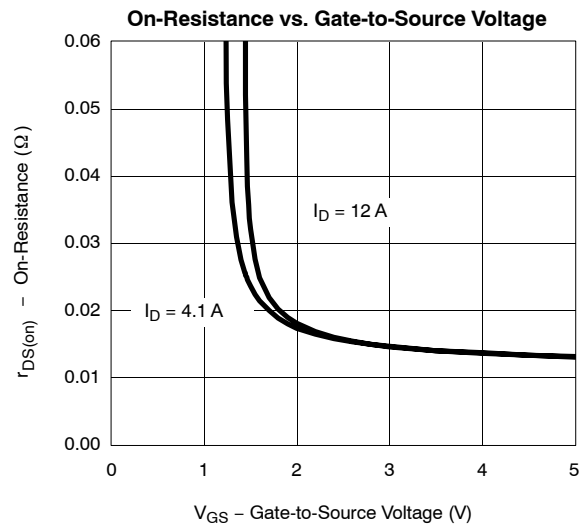
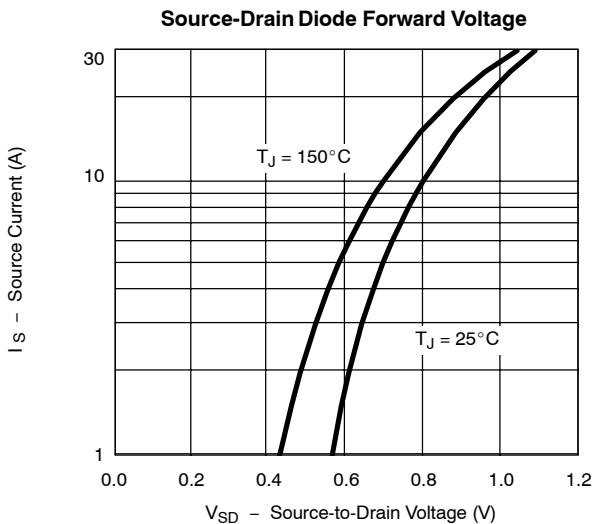
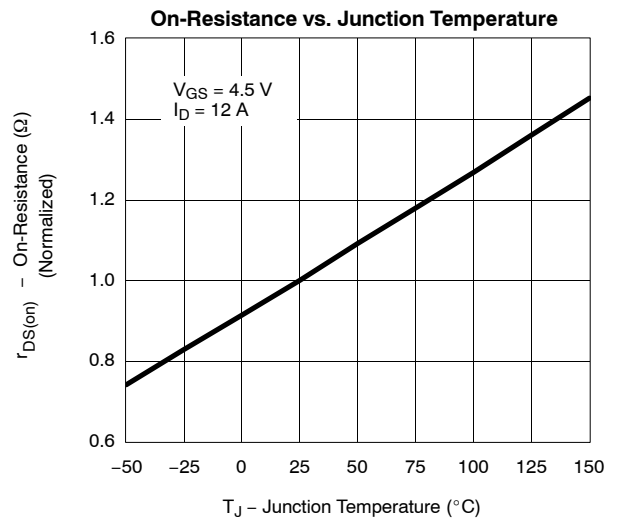
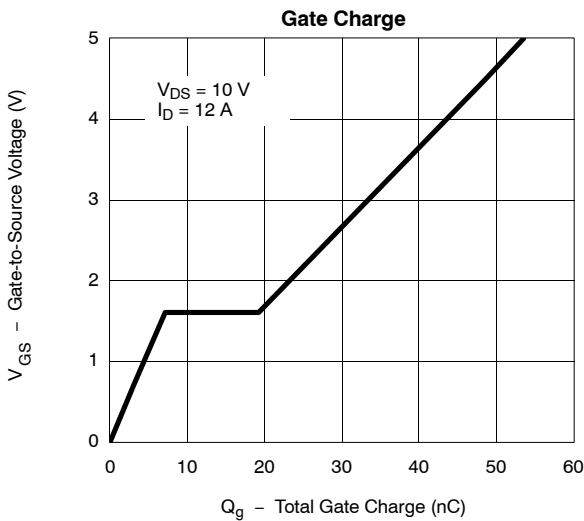
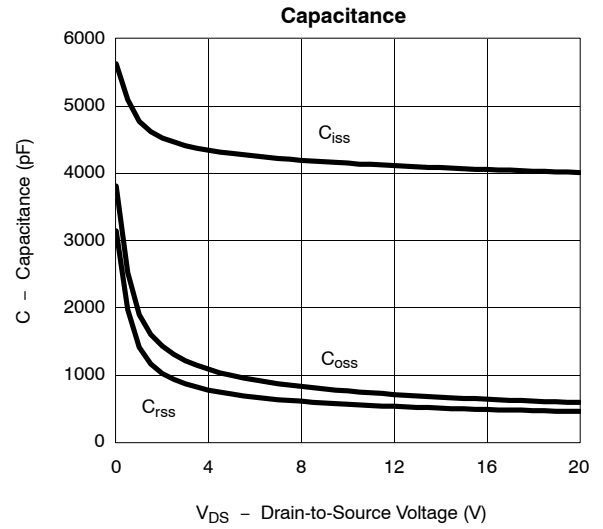
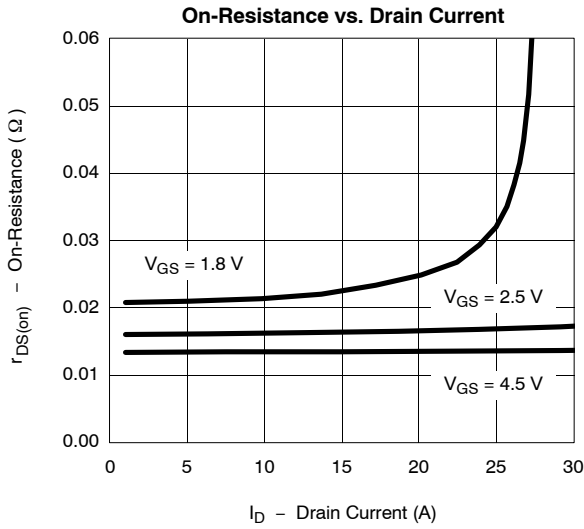
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -600 μA	-0.40		-1	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			-5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -12 A		0.014	0.017	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -11 A		0.016	0.020	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -4.1 A		0.020	0.024	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -12 A		41		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -2.9 A, V <sub>GS</sub> = 0 V		-0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -12 A		49	74	nC
Gate-Source Charge	Q <sub>gs</sub>			7.2		
Gate-Drain Charge	Q <sub>gd</sub>			12.1		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		8		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≈ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 Ω		35	55	ns
Rise Time	t <sub>r</sub>			60	90	
Turn-Off Delay Time	t <sub>d(off)</sub>			390	585	
Fall Time	t <sub>f</sub>			190	285	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = -2.9 A, di/dt = 100 A/μs		106	

## Notes

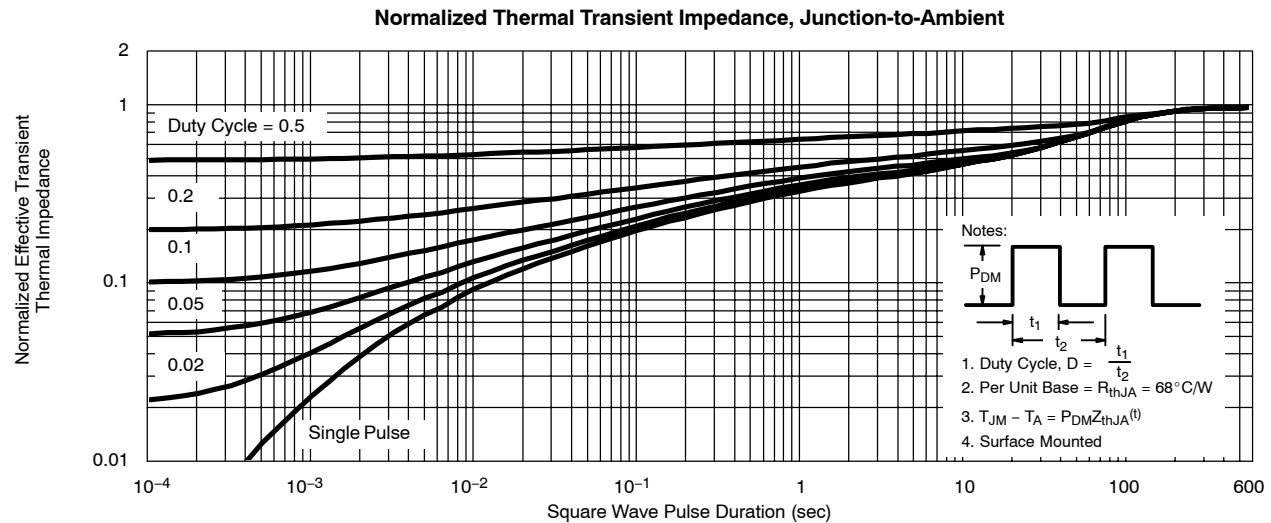
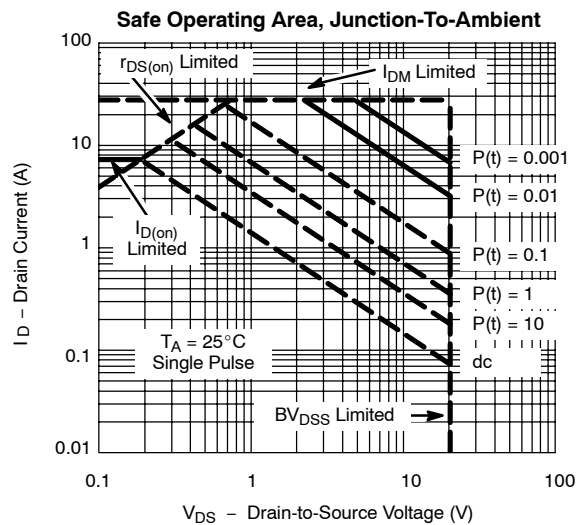
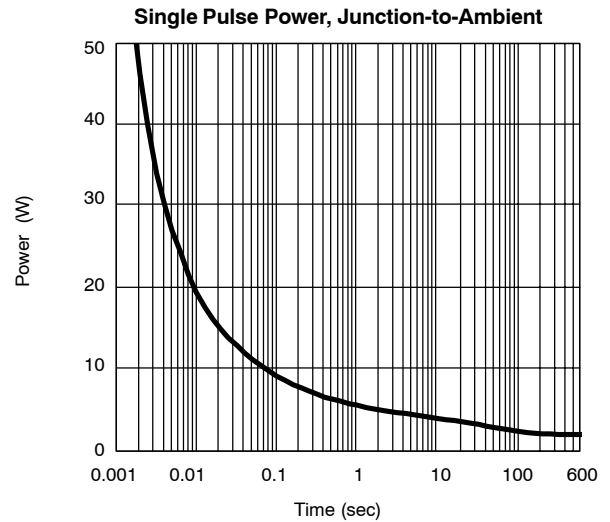
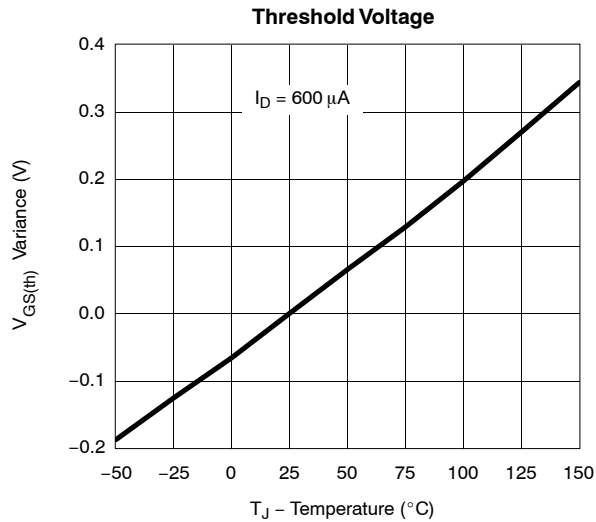
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

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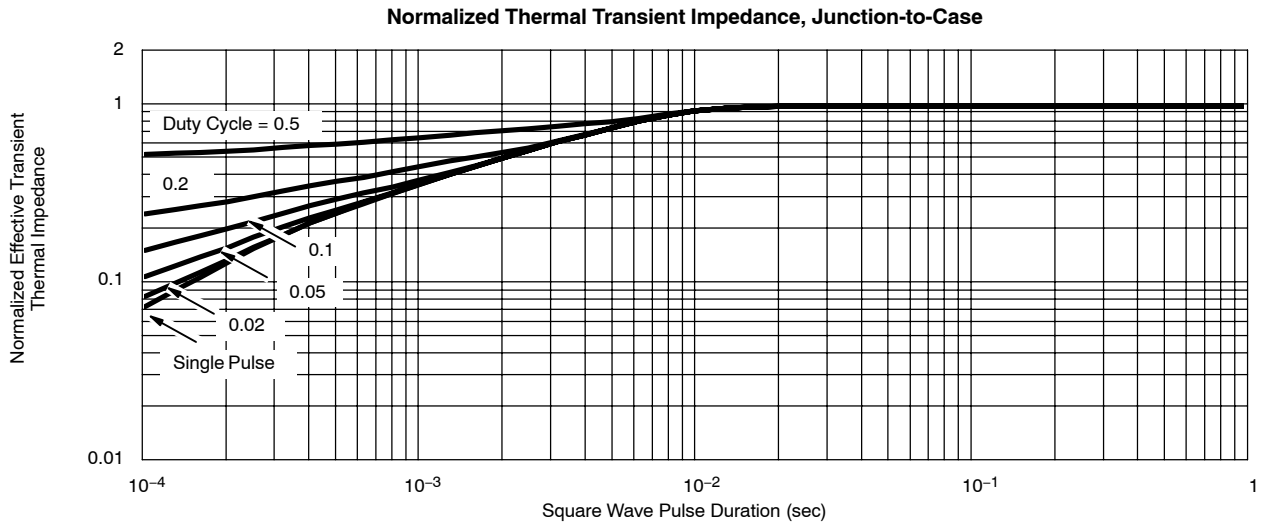


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