

### **New Product**

Si7439DP **Vishay Siliconix** 

# P-Channel 150-V (D-S) MOSFET

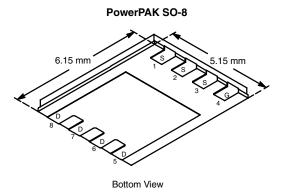
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)			
- 150	0.090 at $V_{GS} = -10 \text{ V}$	- 5.2			
	0.095 at V <sub>GS</sub> = $-6$ V	- 5.0			

#### **FEATURES**

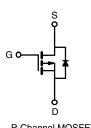
- TrenchFET<sup>®</sup> Power MOSFETS
- Ultra-Low On-Resistance Critical for Application
  - Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100 % R<sub>g</sub> and Avalanche Tested

#### **APPLICATIONS**

• Active Clamp in Intermediate DC/DC Power Supplies



Ordering Information: Si7439DP-T1-E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	<sub>A</sub> = 25 °C, unles	ss otherwise r	oted			
Parameter		Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 150		V	
Gate-Source Voltage		V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>1</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 5.2	- 3.0		
Continuous Drain Current $(T_J = 150^{\circ} \text{ C})^{\circ}$	T <sub>A</sub> = 70 °C		- 4.1	- 2.4		
Pulsed Drain Current		I <sub>DM</sub>	- 50		А	
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	- 4.2	- 1.6	A	
Single Pulse Avalanche Current	L = 1.0 mH	I <sub>AS</sub>	- 40 80			
Single Pulse Avalanche Energy		E <sub>AS</sub>				
Maria Dissingtion	T <sub>A</sub> = 25 °C	P.	5.4	1.9	W	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	PD	3.4	1.2	vv	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	– 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>		*	260		U	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum hunstion to Anglianta	$t \le 10$ sec	R <sub>thJA</sub>	18	23	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		50	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.0	1.5	

Notes

a. Surface Mounted on 1" x 1" FR4 Board. b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection. c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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COMPLIANT

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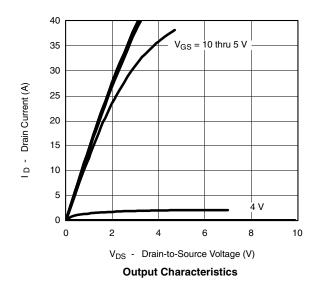


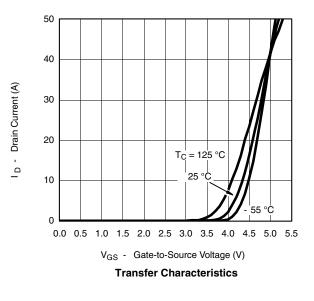
<b>SPECIFICATIONS</b> T <sub>J</sub> = 25 °C, unless otherwise noted								
Parameter	Symbol	mbol Test Condition Min Typ		Тур	Max	Unit		
Static								
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 2.0		- 4.0	V		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -150 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1			
		$V_{DS} = -150 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			- 10	μΑ		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 30			А		
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = -10$ V, $I_D = -5.2$ A		0.073	0.090	0		
	r <sub>DS(on)</sub>	$V_{GS} = -6 V, I_{D} = -5.0 A$		0.077	0.095	Ω		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -15 \text{ V}, \text{ I}_{D} = -5.2 \text{ A}$		19		S		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{S} = -4.2 \text{ A}, V_{GS} = 0 \text{ V}$		- 0.78	- 1.2	V		
Dynamic <sup>b</sup>	•			•	•			
Total Gate Charge	Qg			88	135			
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -75$ V, $V_{GS} = -10$ V, $I_{D} = -5.2$ A		17.5		nC		
Gate-Drain Charge	Q <sub>gd</sub>			26.5				
Gate Resistance	Rg		1.5	3	4.5	Ω		
Turn-On Delay Time	t <sub>d(on)</sub>			25	40			
Rise Time	t <sub>r</sub>	$V_{DD}$ = – 75 V, R <sub>L</sub> = 15.5 Ω		46	70			
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_{\text{D}}\cong$ – 4.8 A, $\text{V}_{\text{GEN}}$ = – 10 V, $\text{R}_{\text{G}}$ = 6 $\Omega$		115	180	ns		
Fall Time	t <sub>f</sub>			64	100			
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 2.9 A, di/dt = 100 A/μs		100	150			

Notes a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

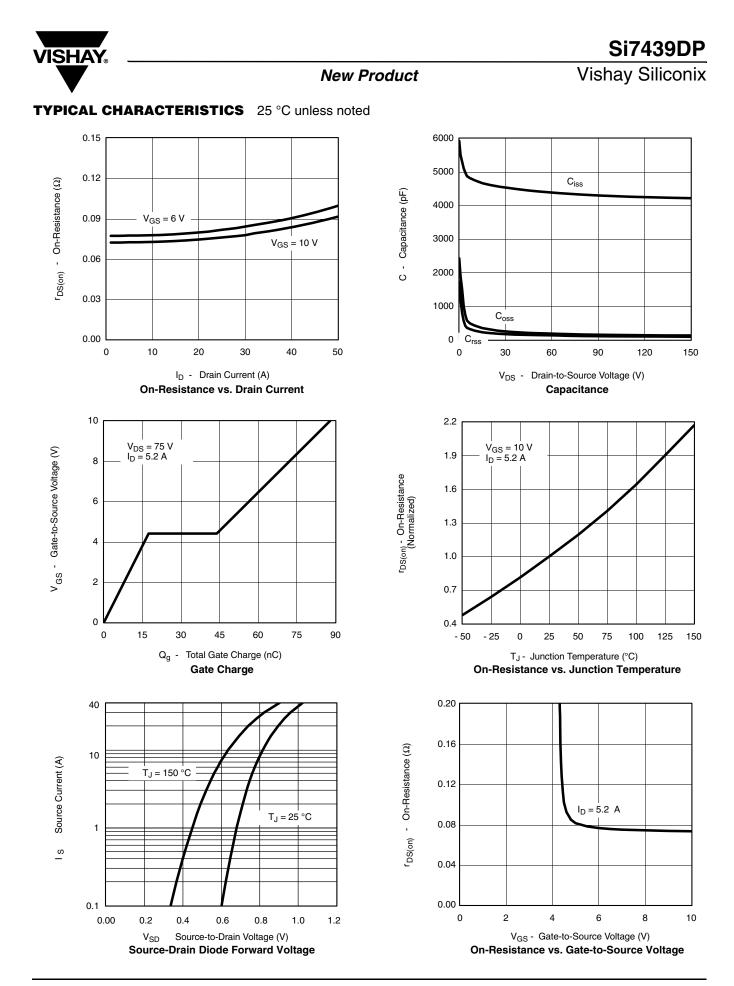
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C unless noted





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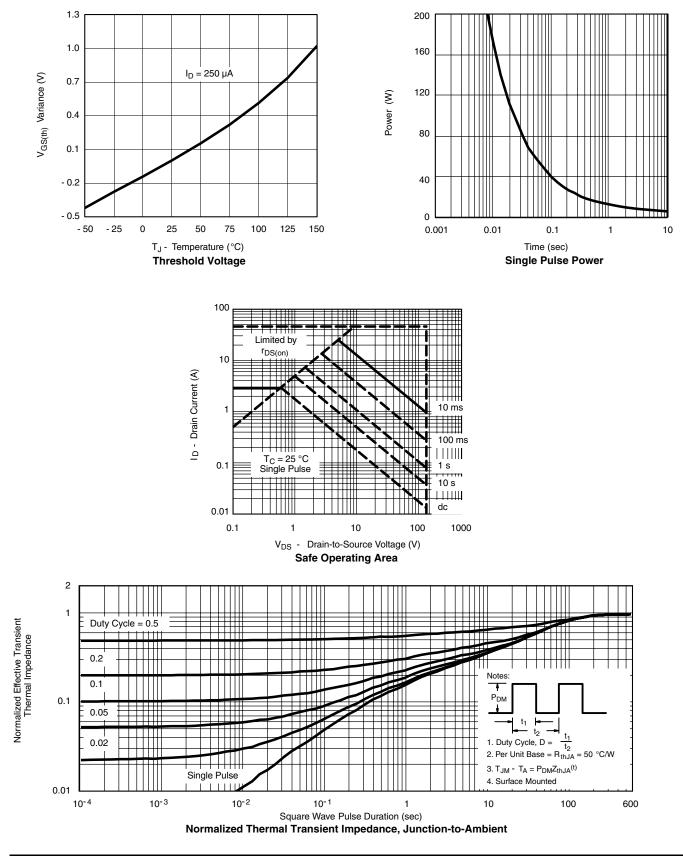


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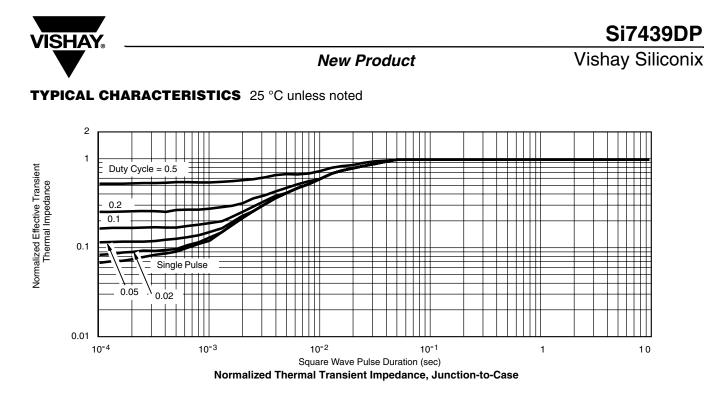
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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73106.



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