

## P-Channel 60-V (D-S) MOSFET



RoHS  
COMPLIANT

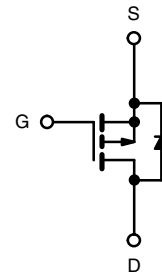
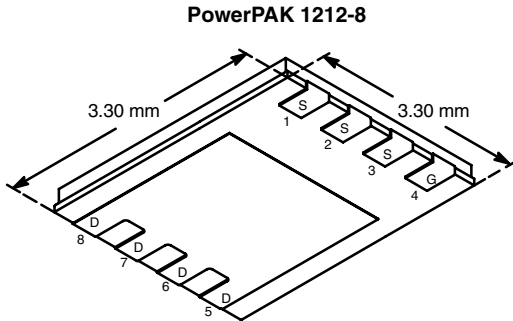
PRODUCT SUMMARY			
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ)
-60	0.115 @ $V_{GS} = -10$ V	-8	14.5 nC
	0.146 @ $V_{GS} = -4.5$ V	-8	

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Low Thermal Resistance PowerPAK<sup>®</sup> Package with Small Size and Low 1.07 mm Profile

### APPLICATIONS

- CCFL inverter
- Class D-amp



Ordering Information: Si7309DN-T1—E3 (Lead (Pb)-Free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	-60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	$I_D$	-8 <sup>a</sup>	A
	$T_C = 70^\circ\text{C}$		-7.8	
	$T_A = 25^\circ\text{C}$		-3.9 <sup>b, c</sup>	
	$T_A = 70^\circ\text{C}$		-3.1 <sup>b, c</sup>	
Pulsed Drain Current (10 $\mu\text{s}$ Width)		$I_{DM}$	-20	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	$I_S$	-8 <sup>a</sup>	A
	$T_A = 25^\circ\text{C}$		-2.7 <sup>b, c</sup>	
Avalanche Current		$I_{AS}$	-15	
Single-Pulse Avalanche Energy		$E_{AS}$	11	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	19.8	W
	$T_C = 70^\circ\text{C}$		12.7	
	$T_A = 25^\circ\text{C}$		3.2 <sup>b, c</sup>	
	$T_A = 70^\circ\text{C}$		2.1 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, d</sup>		$R_{thJA}$	31	39	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	5	6.3	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 Board.
- $t = 10$  sec
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is  $81^\circ\text{C/W}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA		-50		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		+3.8			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1		-3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20			±100	ns
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			-10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ -5 V, V <sub>GS</sub> = -10 V	-20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.9 A		0.092	0.115	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.5 A		0.120	0.146	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.9 A		10		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V, f = 1 MHz		600		pF
Output Capacitance	C <sub>oss</sub>			70		
Reverse Transfer Capacitance	C <sub>rSS</sub>			50		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.9 A		14.5	22	nC
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A		7.5	12	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A		2.2		
Gate-Drain Charge	Q <sub>gd</sub>			3.7		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		14		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, R <sub>L</sub> = 9.4 Ω I <sub>D</sub> ≅ -3.2 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω		25	40	ns
Rise Time	t <sub>r</sub>			80	120	
Turn-Off Delay Time	t <sub>d(off)</sub>			33	50	
Fall Time	t <sub>f</sub>			35	50	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, R <sub>L</sub> = 9.4 Ω I <sub>D</sub> ≅ -3.2 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		10	15	
Rise Time	t <sub>r</sub>			15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			30	45	
Fall Time	t <sub>f</sub>			33	50	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			-8	A
Pulse Diode Forward Current	I <sub>SM</sub>				-20	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = -1.3 A, V <sub>GS</sub> = 0 V		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.3 A, di/dt = -100 A/μs, T <sub>J</sub> = 25 °C		30	50	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			32	50	nC
Reverse Recovery Fall Time	t <sub>a</sub>			17		ns
Reverse Recovery Rise Time	t <sub>b</sub>			13		

## Notes

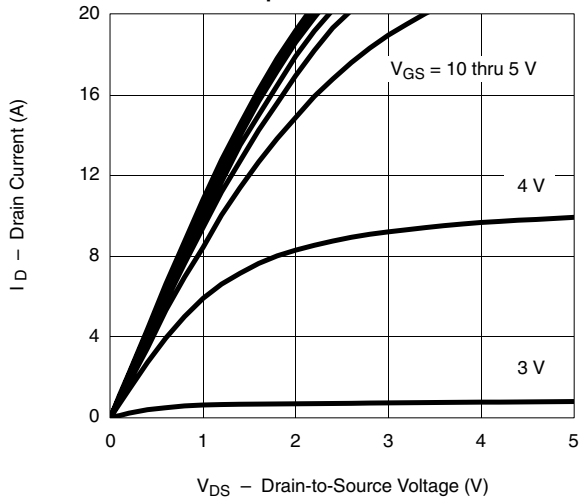
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

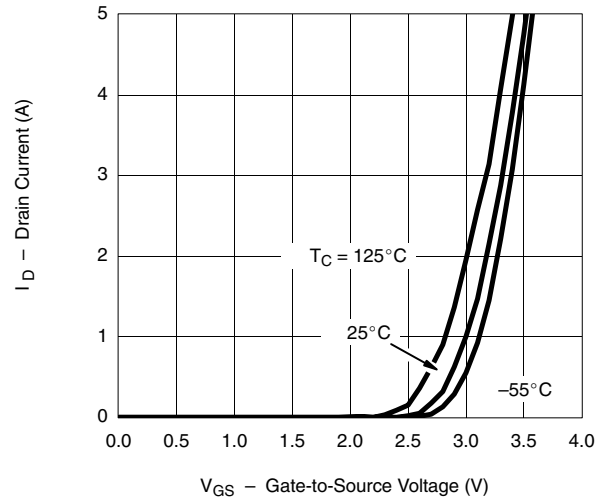


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

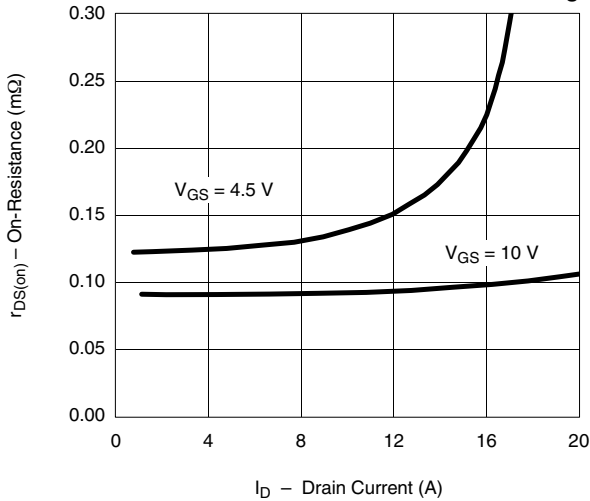
Output Characteristics



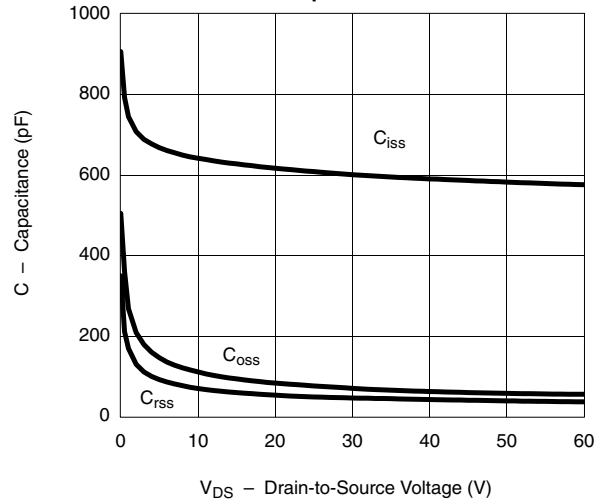
Transfer Characteristics



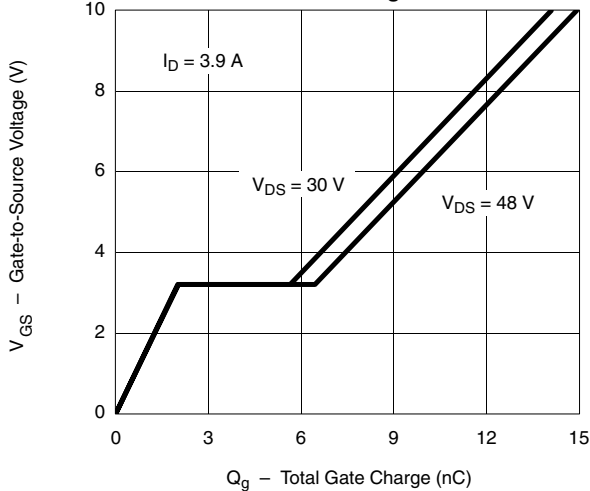
On-Resistance vs. Drain Current and Gate Voltage



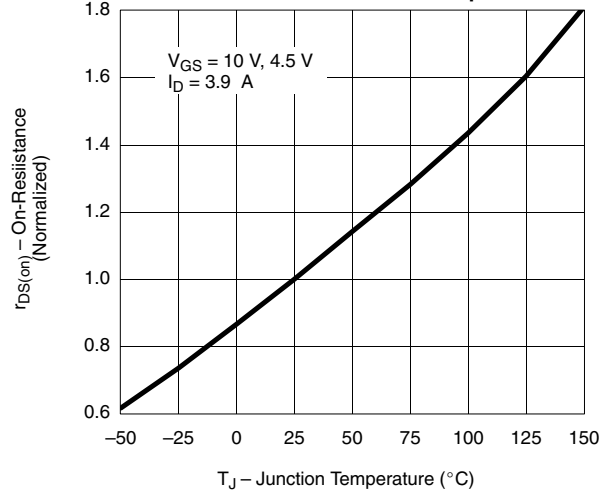
Capacitance



Gate Charge



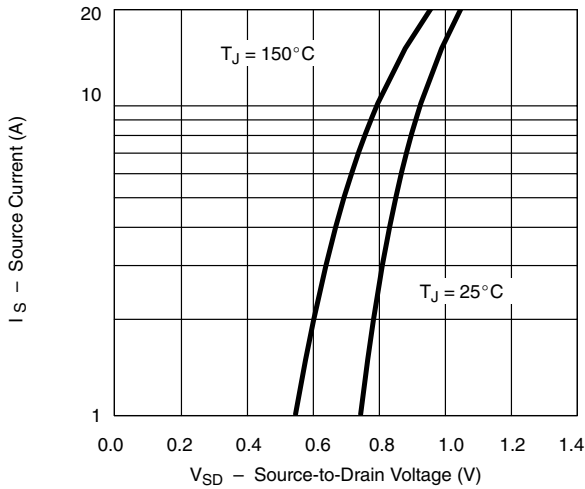
On-Resistance vs. Junction Temperature



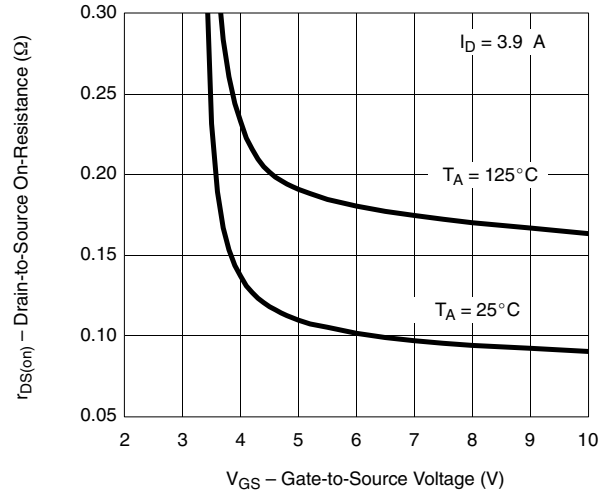


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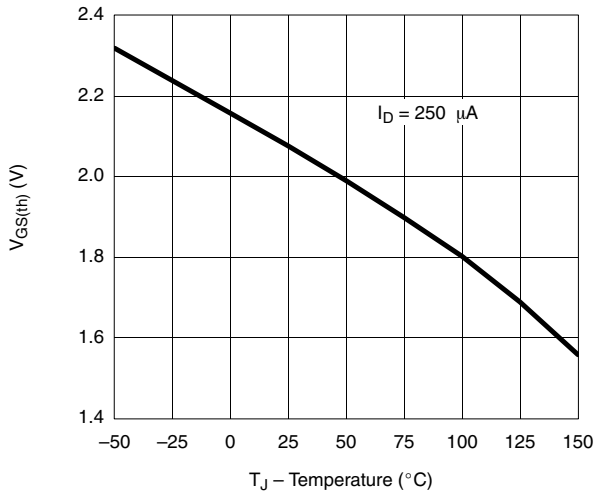
Source-Drain Diode Forward Voltage



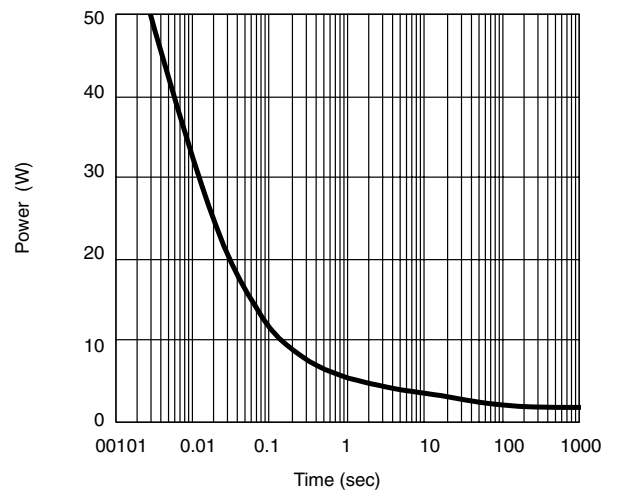
On-Resistance vs. Gate-to-Source Voltage



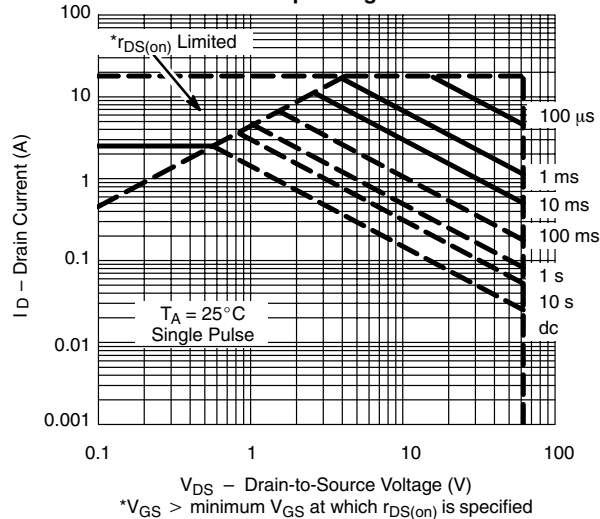
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

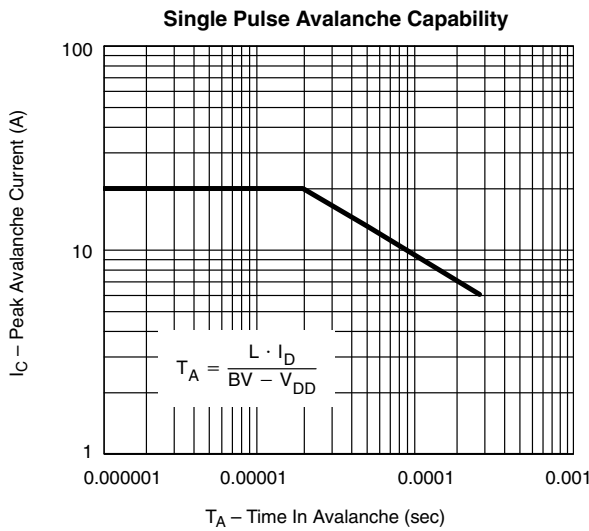
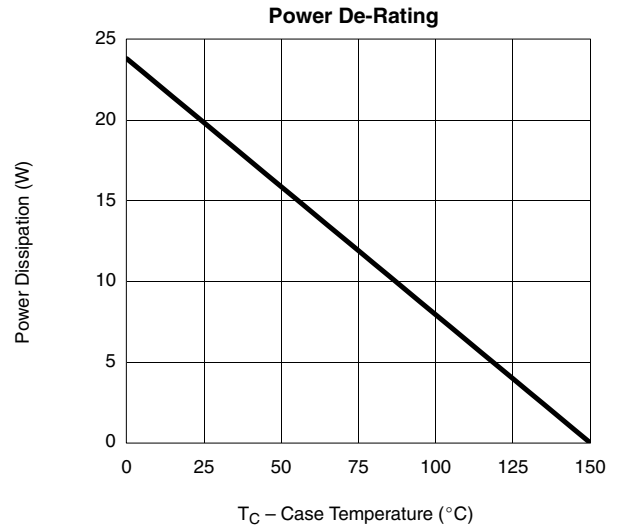
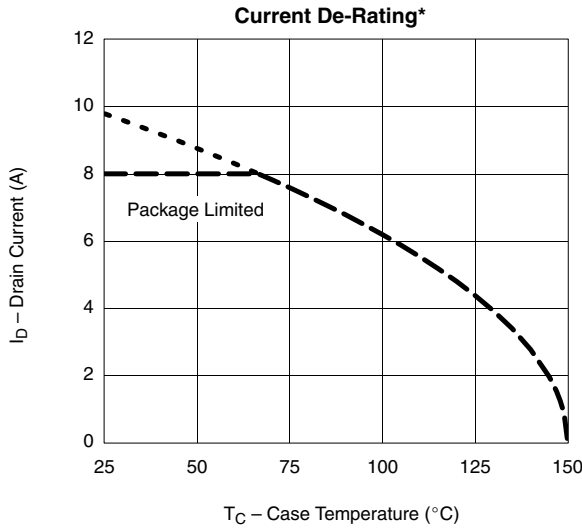


Safe Operating Area





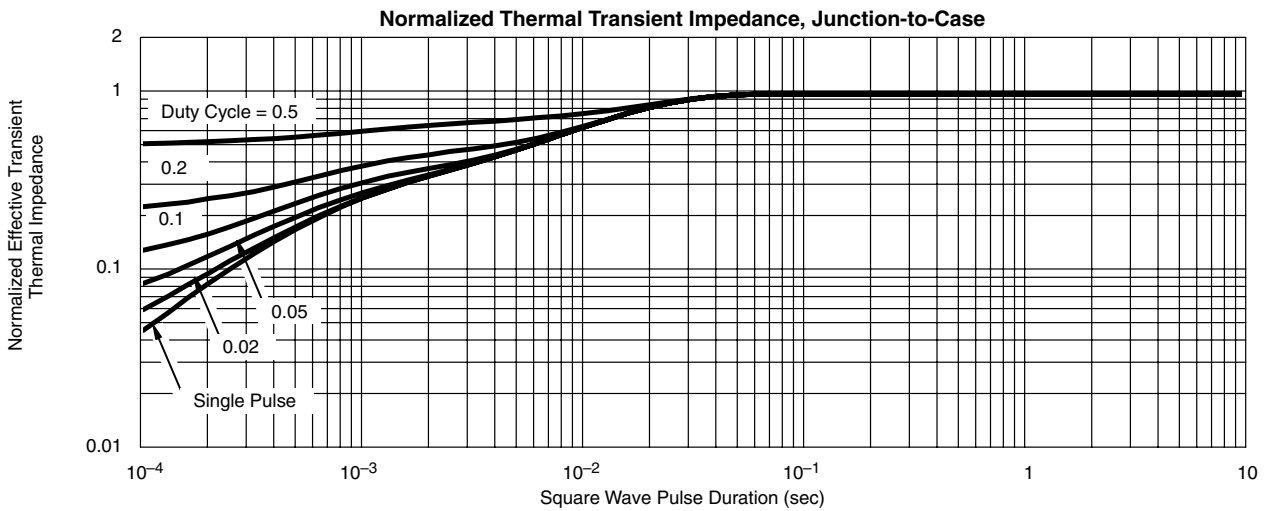
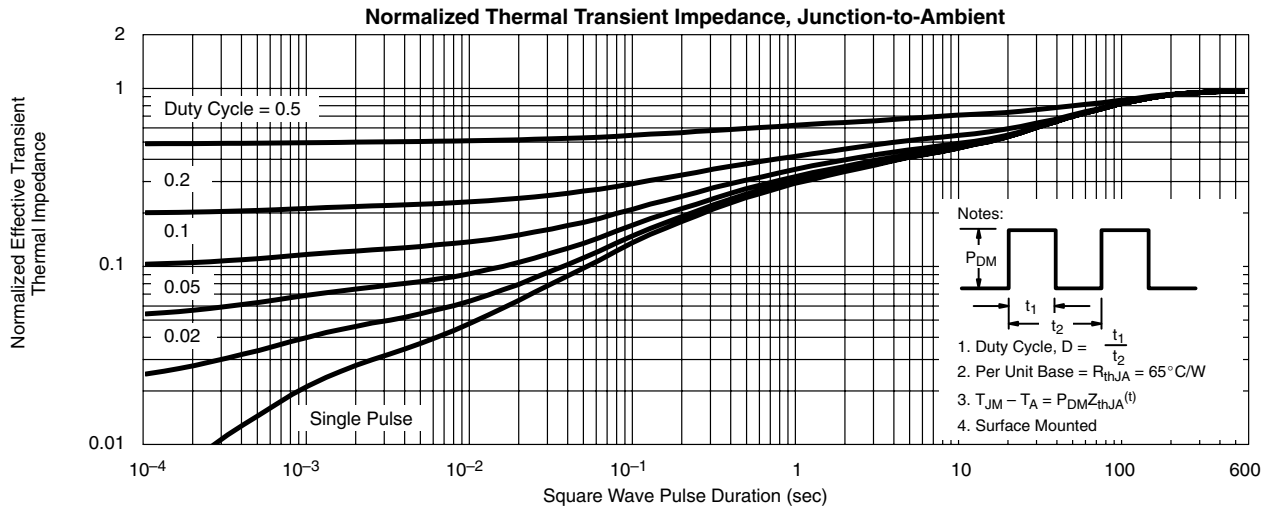
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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