

P-Channel 150-V (D-S) MOSFET



Product Is Completely Pb-free

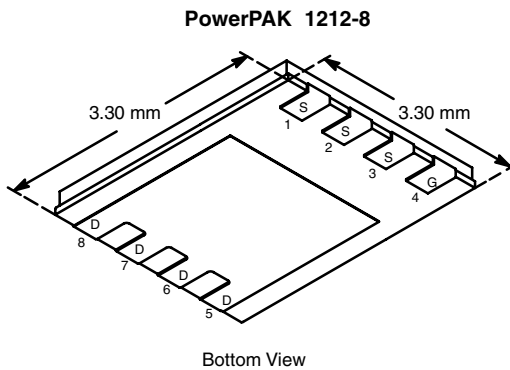
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
-150	1.2 @ $V_{GS} = -10$ V	-2.17	7.7 nC
	1.3 @ $V_{GS} = -6$ V	-2.1	

FEATURES

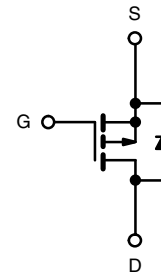
- TrenchFET® Power MOSFETs
- PowerPAK® Package
 - Low Thermal Resistance
 - Low 1.07-mm Profile

APPLICATIONS

- Active Clamp circuits in DC/DC Power Supplies



Ordering Information: Si7117DN-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	I_D	$T_C = 25^\circ\text{C}$	-2.17 ^c
		$T_C = 70^\circ\text{C}$	-1.7
		$T_A = 25^\circ\text{C}$	-1.1 ^{a, b}
		$T_A = 70^\circ\text{C}$	-0.9 ^{a, b}
Pulsed Drain Current	I_{DM}	-2.2	A
Continuous Source-Drain Diode Current ^{a, b}	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	-2.6 ^{a, b}
Single Pulse Avalanche Current	I_{AS}	4.5	A
Single Pulse Avalanche Energy	E_{AS}	1.01	mJ
Maximum Power Dissipation ^{a, b}	P_D	$T_C = 25^\circ\text{C}$	12.5
		$T_C = 70^\circ\text{C}$	8
		$T_A = 25^\circ\text{C}$	3.2 ^{a, b}
		$T_A = 70^\circ\text{C}$	2 ^{a, b}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^c		260	

Notes:

- Surface Mounted on 1" x 1" FR4 Board.
- $t = 5$ sec
- See Solder Profile (<http://www.vishay.com/doc/73478>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ sec	R_{thJA}	31	39	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	8	10	

Notes:

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. Maximum under steady state conditions is 81 °C/W.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\ \mu\text{A}$		145		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.5		-4.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			-100	ns
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -150\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 15\text{ V}, V_{GS} = -10\text{ V}$	-1.6			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}$		1.0	1.2	Ω
		$V_{GS} = -6\text{ V}, I_D = -0.5\text{ A}$		1.05	1.3	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -0.5\text{ A}$		2.2		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		340	510	pF
Output Capacitance	C_{oss}			30		
Reverse Transfer Capacitance	C_{rss}			16		
Total Gate Charge	Q_g	$V_{DS} = -75\text{ V}, V_{GS} = -10\text{ V}, I_D = -0.5\text{ A}$		7.7	12	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			2.5		
Gate Resistance	R_g	$f = 1\text{ MHz}$		9		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75\text{ V}, R_L = 7.5\ \Omega$ $I_D \cong -1.0\text{ A}, V_{GEN} = -10\text{ V}, R_g = 6\ \Omega$		7	11	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			16	25	
Fall Time	t_f			11	17	



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-12	A
Pulse Diode Forward Current	I_{SM}				-12	
Body Diode Voltage	V_{SD}	$I_S = -1.0\text{ A}, V_{GS} = 0\text{ V}$		-0.7	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -0.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		42	65	ns
Body Diode Reverse Recovery Charge	Q_{rr}			90	135	nC
Reverse Recovery Fall Time	t_a			35		ns
Reverse Recovery Rise Time	t_b			7		

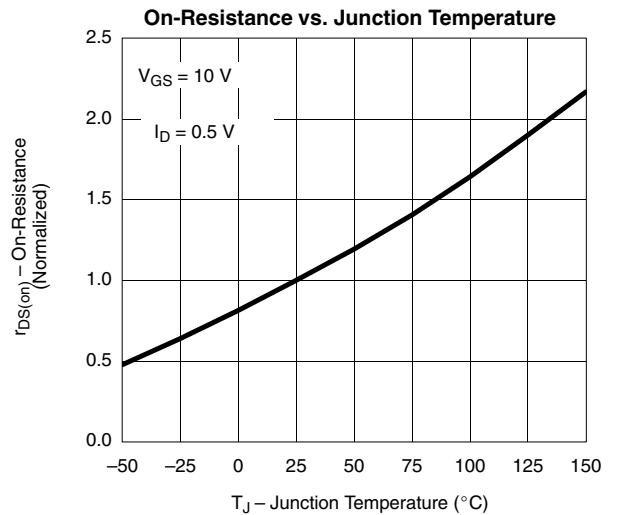
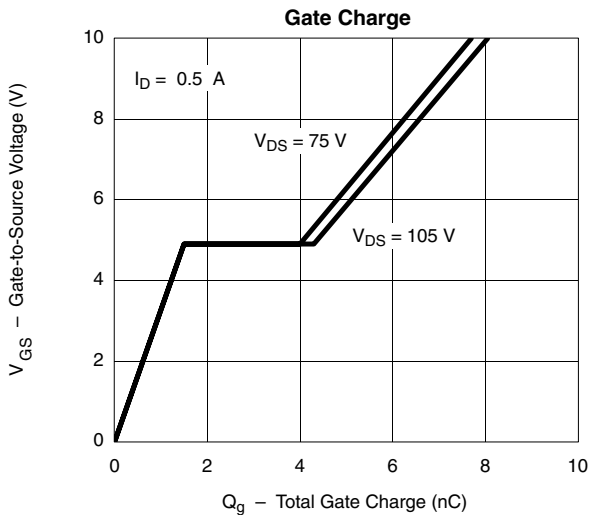
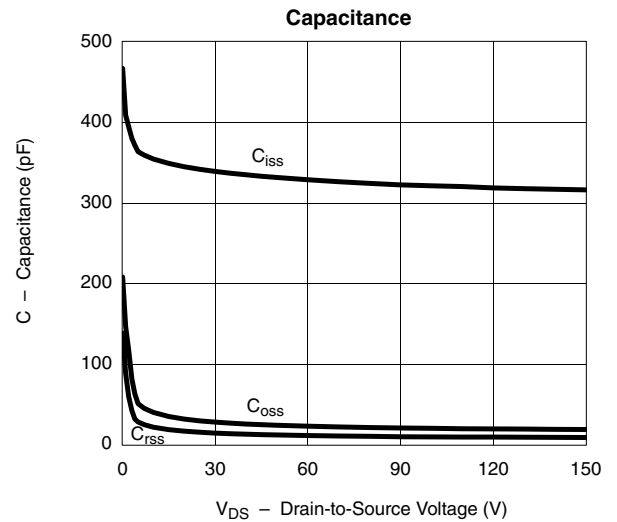
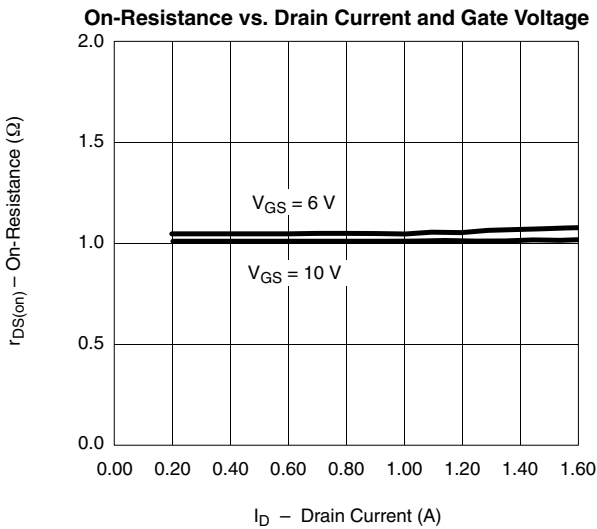
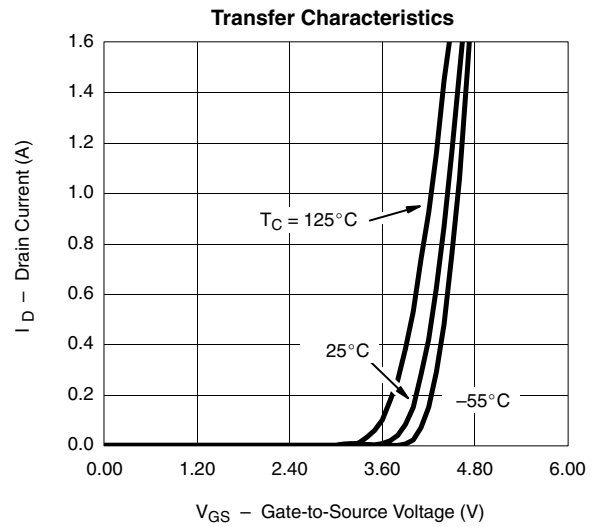
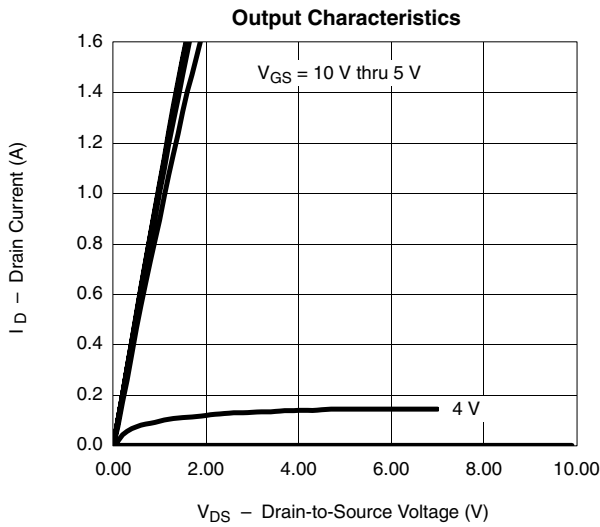
Notes

- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



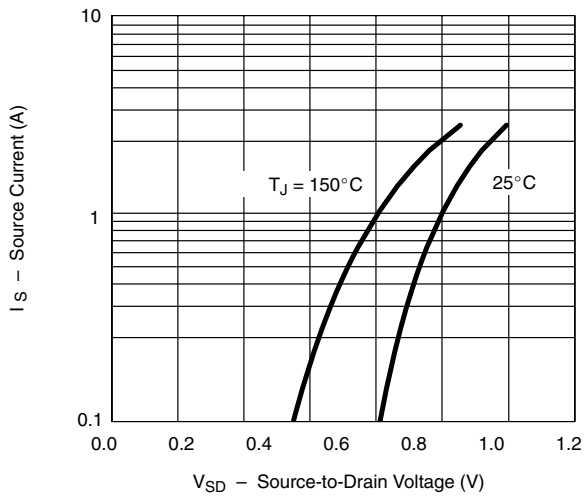
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



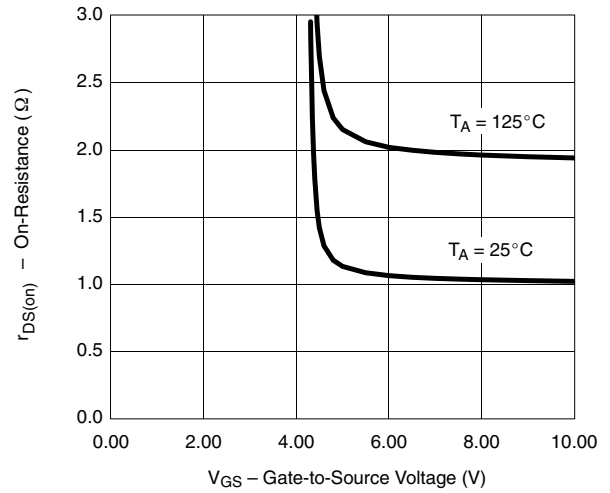


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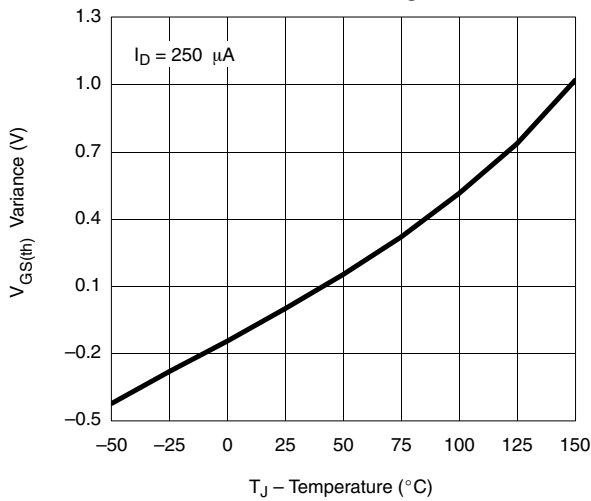
Source-Drain Diode Forward Voltage



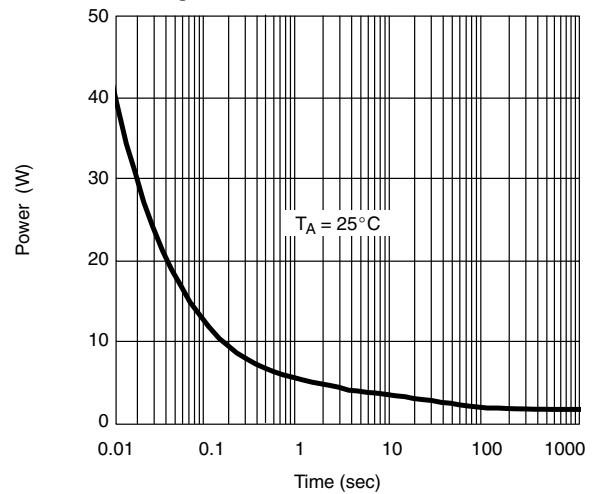
On-Resistance vs. Gate-to-Source Voltage



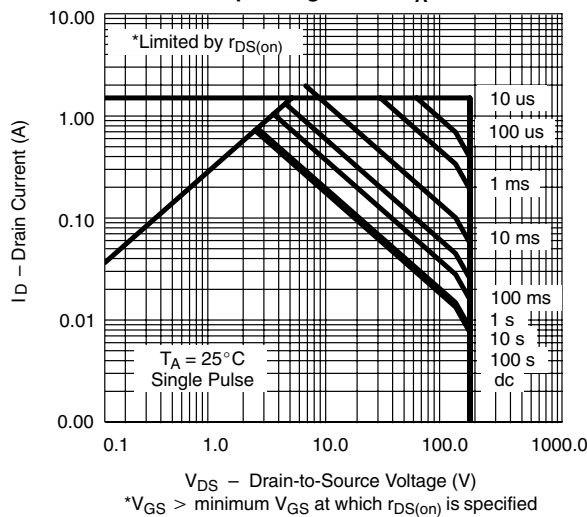
Threshold Voltage



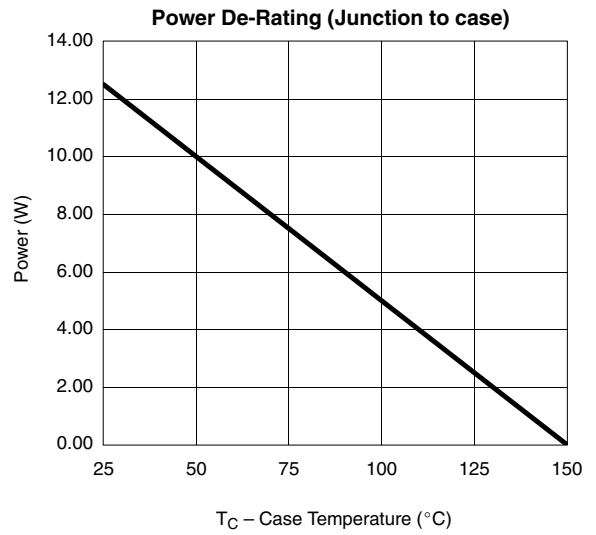
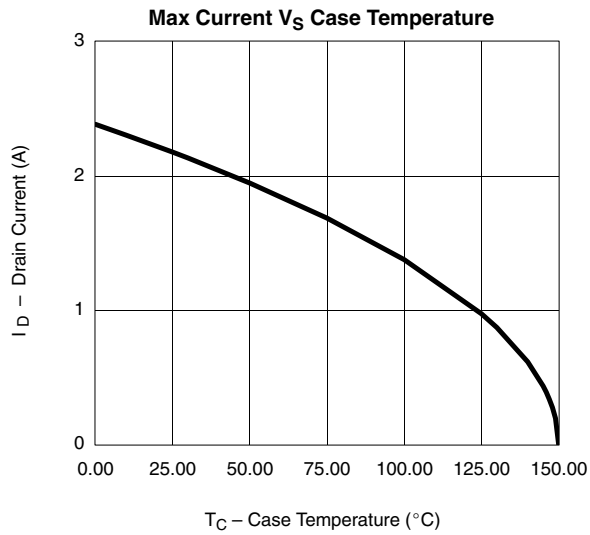
Single Pulse Power, Junction-to-Ambient



Safe Operating Area at $T_A = 25^\circ\text{C}$



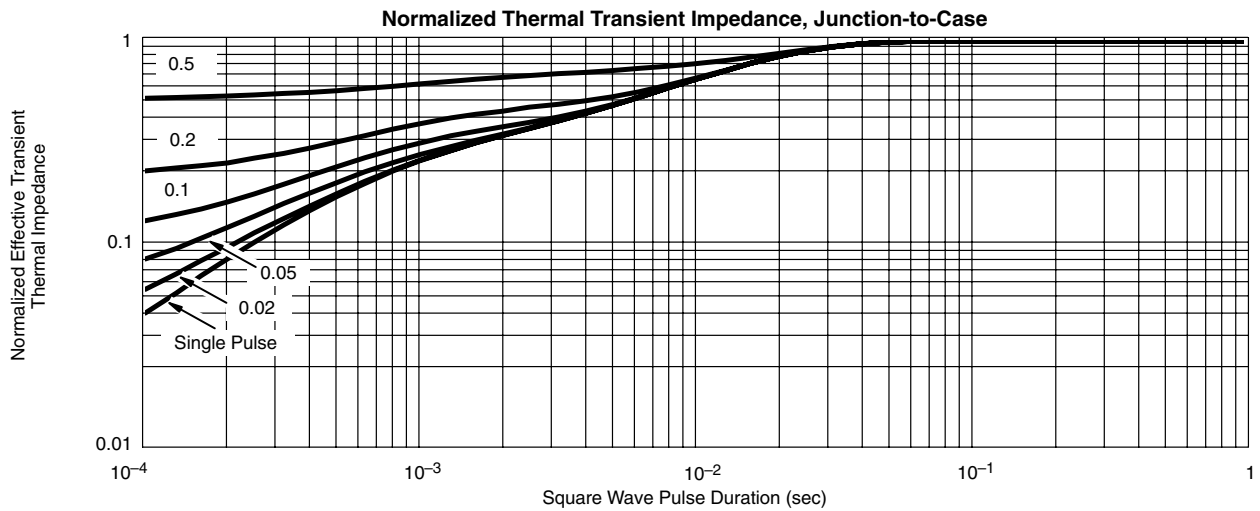
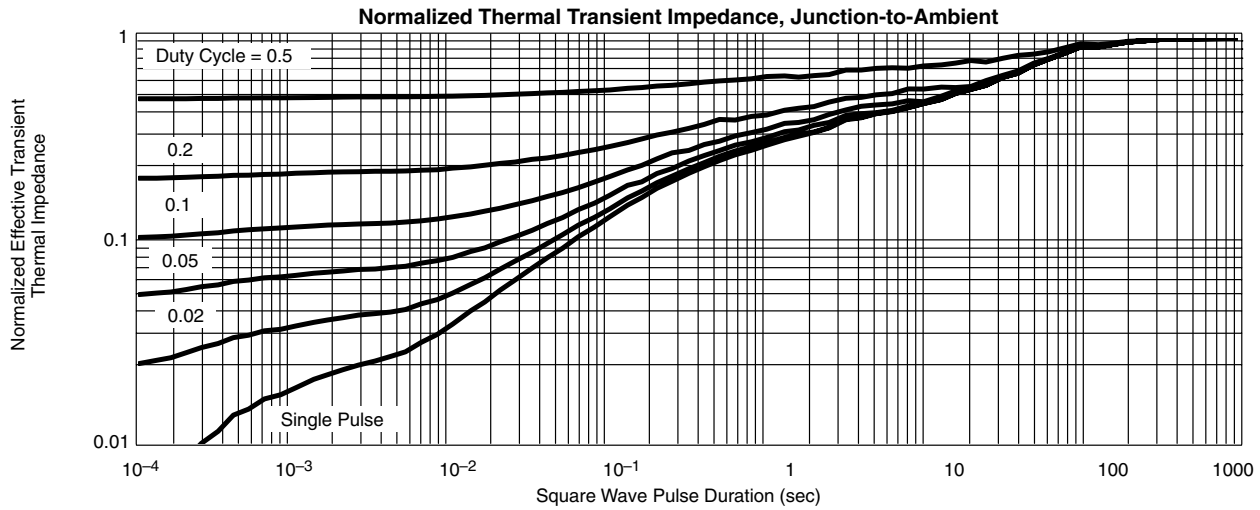
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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