EVB71121

300 to 930MHz Receiver Evaluation Board Description

Features

- Dual RF input for antenna space and frequency diversity, LNA cascading or differential feeding
- Fully integrated PLL-based synthesizer
- 2^{nd} mixer with image rejection
- Reception of ASK or FSK modulated signals
- Wide operating voltage and temperature ranges
- Very low standby current consumption
- Low operating current consumption
- Internal IF filter
- Internal FSK demodulator
- Average or peak detection data slicer mode
- RSSI output with high dynamic range for RF level indication
- Output noise cancellation filter
- MCU clock output
- High over-all frequency accuracy

Ordering Information

Part No. (see paragraph 4)

EVB71121-315-C
EVB71121-433-C
EVB71121-868-C
EVB71121-915-C

Note 1: Peak detection mode is default population.

Application Examples

- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

General Description

The MLX71121 is a multi-band, single-channel RF receiver based on a double-conversion super-heterodyne architecture. It can receive FSK and ASK modulated signals. The IC is designed for general purpose applications for example in the European bands at 433MHz and 868MHz or for similar applications in North America or Asia, e.g. at 315MHz or 915MHz.
The receiver's extended temperature and supply voltage ranges make the device a perfect fit for automotive or similar applications where harsh environmental conditions are expected.

Document Content

1 Theory of Operation

1.1 General

The MLX71121 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). As the first intermediate frequency (IF1) is very high, a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA. The second mixer MIX2 is an image-reject mixer.

The receiver signal chain is setup by one (or two) low noise amplifier(s) (LNA1, LNA2), two down-conversion mixers (MIX1, MIX2), an on-chip IF filter (IFF) as well as an IF amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-). A digital post-processing of the sliced data signal can be performed by a noise filter (NF) building block.

The dual LNA configuration can be used for antenna space diversity or antenna frequency diversity or to setup an LNA cascade (to further improve the input sensitivity). The two LNAs can also be setup to feed the RF signal differentially.

A sequencer circuit (SEQ) controls the timing during start-up. This is to reduce start-up time and to minimize power dissipation.

A clock output, which is a divide-by-8 version of the crystal oscillator signal, can be used to drive a microcontroller. The clock output is open collector and gets activated through a load connected to positive supply.

1.2 Technical Data Overview

- ❒ Input frequency ranges: 300 to 470MHz
  610 to 930MHz
- ❒ Power supply range: 2.1 to 5.5V
- ❒ Temperature range: -40 to +125°C
- ❒ Shutdown current: 50 nA
- ❒ Operating current: 10.0 to 11.1mA
- ❒ Internal IF: 1.8MHz with 300kHz 3dB bandwidth
- ❒ FM/FSK deviation range: ±10kHz to ±100kHz
- ❒ Image rejection:
  65dB 1st IF (with external RF front-end filter)
  25dB 2nd IF (internal image rejection)
- ❒ Maximum data rate: 50kps RZ (bi-phase) code,
  100kps NRZ
- ❒ Spurious emission: < -54dBm
- ❒ Linear RSSI range: > 60dB
- ❒ Crystal reference frequency: 16 to 27MHz
- ❒ MCU clock frequency: 2.0 to 3.4MHz

❒ Input Sensitivity: at 4kbps NRZ, BER = $3 \cdot 10^{-3}$

Frequency		315 MHz	433 MHz	868 MHz	915 MHz
FSK	internal IF2=1.8MHz, 300kHz BW, Δf = ±20kHz	-107dBm	-107dBm	-104dBm	-102dBm
ASK	internal IF2=1.8MHz, 300kHz BW	-112dBm	-112dBm	-108dBm	-105dBm

Note: - Sensitivities given for RF input 1 (without SAW filter)
- Sensitivity for RF input 2 is about 2 to 3dB worse (because of SAW filter loss)

1.3 Block Diagram

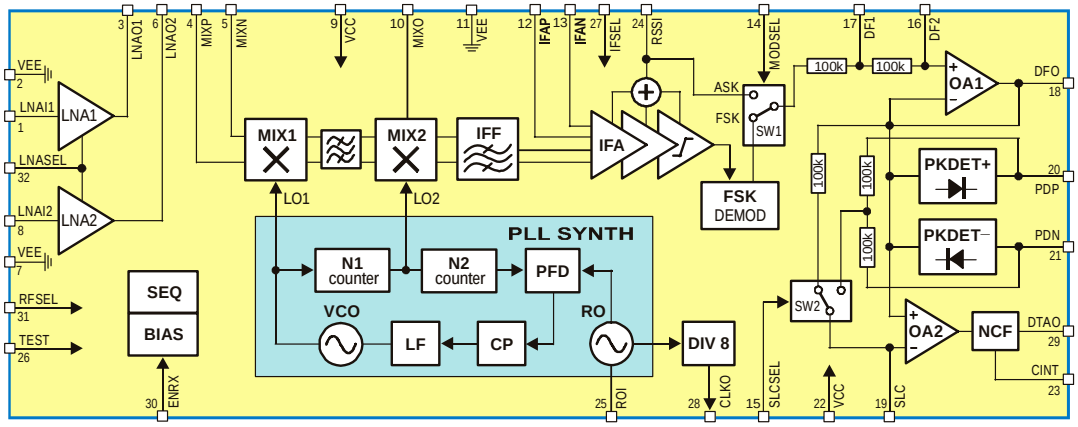


Fig. 1: MLX71121 block diagram

The MLX71121 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2. The PLL SYNTH consists of a fully integrated voltage-controlled oscillator (VCO), a distributed feedback divider chain (N1, N2), a phase-frequency detector (PFD) a charge pump (CP), a loop filter (LF) and a crystal-based reference oscillator (RO).
- Two low-noise amplifiers (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF Filter (IFF) with a 1.8MHz center frequency and a 300kHz 3dB bandwidth
- IF amplifier (IFA) to provide a high voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detection mode.
- Noise cancellation filter (NCF)
- Sequencer circuit (SEQ) and biasing (BIAS) circuit
- Clock output (DIV8)

1.4 Operating Modes

ENRX	Description
0	Shutdown mode
1	Receive mode

Note: ENRX is pulled down internally.

1.5 Frequency Range

Two different receive frequency ranges can be selected by the control signal RFSEL.

RFSEL	Description
0	Input frequency range 300 to 470MHz
1	Input frequency range 610 to 930MHz

1.6 LNA Selection

LNASEL	Description
0	LNA1 active, LNA2 shutdown
Hi-Z	LNA1 and LNA2 active
1	LNA1 shutdown, LNA2 active

Note: Hi-Z state means pin LNASEL is left floating (pin is internally pulled to $V_{CC}/2$ in this case).

1.7 Demodulation Selection

MODSEL	Description
0	ASK demodulation
1	FSK demodulation

1.8 Data Slicer

SLCSEL	Description
0	Averaging detection mode
1	Peak detection mode

2 Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

LO1 high side and LO2 high side: receiving at f_{RF}(high-high)
LO1 high side and LO2 low side: receiving at f_{RF}(high-low)
LO1 low side and LO2 high side: receiving at f_{RF}(low-high)
LO1 low side and LO2 low side: receiving at f_{RF}(low-low)

As a result, four different radio frequencies (RFs) could yield one and the same second IF (IF2). Fig. 2 shows this for the case of receiving at f_{RF}(high-high). In the example of Fig. 2, the image signals at f_{RF}(low-high) and f_{RF}(low-low) are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at f_{RF}(low-high) and f_{RF}(low-low).

The two remaining signals at IF1 resulting from f_{RF}(high-high) and f_{RF}(high-low) are entering the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 2, LO2 high-side injection has been chosen to select the IF2 signal resulting from f_{RF}(high-high).

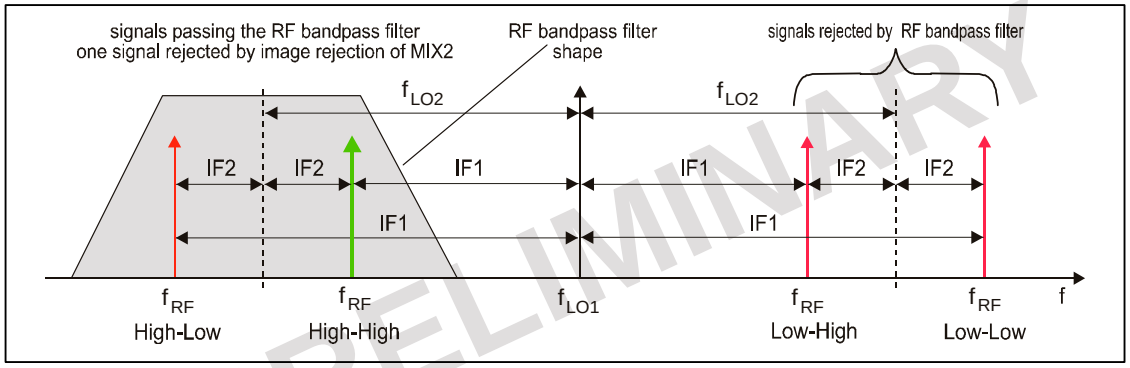


Fig. 2: The four receiving frequencies in a double conversion superhet receiver

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO signal frequencies (f_{LO1} , f_{LO2}) and the reference oscillator frequency f_{RO}.

$$f_{LO1} = N_1 \cdot f_{LO2} \qquad f_{LO2} = N_2 \cdot f_{RO}$$

The operating frequency of the internal IF filter (IFF) and FSK demodulator (FSK DEMOD) is 1.8MHz. Therefore the second IF (IF2) is set to 1.8MHz as well.

2.1 Calculation of Frequency Settings

The receiver has two predefined receive frequency plans which can be selected by the RFSEL control pin. Depending on the logic level of RFSEL pin the sideband selection of the second mixer and the counter settings for N_1 and N_2 are changed accordingly. (see in 1.5)

RFSEL	Injection	f_{Rfmin} [MHz]	f_{Rfmax} [MHz]	N_1	N_2
0	high-low	300	470	4	6
1	low-high	610	930	2	12

The following table shows the relationships of several internal receiver frequencies for the two input frequency ranges.

f_{RF} [MHz]	f_{IF1}	f_{LO1}	f_{LO2}	f_{RO}
300 to 470	$\frac{f_{RF}+N_1 f_{IF2}}{N_1-1}$	$\frac{N_1(f_{RF}+f_{IF2})}{N_1-1}$	$\frac{f_{RF}+f_{IF2}}{N_1-1}$	$\frac{f_{RF}+f_{IF2}}{N_2(N_1-1)}$
610 to 930	$\frac{f_{RF}-N_1 f_{IF2}}{N_1+1}$	$\frac{N_1(f_{RF}+f_{IF2})}{N_1+1}$	$\frac{f_{RF}+f_{IF2}}{N_1+1}$	$\frac{f_{RF}+f_{IF2}}{N_2(N_1+1)}$

Given IF2 = 1.8MHz and the corresponding N_1, N_2 counter settings, above equations can be transferred into the following table.

f_{RF} [MHz]	f_{IF1}	f_{LO1}	f_{LO2}	f_{RO}
300 to 470	$\frac{f_{RF}+7.2MHz}{3}$	$\frac{4(f_{RF}+1.8MHz)}{3}$	$\frac{f_{RF}+1.8MHz}{3}$	$\frac{f_{RF}+1.8MHz}{18}$
610 to 930	$\frac{f_{RF}-3.6MHz}{3}$	$\frac{2(f_{RF}+1.8MHz)}{3}$		$\frac{f_{RF}+1.8MHz}{36}$

2.2 Standard Frequency Plans

IF2 = 1.8MHz.

RFSEL	f_{RF} [MHz]	f_{IF1} [MHz]	f_{LO1} [MHz]	f_{LO2} [MHz]	f_{RO} [MHz]
0	315	107.40	422.40	105.60	17.600000
	433.92	147.04	580.96	145.24	24.206667
1	868.3	288.23	580.07	290.03	24.169444
	915	303.80	611.20	305.60	25.466667

2.3 433/868MHz Frequency Diversity

The receiver's multi-band functionality can be used to operate at two different frequency bands just by changing the logic level at pin RFSEL and without changing the crystal. This feature is applicable for common use of the 433 and 868MHz bands. Below table shows the corresponding frequency plans.

IF2 = 1.8MHz.

RFSEL	f_{RF} [MHz]	f_{IF1} [MHz]	f_{LO1} [MHz]	f_{LO2} [MHz]	f_{RO} [MHz]
0	433.25	146.82	580.07	145.02	24.169444
1	868.3	288.23	580.07	290.03	

3 Dual-Channel Application Circuits for FSK & ASK Reception

3.1 Peak Detector Data Slicer

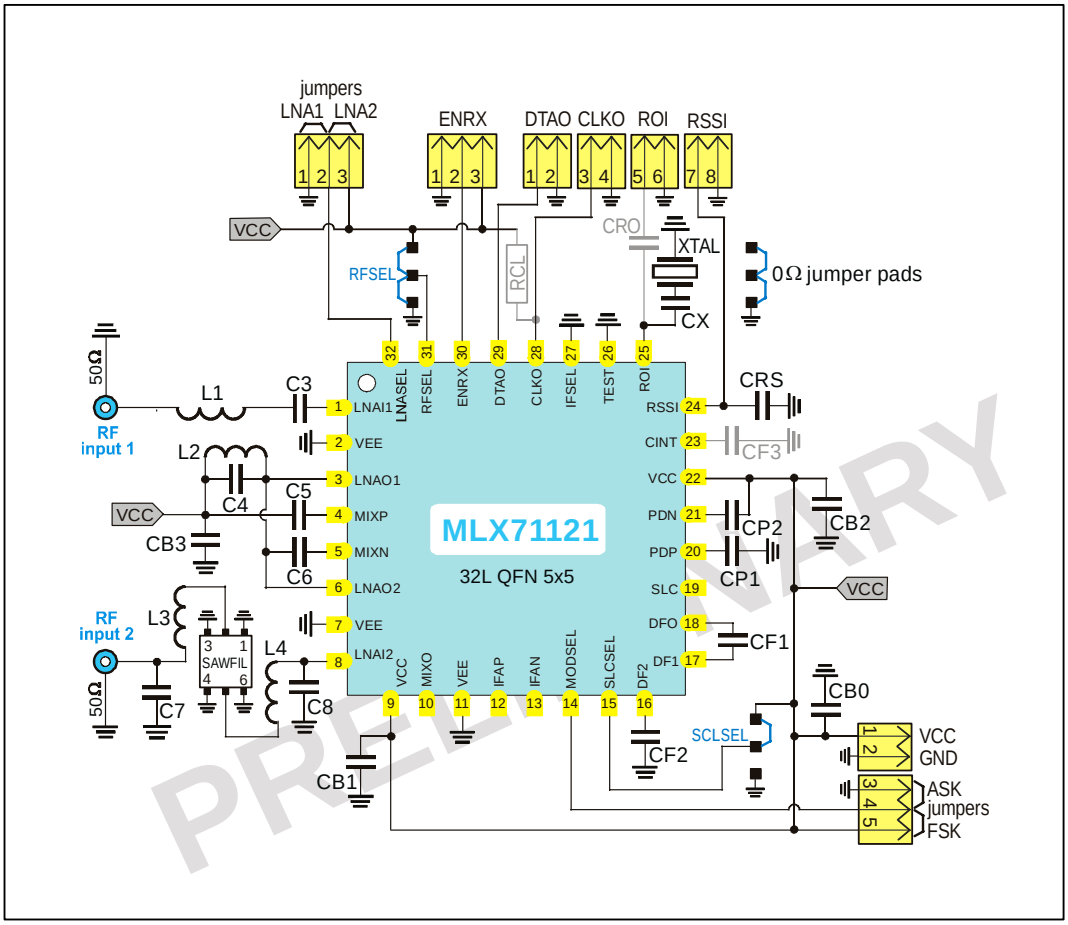


Fig. 3: Circuit schematic

3.1.1 Component Arrangement Top Side (Peak Detection Data Slicer)

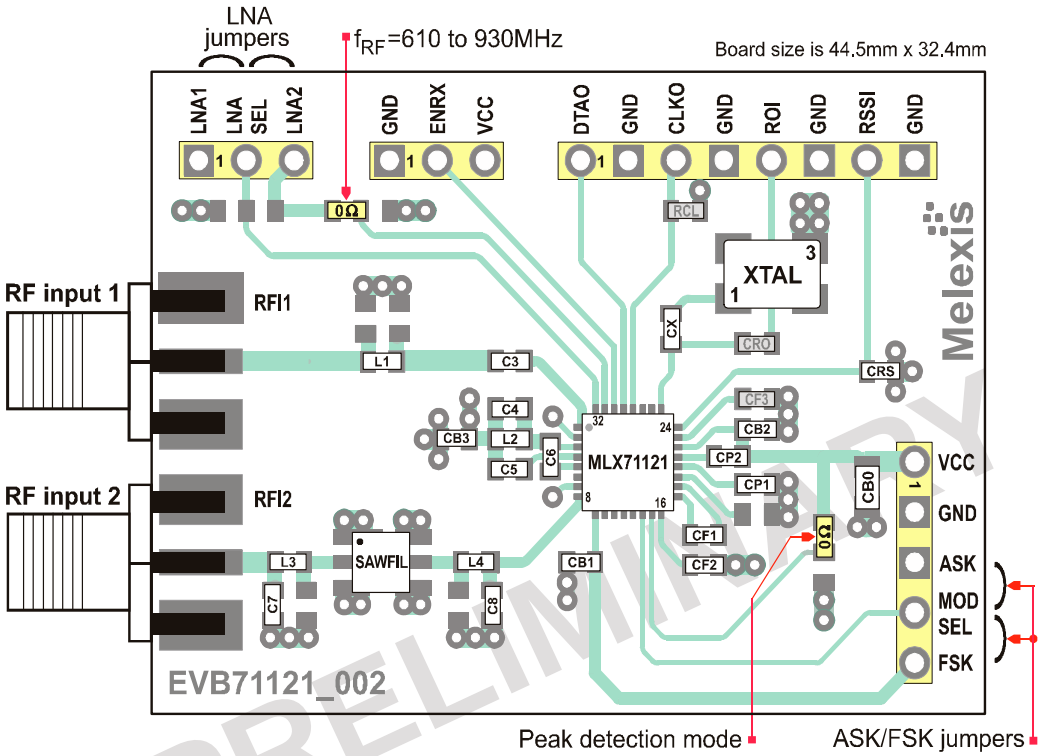


Fig. 4: PCB top-side view

3.2 Averaging Data Slicer Configured for Bi-Phase Codes

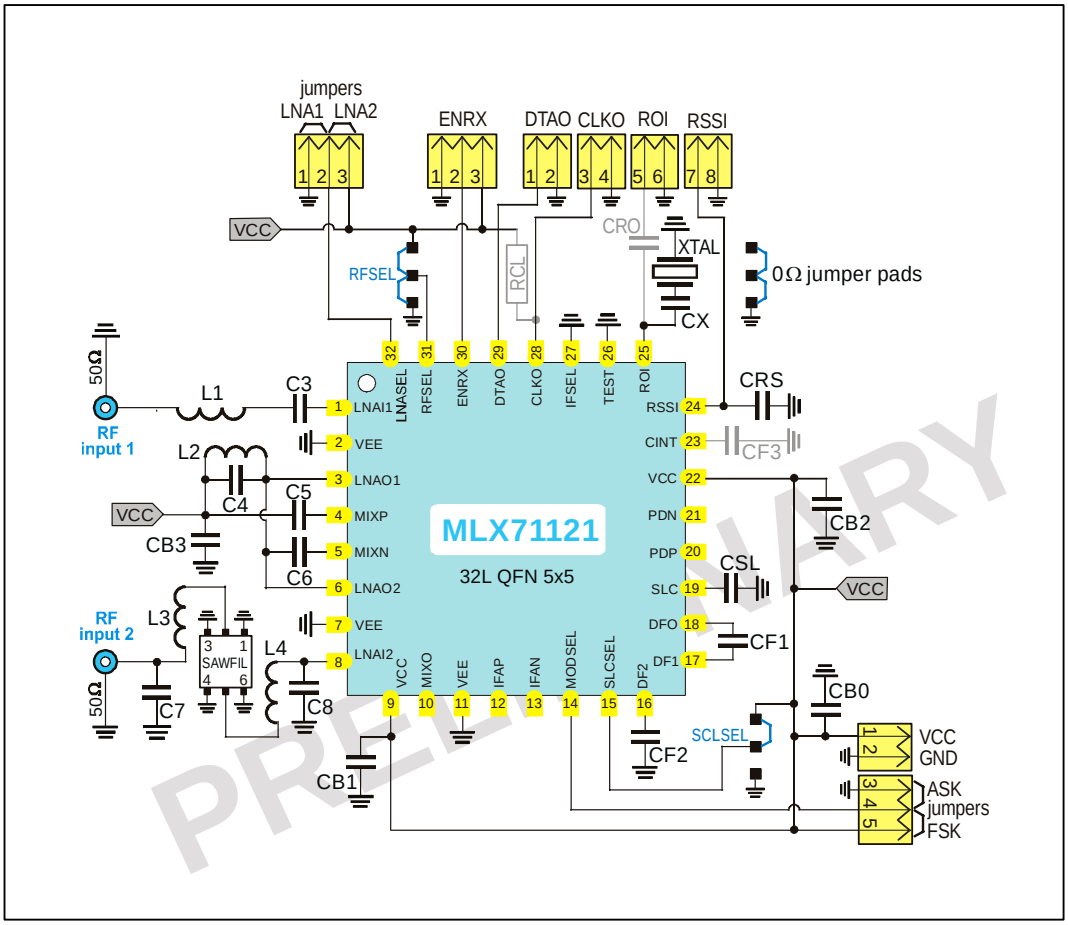


Fig. 5: Circuit schematic

3.2.1 Component Arrangement Top Side (Averaging Data Slicer)

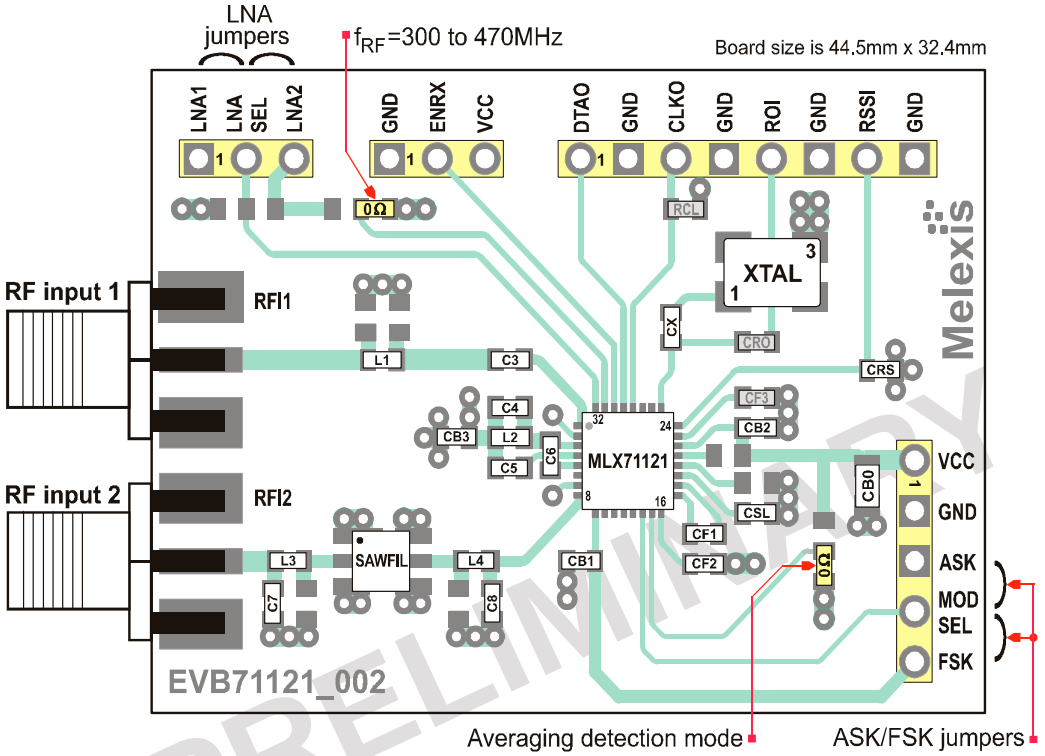


Fig. 6: PCB top-side view

3.3 Component List for Antenna Space Diversity

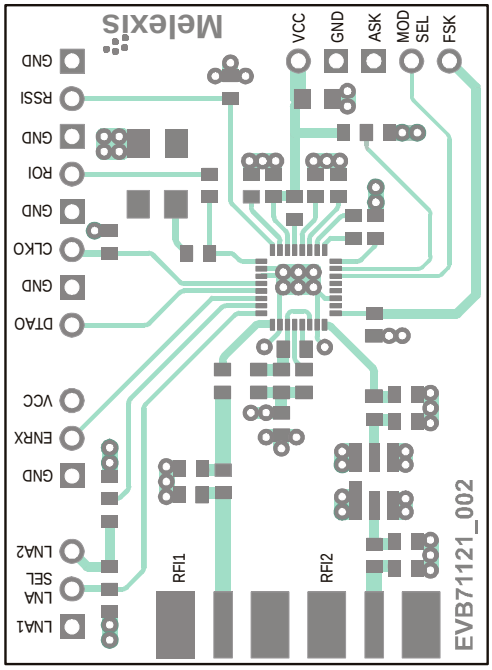
Below table is for all application circuits shown in Figures 3.1 and 3.2

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C3	0603	100 pF	100 pF	100 pF	100 pF	±5%	LNA input filtering capacitor
C4	0603	4.7 pF	3.9 pF	2.2 pF	1.5 pF	±5%	LNA output tank capacitor
C5	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 positive input matching capacitor
C6	0603	100 pF	100 pF	100 pF	100 pF	±5%	MIX1 negative input matching capacitor
C7	0603	NIP	NIP	3.9 pF	NIP	±5%	matching capacitor
C8	0603	NIP	NIP	1.0 pF	NIP	±5%	matching capacitor
CB0	0805	33 nF	33 nF	33 nF	33 nF	±10%	decoupling capacitor,
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor,
CB2	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor,
CB3	0603	330 pF	330 pF	330 pF	330 pF	±10%	decoupling capacitor,
CF1	0603	680 pF	680 pF	680 pF	680 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
CF2	0603	330 pF	330 pF	330 pF	330 pF	±10%	data low-pass filter capacitor, for data rate of 4 kbps NRZ
CF3	0603	value according to the date rate connected to ground if noise filter not used				±10%	optional capacitance for noise filter
CP1	0603	33 nF	33 nF	33 nF	33 nF	±10%	PKDET positive filtering capacitor, for data rate of 4 kbps NRZ
CP2	0603	33 nF	33 nF F	33 nF	33 nF	±10%	PKDET negative filtering capacitor, for data rate of 4 kbps NRZ
CRS	0603	1 nF	1 nF	1 nF	1 nF	±10%	RSSI output low pass capacitor, for data rate of 4 kbps NRZ
CRO	0603	1 nF	1 nF	1 nF	1 nF	±5%	optional capacitor, to couple external RO signal
CSL	0603	100 nF for averaging detection mode only	100 nF	100 nF	100 nF	±10%	data slicer capacitor, for data rate of 4 kbps NRZ
CX	0603	27 pF	27 pF	27 pF	27 pF	±5%	crystal series capacitor
L1	0603	56 nH	27 nH	0 Ω	0 Ω	±5%	matching inductor
L2	0603	27 nH	15 nH	3.9 nH	3.9 nH	±5%	LNA output tank inductor
L3	0603	0 Ω	68 nH	22 nH	0 Ω	±5%	matching inductor
L4	0603	56 nH	82 nH	22 nH	0 Ω	±5%	matching inductor
RCL	0603	3.3 kΩ	3.3 kΩ	3.3 kΩ	3.3 kΩ	±5%	optional CLK output resistor, to clock output signal generated
SAW FIL	SMD 3x3	SAFDC315M SM0T00 (315 MHz)	SAFCC433M BL0X00 (433.92 MHz)	SAFCC868M SL0X00 (868.3 MHz)	SAFCC915M AL0N00 (915 MHz)		low-loss SAW filter from Murata or equivalent part
XTAL	SMD 5x3.2	17.60000 MHz ±20ppm cal., ±30ppm temp.	24.206667 MHz	24.169444 MHz	25.46667 MHz		fundamental-mode crystal

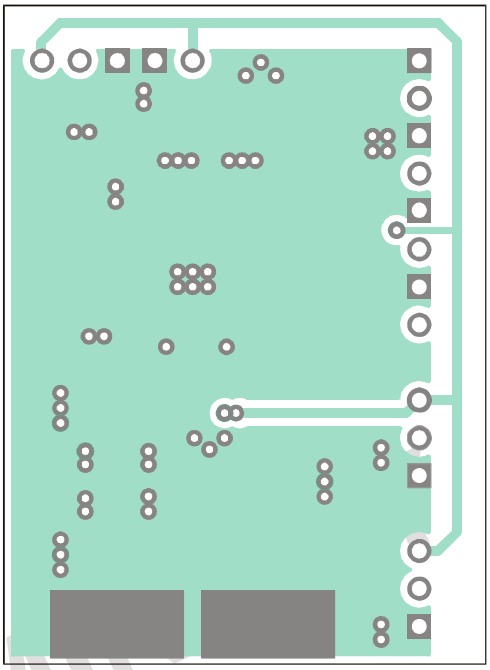
Note: NIP – not in place, may be used optionally

3.4 PCB Layouts for Antenna Space Diversity

- Board layout data in Gerber format is available, board size is 32.4mm x 44.5mm.



PCB top view



PCB bottom view

4 Board Variants

Type	Frequency/MHz	Modulation		Board Execution	
EVB71121	**–315**	**–FSK**	according to section 3.1 / 3.2	**–A**	antenna version
	–433	**–ASK**	according to section 3.1 / 3.2	**–C**	connector version
	–868	**–FM**			
	–915				

Note: **available EVB setups**

5 Package Description

The device MLX71121 is RoHS compliant.

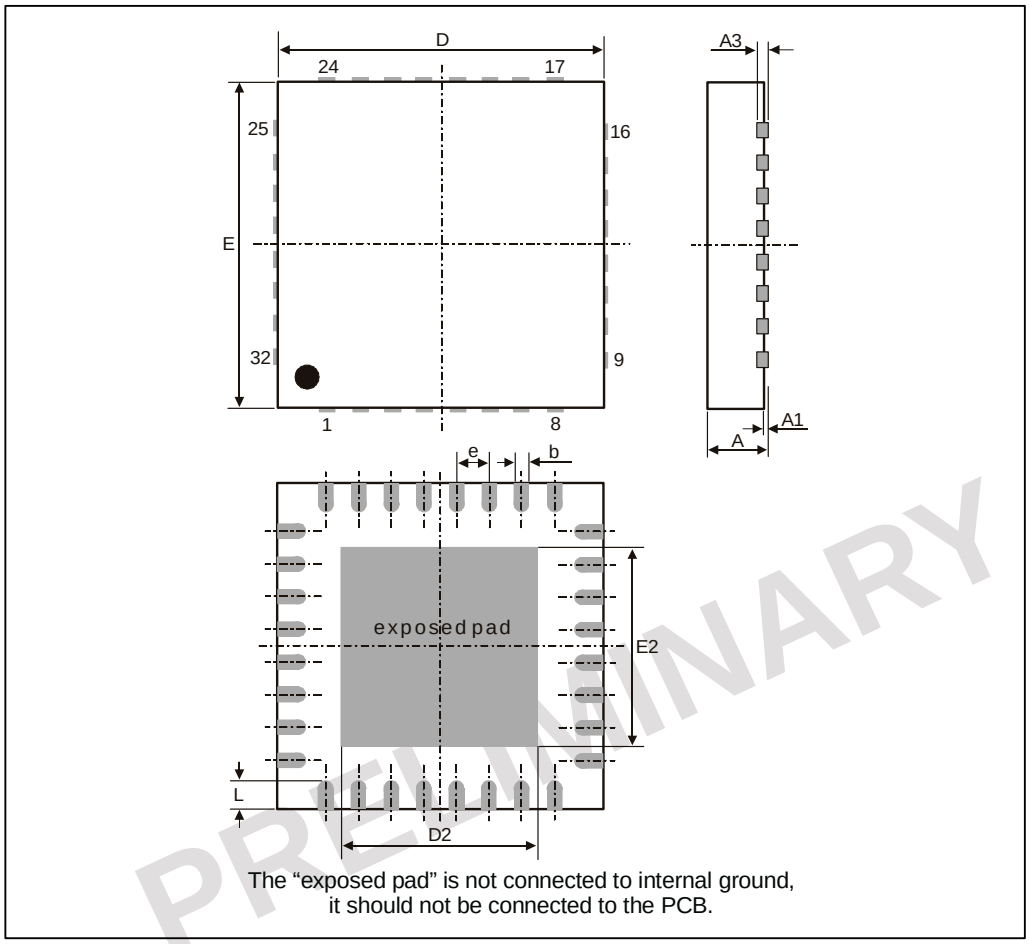


Fig 5: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

5.1 Soldering Information

- The device MLX71121 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

6 Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)"
- EIA/JEDEC JESD22-A113
  "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)"

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  "Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat"
- EIA/JEDEC JESD22-B106 and EN60749-15
  "Resistance to soldering temperature for through-hole mounted devices"

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  "Resistance to soldering temperature for through-hole mounted devices"

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  "Solderability"

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualification of **RoHS** compliant products (RoHS = European directive on the Restriction Of the Use of Certain Hazardous Substances) please visit the quality page on our website:

http://www.melexis.com/quality_leadfree.aspx

7 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

Your Notes

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