

## Features

- Supply Voltage up to 40 V
- $R_{DSon}$  Typically 0.5  $\Omega$  at 25°C, Maximum 1.1  $\Omega$  at 150°C
- Up to 1.5 A Output Current
- Three Half-bridge Outputs Formed by Three High-side and Three Low-side Drivers
- Capable to Switch all Kinds of Loads Such as DC Motors, Bulbs, Resistors, Capacitors and Inductors
- No Shoot-through Current
- Very Low Quiescent Current  $I_S < 5 \mu A$  in Standby Mode versus Total Temperature Range
- Outputs Short-circuit Protected
- Overtemperature Protection for Each Switch and Overtemperature Prewarning
- Undervoltage Protection
- Various Diagnostic Functions Such as Shorted Output, Open-load, Overtemperature and Power-supply Fail Detection
- Serial Data Interface, Daisy Chain Capable, up to 2 MHz Clock Frequency
- SO14 Power Package



## 1. Description

The T6818/ATA6828 are fully protected driver interfaces designed in 0.8- $\mu m$  BCD-MOS technology. They are used to control up to 3 different loads by a microcontroller in automotive and industrial applications.

Each of the 3 high-side and 3 low-side drivers is capable to drive currents up to 1.5 A. The drivers are internally connected to form 3 half-bridges and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the application of H-bridges to drive DC motors.

Protection is guaranteed regarding short-circuit conditions, overtemperature and undervoltage. Various diagnostic functions and a very low quiescent current in stand-by-mode opens a wide range of applications. Automotive qualification (protection against conducted interferences, EMC protection and 2-kV ESD protection) gives added value and enhanced quality for exacting requirements of automotive applications.



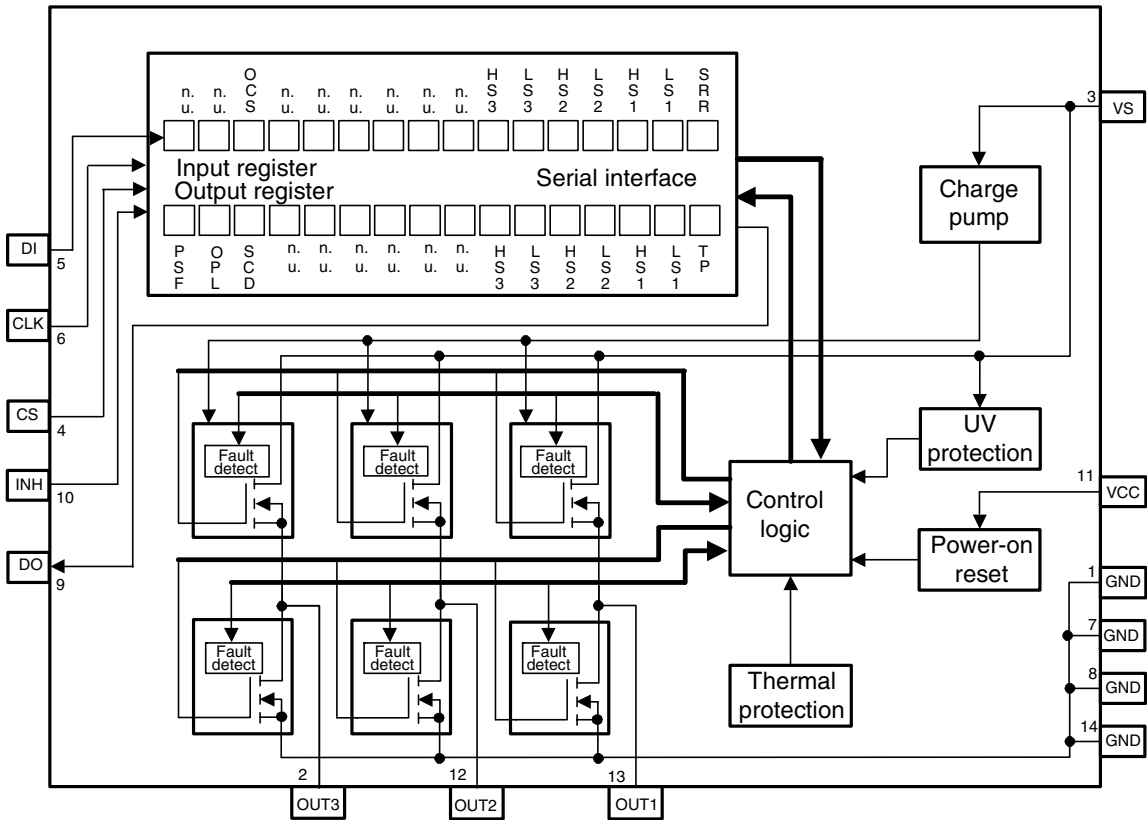
## Triple Half-bridge DMOS Output Driver with Serial Input Control

### T6818/ATA6828

Rev. 4530G-BCD-09/05



Figure 1-1. Block Diagram



## 2. Pin Configuration

Figure 2-1. Pining SO14/PSO14

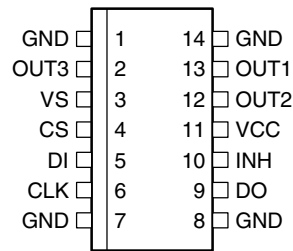


Table 2-1. Pin Description

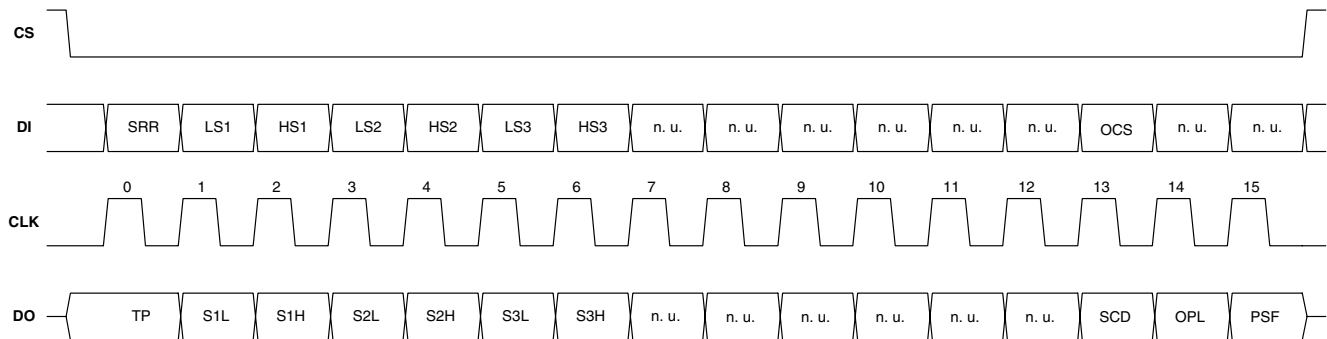
Pin	Symbol	Function
1	GND	T6818: ground; reference potential; internal connection to pin 7, 8 and 14; cooling tab ATA6828: additional connection to heat slug
2	OUT3	Half-bridge output 3; formed by internally connected power MOS high-side switch 3 and low-side switch 3 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load
3	VS	Power supply for output stages OUT1, OUT2 and OUT3, internal supply
4	CS	Chip select input; 5-V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
5	DI	Serial data input; 5-V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
6	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register ( $f_{max} = 2$ MHz)
7	GND	Ground; see pin 1
8	GND	Ground; see pin 1
9	DO	Serial data output; 5-V CMOS logic level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first); output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only.
10	INH	Inhibit input; 5-V logic input with internal pull down; low = standby, high = normal operation
11	VCC	Logic supply voltage (5 V)
12	OUT2	Half-bridge output 2; see pin 2
13	OUT1	Half-bridge output 1; see pin 2
14	GND	Ground; see pin 1

### 3. Functional Description

#### 3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

**Figure 3-1.** Data Transfer



**Table 3-1.** Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, OPL and SCD in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
14	n. u.	Not used
15	n. u.	Not used

**Table 3-2.** Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning
1	Status LS1	High = output is on, low = output is off; not affected by SRR
2	Status HS1	High = output is on, low = output is off; not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	SCD	Short circuit detected: set high when at least one high-side or low-side switch is switched off by a short-circuit condition. Bits 1 to 6 can be used to detect the shorted switch.
14	OPL	Open load detected: set high, when at least one active high-side or low-side switch sinks/sources a current below the open load threshold current.
15	PSF	Power-supply fail: undervoltage at pin VS detected

After power-on reset, the input register has the following status:

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
x	x	H	x	x	x	x	x	x	L	L	L	L	L	L	L

The following patterns are used to enable internal test modes of the IC. It is not recommended to use these patterns during normal operation.

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	H	H	L	L	L	L	L	L	L

### 3.2 Power-supply Fail

In case of undervoltage at pin VS, the Power-Supply Fail bit (PSF) in the output register is set and all outputs are disabled. To detect an undervoltage, its duration has to last longer than the undervoltage detection delay time  $t_{dUV}$ . The outputs are enabled immediately when supply voltage recovers normal operation value. The PSF bit stays high until it is reset by the SRR bit in the input register.

### 3.3 Open-load Detection

If the current through a high-side or low-side switch in ON-state stays below the open-load detection threshold, the open-load detection bit (OPL) in the output register is set.

The OPL bit stays high until it is reset by the SRR bit in the input register. To detect an open load, its duration has to last longer than the open-load detection delay time  $t_{dSd}$ .

### 3.4 Overtemperature Protection

If the junction temperature of one or more output stages exceeds the thermal prewarning threshold,  $T_{jPW\ set}$ , the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold,  $T_{jPW\ reset}$ , the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word. The status of TP is available at pin DO with the falling edge of CS. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the status of input and output registers.

If the junction temperature of one or more output stages exceeds the thermal shutdown threshold,  $T_{j\ switch\ off}$ , all outputs are disabled and the corresponding bits in the output register are set to low. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold,  $T_{j\ switch\ on}$  and the SRR bit in the input register is set to high. Hysteresis of thermal prewarning and shutdown threshold avoids oscillations.

### 3.5 Short-circuit Protection

The output currents are limited by a current regulator. Overcurrent detection is activated by writing a high to the OCS bit in the input register. When the current in an output stage exceeds the overcurrent limitation and shutdown threshold, it is switched off after a delay time ( $t_{dSd}$ ). The short-circuit detection bit (SCD) is set and the corresponding status bit in the output register is set to low. For OCS = low the overcurrent shutdown is inactive. The SCD bit is also set if the current exceeds the overcurrent limitation and shutdown threshold, but the outputs are not affected. By writing a high to the SRR bit in the input register the SCD bit is reset and the disabled outputs are enabled.

### 3.6 Inhibit

0 V applied to pin 10 (INH) inhibits the T6818/ATA6828.

All output switches are then turned off and switched to tri-state. The data in the output register are deleted. The current consumption is reduced to less than 5  $\mu$ A at pin VS and less than 25  $\mu$ A at pin VCC. The output switches can be activated again by switching pin 10 (INH) to 5 V which initiates an internal power-on reset.

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

Parameters	Pin	Symbol	Value	Unit
Supply voltage	3	$V_{VS}$	-0.3 to +40	V
Supply voltage $t < 0.5$ s; $I_S > -2$ A	3	$V_{VS}$	-1	V
Logic supply voltage	11	$V_{VCC}$	-0.3 to +7	V
Logic input voltage	4 to 6, 10	$V_{CS}, V_{DI}, V_{CLK}, V_{INH}$	-0.3 to $V_{VCC}+0.3$	V
Logic output voltage	9	$V_{DO}$	-0.3 to $V_{VCC}+0.3$	V
Input current	4 to 6, 10	$I_{CS}, I_{DI}, I_{CLK}, I_{INH}$	-10 to +10	mA
Output current	9	$I_{DO}$	-10 to +10	mA
Output current	2, 12 and 13	$I_{Out3}, I_{Out2}, I_{Out1}$	Internally limited, see output specification	
Output voltage	2, 12 and 13	$I_{Out3}, I_{Out2}, I_{Out1}$	-0.3 to +40	V
Reverse conducting current ( $t_{pulse} = 150$ $\mu$ s)	2, 12 and 13 towards pin 3	$I_{Out3}, I_{Out2}, I_{Out1}$	17	A
Junction temperature range		$T_J$	-40 to +150	°C
Storage temperature range		$T_{STG}$	-55 to +150	°C

## 5. Thermal Resistance

Parameters	Test Conditions	Symbol	Value	Unit
T6818				
Junction pin	Measured to GND Pins 1, 7, 8 and 14	$R_{thJP}$	30	K/W
Junction ambient		$R_{thJA}$	65	K/W
ATA6828				
Junction pin	Measured to heat slug GND pins 1, 7, 8 and 14	$R_{thJP}$	5	K/W
Junction ambient		$R_{thJA}$	30	K/W

## 6. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	$V_{VS}$	$V_{UV}^{(1)}$ to 40	V
Logic supply voltage	$V_{VCC}$	4.75 to 5.25	V
Logic input voltage	$V_{CS}, V_{DI}, V_{CLK}, V_{INH}$	-0.3 to $V_{VCC}$	V
Serial interface clock frequency	$f_{CLK}$	2	MHz
Junction temperature range	$T_j$	-40 to +150	°C

Note: 1. Threshold for undervoltage detection

## 7. Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4 <sup>(1)</sup>
Interference suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model)	ESD S 5.1	2 kV
ESD (Machine Model)	JEDEC A115A	200 V

Note: 1. Test pulse 5:  $V_{smax} = 40$  V

## 8. Electrical Characteristics

7.5 V <  $V_{VS}$  < 40 V; 4.75 V <  $V_{VCC}$  < 5.25 V; INH = High;  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$ ; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>1</b>	<b>Current Consumption</b>								
1.1	Quiescent current VS	$V_{VS} < 20$ V, INH = low	3	$I_{VS}$		1	5	$\mu\text{A}$	A
1.2	Quiescent current VCC	4.75 V < $V_{VCC} < 5.25$ V, INH = low	11	$I_{VCC}$		15	25	$\mu\text{A}$	A
1.3	Supply current VS	$V_{VS} < 20$ V normal operating, all outputs off	3	$I_{VS}$		4	6	mA	A
1.4	Supply current VCC	4.75 V < $V_{VCC} < 5.25$ V, normal operating	11	$I_{VCC}$		350	500	$\mu\text{A}$	A
1.5	Discharge current VS	$V_{VS} = 32.5$ V, INH = low	3	$I_{VS}$	0.5		5.5	mA	A
1.6	Discharge current VS	$V_{VS} = 40$ V, INH = low	3	$I_{VS}$	2.5		10	mA	A
<b>2</b>	<b>Undervoltage Detection, Power-on Reset</b>								
2.1	Power-on reset threshold		11	$V_{VCC}$	3.2	3.9	4.4	V	A
2.2	Power-on reset delay time	After switching on $V_{CC}$		$t_{dPor}$	30	95	190	$\mu\text{s}$	A
2.3	Undervoltage-detection threshold	$V_{CC} = 5$ V	3	$V_{UV}$	5.6		7.0	V	A
2.4	Undervoltage-detection hysteresis	$V_{CC} = 5$ V	3	$\Delta V_{UV}$		0.6		V	A
2.5	Undervoltage-detection delay time			$t_{dUV}$	10		40	$\mu\text{s}$	A
<b>3</b>	<b>Thermal Prewarning and Shutdown</b>								
3.1	Thermal prewarning set			$T_{jPW\ set}$	120	145	170	$^{\circ}\text{C}$	B
3.2	Thermal prewarning reset			$T_{jPW\ reset}$	105	130	155	$^{\circ}\text{C}$	B
3.3	Thermal prewarning hysteresis			$\Delta T_{jPW}$		15		$^{\circ}\text{C}$	B
3.4	Thermal shutdown off			$T_{j\ switch\ off}$	150	175	200	$^{\circ}\text{C}$	B
3.5	Thermal shutdown on			$T_{j\ switch\ on}$	135	160	185	$^{\circ}\text{C}$	B

\* ) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for  $t > 1$  ms



## 8. Electrical Characteristics (Continued)

7.5 V < V<sub>VS</sub> < 40 V; 4.75 V < V<sub>VCC</sub> < 5.25 V; INH = High; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.6	Thermal shutdown hysteresis			$\Delta T_{j \text{ switch off}}$		15		°C	B
3.7	Ratio thermal shutdown off/thermal prewarning set			$\frac{T_{j \text{ switch off}}}{T_{jPW \text{ set}}}$	1.05	1.2			B
3.8	Ratio thermal shutdown on/thermal prewarning reset			$\frac{T_{j \text{ switch on}}}{T_{jPW \text{ reset}}}$	1.05	1.2			B
<b>4</b>	<b>Output Specification (OUT1-OUT3)</b>								
4.1	On resistance	I <sub>Out 1-3</sub> = -1.3 A	2, 12, 13	R <sub>DSON1-3</sub>			1.1	Ω	A
4.2		I <sub>Out 1-3</sub> = 1.3 A	2, 12, 13	R <sub>DSON1-3</sub>			1.1	Ω	A
4.3	High-side output leakage current	V <sub>Out 1-3</sub> = 0 V, output stages off	2, 12, 13	I <sub>Out1-3</sub>	-15			μA	A
4.4	Low-side output leakage current	V <sub>Out 1-3</sub> = V <sub>VS</sub> , output stages off	2, 12, 13	I <sub>Out1-3</sub>			200	μA	A
4.5	High-side switch reverse diode forward voltage	I <sub>Out 1-3</sub> = 1.5 A	2, 12, 13	V <sub>Out1-3</sub> - V <sub>VS</sub>			1.5	V	A
4.6	Low-side switch reverse diode forward voltage	I <sub>Out 1-3</sub> = -1.5 A	2, 12, 13	V <sub>Out 1-3</sub>	-1.5			V	A
4.7	High-side overcurrent limitation and shutdown threshold		2, 12, 13	I <sub>Out1-3</sub>	-2.5	-2	-1.5	A	A
4.8	Low-side overcurrent limitation and shutdown threshold		2, 12, 13	I <sub>Out1-3</sub>	1.5	2	2.5	A	A
4.9	Overcurrent shutdown delay time			t <sub>dSd</sub>	10		40	μs	A
4.10	High-side open-load detection threshold		2, 12, 13	I <sub>Out1-3</sub>	-45	-30	-15	mA	A
4.11	Low-side open-load detection threshold		2, 12, 13	I <sub>Out1-3</sub>	15	30	45	mA	A
4.12	Open-load detection delay time			t <sub>dSd</sub>	200		600	μs	A
4.13	High-side output switch on delay <sup>(1)</sup>	V <sub>VS</sub> = 13 V R <sub>Load</sub> = 30 Ω		t <sub>don</sub>			20	μs	A
4.14	Low-side output switch on delay <sup>(1)</sup>	V <sub>VS</sub> = 13 V R <sub>Load</sub> = 30 Ω		t <sub>don</sub>			20	μs	A
4.15	High-side output switch off delay <sup>(1)</sup>	V <sub>VS</sub> = 13 V R <sub>Load</sub> = 30 Ω		t <sub>doff</sub>			20	μs	A

\* ) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for t > 1 ms

## 8. Electrical Characteristics (Continued)

7.5 V < V<sub>VS</sub> < 40 V; 4.75 V < V<sub>VCC</sub> < 5.25 V; INH = High; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.16	Low-side output switch off delay <sup>(1)</sup>	V <sub>VS</sub> = 13 V R <sub>Load</sub> = 30 Ω		t <sub>doff</sub>			3	μs	A
4.17	Dead time between corresponding high- and low-side switches	V <sub>VS</sub> = 13 V R <sub>Load</sub> = 30 Ω		t <sub>don</sub> - t <sub>doff</sub>	1			μs	A
<b>5</b>	<b>Logic Inputs DI, CLK, CS, INH</b>								
5.1	Input voltage low-level threshold		4-6, 10	V <sub>IL</sub>	0.3 × V <sub>VCC</sub>			V	A
5.2	Input voltage high-level threshold		4-6, 10	V <sub>IH</sub>			0.7 × V <sub>VCC</sub>	V	A
5.3	Hysteresis of input voltage		4-6, 10	ΔV <sub>I</sub>	50		700	mV	B
5.4	Pull-down current pin DI, CLK, INH	V <sub>DI</sub> , V <sub>CLK</sub> , V <sub>INH</sub> = V <sub>CC</sub>	5, 6, 10	I <sub>PD</sub>	10		65	μA	A
5.5	Pull-up current Pin CS	V <sub>CS</sub> = 0 V	4	I <sub>PU</sub>	-65		-10	μA	A
<b>6</b>	<b>Serial Interface – Logic Output DO</b>								
6.1	Output-voltage low level	I <sub>DOL</sub> = 2 mA	9	V <sub>DOL</sub>			0.4	V	A
6.2	Output-voltage high level	I <sub>DOL</sub> = -2 mA	9	V <sub>DOH</sub>	V <sub>VCC</sub> - 0.7 V			V	A
6.3	Leakage current (tri-state)	V <sub>CS</sub> = V <sub>CC</sub> 0V < V <sub>DO</sub> < V <sub>VCC</sub>	9	I <sub>DO</sub>	-10		10	μA	A
<b>7</b>	<b>Inhibit Input — Timing</b>								
7.1	Delay time from standby to normal operation			t <sub>dINH</sub>			100	μs	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for t > 1 ms

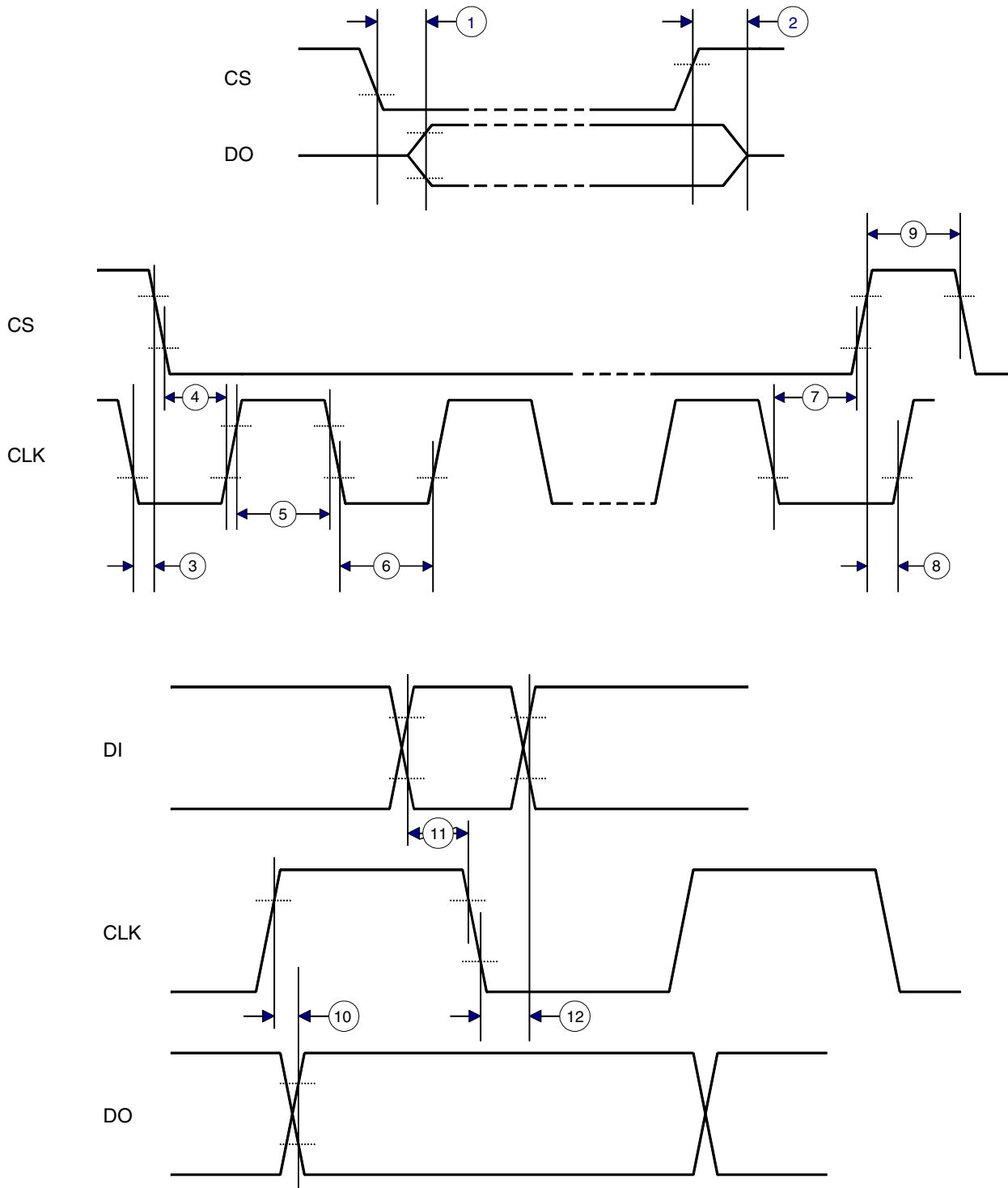
## 9. Serial Interface – Timing

No.	Parameters	Test Conditions	Pin	Timing Chart No. <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit	Type*
8.1	DO enable after CS falling edge	$C_{DO} = 100 \text{ pF}$	9	1	$t_{\text{ENDO}}$			200	ns	D
8.2	DO disable after CS rising edge	$C_{DO} = 100 \text{ pF}$	9	2	$t_{\text{DISDO}}$			200	ns	D
8.3	DO fall time	$C_{DO} = 100 \text{ pF}$	9	–	$t_{\text{DOF}}$			100	ns	D
8.4	DO rise time	$C_{DO} = 100 \text{ pF}$	9	–	$t_{\text{DOR}}$			100	ns	D
8.5	DO valid time	$C_{DO} = 100 \text{ pF}$	9	10	$t_{\text{DOVal}}$			200	ns	D
8.6	CS setup time		4	4	$t_{\text{CSSethl}}$	225			ns	D
8.7	CS setup time		4	8	$t_{\text{CSSethh}}$	225			ns	D
8.8	CS high time		4	9	$t_{\text{CSh}}$	500			ns	D
8.9	CLK high time		6	5	$t_{\text{CLKh}}$	225			ns	D
8.10	CLK low time		6	6	$t_{\text{CLKl}}$	225			ns	D
8.11	CLK period time		6	–	$t_{\text{CLKp}}$	500			ns	D
8.12	CLK setup time		6	7	$t_{\text{CLKsethl}}$	225			ns	D
8.13	CLK setup time		6	3	$t_{\text{CLKsethh}}$	225			ns	D
8.14	DI setup time		5	11	$t_{\text{DIset}}$	40			ns	D
8.15	DI hold time		5	12	$t_{\text{DIHold}}$	40			ns	D

\*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

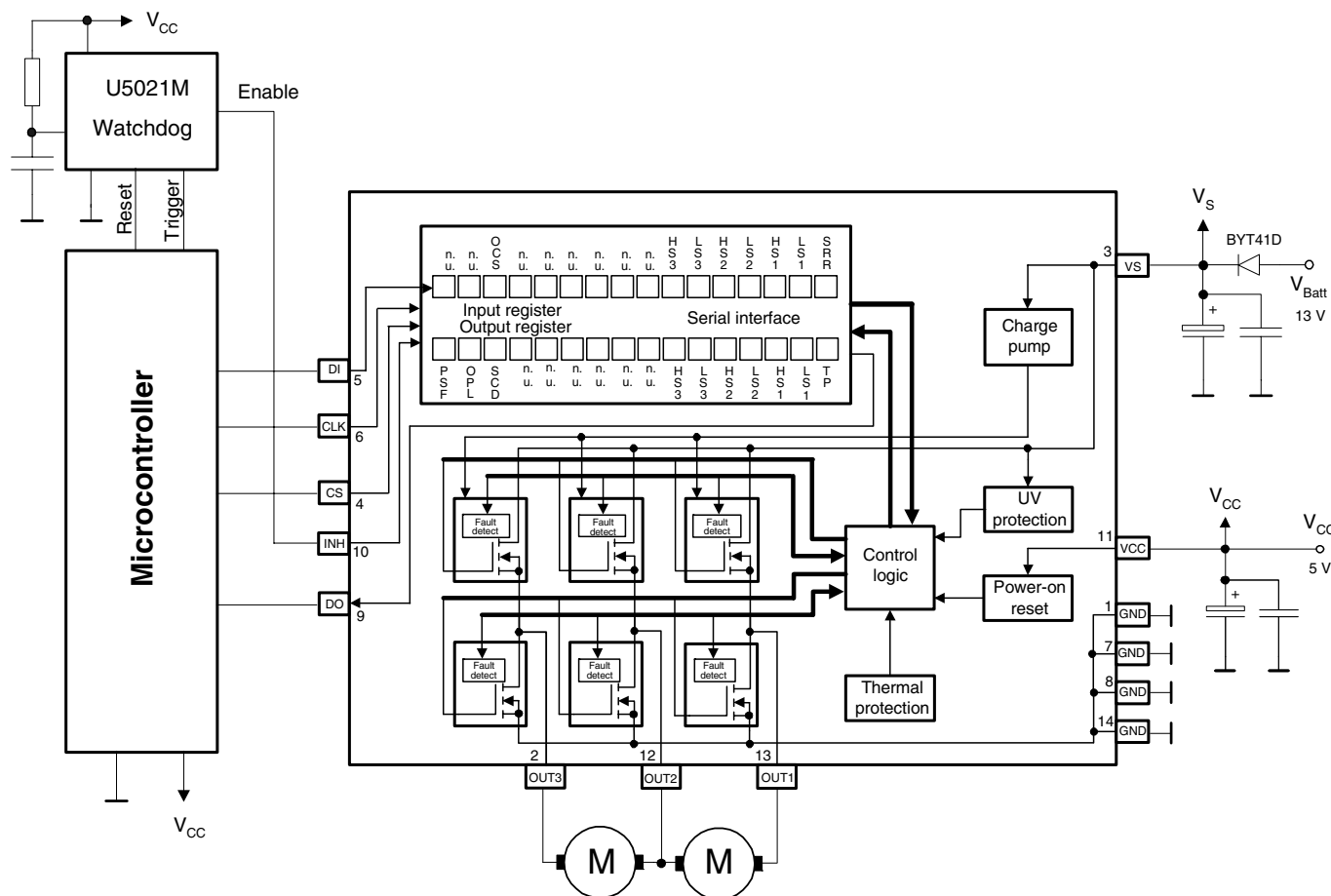
Note: 1. See [Figure 9-1 on page 12](#)

**Figure 9-1.** Serial Interface Timing with Chart Numbers



Inputs DI, CLK, CS: High level =  $0.7 \times V_{CC}$ , low level =  $0.3 \times V_{CC}$   
 Output DO: High level =  $0.8 \times V_{CC}$ , low level =  $0.2 \times V_{CC}$

## 10. Application Circuit



### 10.1 Application Notes

It is strongly recommended to connect the blocking capacitors at  $V_{CC}$  and  $V_S$  as close as possible to the power supply and GND pins.

Recommended value for capacitors at  $V_S$ :

Electrolytic capacitor  $C > 22 \mu\text{F}$  in parallel with a ceramic capacitor  $C = 100 \text{ nF}$ . Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current  $I_{\text{Out}1,2,3}$  (see “[Absolute Maximum Ratings](#)” on page 7).

Recommended value for capacitors at  $V_{CC}$ :

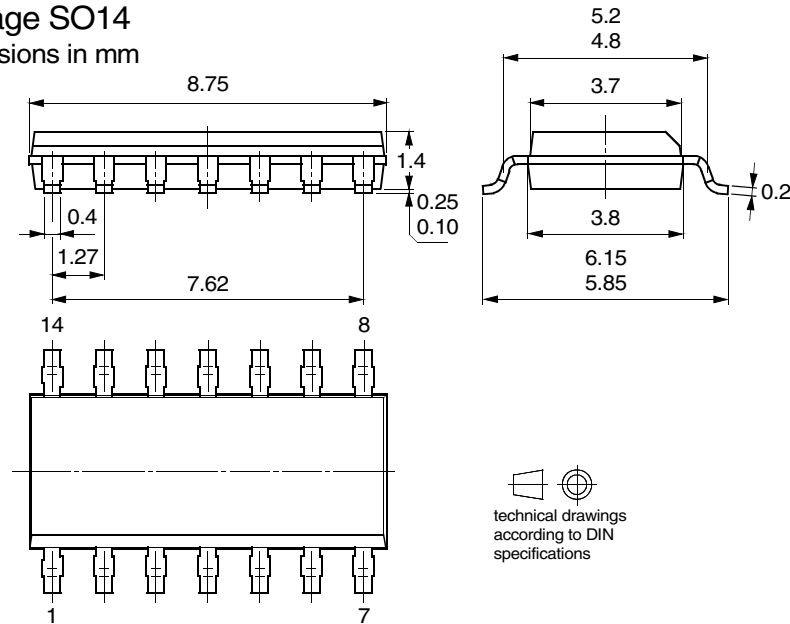
Electrolytic capacitor  $C > 10 \mu\text{F}$  in parallel with a ceramic capacitor  $C = 100 \text{ nF}$ . To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to the GND pins. Negative spikes at the output pins (e.g. negative spikes caused by an inductive load switched off with a high side driver) may activate the overtemperature protection function of the T6818/ATA6828. In this condition, all outputs will be switched off simultaneously. If this behavior is not acceptable or compatible with your application functionally, it is necessary, that for switching on required outputs again, the SRR bit (**S**tatus **R**egister **R**eset) is set, to ensure a reset of the overtemperature function.

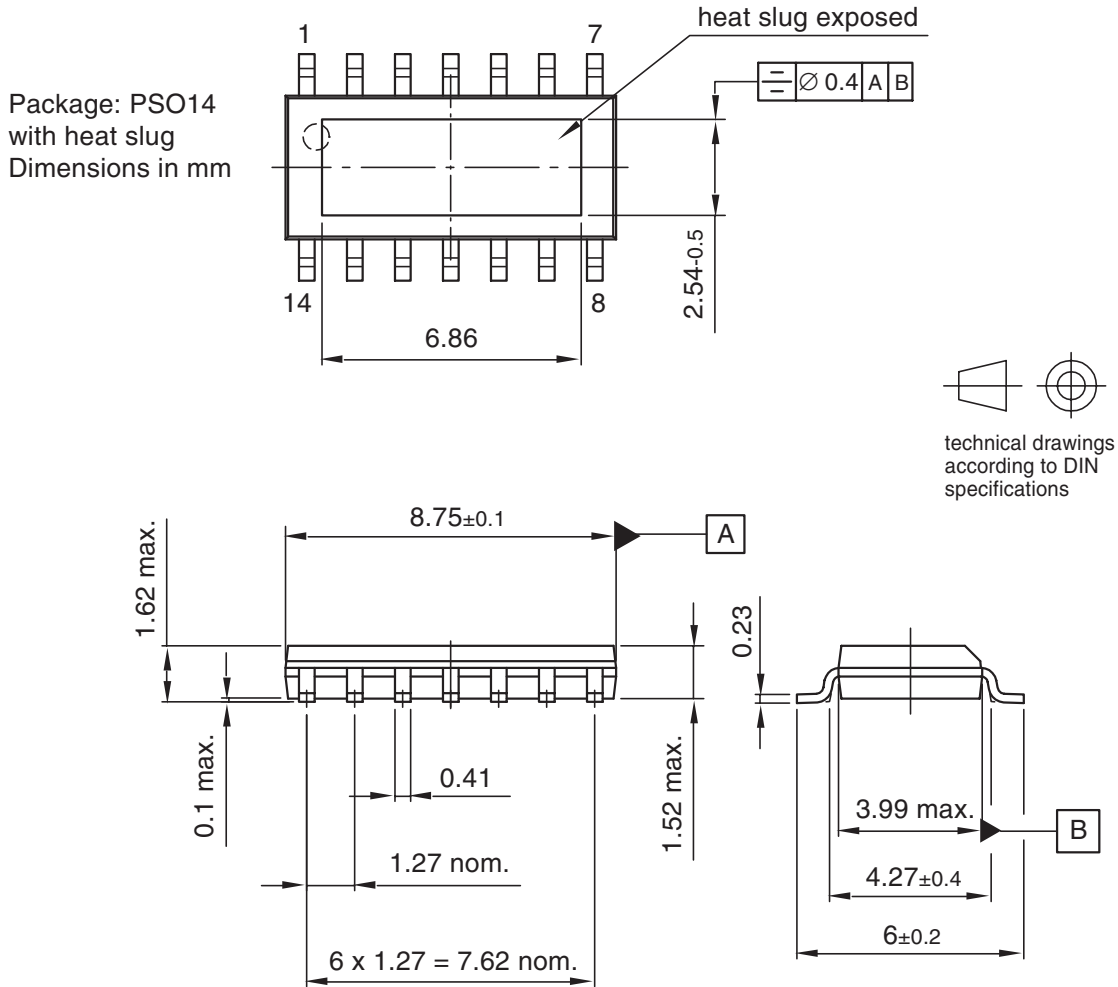
## 11. Ordering Information

Extended Type Number	Package	Remarks
T6818-TUSY	SO14	Power package, tubed, lead-free
T6818-TUQY	SO14	Power package, taped and reeled, lead-free
ATA6828-T2SY	PSO14	Power package with heat slug, tubed, lead-free
ATA6828-T2QY	PSO14	Power package with heat slug, taped and reeled, lead-free

## 12. Package Information

Package SO14  
Dimensions in mm





Drawing-No.: 6.541-5051.01-4

Issue: 2; 18.08.05

### 13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4530G-BCD-09/05	<ul style="list-style-type: none"> <li>Complete datasheet: T6828 changed in ATA6828</li> <li>Ordering Information on page 14 changed</li> <li>Package drawing on page 15 changed</li> </ul>
4530F-BCD-03/05	<ul style="list-style-type: none"> <li>Lead-free Logo on page 1 added</li> <li>Table "Ordering Information" on page 14 changed</li> </ul>
4530E-BCD-07/04	<ul style="list-style-type: none"> <li>Table "Ordering Information" on page 14 changed</li> </ul>
4530D-BCD-04/04	<ul style="list-style-type: none"> <li>Features on page 1 changed</li> </ul>



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenaux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
13106 Rousset Cedex, France  
Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

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BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

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