

FEATURES

- Complete angular rate gyroscope
- Z-axis (yaw rate) response
- SPI digital output interface
- High vibration rejection over wide frequency
- 2000 g-powered shock survivability
- Externally controlled self-test
- Internal temperature sensor output
- Dual auxiliary 12-bit ADC inputs
- Absolute rate output for precision applications
- 5 V single-supply operation
- 8.2 mm × 8.2 mm × 5.2 mm package
- RoHS compliant

APPLICATIONS

- Platform stabilization
- Image stabilization
- Guidance and control
- Inertia measurement units
- Robotics

GENERAL DESCRIPTION

The ADIS16100 is a gyroscope that uses the Analog Devices, Inc. surface-micromachining process to make a functionally complete angular rate sensor with an integrated serial peripheral interface (SPI).

The digital data available at the SPI port is proportional to the angular rate about the axis that is normal to the top surface of the package (see Figure 20). A single external resistor can be used to increase the measurement range. An external capacitor can be used to lower the bandwidth.

Access to an internal temperature sensor measurement is provided through the SPI for compensation techniques. Two pins are available for the user to input analog signals for digitization. An additional output pin provides a precision voltage reference. Two digital self-test inputs electromechanically excite the sensor to test the operation of the sensor and the signal-conditioning circuits.

The ADIS16100 is available in an 8.2 mm × 8.2 mm × 5.2 mm, 16-terminal, peripheral land grid array (LGA) package.

FUNCTIONAL BLOCK DIAGRAM

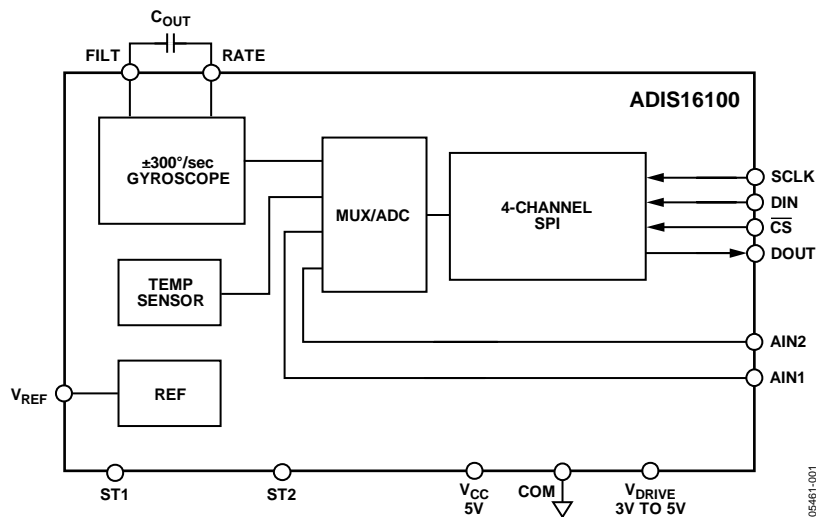


Figure 1.

Rev. B

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REVISION HISTORY

6/07—Rev. A to Rev. B

| | |
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| Changes to Table 1..... | 3 |
| Changes to Table 2..... | 5 |
| Changes to Absolute Maximum Ratings | 6 |
| Changes to Table 4..... | 7 |
| Added Figure 5..... | 7 |
| Changes to Theory of Operation Section..... | 11 |
| Added Basic Operation Section..... | 12 |
| Deleted Second Level Assembly Section | 14 |

5/06—Rev. 0 to Rev. A

| | |
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| Changes to Table 1..... | 4 |
| Changes to Setting Bandwidth Section..... | 11 |
| Changes to Table 9 and Table 10..... | 13 |

1/06—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{CC} = V_{DRIVE} = 5\text{ V}$, angular rate = $0^\circ/\text{sec}$, $C_{OUT} = 0\ \mu\text{F}$, $\pm 1\text{ g}$, unless otherwise noted.

Table 1.

| Parameter | Conditions | Min ¹ | Typ | Max ¹ | Unit |
|-----------------------------------------------|--------------------------------------------------------------------------------------------|------------------------|----------|------------------------|--------------------------------------|
| SENSITIVITY | | | | | |
| Dynamic Range ² | Full-scale range over specifications range | ± 300 | | | $^\circ/\text{sec}$ |
| Initial | Clockwise rotation is positive output, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 0.2212 | 0.2439 | 0.2717 | $^\circ/\text{sec}/\text{LSB}$ |
| Change Over Temperature ³ | $V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to 5.25 V | | ± 5 | | % |
| Nonlinearity | Best fit straight line | | 0.12 | | $^\circ/\text{sec}$ |
| NULL | | | | | |
| Initial | Nominal $0^\circ/\text{sec}$ output is 2048 LSB | -42 | | +37 | $^\circ/\text{sec}$ |
| Change Over Temperature ³ | $V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to 5.25 V | | ± 10 | | $^\circ/\text{sec}$ |
| Turn-On Time | Power on to $\pm 0.5^\circ/\text{sec}$ of final value | | 35 | | ms |
| Linear Acceleration Effect | Any axis | | 0.2 | | $^\circ/\text{sec}/\text{g}$ |
| Voltage Sensitivity | $V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to 5.25 V | | ± 1 | | $^\circ/\text{sec}/\text{V}$ |
| NOISE PERFORMANCE | | | | | |
| Total Noise | 0.1 Hz to 40 Hz; no averaging | | 0.43 | | $^\circ/\text{sec}$ rms |
| Rate Noise Density | @ 25°C | | 0.05 | | $^\circ/\text{sec}/\sqrt{\text{Hz}}$ |
| FREQUENCY RESPONSE | | | | | |
| 3 dB Bandwidth (User-Selectable) ⁴ | $C_{OUT} = 0\ \mu\text{F}$ | | 40 | | Hz |
| Sensor Resonant Frequency | | | 14 | | kHz |
| SELF-TEST INPUTS | | | | | |
| ST1 Rateout Response ⁵ | ST1 pin from Logic 0 to Logic 1 | -121 | -221 | -376 | LSB |
| ST2 Rateout Response ⁵ | ST2 pin from Logic 0 to Logic 1 | +121 | +221 | +376 | LSB |
| Logic 1 Input Voltage | Standard high logic level definition | 3.3 | | | V |
| Logic 0 Input Voltage | Standard low logic level definition | | | 1.7 | V |
| Input Impedance | To common | | 50 | | k Ω |
| TEMPERATURE SENSOR | | | | | |
| Reading at 298 K | | | 2048 | | LSB |
| Scale Factor | Proportional to absolute temperature | | 0.1453 | | K/LSB |
| 2.5 V REFERENCE | | | | | |
| Voltage Value | | 2.45 | 2.5 | 2.55 | V |
| Load Drive to Ground | Source | | 100 | | μA |
| Load Regulation | $0\ \mu\text{A} < I_{OUT} < 100\ \mu\text{A}$ | | 5.0 | | mV/mA |
| Power Supply Rejection | $V_{CC} = V_{DRIVE} = 4.75\text{ V}$ to 5.25 V | | 1.0 | | mV/V |
| Temperature Drift | Delta from 25°C | | 5.0 | | mV |
| LOGIC INPUTS | | | | | |
| Input High Voltage, V_{INH} | | $0.7 \times V_{DRIVE}$ | | | V |
| Input Low Voltage, V_{INL} | | | | $0.3 \times V_{DRIVE}$ | V |
| Input Current, I_{IN} | Typically 10 nA | -1 | | +1 | μA |
| Input Capacitance, C_{IN} | | | 10 | | pF |
| ANALOG INPUTS | | | | | |
| Resolution | For $V_{IN} < V_{CC}$ | | 12 | | Bits |
| Integral Nonlinearity | | -2 | | +2 | LSB |
| Differential Nonlinearity | | -2 | | +2 | LSB |
| Offset Error | | -8 | | +8 | LSB |
| Gain Error | | -2 | | +2 | LSB |
| Input Voltage Range | | 0 | | $V_{REF} \times 2$ | V |
| Leakage Current | | -1 | | +1 | μA |
| Input Capacitance | | | 20 | | pF |
| Full Power Bandwidth | | | 8 | | MHz |

ADIS16100

| Parameter | Conditions | Min ¹ | Typ | Max ¹ | Unit |
|---------------------------------------------|-------------------------------------------------------------------------|--------------------------|-----|------------------|------|
| DIGITAL OUTPUTS | | | | | |
| Output High Voltage (V _{OH}) | I _{SOURCE} = 200 μA | V _{DRIVE} - 0.2 | | | V |
| Output Low Voltage (V _{OL}) | I _{SINK} = 200 μA | | | 0.4 | V |
| CONVERSION RATE | | | | | |
| Conversion Time | 16 SCLK cycles with SCLK at 20 MHz | | | 800 | ns |
| Throughput Rate | | | | 1 | MSPS |
| POWER SUPPLY | All at T _A = -40°C to +85°C | | | | |
| V _{CC} | | 4.75 | 5 | 5.25 | V |
| V _{DRIVE} | | 2.7 | | 5.25 | V |
| V _{CC} Quiescent Supply Current | V _{CC} = 5 V, f _{SCLK} = 50 kSPS | | 7.0 | 9.0 | mA |
| V _{DRIVE} Quiescent Supply Current | V _{DRIVE} = 5 V, f _{SCLK} = 50 kSPS | | 70 | 500 | μA |
| Power Dissipation | V _{CC} = V _{DRIVE} = 5 V, f _{SCLK} = 50 kSPS | | 40 | | mW |
| TEMPERATURE RANGE | | | | | |
| Specified Performance | Tested to max and min specifications | -40 | | +85 | °C |

¹ All minimum and maximum specifications are guaranteed. Typical specifications are neither tested nor guaranteed.

² Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 5 V supplies.

³ Defined as the output change from ambient to maximum temperature, or ambient to minimum temperature.

⁴ Frequency at which the response is 3 dB down from dc response. Bandwidth = $1/(2 \times \pi \times 180 \text{ k}\Omega \times (22 \text{ nF} + C_{\text{OUT}}))$. For C_{OUT} = 0, bandwidth = 40 Hz. For C_{OUT} = 1 μF, bandwidth = 0.87 Hz.

⁵ Self-test response varies with temperature.

TIMING SPECIFICATIONS

$T_A = 25^\circ\text{C}$, angular rate = $0^\circ/\text{sec}$, unless otherwise noted.¹

Table 2.

| Parameter | $V_{CC} = V_{DRIVE} = 5\text{ V}$ | Unit | Description |
|---------------|-----------------------------------|--------------------|-----------------------------------------------------------------------------------------------|
| f_{SCLK}^2 | 10 20 | kHz min MHz max | |
| $t_{CONVERT}$ | $16 \times t_{SCLK}$ | | |
| t_{QUIET} | 50 | ns min | Minimum quiet time required between \overline{CS} rising edge and start of next conversion. |
| t_2 | 10 | ns min | \overline{CS} to SCLK setup time. |
| t_3^3 | 30 | ns max | Delay from \overline{CS} until DOUT three-state disabled. |
| t_4^3 | 40 | ns max | Data access time after SCLK falling edge. |
| t_5 | $0.4 \times t_{SCLK}$ | ns min | SCLK low pulse width. |
| t_6 | $0.4 \times t_{SCLK}$ | ns min | SCLK high pulse width. |
| t_7 | 10 | ns min | SCLK to DOUT valid hold time. |
| t_8^4 | 15/35 | ns min/max | SCLK falling edge to DOUT high impedance. |
| t_9 | 10 | ns min | DIN setup time prior to SCLK falling edge. |
| t_{10} | 5 | ns min | DIN hold time after SCLK falling edge. |
| t_{11} | 20 | ns min | 16 th SCLK falling edge to \overline{CS} high. |

¹ Guaranteed by design. All input signals are specified with t_r and $t_f = 5\text{ ns}$ (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

² Mark/space ratio for the SCLK input is 40/60 to 60/40.

³ Measured with the load circuit in Figure 3 and defined as the time required for the output to cross 0.4 V, or $0.7 \times V_{DRIVE}$.

⁴ t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8 , quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

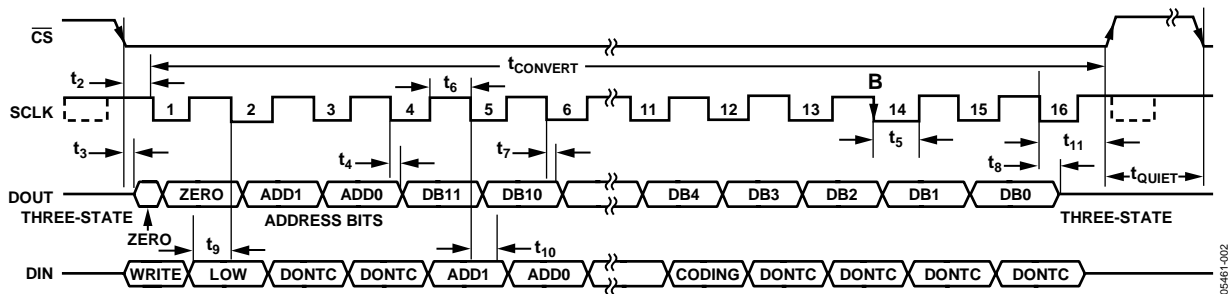


Figure 2. Gyroscope Serial Interface Timing Diagram

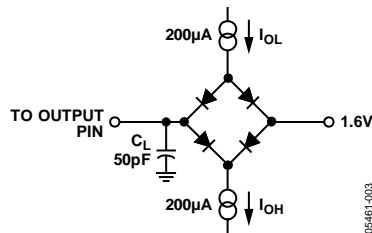


Figure 3. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--------------------------------------------|-----------------------------------|
| Acceleration (Any Axis, Unpowered, 0.5 ms) | 2000 <i>g</i> |
| Acceleration (Any Axis, Powered, 0.5 ms) | 2000 <i>g</i> |
| V _{CC} to COM | -0.3 V to +6.0 V |
| V _{DRIVE} to COM | -0.3 V to V _{CC} + 0.3 V |
| Analog Input Voltage to COM | -0.3 V to V _{CC} + 0.3 V |
| Digital Input Voltage to COM | -0.3 V to +7.0 V |
| Digital Output Voltage to COM | -0.3 V to V _{CC} + 0.3 V |
| ST1/ST2 Input Voltage to COM | -0.3 V to V _{CC} + 0.3 V |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

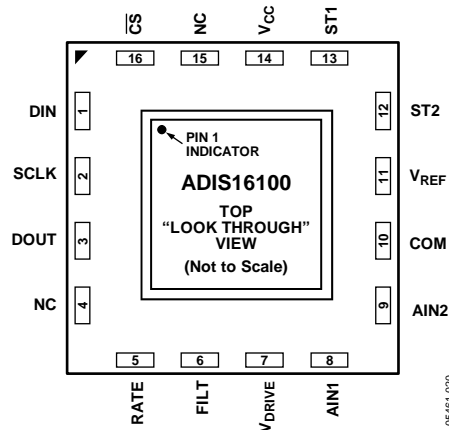
Drops onto hard surfaces can cause shocks of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised in handling to avoid damage.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. NC = NO CONNECT
 2. THIS IS NOT AN ACTUAL "TOP VIEW," AS THE PINS ARE NOT VISIBLE FROM THE TOP. THIS IS A LAYOUT VIEW, WHICH REPRESENTS THE PIN CONFIGURATION, IF THE PACKAGE IS LOOKED THROUGH FROM THE TOP. THIS CONFIGURATION IS PROVIDED FOR PCB LAYOUT PURPOSES.

Figure 4. Pin Configuration, Top Look-Through View

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|--------------------|-------------------|-----------------------------------------------------------------------------------------------------------|
| 1 | DIN | I | SPI Data Input. |
| 2 | SCLK | I | SPI Serial Clock. |
| 3 | DOUT | O | SPI Data Output. |
| 4 | NC | | No Connect. |
| 5 | RATE | O | Buffered Analog Output. Represents the angular rate signal. |
| 6 | FILT | I | External Capacitor Connection to Control Bandwidth. |
| 7 | V _{DRIVE} | S | SPI Power Supply. This can be the receive processing circuit's supply to simplify interfacing. |
| 8 | AIN1 | I | External Analog Input Channel 1. See ADD0 and ADD1 address bits in Table 5. |
| 9 | AIN2 | I | External Analog Input Channel 2. See ADD0 and ADD1 address bits in Table 5. |
| 10 | COM | S | Common. Reference point for all circuitry in the ADIS16100. |
| 11 | V _{REF} | O | Precision 2.5 V Reference. |
| 12 | ST2 | I | Self-Test Input 2. |
| 13 | ST1 | I | Self-Test Input 1. |
| 14 | V _{CC} | S | Analog Power. |
| 15 | NC | | No Connect. |
| 16 | \overline{CS} | I | Chip Select. Active low. This input frames the serial data transfer and initiates the conversion process. |

¹ I = input; O = output; S = power supply.

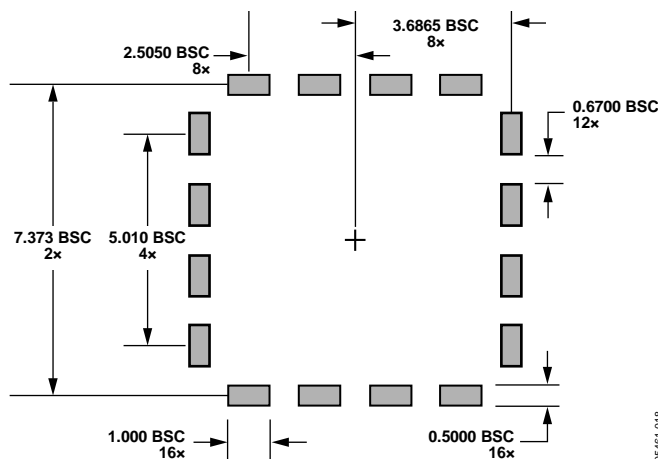


Figure 5. Second-Level Assembly Pad Layout

TYPICAL PERFORMANCE CHARACTERISTICS

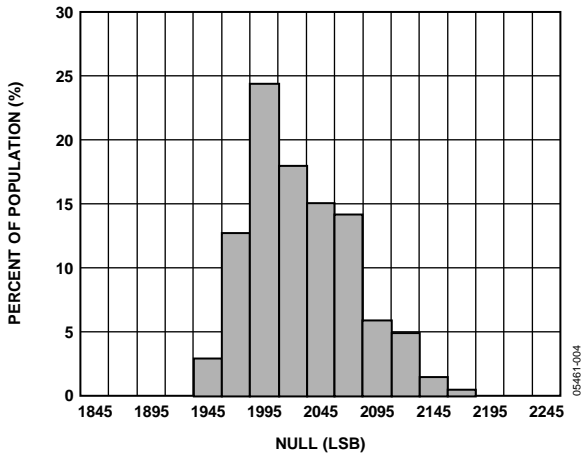


Figure 6. Initial Null Histogram

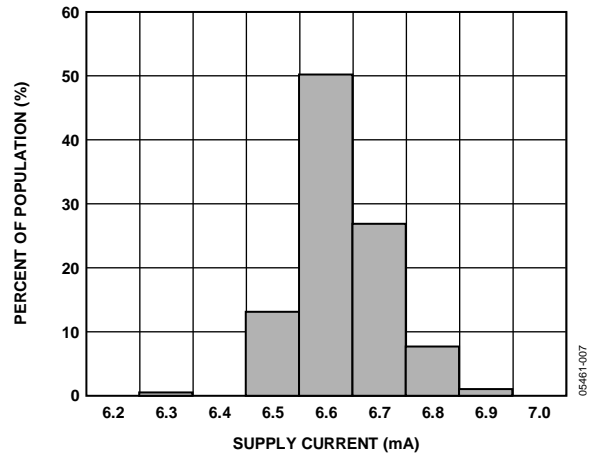


Figure 9. Supply Current Histogram

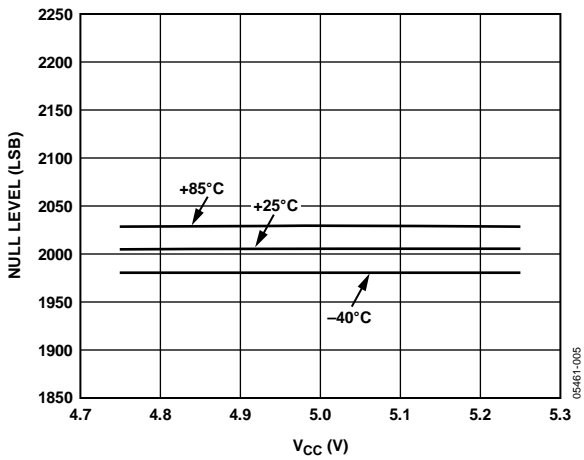


Figure 7. Null Level vs. Supply Voltage

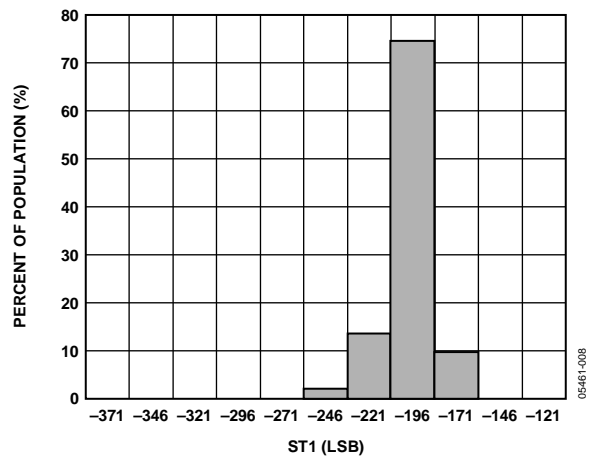


Figure 10. Self-Test 1 Histogram

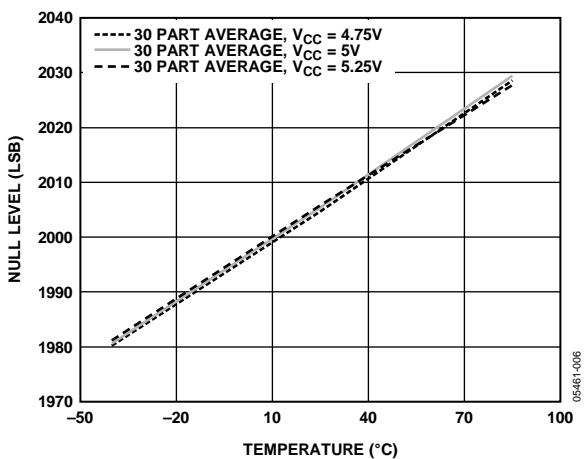


Figure 8. Null Level vs. Temperature

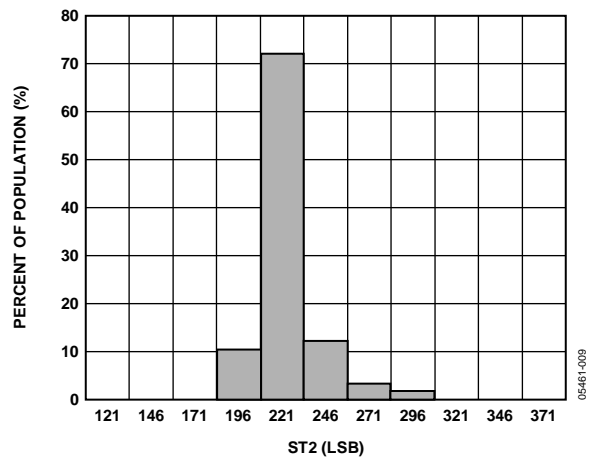


Figure 11. Self-Test 2 Histogram

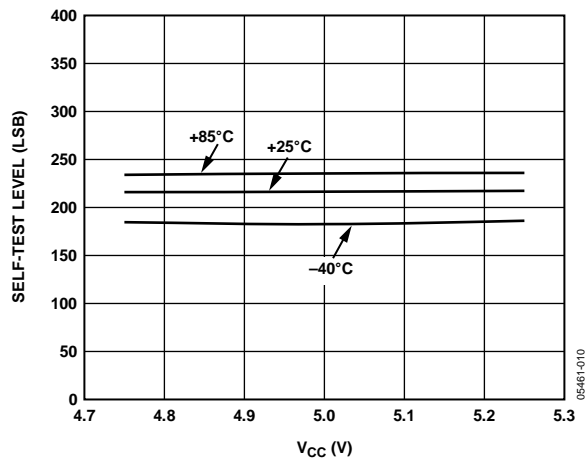


Figure 12. Self-Test 1 vs. Supply Voltage

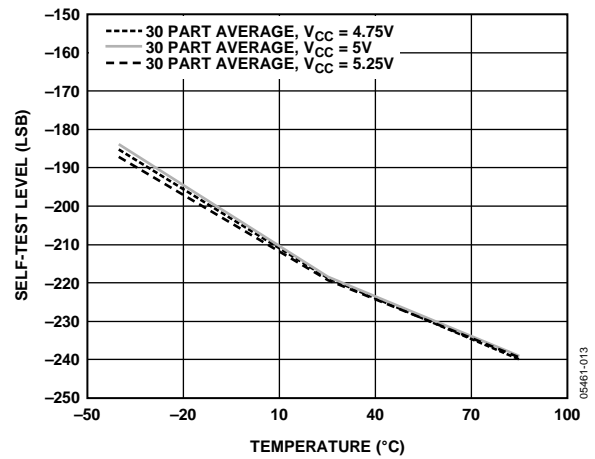


Figure 15. Self-Test 2 vs. Temperature

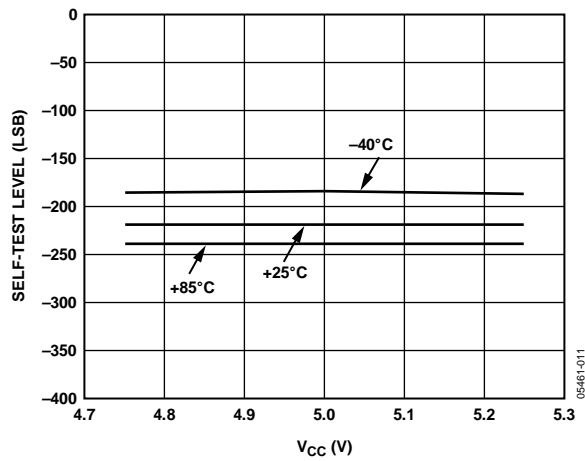


Figure 13. Self-Test 2 vs. Supply Voltage

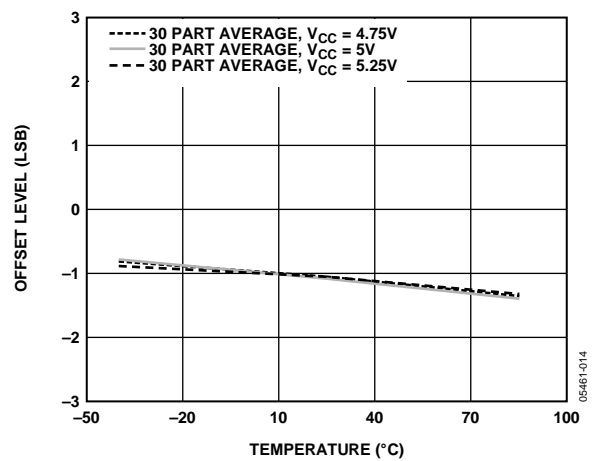


Figure 16. ADC Offset vs. Temperature and Supply Voltage

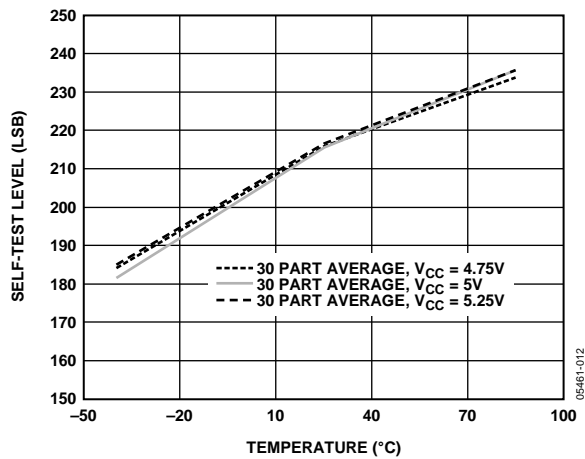


Figure 14. Self-Test 1 vs. Temperature

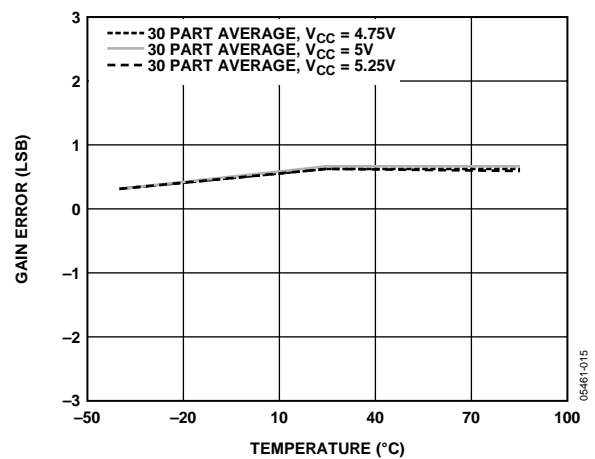


Figure 17. ADC Gain Error vs. Temperature (Excluding V_{REF})

ADIS16100

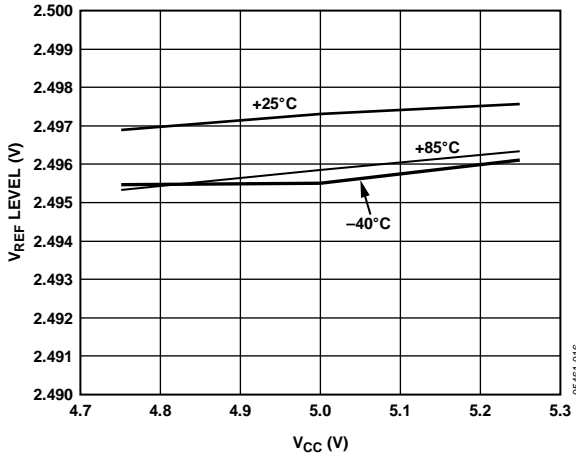


Figure 18. V_{REF} vs. Supply Voltage

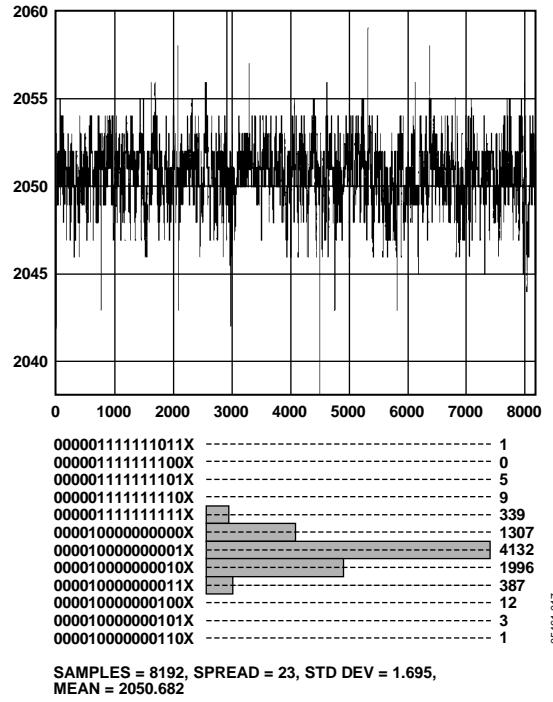


Figure 19. Noise Histogram

THEORY OF OPERATION

The ADIS16100 operates on the principle of a resonator gyroscope. Two polysilicon sensing structures each contain a dither frame that is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force while rotating. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers that are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The rate signal is then converted to a digital representation of the output on the SPI pins. The dual-sensor design rejects external g forces and vibration. Fabricating the sensor with the signal conditioning electronics preserves signal integrity in noisy environments.

The electrostatic resonator requires 14 V to 16 V for operation. Because only 5 V is typically available in most applications, a charge pump is included on-chip. After the demodulation stage, there is a single-pole, low-pass filter included on-chip that is used to limit high frequency artifacts before final amplification. The frequency response is dominated by the second low-pass filter, which is set at 40 Hz. For additional bandwidth reduction options, see the Setting Bandwidth section.

SUPPLY AND COMMON CONSIDERATIONS

Power supply noise and transient behaviors can influence the accuracy and stability of any sensor-based measurement system. When considering the power supply for the ADIS16100, it is important to understand that the ADIS16100 provides 0.2 μF of decoupling capacitance on the V_{CC} pin. Depending on the level of noise present in the system power supply, the ADIS16100 may not require any additional decoupling capacitance for this supply. The analog supply, V_{CC} , and the digital drive supply, V_{DRIVE} , are segmented to allow multiple logic levels to be used in receiving the digital output data. V_{DRIVE} is intended for the downstream logic power supply and supports standard 3.3 V and 5 V logic families. The V_{DRIVE} supply does not have internal decoupling capacitors.

INCREASING MEASUREMENT RANGE

The full-scale measurement range of the ADIS16100 is increased by placing an external resistor between the RATE pin and FILT pin, which results in a parallel connection with the internal 180 k Ω , 1% resistor. For example, a 330 k Ω external resistor gives ~50% increase in the full-scale range. This is effective for up to a 4 \times increase in the full-scale range (minimum value of the parallel resistor allowed is 45 k Ω). The internal circuitry headroom requirements prevent further increase in the linear full-scale output range. The trade-offs associated with increasing the full-scale range are potential increase in output null drift (as much as 2 $^\circ$ /sec over temperature) and introducing initial null bias errors that must be calibrated.

SETTING BANDWIDTH

An external capacitor can be used in combination with an on-chip resistor to create a low-pass filter to limit the bandwidth of the ADIS16100 rate response.

The -3 dB frequency is defined as

$$f_{\text{OUT}} = 1 / (2 \times \pi \times R_{\text{OUT}} \times (C_{\text{OUT}} + 0.022 \mu\text{F}))$$

where:

R_{OUT} is the internal impedance that was trimmed during manufacturing to 180 k $\Omega \pm 1\%$.

C_{OUT} is the external capacitance across the RATE and FILT pins.

Any external resistor applied between the RATE pin and the FILT pin results in

$$R_{\text{OUT}} = (180 \text{ k}\Omega \times R_{\text{EXT}}) / (180 \text{ k}\Omega + R_{\text{EXT}})$$

where R_{EXT} is the external resistor.

With $C_{\text{OUT}} = 0 \mu\text{F}$, a default -3 dB frequency response of 40 Hz is obtained based upon an internal 0.022 μF capacitor implemented on-chip.

SELF-TEST FUNCTION

The ADIS16100 includes a self-test feature that actuates each of the sensing structures and associated electronics in the same manner as if subjected to an angular rate. It provides a simple method for exercising the mechanical structure of the sensor, along with the entire signal processing circuit. It is activated by standard logic high levels applied to Input ST1, Input ST2, or both. ST1 causes a change in the digital output equivalent to typically -220 LSB, and ST2 causes an opposite +220 LSB change. The self-test response follows the viscosity temperature dependence of the package atmosphere, approximately 0.25%/ $^\circ\text{C}$. Activating both ST1 and ST2 simultaneously is not damaging. Because ST1 and ST2 are not necessarily closely matched, actuating both simultaneously can result in an apparent null bias shift.

Continuous Self-Test

As an additional failure detection measure, a power-on self-test can be performed. However, some applications warrant a continuous self-test while sensing rate.

RATE SENSITIVE AXIS

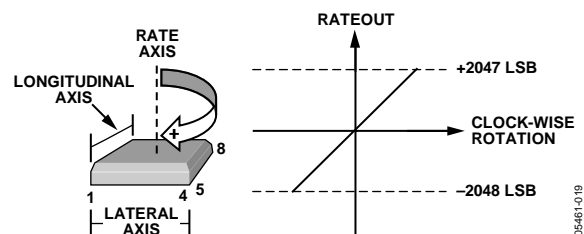


Figure 20. Rate Signal Increases with Clockwise Rotation

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BASIC OPERATION

The ADIS16100 is designed for simple integration into industrial system designs, requiring only a 5.0 V power supply and a 4-wire, industry standard serial peripheral interface (SPI). The SPI handles all digital I/O communication in the ADIS16100.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16100 SPI port includes four signals: chip select (\overline{CS}), serial clock (SCLK), data input (DIN), and data output (DOUT). The \overline{CS} line enables the ADIS16100 SPI port and frames each SPI event. When this signal is high, the DOUT lines are in a high impedance state and the signals on DIN and SCLK have no impact on operation. A complete data frame contains 16 clock cycles. Because the SPI port operates in full duplex mode, it supports simultaneous, 16-bit receive (DIN) and transmit (DOUT) functions within the same data frame.

Control Register

The DIN control register provides controls for two operational settings: the output data source and the coding (twos complement vs. offset binary). Table 5 and Figure 22 provide the proper bit definitions for control register configuration. The DIN sequence starts with a 1 for configuration sequences and a 0 for read sequences. When this bit is 0, the remaining DIN bits do not change the control register and the next sample's output data reflects the existing configuration. Data loads from the DIN pin into the ADIS16100 on the falling edge of SCLK. Once the 16-SCLK sequence is complete, the control register is updated and ready for the next read sequence. If a data frame has less than 16 SCLK cycles, the control register does not update and maintains its previous configuration. The DIN bit definitions in Table 5, which have either 0 or 1 assigned to them, are critical for proper operation.

ADC Conversion

The chip select (\overline{CS}) and serial clock (SCLK) lines control the on-board analog-to-digital conversion process. When the chip select line goes low, the DOUT line comes out of three-state mode, the track-and-hold goes into hold mode, and the ADC samples the analog input at this point. The track-and-hold returns to track mode on the 14th falling edge of the SCLK line. The serial clock drives the internal ADC conversion clock, using its falling edge for control of this process. All 16 SCLK cycles are required for a complete conversion. If a data frame has less than 16 SCLK cycles, the conversion cannot complete and does not update the output data for the next data frame cycle.

Output Data Access

The DOUT sequence starts with two zeros, one that clocks out after the falling edge of \overline{CS} , and a second one that clocks out on the first SCLK falling edge. The next 14 bits, ADD0, ADD1 and the 12 data bits, clock out on SCLK falling edges. After the 16th falling edge, the DOUT line moves to a three-state mode.

When setting up the system process to receive data from the ADIS16100, use a clock phase setting of 0 and a clock polarity setting of 1. These settings reflect the timing displayed in Figure 22. To maintain proper communication at the maximum specified clock rates, the system processor must be able to support the setup time requirement, listed in Figure 2 and Table 2 (t_s).

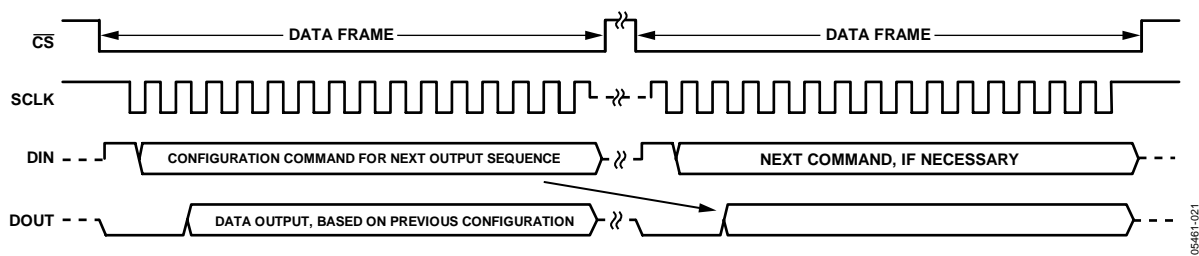


Figure 21. Configuration and Read Sequence

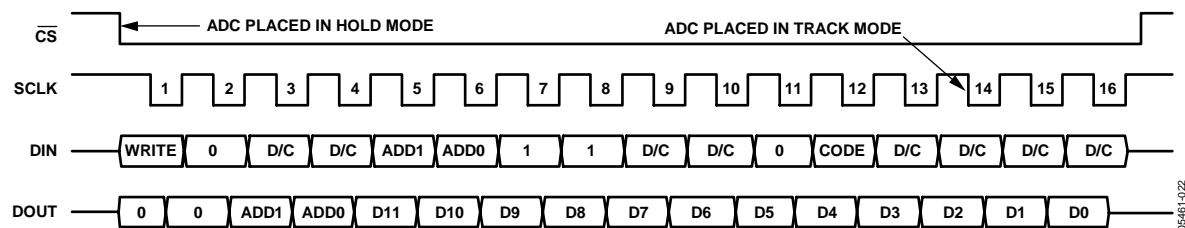


Figure 22. SPI Sequence, Clock Polarity = 1, Clock Phase = 0

Table 5. DIN Bit Assignments

| Bit No. | Mnemonic | Comment |
|---------|------------|------------------------------------------------------------------------------------------------------------------------|
| 15 | WRITE | 1: Write contents on DIN to control register. 0: No changes to control register. |
| 14 | 0 | Low state for normal operation. |
| 13, 12 | D/C | Don't care. |
| 11, 10 | ADD1, ADD0 | Data source setting. 00: Gyroscope output. 01: Temperature output. 10: Analog input 1. 11: Analog input 2. |
| 9, 8 | 1 | High state for normal operation. |
| 7, 6 | D/C | Don't care. |
| 5 | 0 | Low state for normal operation. |
| 4 | CODE | Output data format setting. 0: Twos complement. 1: Offset binary. |
| 3 to 0 | D/C | Don't care. |

Output Coding Examples

Table 6. Gyroscope Data Coding, Twos Complement

| Angular Rate (°/sec) | Code | Bit Pattern |
|----------------------|-------|------------------|
| 300 | 1230 | 0000010011001110 |
| ... | ... | ... |
| 0.4878 | 2 | 0000000000000010 |
| 0.2439 | 1 | 0000000000000001 |
| 0 | 0 | 0000000000000000 |
| -0.2439 | -1 | 1111111111111111 |
| -0.4878 | -2 | 1111111111111110 |
| ... | ... | ... |
| -300 | -1230 | 0000101100110010 |

Table 7. Gyroscope Data Coding, Offset Binary

| Angular Rate (°/sec) | Code | Bit Pattern |
|----------------------|------|------------------|
| 300 | 3278 | 0000110011001110 |
| ... | ... | ... |
| 0.4878 | 2050 | 0000100000000010 |
| 0.2439 | 2049 | 0000100000000001 |
| 0 | 2048 | 0000100000000000 |
| -0.2439 | 2047 | 0000111111111111 |
| -0.4878 | 2046 | 0000111111111110 |
| ... | ... | ... |
| -300 | 818 | 0000001100110010 |

Table 8. Temperature Data Coding, Twos Complement

| Temperature (°C) | Code | Bit Pattern |
|------------------|------|------------------|
| 85 | 585 | 0001001001001001 |
| ... | ... | ... |
| 25 + 0.2906 | 2 | 0001000000000010 |
| 25 + 0.1453 | 1 | 0001000000000001 |
| 25 | 0 | 0001000000000000 |
| 25 - 0.1453 | -1 | 0001111111111111 |
| 25 - 0.2906 | -2 | 0001111111111110 |
| ... | ... | ... |
| -40 | -447 | 0001110010000001 |

Table 9. Temperature Data Coding, Offset Binary

| Temperature (°C) | Code | Bit Pattern |
|------------------|------|------------------|
| 85 | 2633 | 0001101001001001 |
| ... | ... | ... |
| 25 + 0.2906 | 2050 | 0001100000000010 |
| 25 + 0.1453 | 2049 | 0001100000000001 |
| 25 | 2048 | 0001100000000000 |
| 25 - 0.1453 | 2047 | 0001111111111111 |
| 25 - 0.2906 | 2046 | 0001111111111110 |
| ... | ... | ... |
| -40 | 1601 | 0001011001000001 |

Table 10. ADC Data Coding, Twos Complement

| Input Level (V) | Code ¹ | Bit Pattern |
|-----------------|-------------------|------------------|
| 2 | 1638 | 0010011001100110 |
| ... | ... | ... |
| 0.002442 | 2 | 0010000000000010 |
| 0.001221 | 1 | 0010000000000001 |
| 0 | 0 | 0010000000000000 |
| -0.001221 | -1 | 0010111111111111 |
| -0.002442 | -2 | 0010111111111110 |
| ... | ... | ... |
| -2 | -1638 | 0010100110011010 |

¹ Code for AIN1 used in 3rd and 4th bits (11 for AIN2).

Table 11. ADC Data Coding, Offset Binary

| Input Level (V) | Code ¹ | Bit Pattern |
|-----------------|-------------------|------------------|
| 2 | 3686 | 0010011001100110 |
| ... | ... | ... |
| 0.002442 | 2050 | 0010100000000010 |
| 0.001221 | 2049 | 0010100000000001 |
| 0 | 2048 | 0010100000000000 |
| -0.001221 | 2047 | 0010111111111111 |
| -0.002442 | 2046 | 0010111111111110 |
| ... | ... | ... |
| -2 | 410 | 0010000110011010 |

¹ Code for AIN1 used in 3rd and 4th bits (11 for AIN2).

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OUTLINE DIMENSIONS

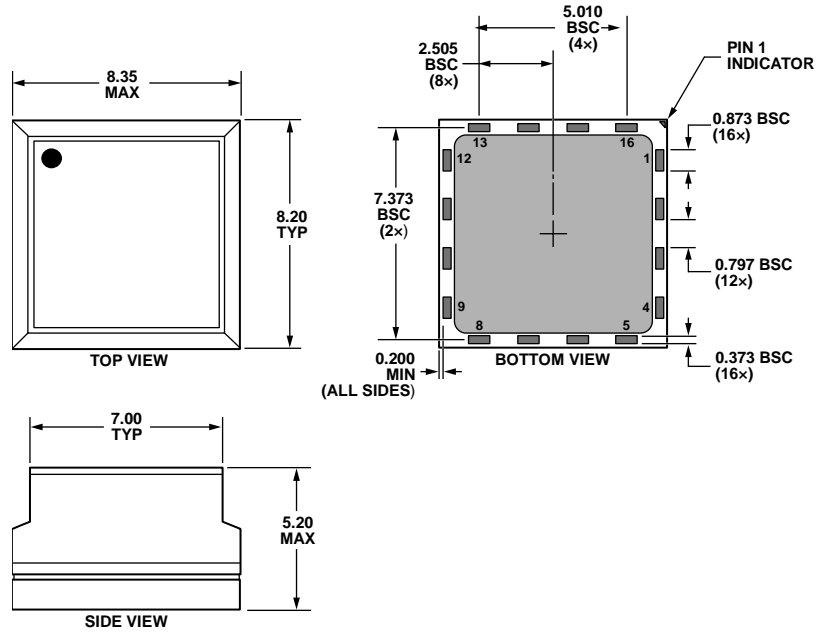


Figure 23. 16-Terminal Stacked Land Grid Array [LGA]
(CC-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|-------------------|-------------------------------------------|----------------|
| ADIS16100ACC | -40°C to +85°C | 16-Terminal Stacked Land Grid Array (LGA) | CC-16-1 |
| ADIS16100/PCB | | Evaluation Board | |

NOTES

ADIS16100

NOTES