HIGH VOLTAGE TFT-LCD LOGIC DRIVER

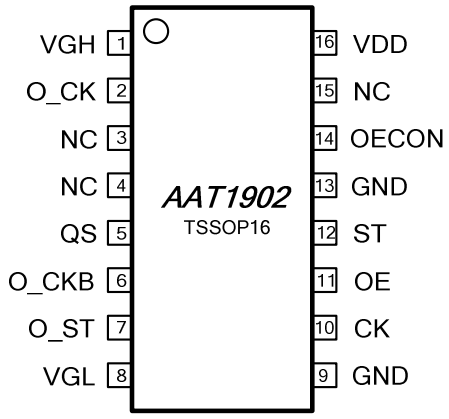
FEATURES

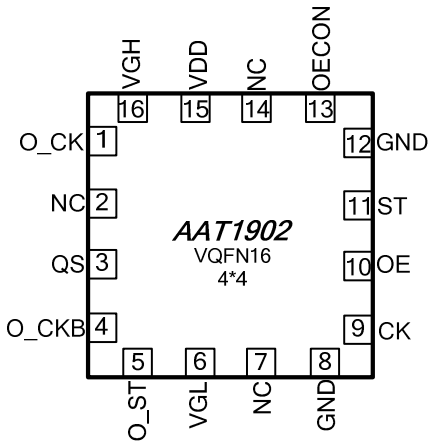
- **3 Channels Level Shift**
- **Charge Sharing Function**
- **3.3V Logic Power Supply Input**
- **40V Output High Level**
- **−20V Output Low Level**
- **TSSOP-16 Package / VQFN16 - 4*4 Package**

GENERAL DESCRIPTION

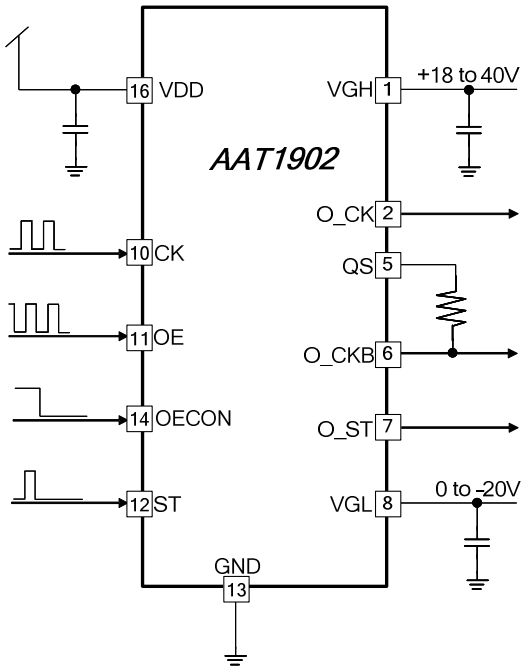
The AAT1902 is a high voltage TFT-LCD logic level shift driver with a wide range output swing capability. The maximum difference between VGH and VGL can be as large as 45V. By using the charge sharing function, AAT1902 consumes less power when the output is switching. With the internal logic control, the AAT1902 can be operated in charge-sharing mode without complicated application design. It is capable of driving a 5nF capacitive load within 1μs rising and falling time respectively.

PIN CONFIGURATION





TYPICAL APPLICATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1902	AAT1902-T1-T	T1: TSSOP16	T: Tape and Reel	−40°C to +85°C	AAT1902 XXXXX	1. Part Name 2. Lot No. (6~9 Digits)
AAT1902	AAT1902-Q11-T	Q11: VQFN16 4*4	T: Tape and Reel	−40°C to +85°C	AAT1902 XXXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VDD	V_{DD}	−0.3 to +7	V
VGH to GND	V_{I1}	40	V
VGL to GND	V_{I2}	−20	V
VGH to VGL	V_{I3}	50	V
Pin Voltage 1 (ST, CK, CKB, OE)	V_{I4}	−0.3 to (V_{DD} +0.3)	V
Pin Voltage 2 (O_ST, O_CK, O_CKB, QS)	V_{I5}	(−0.3+VGL) to (VGH+0.3)	V
Operating Free-Air Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	$T_{STORAGE}$	−45 to +125	°C
Power Dissipation	P_d	1,250	mW

Note: Stresses exceeding ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods of time may compromise device reliability.

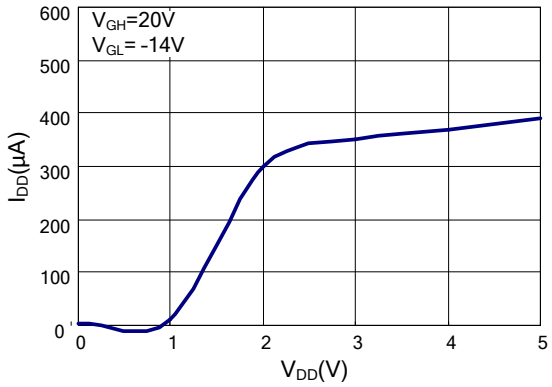
ELECTRICAL CHARACTERISTICS

(T_C = +25°C , V_{DD} = 3.3V, VGH = 25V, VGL = −14V, 5nF Load on O_CK, O_CKB and O_ST, unless otherwise specified.)

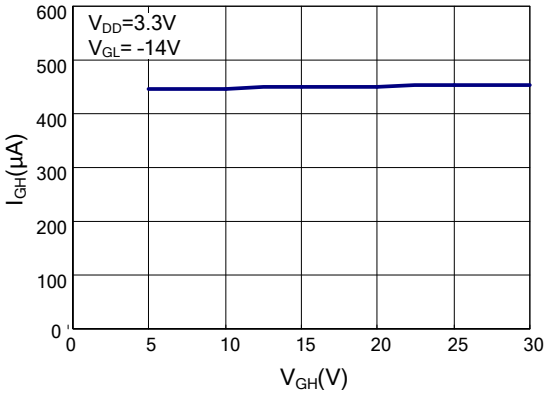
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VGH-VGL Voltage Range	V_{HL}		18	-	45	V
VDD Supply Current	I_{DD}	All Inputs Low	-	0.2	-	mA
		CPV = High, Other Inputs Low	-	0.3	0.6	mA
VGH Supply Current	I_{GH}	All Inputs Low	-	30	-	µA
		CPV = High, Other Inputs Low	-	0.4	0.8	mA
VGL Supply Current	I_{GL}	All Inputs Low	-	0.15	-	mA
		CPV = High, Other Inputs Low	-	0.25	0.50	mA
Input Bias Current (EN, CK, OE, ST)	I_{B1}		-	−0.1	−0.2	µA
EN, CK, OE, ST Input High Level	V_{IH}		-	1.4	1.8	V
EN, CK, OE, ST Input Low Level	V_{IL}		0.4	1.4	-	V
O_CK, O_CKB, O_ST Positive Output Swing	V_{O+}	VGH = 25V, I_O = 10mA	24.6	24.8	-	V
O_CK, O_CKB, O_ST Negative Output Swing	V_{O-}	VGL = −14V, I_O = −10mA	-	−13.8	−13.6	V
O_CK, O_CKB, O_ST Rising Time	T_{R1}	C_L = 5nF	-	0.5	1.0	µs
O_CK, O_CKB, O_ST Falling Time	T_{F1}	C_L = 5nF	-	0.5	1.0	µs
O_CK, O_CKB, O_ST Rising Edge Delay Time	T_{D1}	C_L = 5nF	-	0.5	1.0	µs
O_CK, O_CKB, O_ST Falling Edge Delay Time	T_{D2}	C_L = 5nF	-	0.5	1.0	µs
Charge Sharing MOS Impedance	R_{QS}		-	20	-	Ω

TYPICAL OPERATING CHARACTERISTICS

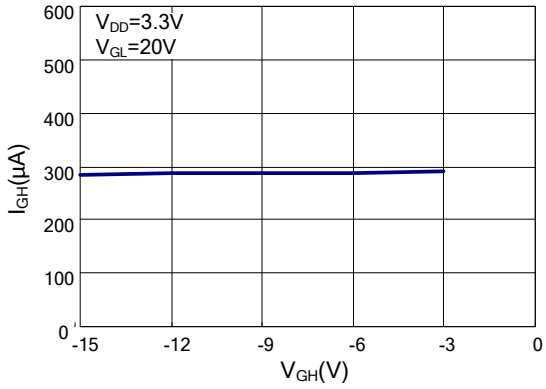
V_{DD} Supply Current vs. V_{DD}



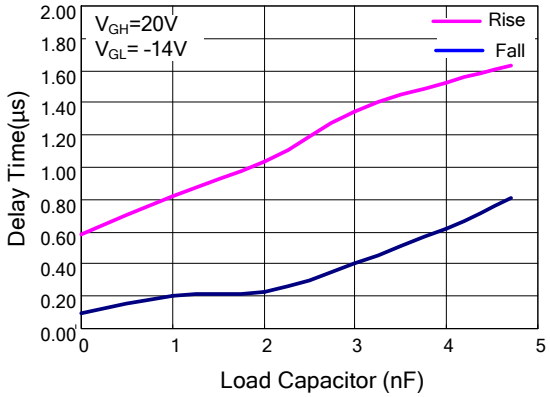
V_{GH} Supply Current vs. I_{GH}



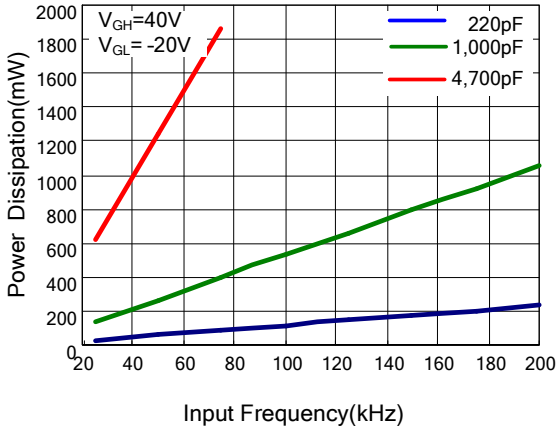
V_{GH} Supply Current vs. I_{GH}



Delay Time vs. Load Capacitor



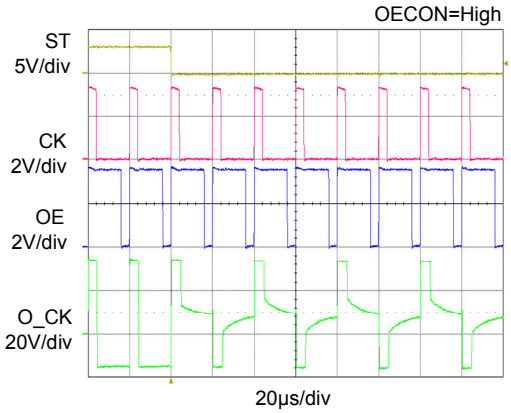
Delay Time vs. Load Capacitor



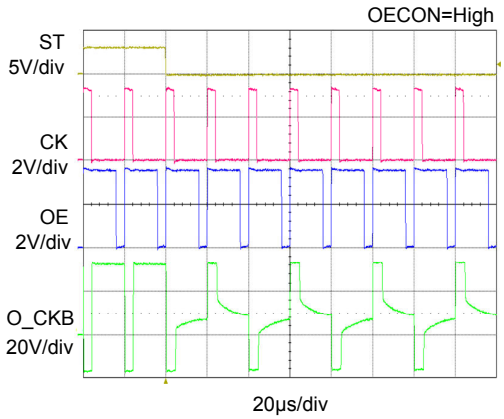
TYPICAL OPERATING CHARACTERISTICS

(TC = 25°C, VDD = 3.3V, VGH = 25V, VGL = −14V, 5nF Load on O_CK, O_CKB and O_ST, unless otherwise specified.)

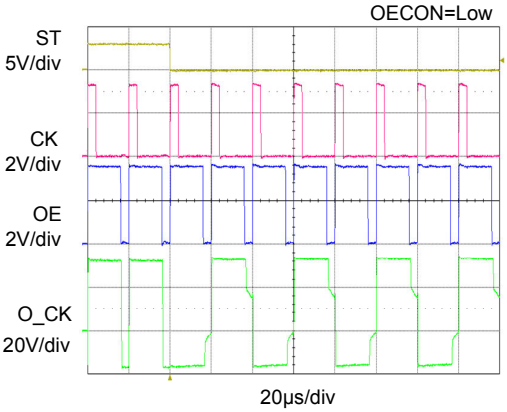
Timing Chart



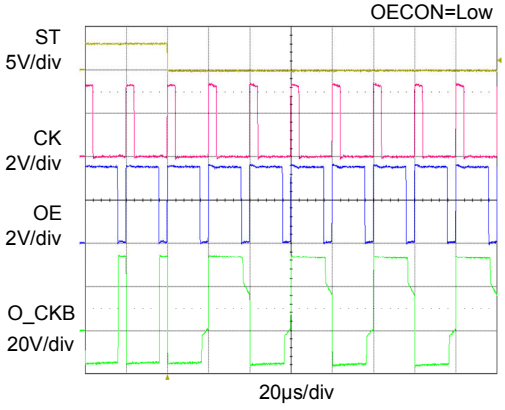
Timing Chart



Timing Chart



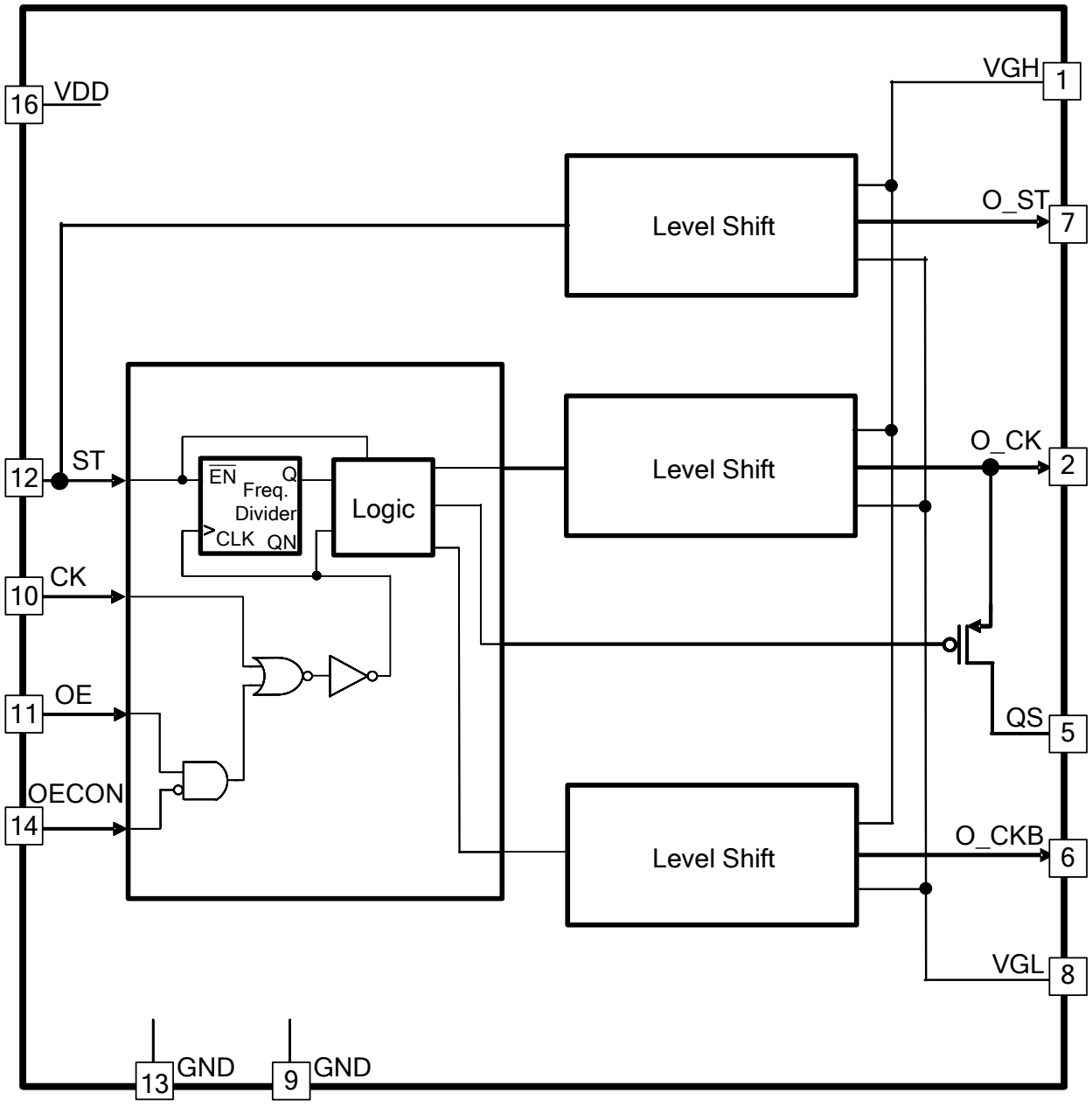
Timing Chart



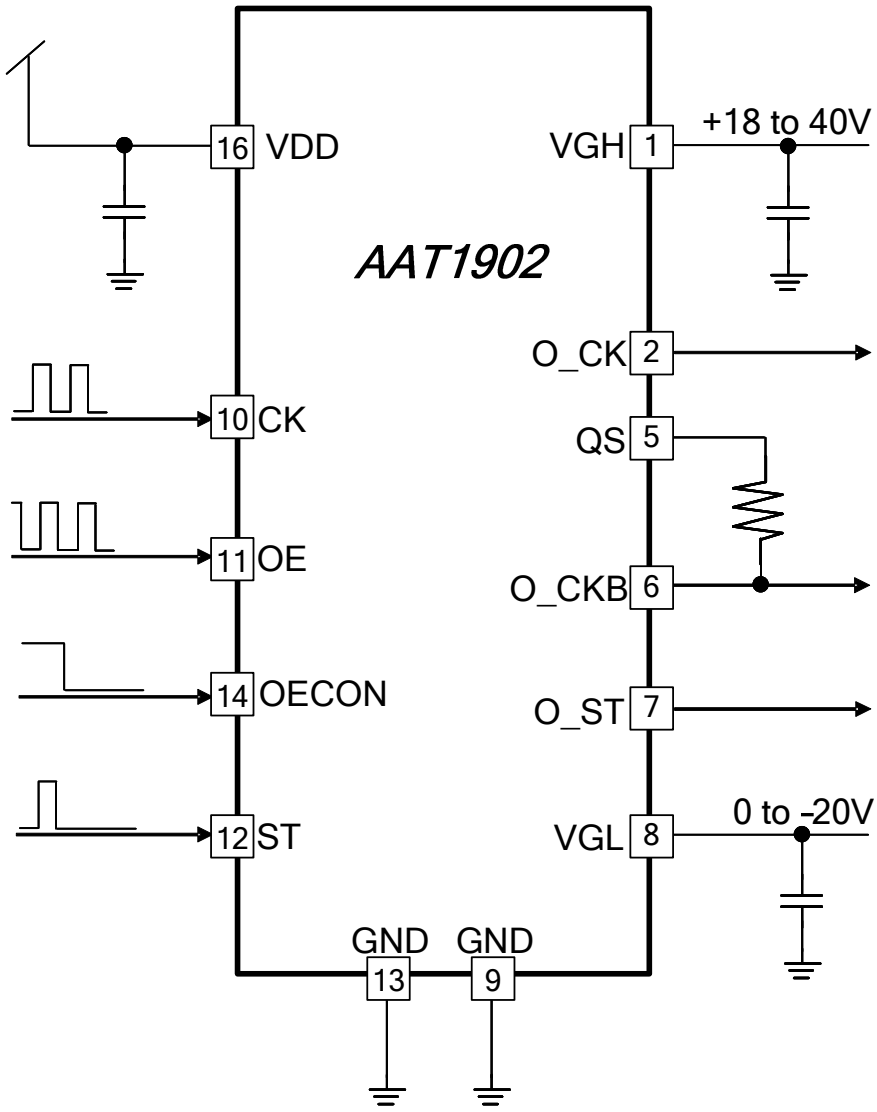
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	VGH	-	Positive Supply
2	O_CK	O	Level Shift High Voltage Output 1
3	NC	-	Not Connected
4	NC	-	Not Connected
5	QS	O	Charge Sharing Pin
6	O_CKB	O	Level Shift High Voltage Output 2
7	O_ST	O	Start Pulse High Voltage Output
8	VGL	-	Negative Supply
9	GND	-	GND
10	CK	I	Horizontal Sync Clock Input 1
11	OE	I	Horizontal Sync Clock Input 2
12	ST	I	Start Pulse Clock Input
13	GND	-	GND
14	OECON	I	Clock Input 2 Disable Pin
15	NC	-	Not Connected
16	VDD	-	Logic Power Supply

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



DETAILED DESCRIPTION

The AAT1902 is a 3 channel TFT-LCD row driver with charge sharing function to lower power dissipation during transition of states. The O_CK and O_CKB are level shifted output signals with level as high as VGH and as low as VGL. The frequency of these output signals is half of the CK input clock signal triggered by CK rising edge. The charge sharing function is enabled whenever ST signal is low. Charge sharing will be performed at the CK signal falling edge when OECON is high; and when OECON=0, it will be performed when both the CK and OE signals are low. The O_ST is simply the level shifted signal of ST. It has no charge sharing function.

DESIGN PROCEDURE

Input Signals

The start pulse signal of the TFT-LCD Panel system is connected to the ST pin of AAT1902. Both CK and OE frequency is adjusted by T-CON; the higher CK and OE frequencies are, the larger power dissipation would be ST-Start Pulse Clock Input signal, frequency range around 60Hz, CK - Horizontal Sync Clock Input signal 1, frequency range up to 166 kHz, OE - Horizontal Sync Clock Input signal 2, frequency range up to 166 kHz

Output Signals

The output signal of AAT1902 includes 3 internal switch sets: O_ST, O_CK, and O_CKB. C_L, the loading capacitor is typically between 1nF and 5nF. The larger C_L gets, the longer delay time would be. The output drop rate of O_CK and O_CKB is determined by the resistance and capacitance of external charge sharing.

Charging Sharing Theory

Charge sharing activates when ST signal is low. Once the charge sharing function is activated, the frequency at the output signal O_CK and O_CKB will automatically be divided by 2. O_CK and O_CKB neutralize charges to produce equal voltage level on two sides via the external resistor on QS when charge sharing initiates. The power dissipation will decrease significantly at this mode.

Power Dissipation

Suppose

V_{DD} = 3.3V

V_{GH} = 25V

V_{GL}= –14V

CK = Horizontal Sync Clock = 60kHz

C_L = 5nF

V_{GH} and V_{GL} balance the voltage level on two sides via charge sharing, so the measured capacitance at QS pin would be around 5.5V as shown in Figure 1.

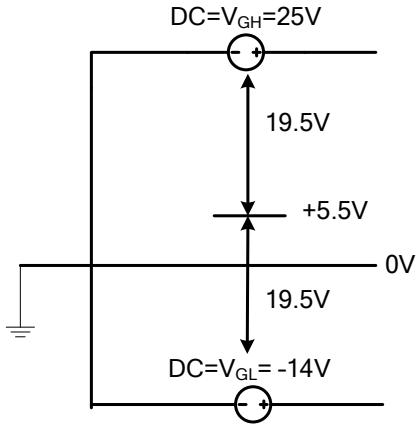


Figure 1.

Conserved power of the capacitance can be calculated following below equation:

$$P_{Cap} = \frac{1}{2} \times V^2 \times C_L = \frac{1}{2} \times (19.5)^2 \times 5 \times 10^{-9} = 0.95\mu W$$

Power loss of the resistor is shown in Figure 2. When the input signal of CK is 60kHz, and the output signal of O_CK and O_CKB is within 60kHz, the power consumption can be calculated as below:

$P_d = 2xP_{CAP}xCK = 2x0.95\mu Wx60x10^3 = 114mW$

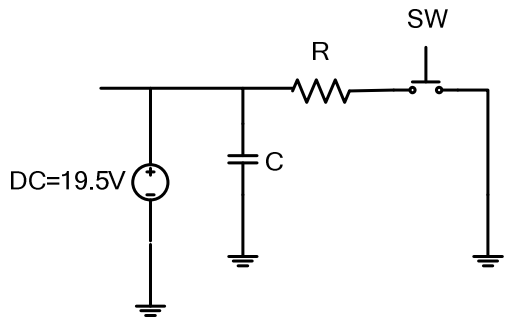


Figure 2.

Therefore, different V_{GH}, V_{GL}, C_L, and CK pose different influence on power dissipation. It is important to include testing parameters of the worst scenario in consideration.

LAYOUT CONSIDERATION

Place output capacitors as close as possible to the IC. Minimize the length and maximize the width of traces to get the best transient response and reduce ripple noise. Users are recommended the use of 10µF ceramics capacitor to reduce the ripple voltage, and use 0.1µF ceramics capacitor to reduce the ripple noise.

PC Board Layout

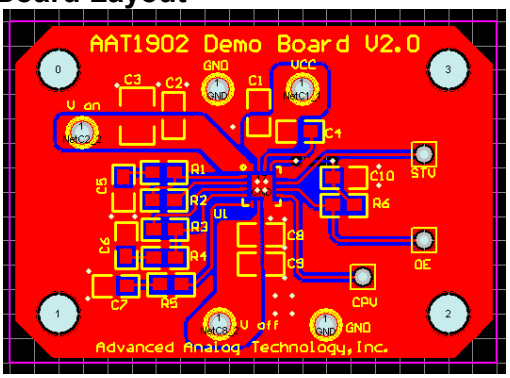


Figure 3. TOP Layout

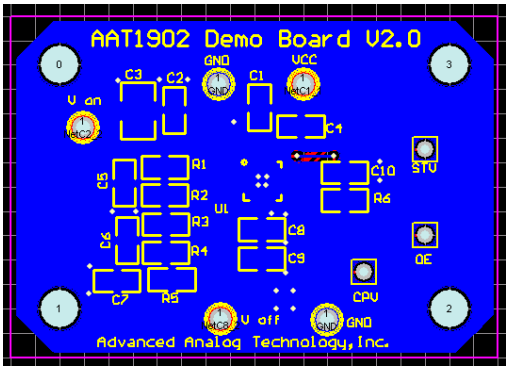
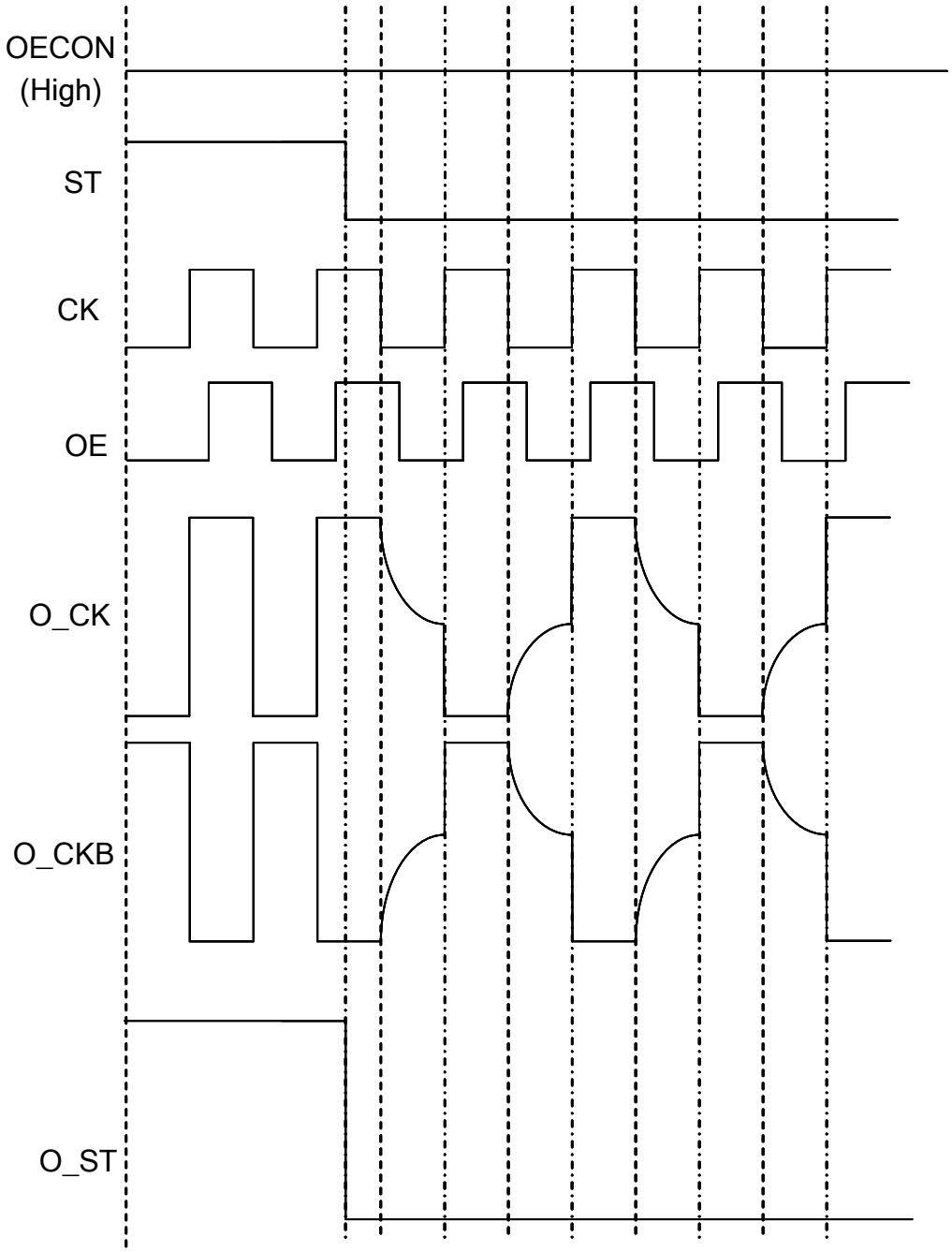
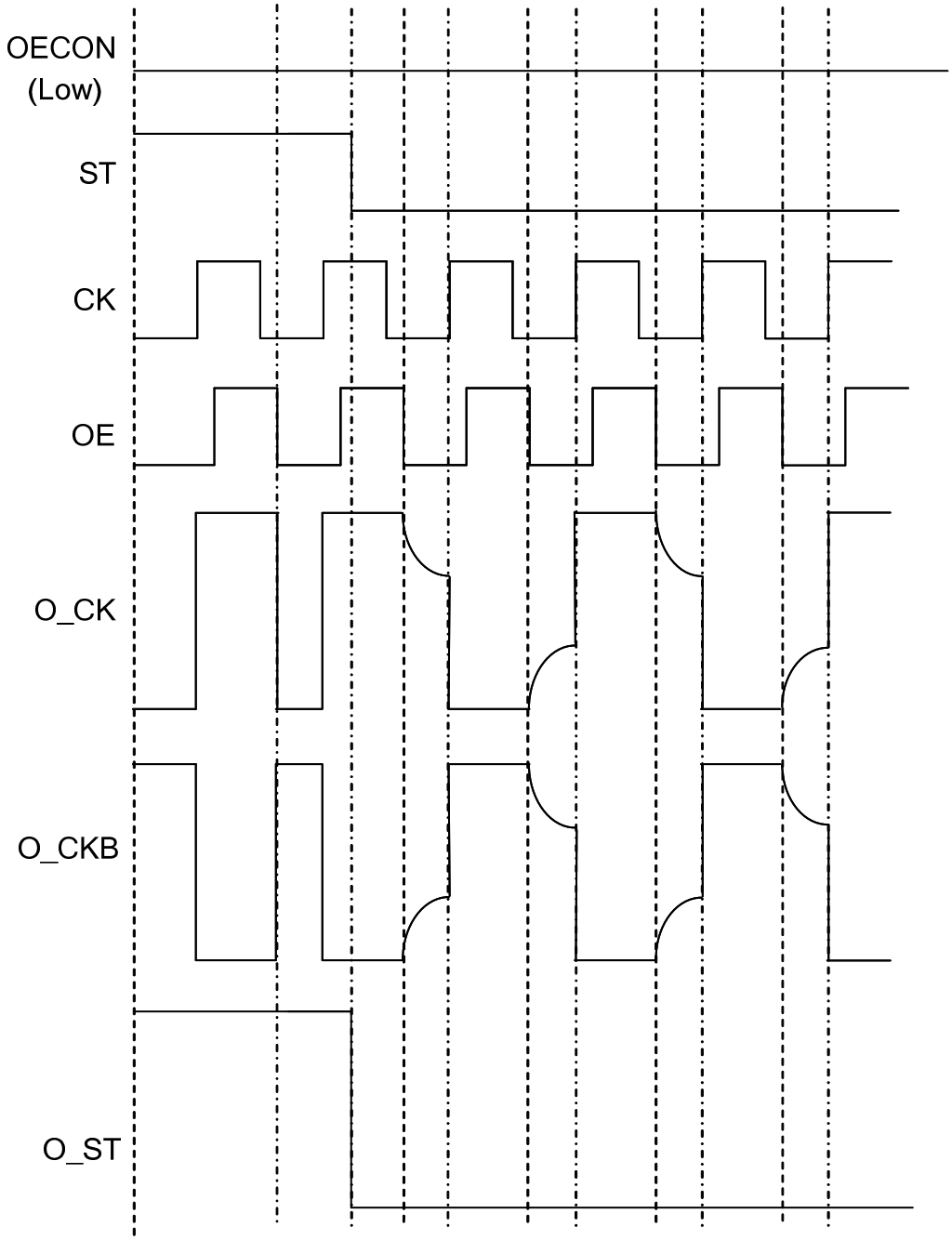


Figure 4. Bottom Layout

TIMING CHART (OECON=HIGH)

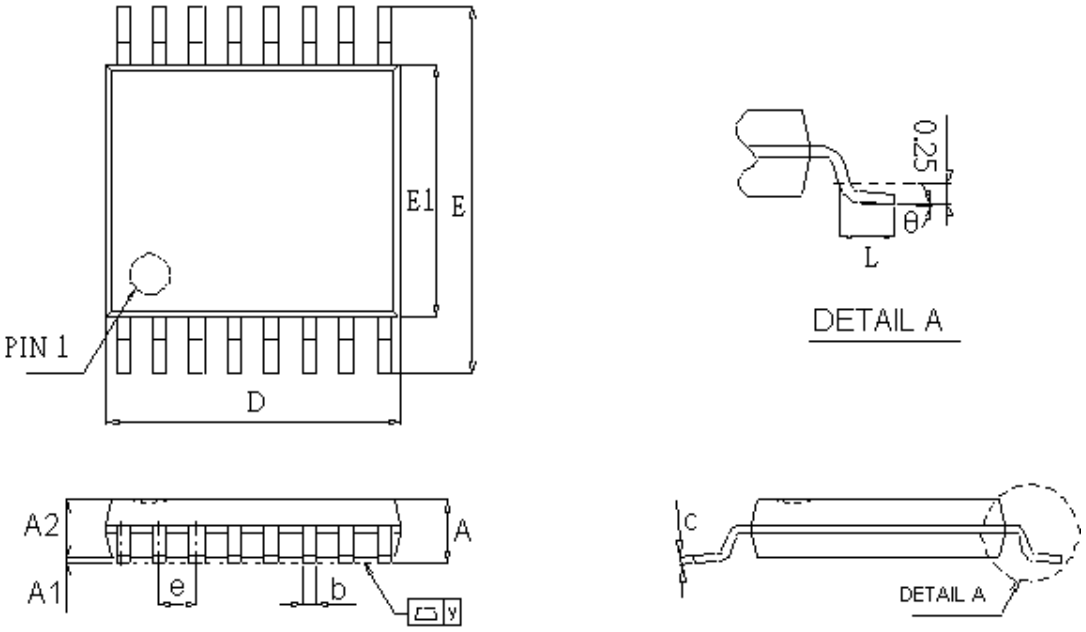


TIMING CHART (OECON=LOW)



PACKAGE DIMENSION

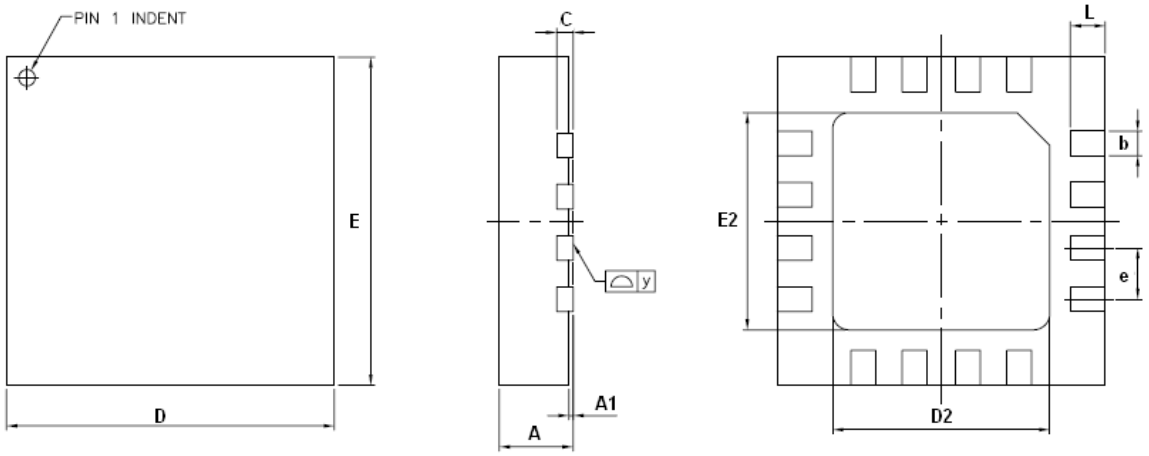
TSSOP-16



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	------	1.00	1.05
b	0.20	0.25	0.28
C	------	0.127	------
D	4.900	5.075	5.100
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
e	------	0.65	------
L	0.5	0.6	0.7
y	------	------	0.076
θ	0°	4°	8°

PACKAGE DIMENSION

VQFN16 4*4



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.8	0.9	1.0
A1	0	0.02	0.05
b	0.25	0.30	0.35
C	------	0.2	------
D	3.9	4.0	4.1
D2	2.60	2.65	2.70
E	3.9	4.0	4.1
E2	2.60	2.65	2.70
e	------	0.65	------
L	0.35	0.40	0.45
y	0	------	0.075