Multi-Output, Sequence Selectable Power-Supply Controller for Mobile Applications

FEATURES

- Up to 95% Efficiency
- ±3% Total Regulation (Line, Load and Temperature)
- 5.5-V to 30-V Input Voltage Range
- 3.3-V, 5-V, and Adjustable 5- to 12-V Outputs
- 300-kHz Low-Noise Fixed Frequency Operation
- Precision 3.3-V Reference Output
- 5-V/30-mA Linear Regulator Output
- High Efficiency Pulse Skipping Mode Operation at Light Load
- Programmable Output Sequencing
- Only Three Inductors Required—No Transformer
- LITTLE FOOT® Optimized Output Drivers
- Internal Soft-Start
- Minimal External Control Components
- 28-Pin SSOP Package
- Output Overvoltage Protection
- Output Undervoltage Shutdown
- Power-Good Output ($\overline{\text{RESET}}$)

APPLICATIONS

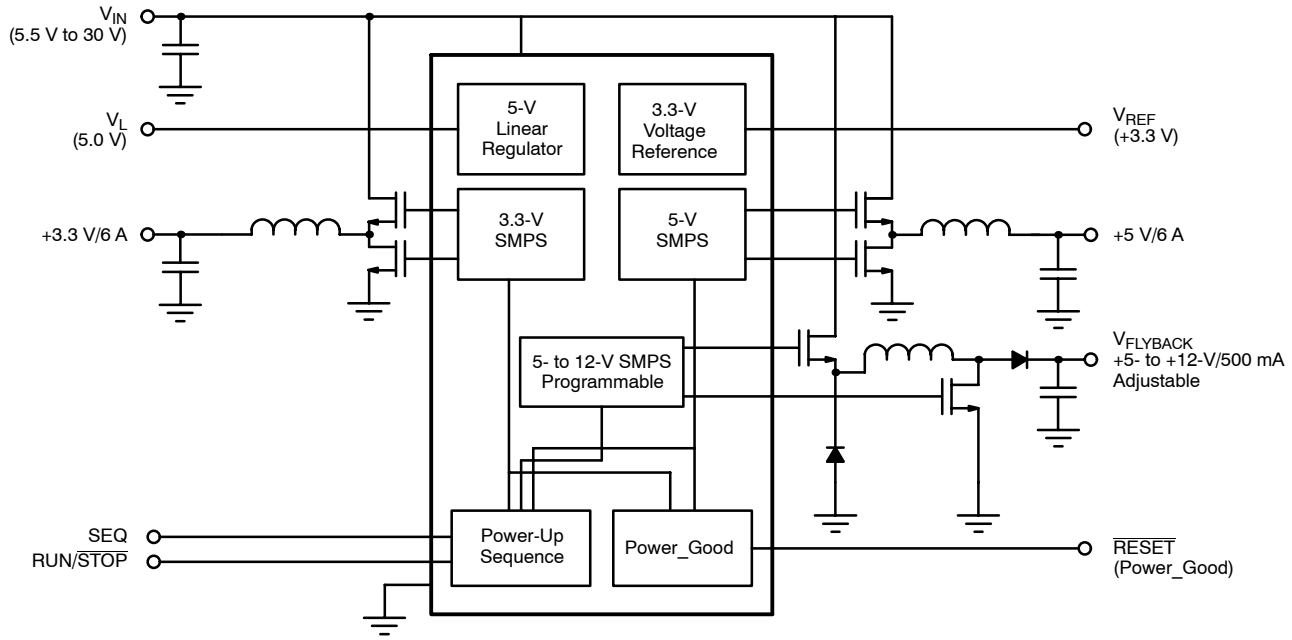
- Notebook and Subnotebook Computers
- PDAs and Mobile Communicators
- Portable Display
- Multimedia Set-Top Box
- Telecommunications Infrastructure
- Distributed Power Conversion

DESCRIPTION

The Si9137 is a current-mode PWM and PSM converter controller, with two synchronous buck converters (3.3 V and 5 V) and an adjustable flyback (non-isolated buck-boost) converter whose output can be set between 5 and 12 V with an external resistor divider. Designed for portable devices, it offers a total of five power outputs (three tightly regulated dc/dc converter outputs, a precision 3.3-V reference and a 5-V LDO output) and includes on-board pre-programmed power-up sequencing, power-good signal with delay, internal frequency compensation networks and automatic boot-strapping. It requires minimum external components and is capable of achieving conversion efficiencies approaching 95%.

The Si9137 is available in both standard and lead (Pb)-free 28-pin SSOP package and specified to operate over the extended commercial (0°C to 90°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND . . . . . −0.3 to +36 V
P_{GND} to GND . . . . . ±2 V
V_L to GND . . . . . −0.3 to +6.5 V
BST_3, BST_5, BSTFY to GND . . . . . −0.3 V to +36 V
V_L Short to GND . . . . . Continuous
LX_3 to BST_3; LX_5 to BST_5; LXFY to BSTFY . . . . . −6.5 V to 0.3 V
Inputs/Outputs to GND
(CS_3, CS_5, CSP, CSN) . . . . . −0.3 V to (V_L +0.3 V)
RUN/$\overline{\text{STOP}}$, SEQ, $\overline{\text{RESET}}$ . . . . . −0.3 V to +5.5 V
DL3, DL5, DLFY to PGND . . . . . −0.3 V to (V_L +0.3 V)
DH3 to LX_3, DH5 to LX_5,
DHFY to LXFY . . . . . −0.3 V to (BSTx +0.3 V)
Continuous Power Dissipation (T_A = 70°C)[a]
28-Pin SSOP[b] . . . . . 762 mW
Operating Temperature Range . . . . . 0°C to 90°C
Storage Temperature Range . . . . . −40°C to 125°C
Lead Temperature (Soldering, 10 Sec.) . . . . . 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 70°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS

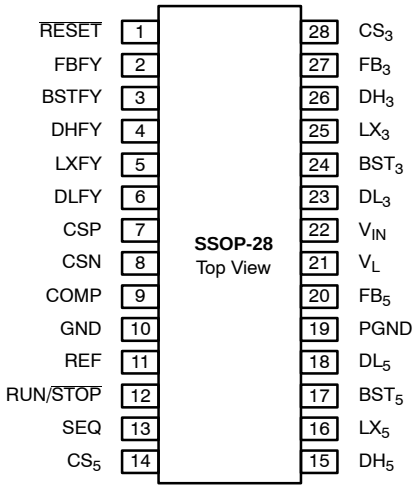
Parameter	Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = 0°C to 90°C, All Controllers ON	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
3.3-V Buck Controller					
Total Regulation (Line, Load, and Temperature)	V_{IN} = 6 to 30 V, 0 < V_{CS3} − V_{FB3} < 90 mV	3.22	3.32	3.42	V
Line Regulation	V_{IN} = 6 to 30 V			± 0.5	%
Load Regulation	0 < V_{CS3} − V_{FB3} < 90 mV			± 0.5	
Current Limit	V_{CS3} − V_{FB3}	90	125	160	mV
Bandwidth	L = 10 µH, C = 330 µF		50		kHz
Phase Margin	R_{SENSE} = 20 mΩ		65		°
5-V Buck Controller					
Total Regulation (Line, Load, and Temperature)	V_{IN} = 6 to 30 V, 0 < V_{CS5} − V_{FB5} < 90 mV	4.87	5.02	5.17	V
Line Regulation	V_{IN} = 6 to 30 V			±0.5	%
Load Regulation	0 < V_{CS5} − V_{FB5} < 90 mV			±0.5	
Current Limit	V_{CS5} − V_{FB5}	90	125	160	mV
Bandwidth	L = 10 µH, C = 330 µF		50		kHz
Phase Margin	R_{SENSE} = 20 mΩ		65		°
5- to 12-V Flyback Controller					
Total Regulation (Line, Load, and Temperature) Output Voltage Set to 12 V	V_{IN} = 6 to 30 V, 0 < V_{CSP} − V_{CSN} < 300 mV R_5 = 26.4 kΩ, R_6 = 10 kΩ (See Figure 1)	11.4	12.0	12.6	V
Line Regulation	V_{IN} = 6 to 30 V			±0.5	%
Load Regulation	0 < V_{CSP} − V_{FBN} < 300 mV			±0.5	
Current Limit	V_{CSP} − V_{CSN}	330	410	500	mV
Bandwidth	L = 10 µH, C = 100 µF		10		kHz
Phase Margin	R_{SENSE} = 100 mΩ, C_{comp} = 120 pF		65		°
Internal Regulator					
V_L Output	All Controllers OFF, V_{IN} >5.5 V, 0 <I_L <30 mA	4.7		5.5	V
V_L Fault Lockout Voltage	V_L Falling Edge	3.6		4.2	
V_L Fault Lockout Hysteresis			75		mV
V_L /FB5 Switchover Voltage	FB_5 Rising Edge	4.2		4.7	V
V_L /FB5 Switchover Hysteresis			75		mV

SPECIFICATIONS

Parameter	Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = 0°C to 90°C, All Controllers ON	Limits			Unit
		Min[a]	Typ[b]	Max[a]	
Reference					
REF Output	No External Load	3.24	3.30	3.36	V
REF Load Regulation	0 to 1 mA		30	75	mV
Supply Current					
Supply Current – Shutdown	RUN/$\overline{\text{STOP}}$ = GND, All Converters OFF, No Load		25	60	µA
Supply Current – Operation	All Controllers ON, No Load, f_{OSC} = 300 kHz		1100	1800	
Oscillator					
Oscillator Frequency		270	300	330	kHz
Maximum Duty Cycle		92	95		%
Fault Detection 3.3-V and 5-V Outputs					
Overvoltage Trip Threshold	With Respect To Unloaded Output Voltage	6	10	14	%
Overvoltage-Fault Propagation Delay	CS3 or CS5 Driven 2% Above Overvoltage Trip Threshold		1.5		µs
Output Undervoltage Threshold	With Respect to Unloaded Output Voltage	–40	–30	–20	%
Output Undervoltage Lockout Time	From each SMPS Enabled	16	20	24	ms
$\overline{\text{RESET}}$					
$\overline{\text{RESET}}$ Start Threshold	With Respect To Unloaded Output Voltage Rising Edge		–5.5		%
$\overline{\text{RESET}}$ Propagation Delay (Falling)	Falling Edge, FB3 or FB5 Driven 2% Above Overvoltage or 2% Below Undervoltage Lockout Thresholds		1.5		µs
$\overline{\text{RESET}}$ Delay Time (Rising)	With Respect to 2nd SMPS Lockout Time Done	92	107	122	ms
Inputs and Outputs					
Feedback Input Leakage Current	FBFY = 3.3 V			1	µA
Input Leakage Current	RUN/$\overline{\text{STOP}}$, SEQ, V_{IN} = 0 V or V_L			±1	
Gate Driver Sink/Source Current (Buck)	DL3, DH3, DL5, DH5 Forced to 2 V		1		A
Gate Driver On-Resistance (Buck)	High or Low		2	7	Ω
Gate Driver Sink/Source Current (Flyback)	DHFY, DLFY Forced to 2 V		0.2		A
Gate Driver On-Resistance (Flyback)	High or Low			15	Ω
$\overline{\text{RESET}}$ Output Low Voltage	$\overline{\text{RESET}}$, I_{SINK} = 4 mA			0.4	V
$\overline{\text{RESET}}$ High Voltage Leakage	$\overline{\text{RESET}}$ = 5 V			1	µA
RUN/$\overline{\text{STOP}}$					
V_{IL}				0.8	V
V_{IH}		2.4			

Notes
a. The algebraic convention is used whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing, and are measured at T_A = 25°C.

PIN CONFIGURATION



ORDERING INFORMATION			
Part Number	Lead (Pb)-Free Part Number	Temperature Range	V_{OUT}
Si9137LG		0 to 90°C	3.3 V, 5 V, 5 to ADJ V
Si9137LG-T1	Si9137LG-T1—E3		

Evaluation Board	Temperature Range	Board Type
Si9137DB	0 to 90°C	Surface Mount

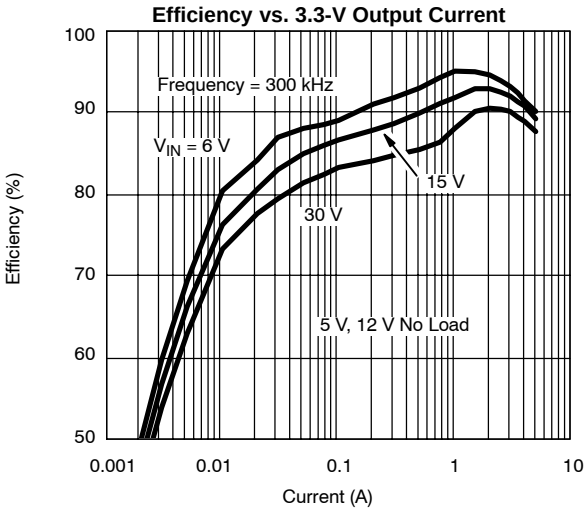
PIN DESCRIPTION

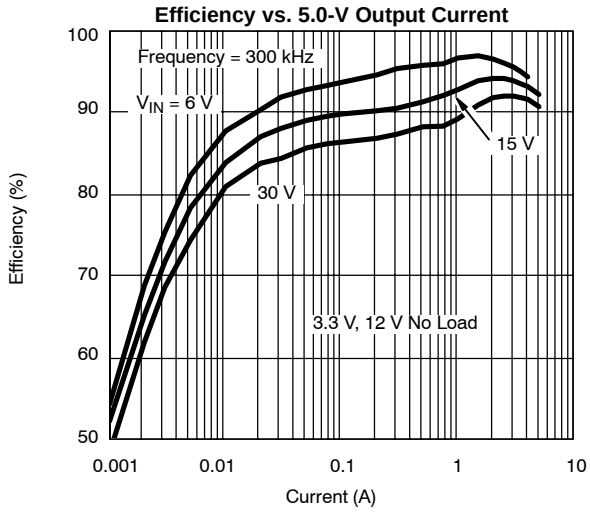
Pin	Symbol	Description
1	$\overline{\text{RESET}}$	Open drain NMOS output active-low timed reset output. $\overline{\text{RESET}}$ swings GND to V_L. Goes high after a fixed 32,000 clock cycle delay following proper power-up of all supply outputs indicating Power_Good.
2	FBFY	Feedback for flyback converter. Normally connected to an external resistor divider used to set the flyback output voltage.
3	BSTFY	Boost capacitor connection for flyback converter.
4	DHFY	Gate-drive output for flyback high-side MOSFET.
5	LXFY	Inductor connection for flyback converter.
6	DLFY	Gate-drive output for flyback low-side MOSFET.
7	CSP	Current sense positive input for flyback converter.
8	CSN	Current sense negative input for flyback converter.
9	COMP	Flyback compensation connection, if required.
10	GND	Analog ground.
11	REF	3.3-V internal reference.
12	RUN/$\overline{\text{STOP}}$	Triple controller ON/OFF control. Logic threshold is 0.8 to 2.4 V. When RUN/$\overline{\text{STOP}}$ is low, all converters are off and supply current is 25-µA typical, 60-µA maximum.
13	SEQ	Pin Strap input that selects SMPS power-up sequence (pin should be fixed to GND, REF or V_L): SEQ = GND: 5-V then 3.3-V then adjustable 5- to 12-V output SEQ = V_L: 3.3-V then 5-V then adjustable 5- to 12-V output SEQ = REF: 3.3-V then 5-V then adjustable 5- to 12-V output, high impedance error detect mode.
14	CS_5	Current sense input for 5-V buck controller.
15	DH_5	Gate-drive output for 5-V buck high-side MOSFET.
16	LX_5	Inductor connection for buck 5-V.
17	BST_5	Boost capacitor connection for 5-V buck converter.
18	DL_5	Gate-drive output for 5-V buck low-side MOSFET.
19	PGND	Power ground.
20	FB_5	Feedback for 5-V buck.
21	V_L	5-V logic supply voltage for internal circuitry.
22	V_{IN}	Input voltage
23	DL_3	Gate-drive output for 3.3-V buck low-side MOSFET.
24	BST_3	Boost capacitor connection for 3.3-V buck converter.
25	LX_3	Inductor connection for 3.3-V buck low-side MOSFET.
26	DH_3	Gate-drive output for 3.3-V buck high-side MOSFET.

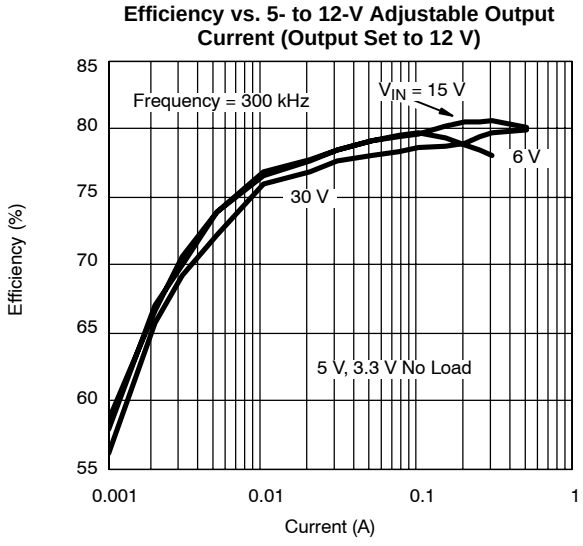
PIN DESCRIPTION

Pin	Symbol	Description
27	FB_3	Feedback for 3.3-V buck.
28	CS_3	Current sense input for 3.3-V buck.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

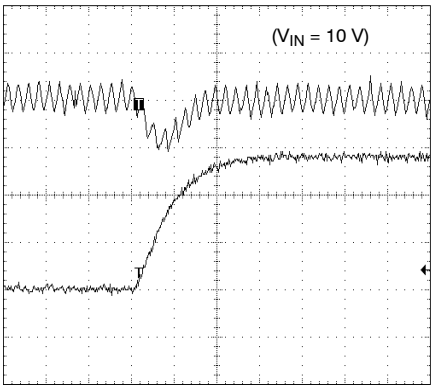




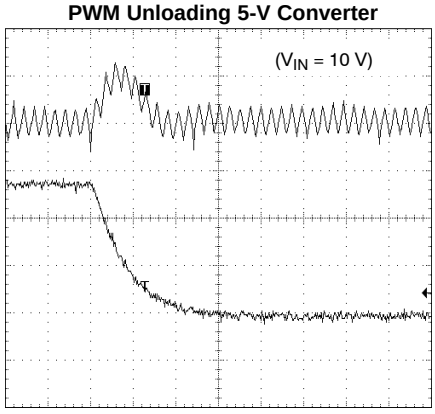


TYPICAL WAVEFORMS

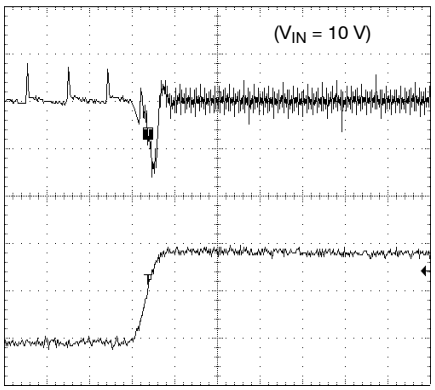
PWM Loading 5-V Converter



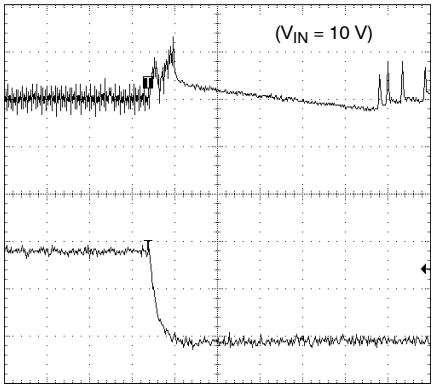
PWM Unloading 5-V Converter



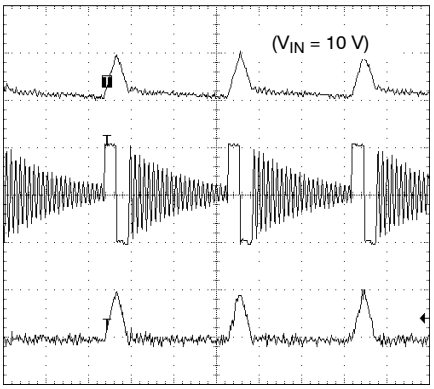
PSM to PWM 5-V Converter



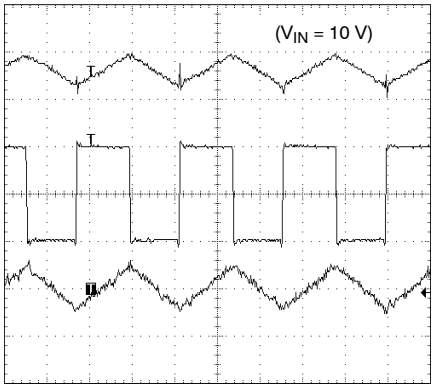
PWM to PSM 5-V Converter



PSM Operation 5-V Converter

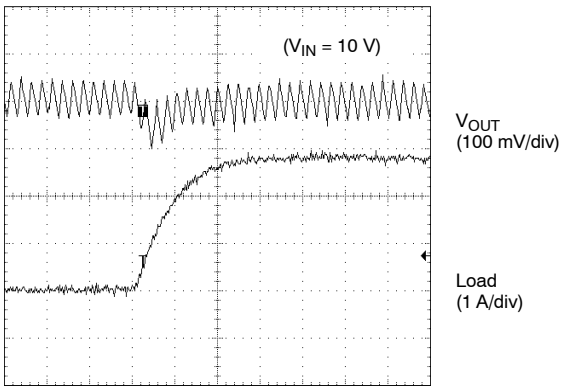


PWM Operation 5-V Converter

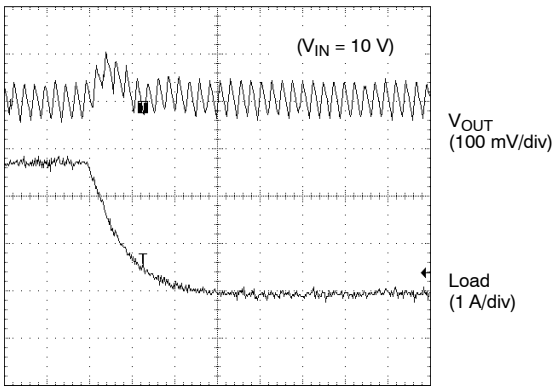


TYPICAL WAVEFORMS

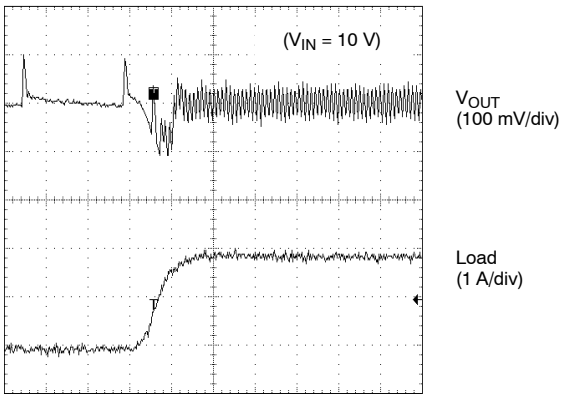
PWM Loading 3-V Converter



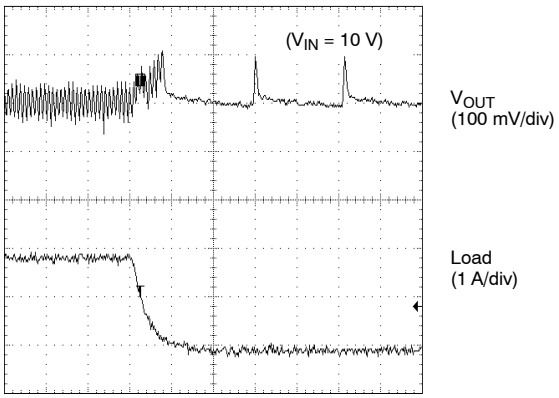
PWM Unloading 3-V Converter



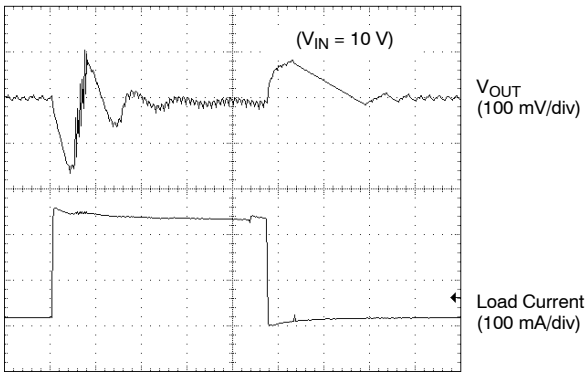
PSM to PWM 3-V Converter



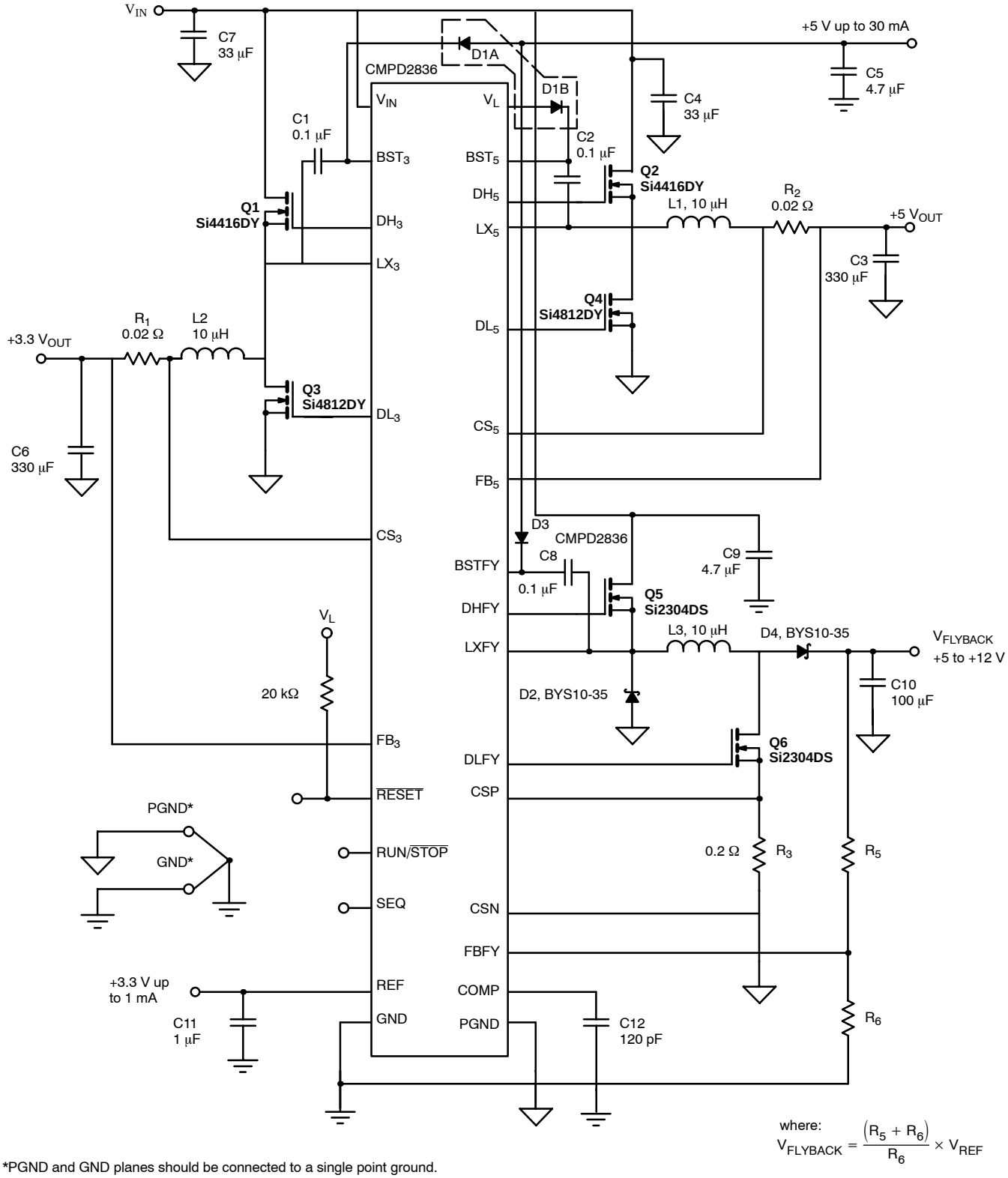
PWM to PSM 3-V Converter



250-mA Transient Adjustable Converter (Output Set To 12 V)



STANDARD APPLICATION CIRCUIT



*PGND and GND planes should be connected to a single point ground.

FIGURE 1.

TIMING DIAGRAMS

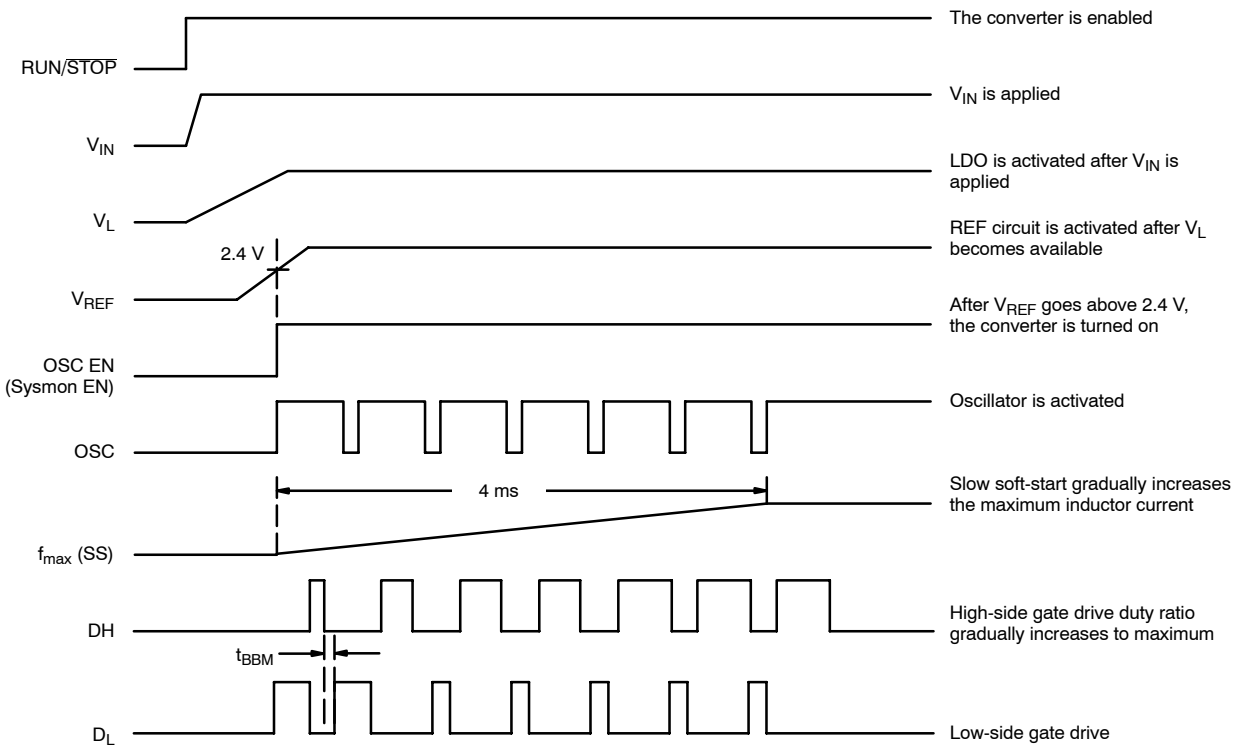


FIGURE 2. Converter is Enabled Before V_{IN} is Applied

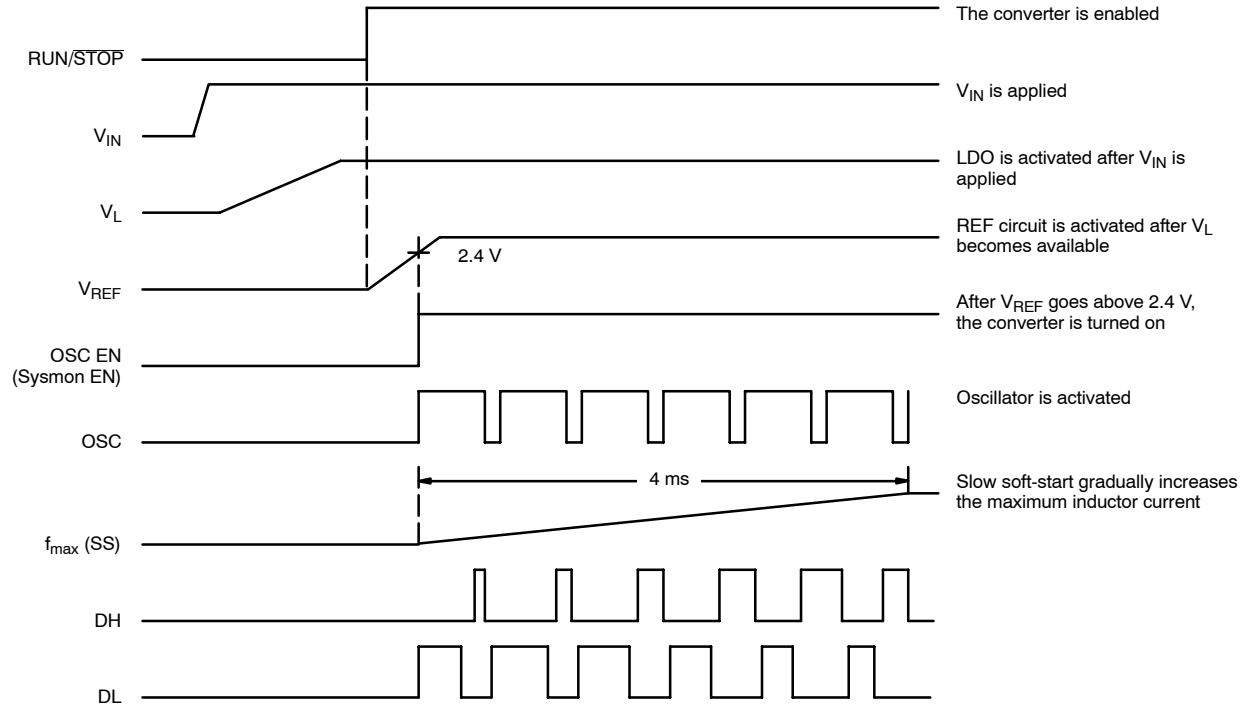


FIGURE 3. Converter is Enabled After V_{IN} is Applied

TIMING DIAGRAMS

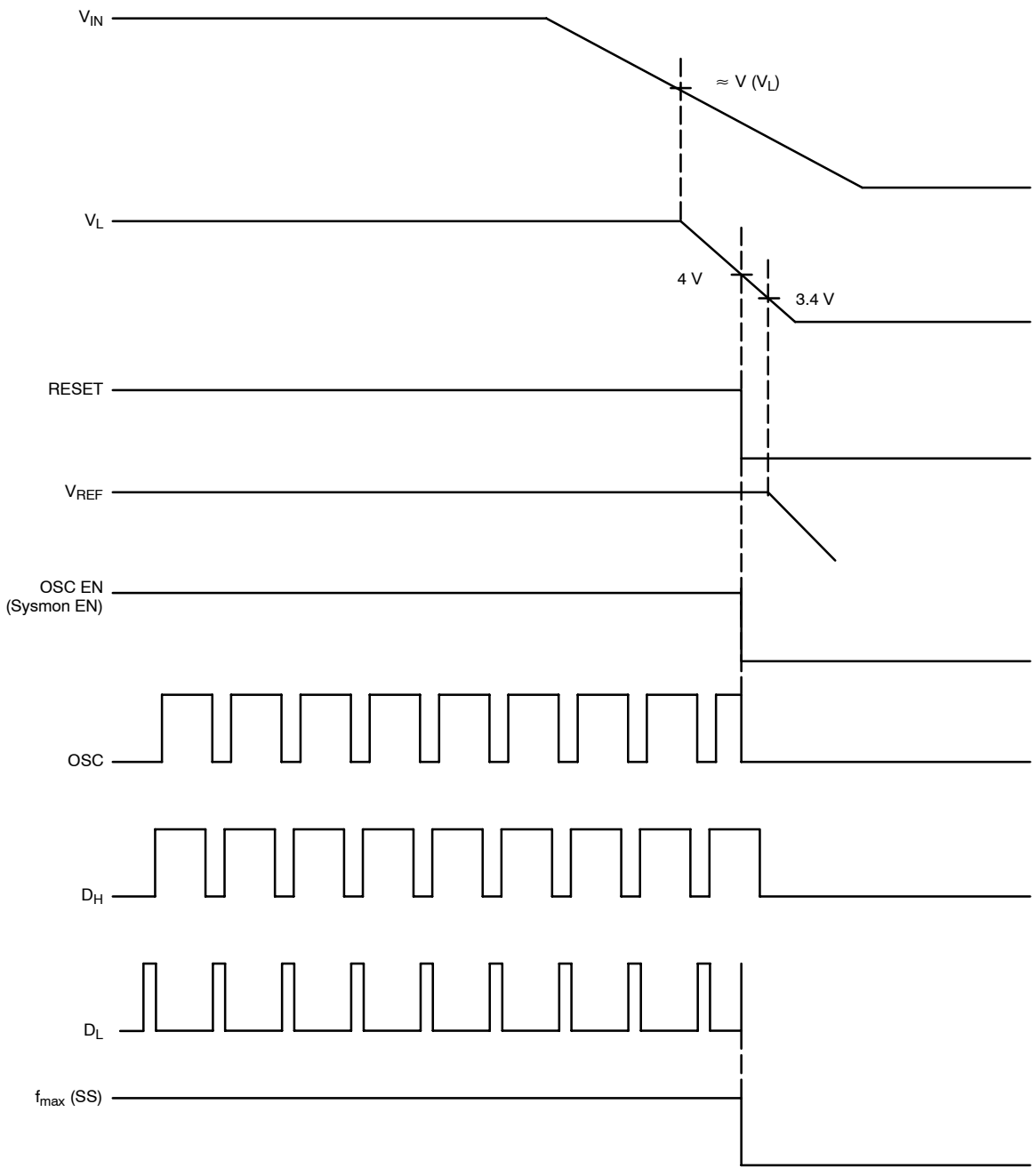


FIGURE 4. Power Off Sequence

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DETAILED FUNCTIONAL BLOCK DIAGRAMS

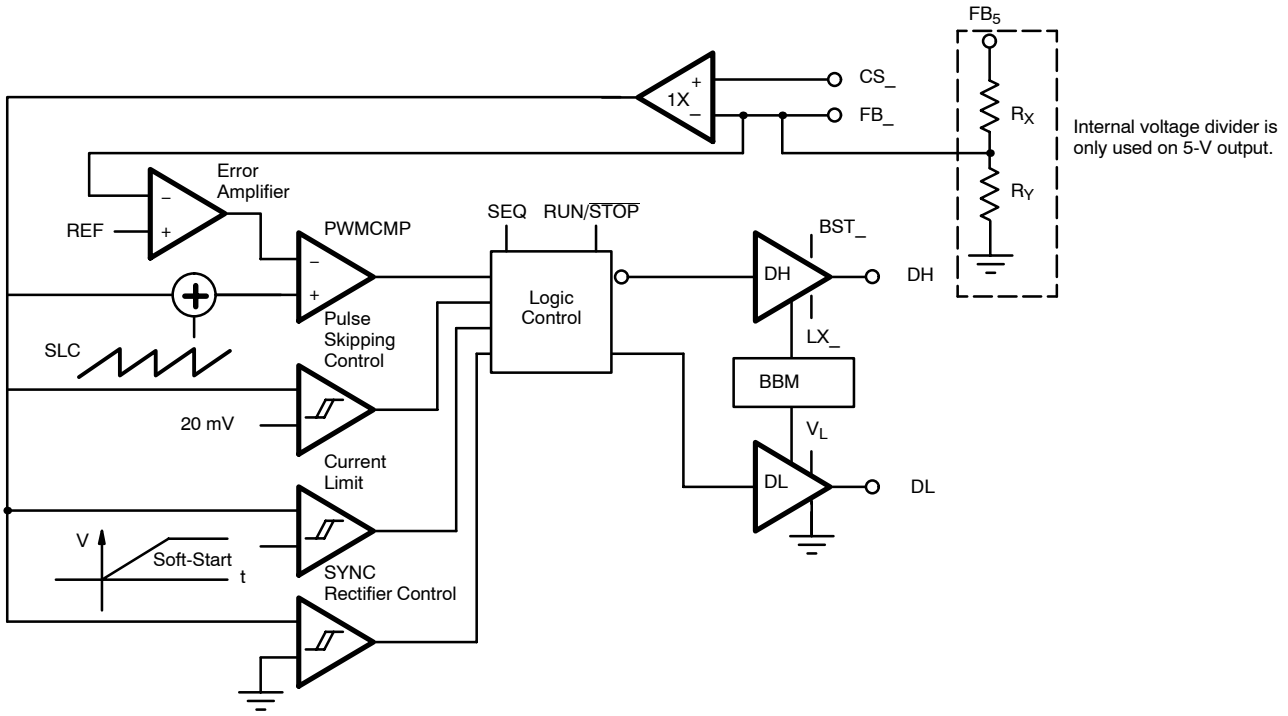

FIGURE 5. Buck Block Diagram (3.3-V and 5-Controllers)

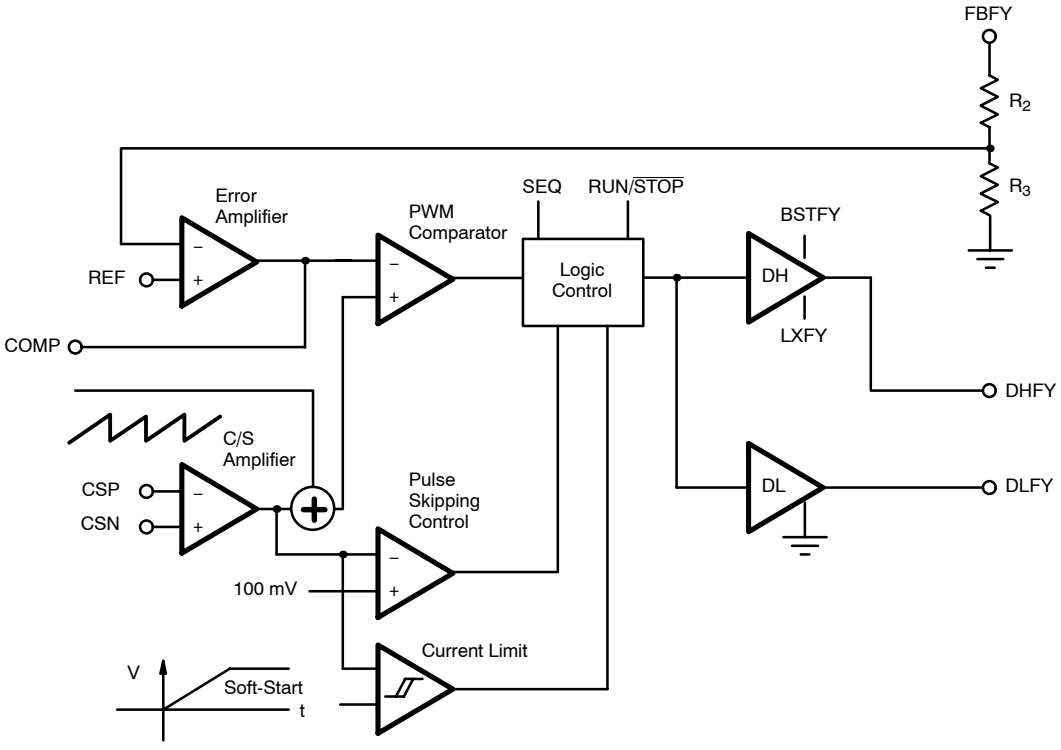

FIGURE 6. Buck-Boost Block Diagram (5- to 12-V Adjustable Controller)

DETAILED FUNCTIONAL BLOCK DIAGRAMS

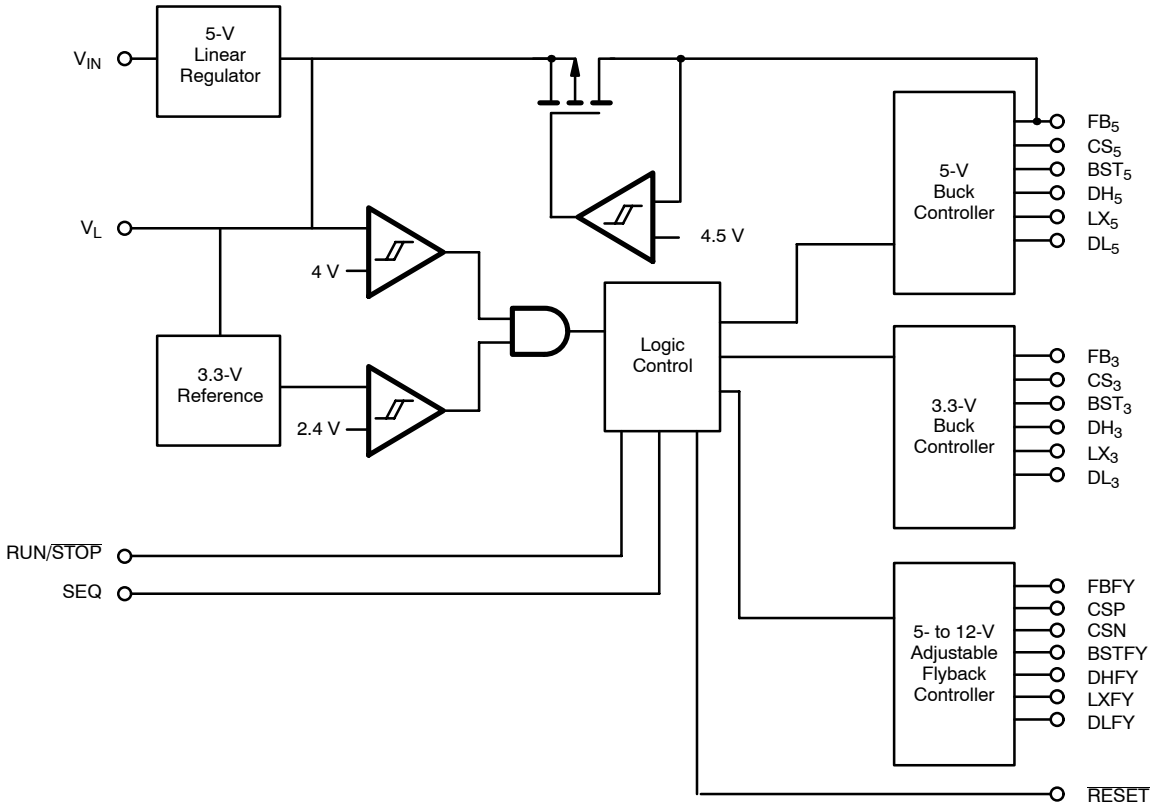

FIGURE 7. Complete Si9137 Block Diagram

DESCRIPTION OF OPERATION

Shutdown Mode

The logic threshold for the RUN/$\overline{\text{STOP}}$ pin is 1.6 V. Input voltage must be 0.8 V or less for logic low and 2.4 V or higher for logic high.

Start-up Sequence

Start-up is controlled by RUN/$\overline{\text{STOP}}$ in conjunction with SEQ. If SEQ is tied to GND, the 5-V SMPS output will come up first, followed by the 3.3-V output and then the adjustable 5- to 12-V output. If SEQ is tied to V_L, then the 3.3-V SMPS output will come up first, followed by the 5-V and then the adjustable 5- to 12-V output.

When the first SMPS output voltage is within tolerance, the second SMPS will begin its soft-start cycle. When the second SMPS output is within tolerance, the third SMPS will start its soft-start cycle. When both the 3.3-V and 5-V SMPS outputs are within tolerance and 32,000 clock cycles (typically equal to 107 ns) have elapsed since the second SMPS output went into regulation, the $\overline{\text{RESET}}$ pin will be pulled high, signifying that all converters are operating correctly (see $\overline{\text{RESET}}$ Power Good Voltage Monitor).

The Si9137 converts a 5.5-V to 30-V input voltage to five different output voltages; two buck (step-down) high current, PWM, switch-mode supplies of 3.3 V and 5 V, one “flyback” PWM switch-mode supply adjustable from 5 V to 12 V, one precision 3.3-V reference and one 5-V between low drop out (LDO) linear regulator output. Switch-mode supply output current capabilities depend on external components (can be selected to exceed 10 A). In the standard application circuit illustrated in Figure 1, each buck converter is capable of delivering 5 A, with the flyback converter delivering 250 mA. The recommended load current for the precision 3.3-V reference output is less than 1 mA, and for the 5-V LDO output is less than 30 mA. In order to maximize power efficiency of the converter, when the 5-V buck converter output (FB5) voltage is above 4.5-V, the internal 5-V LDO is turned off and V_L is supplied by the 5-V converter output.

DESCRIPTION OF OPERATION (CONT'D)

Buck Converter Operation:

The 3.3-V and 5-V buck converters are both current-mode PWM and PSM (during light load operation) regulators using high-side bootstrap n-channel and low-side n-channel MOSFETs. At light load conditions, the converters switch at a lower frequency than the clock frequency. This operating condition is defined as pulse-skipping. The operation of the converter(s) switching at clock frequency is defined as normal operation.

Normal Operation: Buck Converters

In normal operation, the buck converter high-side MOSFET is turned on with a delay (known as break-before-make time - t_{BBM}), after the rising edge of the clock. After a certain on time, the high-side MOSFET is turned off and then after a delay (t_{BBM}), the low-side MOSFET is turned on until the next rising edge of the clock, or the inductor current reaches zero. The t_{BBM} (approximately 25 ns to 60 ns), has been optimized to guarantee the efficiency is not adversely affected at the high switching frequency and a specified minimum to account for variations of possible MOSFET gate capacitances.

During the normal operation, the high-side MOSFET switch on-time is controlled internally to provide excellent line and load regulation over temperature. Both buck converters should have load, line, regulation to within 0.5% tolerance.

Pulse Skipping: Buck Converters

When the buck converter switching frequency is less than the internal clock frequency, its operation mode is defined as pulse skipping mode. During this mode, the high-side MOSFET is turned on until V_{CS}-V_{FB} reaches 20 mV, or the on time reaches its maximum duty ratio. After the high-side MOSFET is turned off, the low-side MOSFET is turned on after the t_{BBM} delay, which will remain on until the inductor current reaches zero. The output voltage will rise slightly above the regulation voltage after this sequence, causing the controller to stay idle for the next clock cycle, or several clock cycles. When the output voltage falls slightly below the regulation level, the high-side MOSFET will be turned on again at the next clock cycle. With the converter remaining idle during some clock cycles, the switching losses are reduced preserving conversion efficiency during the light output current condition.

Current Limit: Buck Converters

When the buck converter inductor current is too high, the voltage across pin CS3(5) and pin FB3(5) will exceed approximately 125 mV causing the high-side MOSFET to be turned off instantaneously regardless of the input, or output condition. The Si9137 features clock cycle by clock cycle current limiting capability.

Flyback Converter Operation:

The Si9137 has an adjustable 5-V to 12-V output non-isolated buck-boost converter, called for brevity a flyback. The input voltage range can span above or below the regulated output voltage. It consists of two n-channel MOSFET switches that are turned on and off in phase, and two diodes. Similar to the buck converter, during the light load conditions, the flyback converter will switch at a frequency lower than the internal clock frequency, which can be defined as pulse skipping mode (PSM); otherwise, it operates in normal PWM mode.

The output voltage of the flyback converter is set by two resistors (R_5 and R_6, see Figure 1) where,

$$V_{FLYBACK} = \frac{(R_5 + R_6)}{R_6} \times V_{REF}$$

Normal Operation: Flyback Converter

In normal operation mode, the two MOSFETs are turned on at the rising edge of the clock, and then turned off. The on time is controlled internally to provide excellent load, line, and temperature regulation. The flyback converter has load, line and temperature regulation well within 0.5%.

Pulse Skipping: Flyback Converter

Under the light load conditions, similar to the buck converter, the flyback converter will enter pulse skipping mode. The MOSFETs will be turned on until the inductor current increases to such a level that the voltage across the pin CSP and pin CSN reaches 410 mV, or the on time reaches the maximum duty cycle. After the MOSFETs are turned off, the inductor current will conduct through two diodes until it reaches zero. At this point, the flyback converter output will rise slightly above the regulation level, and the converter will stay idle for one or several clock cycle(s) until the output falls back slightly below the regulation level. The switching losses are reduced by skipping pulses preserving the efficiency during light load.

DESCRIPTION OF OPERATION (CONT'D)

Current Limit: Flyback Converter

Similar to the buck converter; when the voltage across pin CSP and pin CSN exceeds 410-mV typical, the two MOSFETs will be turned off regardless of the input and output conditions.

Grounding:

There are two separate grounds on the Si9137, analog signal ground (GND) and power ground (PGND). The purpose of two separate grounds is to prevent the high currents on the power devices (both external and internal) from interfering with the analog signals. The internal components of Si9137 have their grounds tied (internally) together. These two grounds are then tied together (externally) at a single point, to ensure Si9137 noise immunity.

This separation of grounds should be maintained in the external circuitry, with the power ground of all power devices being returned directly to the input capacitors, and the small signal ground being returned to the GND pin of Si9137.

$\overline{\text{RESET}}$ Power-Good Voltage Monitor

The power-good monitor generates a system $\overline{\text{RESET}}$ signal. At first power-up (RUN/$\overline{\text{STOP}}$ going high), $\overline{\text{RESET}}$ is held low until the 3.3-V, 5-V outputs are in regulation and beyond the UVLO timer. At this point, an internal timer begins counting oscillator pulses and $\overline{\text{RESET}}$ continues to be held low until 32,000 cycles have elapsed. After this timeout period, 107 ms @ 300 kHz, $\overline{\text{RESET}}$ is actively pulled up to V_L, when the recommended 20-kΩ resistor to V_L is on the $\overline{\text{RESET}}$ pin.

Output Overvoltage Protection

The 5-V and 3.3-V SMPS outputs are monitored for overvoltage. If either output is typically more than 10% above the nominal regulation point, all low-side gate drivers are latched high until RUN/$\overline{\text{STOP}}$ is toggled. This action turns on the synchronous rectifier MOSFETs with a 100% duty cycle, in turn rapidly discharging the output capacitors and forcing all SMPS outputs to ground.

Output Undervoltage Protection

Each of the Si9137 5-V and 3.3-V SMPS outputs has an undervoltage protection circuit that is activated 6,144 clock cycles (20.48 ms) after the SMPS is enabled. If either SMPS output is typically under 70% of the nominal value, all SMPSs are latched off and their outputs are clamped to ground by the synchronous rectifier MOSFETs. The SMPS will not restart until RUN/$\overline{\text{STOP}}$ is toggled.

Stability:

Buck Converters:

In order to simplify designs, the 5-V and 3.3-V supplies do not require external frequency compensation. Meanwhile, it achieves excellent regulation and efficiency. The converters are current mode control, with a bandwidth substantially higher than the LC tank dominant pole frequency of the output filter. To ensure stability, the minimum capacitance and maximum ESR values are:

$$C_{LOAD} \geq \frac{V_{REF}}{2\pi \times V_{OUT} \times R_{CS} \times BW} \qquad ESR \leq \frac{V_{OUT} \times Rcs}{V_{REF}}$$

where V_{REF} = 3.3 V, V_{OUT} is the output voltage (5 V or 3.3 V), Rcs is the current sensing resistor in ohms and BW = 50 khz

With the components specified in the application circuit (L = 10 µH, R_{CS} = 0.02 Ω, C_{OUT} = 330 µF, ESR approximately 0.1 Ω), the converter should have a bandwidth of approximately 50 kHz, with minimum phase margin of 65°, and dc gain above 50 dB.

Other Outputs

The Si9137 also provides a 3.3-V reference which can be externally loaded up to 1 mA, as well as, a 5-V LDO output which can be loaded up to 30 mA, or even more depending on the system application. When the 5-V buck converter is turned on, the 5-V LDO output is shorted with the 5-V buck converter output, so its loading capability is substantially increased. For stability, the 3.3-V reference output requires a 1-µF capacitor, and the 5-V LDO output requires a 4.7-µF capacitor.

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