

High-Voltage Current-Mode PWM Controller

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options			
Min	Max			16 Pin Plastic DIP	16 Pin SOIC	20 Pin Plastic PLCC	DIE
10V	450V	< $\pm 2\%$	49%	HV9120P	HV9120NG	HV9120PJ	HV9120X
10V	450V	< $\pm 2\%$	99%	HV9123P	HV9123NG	HV9123PJ	HV9123X

Standard temperature range for all parts is industrial (-40° to +85°C).

Features

- 10 to 450V input acceptance range
- <1.3mA supply current
- >1.0MHz clock
- >20:1 dynamic range @ 500KHz
- Low internal noise

Applications

- Off-line high frequency power supplies
- Universal input power supplies
- High density power supplies
- Very high efficiency power supplies
- Extra wide load range power supplies

Absolute Maximum Ratings

Voltages are referenced to $-V_{IN}$

$+V_{IN}$ Input Voltage	450V
V_{DD} Device Supply Voltage	15.5V
Logic Input Voltages	-0.3 to $V_{DD} + 0.3V$
Linear Input Voltages	-0.3 to $V_{DD} + 0.3V$
I_{IN} Preregulator Input Current (continuous)	2.5mA
T_j Operating Junction Temperature	150° C
Storage Temperature	-65°C to 150°C
Power Dissipation, PDIP	1000mW
Power Dissipation PLCC	1400mW
Power Dissipation SOIC	900mW

General Description

The Supertex HV9120 and HV9123 are Switch Mode Power Supply (SMPS) controller subsystems that can start and run directly from almost any DC input, from a 12V battery to a rectified and filtered 240V AC line. They contain all the elements required to build a single-switch converter except for the switch, magnetic assembly, output rectifier(s) and filter(s).

A unique input circuit allows the 912x to self-start directly from a high voltage input, and subsequently take the power to operate from one of the outputs of the converter it is controlling, allowing very efficient operation while maintaining input-to-output galvanic isolation limited in voltage only by the insulation system of the associated magnetic assembly. A $\pm 2\%$ internal bandgap reference, internal operational amplifier, very high speed comparator, and output buffer allow production of rugged, high performance, high efficiency power supplies of 50 watts or more, which can still be over 80% efficient at outputs of 1.0W or less. The wide dynamic range of the controller system allows designs with extremely wide line and load variations with much less difficulty and much higher efficiency than usual. The exceptionally wide input voltage acceptance range also allows much better usage of energy stored in input dropout capacitors than with other PWM ICs. Remote on/off controls allow either latching or nonlatching remote shutdown. During shutdown, power required is under 6.0mW.

For detailed circuit and application information, please refer to application notes AN-H13 and AN-H21 to AN-H24.

Electrical Characteristics

(Unless otherwise specified, $V_{DD} = 10V$, $+V_{IN} = 48V$, Discharge = $-V_{IN} = 0V$, $R_{BIAS} = 390K\Omega$, $R_{OSC} = 330K\Omega$, $T_A = 25^\circ C$.)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
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Reference

V_{REF}	Output Voltage	3.92	4.00	4.08	V	$R_L = 10M\Omega$
		3.84	4.00	4.16		$R_L = 10M\Omega$, $T_A = -55^\circ C$ to $125^\circ C$
Z_{OUT}	Output Impedance ¹	15	30	45	K Ω	
I_{SHORT}	Short Circuit Current		125	250	μA	$V_{REF} = -V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature ¹		0.25		mV/ $^\circ C$	$T_A = -55^\circ C$ to $125^\circ C$

Oscillator

f_{MAX}	Oscillator Frequency	1.0	3.0		MHz	$R_{OSC} = 0\Omega$
f_{OSC}	Initial Accuracy ²	80	100	120	KHz	$R_{OSC} = 330K\Omega$
		160	200	240		$R_{OSC} = 150K\Omega$
ΔV_{OSC}	Voltage Stability			15	%	$9.5V < V_{DD} < 13.5V$
TC_{OSC}	Temperature Coefficient ¹		170		ppm/ $^\circ C$	$T_A = -55^\circ C$ to $125^\circ C$

PWM

D_{MAX}	Maximum Duty Cycle ¹	HV9120	49.0	49.4	49.6	%	
		HV9123	95	97	99		
D_{MIN}	Deadtime ¹	HV9123		225		nsec	
	Minimum Duty Cycle			0		%	
	Minimum Pulse Width Before Pulse Drops Out ¹			80	125		nsec

Current Limit

V_{lim}	Maximum Input Signal	1.0	1.2	1.4	V	$V_{FB} = 0V$
t_d	Delay to Output ¹		80	150	ns	$V_{SENSE} = 1.5V$, $V_{COMP} \leq 2.0V$

Error Amplifier

V_{FB}	Feedback Voltage	3.92	4.00	4.08	V	V_{FB} Shorted to Comp
I_{IN}	Input Bias Current		25	500	nA	$V_{FB} = 4.0V$
V_{OS}	Input Offset Voltage	nulled during trim				
A_{VOL}	Open Loop Voltage Gain ¹	60	80		dB	
GB	Unity Gain Bandwidth ¹	1.0	1.3		MHz	
Z_{OUT}	Output Impedance ¹	see fig. 1			Ω	
I_{SOURCE}	Output Source Current	-1.4	-2.0		mA	$V_{FB} = 3.4V$
I_{SINK}	Output Sink Current	0.12	0.15		mA	$V_{FB} = 4.5V$
PSRR	Power Supply Rejection ¹	see fig. 2			dB	

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin must be $\leq 5pF$.

Electrical Characteristics (continued)

(Unless otherwise specified, $V_{DD} = 10V$, $+V_{IN} = 48V$, Discharge = $-V_{IN} = 0V$, $R_{BIAS} = 390K\Omega$, $R_{OSC} = 330K\Omega$, $T_A = 25^\circ C$.)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
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Pre-regulator/Startup

$+V_{IN}$	Input Voltage			450	V	$I_{IN} < 10\mu A$; $V_{CC} > 9.4V$
$+I_{IN}$	Input Leakage Current			10	μA	$V_{DD} > 9.4V$
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage	8.0	8.7	9.4	V	$I_{PREREG} = 10\mu A$
V_{LOCK}	Undervoltage Lockout	7.0	8.1	8.9	V	

Supply

I_{DD}	Supply Current		0.75	1.3	mA	$C_L < 75pF$
I_Q	Quiescent Supply Current		0.55		mA	$\overline{Shutdown} = -V_{IN}$
I_{BIAS}	Nominal Bias Current		20		μA	
V_{DD}	Operating Range	9.0		13.5	V	

Shutdown Logic

t_{SD}	$\overline{Shutdown}$ Delay ¹		50	100	ns	$C_L = 500pF$, $V_{SENSE} = -V_{IN}$
t_{SW}	$\overline{Shutdown}$ Pulse Width ¹	50			ns	
t_{RW}	RESET Pulse Width ¹	50			ns	
t_{LW}	Latching Pulse Width ¹	25			ns	$\overline{Shutdown}$ and reset low
V_{IL}	Input Low Voltage			2.0	V	
V_{IH}	Input High Voltage	7.0			V	
I_{IH}	Input Current, Input Voltage High		1.0	5.0	μA	$V_{IN} = V_{DD}$
I_{IL}	Input Current, Input Voltage Low		-25	-35	μA	$V_{IN} = 0V$

Output

V_{OH}	Output High Voltage	$V_{DD} - 0.25$			V	$I_{OUT} = 10mA$	
		$V_{DD} - 0.3$				$I_{OUT} = 10mA$, $T_A = -55^\circ C$ to $125^\circ C$	
V_{OL}	Output Low Voltage			0.2	V	$I_{OUT} = -10mA$	
				0.3		$I_{OUT} = -10mA$, $T_A = -55^\circ C$ to $125^\circ C$	
R_{OUT}	Output Resistance	Pull Up		15	25	Ω	$I_{OUT} = \pm 10mA$
		Pull Down		8.0	20		
		Pull Up		20	30	Ω	$I_{OUT} = \pm 10mA$, $T_A = -55^\circ C$ to $125^\circ C$
		Pull Down		10	30		
t_R	Rise Time ¹		30	75	ns	$C_L = 500pF$	
t_F	Fall Time ¹		20	75	ns	$C_L = 500pF$	

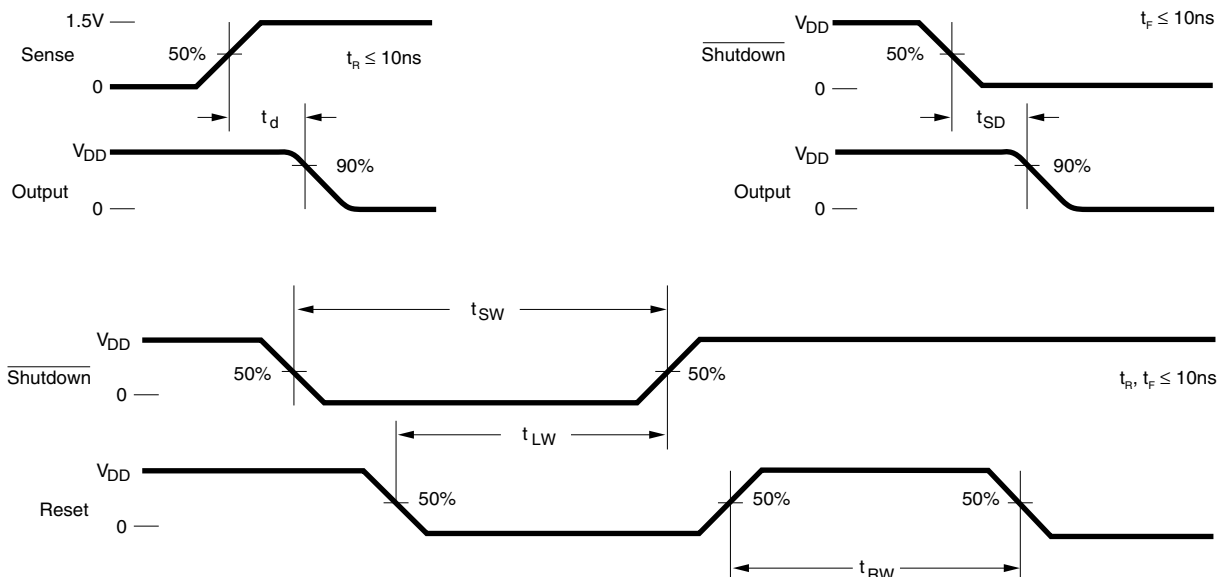
Note:

1. Guaranteed by design. Not subject to production test.

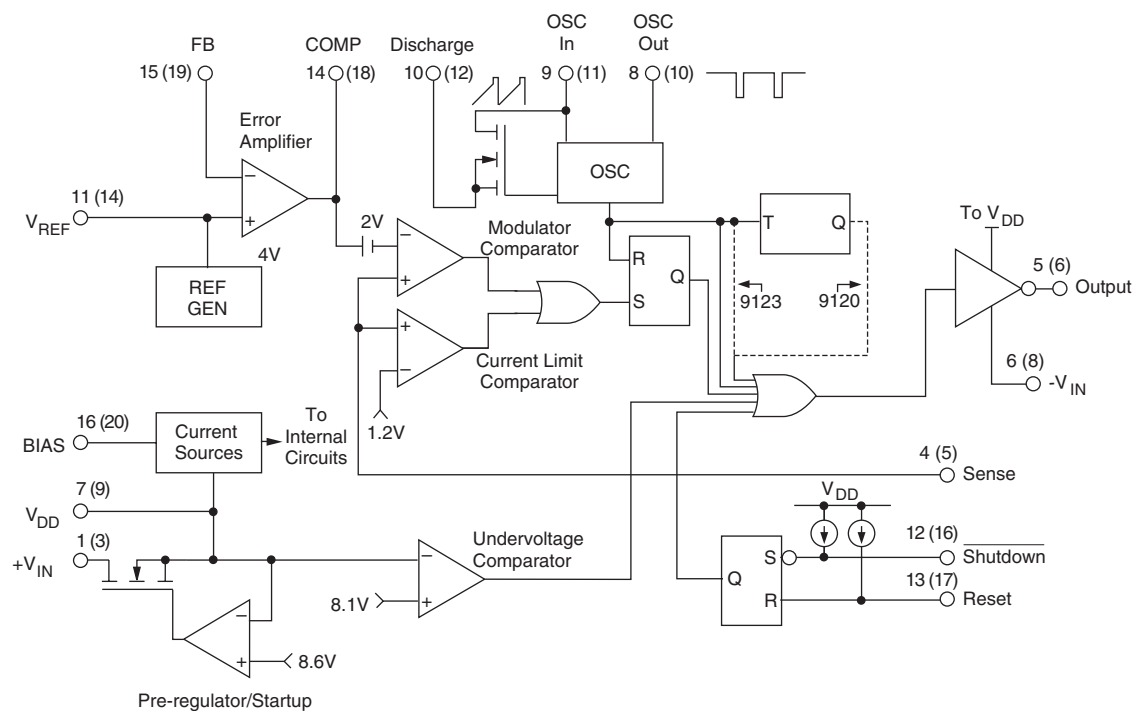
Truth Table

Shutdown	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Shutdown Timing Waveforms

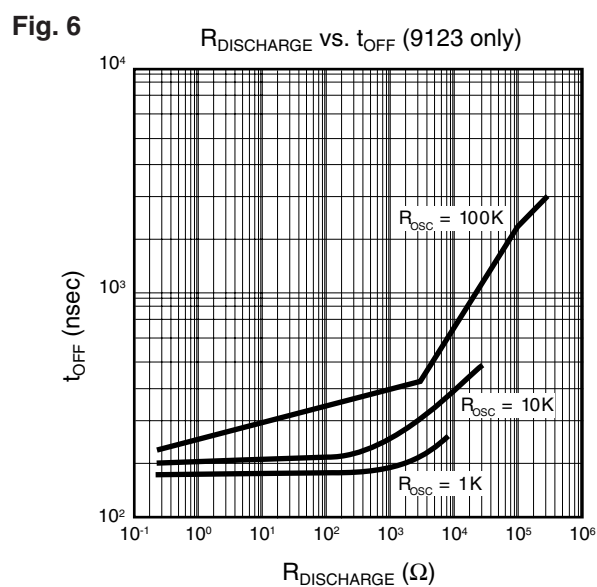
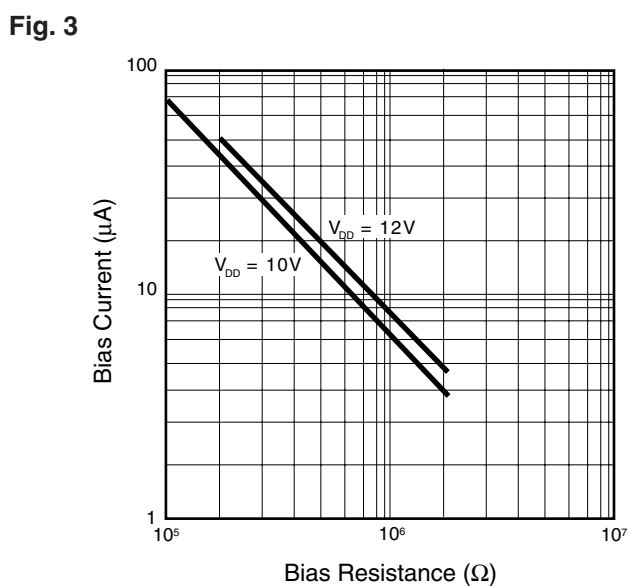
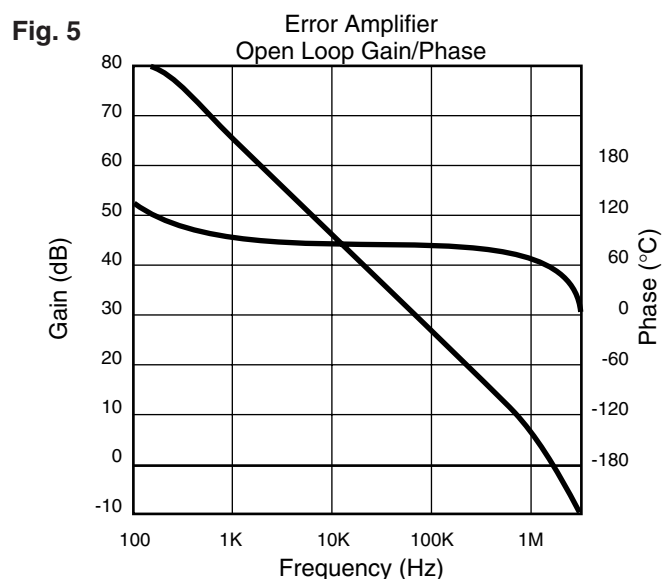
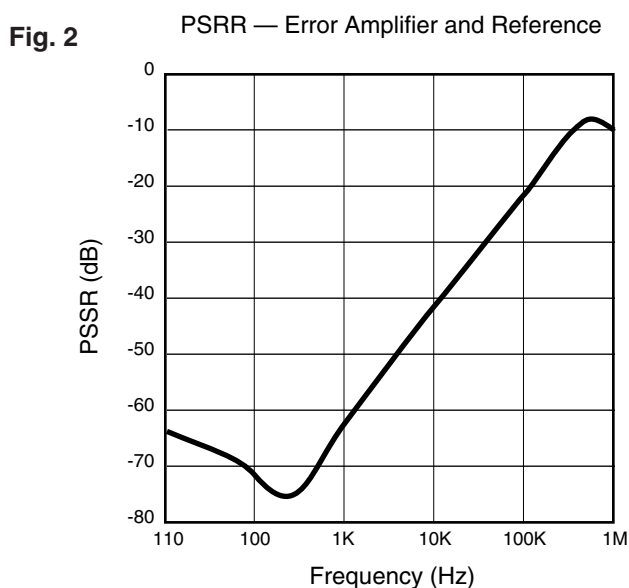
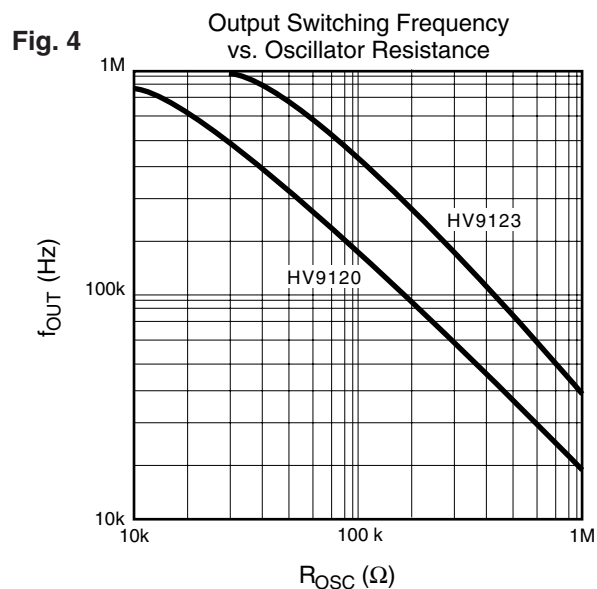
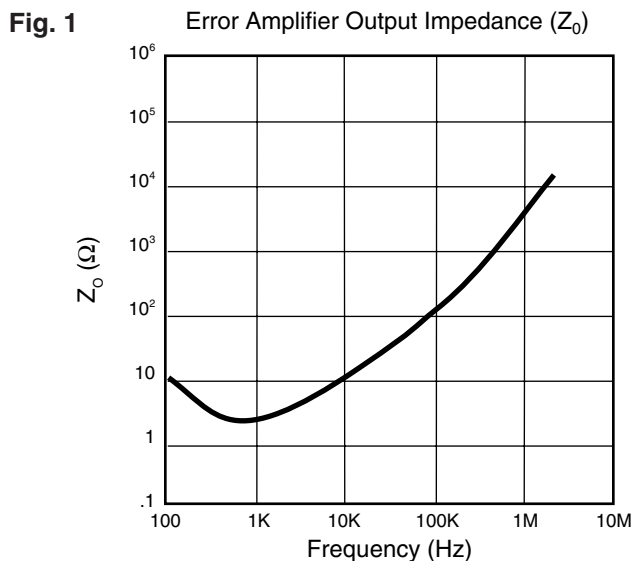


Functional Block Diagram

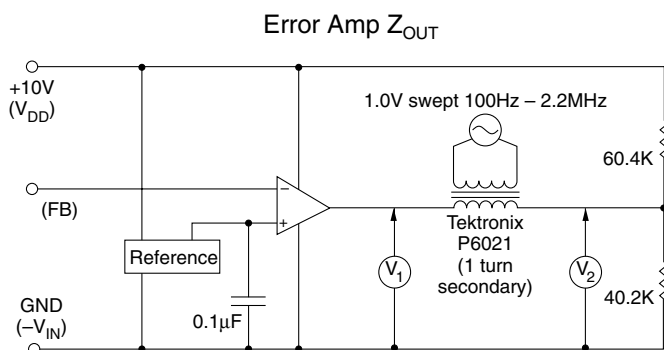


Pin number in parentheses are for PLCC package.

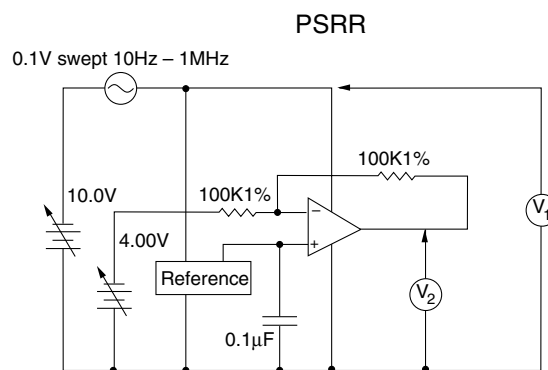
Typical Performance Curves



Test Circuits



NOTE: Set Feedback Voltage so that
 $V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer



Detailed Description

Preregulator

The preregulator/startup circuit for the HV912x consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the *effective* gate capacitance of the MOSFET being driven, i.e.,

$$C_{storage} \geq 100 \times (\text{gate charge of FET at } 10V \div 10V)$$

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytic capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV912x to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510KΩ to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is *not* required; $\pm 5\%$ is fine.

Clock Oscillator

The clock oscillator of the HV912x consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in

the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC In and OSC Out pins is required to set oscillator frequency (see graph). For the 50% maximum duty cycle versions the Discharge pin is internally connected to V_{SS} (ground). For the 99% duty cycle version, Discharge can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadline.

One difference exists between the Supertex HV912x and competitive 912x's: The oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV912x consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of -1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be.

A $\approx 50K\Omega$ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source $\leq 6.0V$. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV912x is not noisy, as some previous examples have been, overriding the reference should seldom be necessary.

Because the reference of the 912x is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Detailed Description (continued)

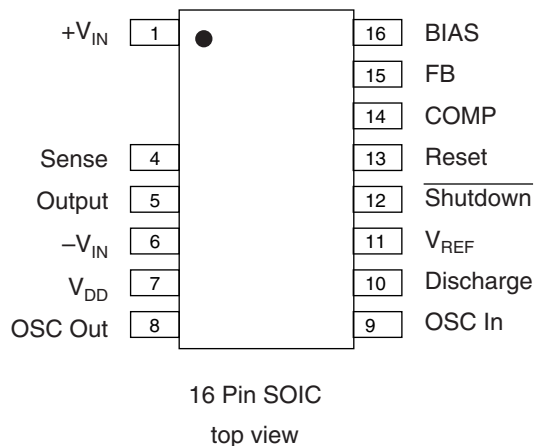
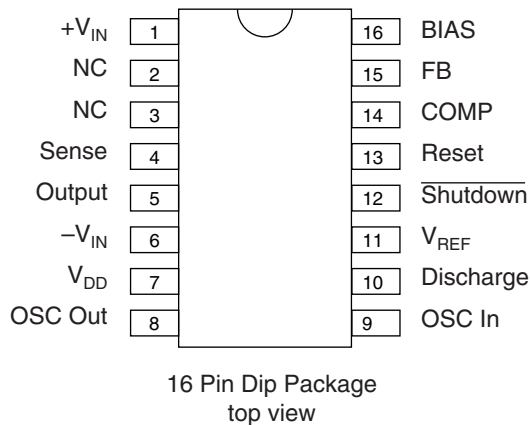
Error Amplifier

The error amplifier in the HV912x is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV912x uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

Pinout



Note: Pins 2 and 3 are removed

Remote Shutdown

The shutdown and reset pins of the HV912x can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

Output Buffer

The output buffer of the HV912x is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

