

Dual, High Voltage, Isolated MOSFET Driver

Features

- ▶ $\pm 400V$ input to output isolation
- ▶ $\pm 700V$ isolation between outputs
- ▶ No external voltage supply required
- ▶ Dual isolated output drivers
- ▶ Option of internal or external clock

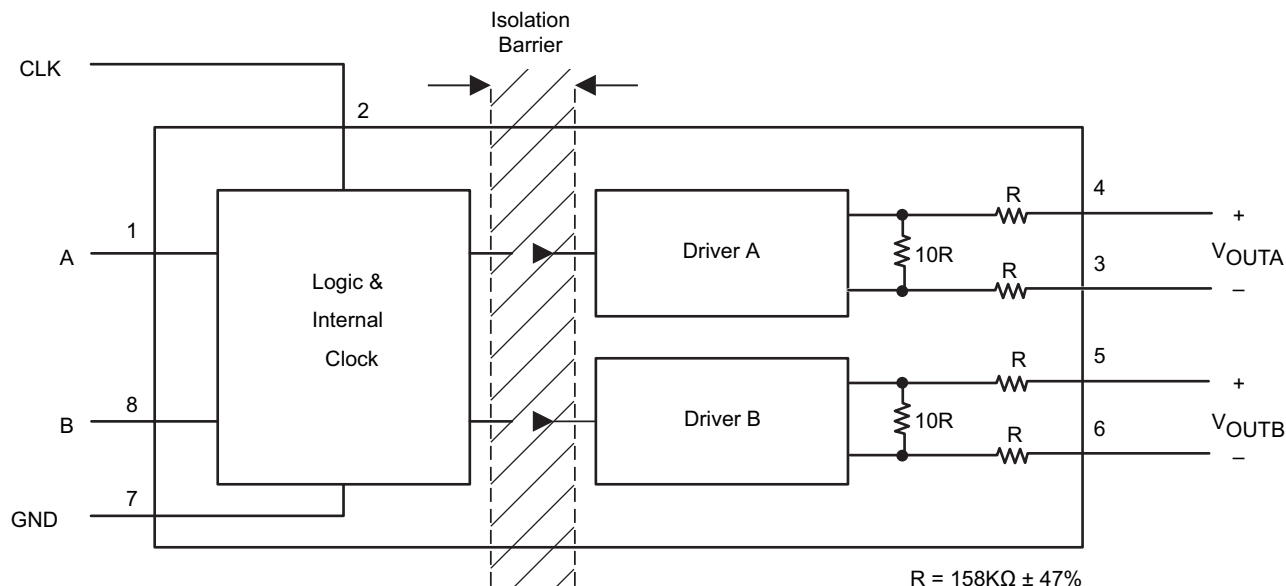
Applications

- ▶ Telecommunications
- ▶ Modems
- ▶ Solid state relays
- ▶ High side switches
- ▶ High end audio switches
- ▶ Avionics
- ▶ ATE

General Description

The Supertex HT0440 is a dual, high voltage, isolated MOSFET driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs configured as bi-directional or unidirectional switches. It can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC isolated voltages to the outputs, V_{OUTA} and V_{OUTB} when logic inputs A and B are at logic high. The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies, the internal supply voltage is supplied by either of the two logic inputs, A or B, when they are at logic high.

Block Diagram



Ordering Information

Device	Package Options	
	8-Lead SOIC (Narrow Body)	
HT0440	HT0440LG	HT0440LG-G

-G indicates package is RoHS compliant ('Green')



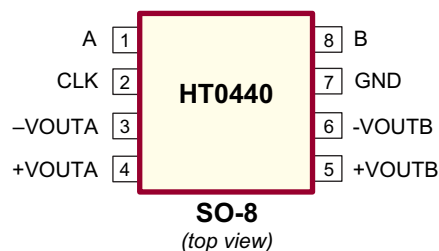
Absolute Maximum Ratings

Parameter	Value
Input to output isolation voltage, V_{ISO}	$\pm 400V$
Logic input voltage, V_A, V_B	-0.5 to +7.0V
Operating temperature	-40°C to +85°C
Storage temperature	-55°C to +150°C
Soldering temperature ¹	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note 1. Distance of 1.6mm from case for 10 seconds.

Pin Configuration



DC Electrical Characteristics ($T_J=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{HA} + I_{HB}$	Total logic high input current	-	-	300	μA	$V_A = 3.5V, V_B = 3.5V, CLK = 0V$
		-	-	500	μA	$V_A = 3.5V, V_B = 3.5V, CLK = 500KHz$
		-	-	2.0	mA	$V_A = 3.5V, V_B = 3.5V, CLK = 2.0MHz$
		-	-	1.0	mA	$V_A = 5.5V, V_B = 5.5V, CLK = 0V$
		-	-	2.0	mA	$V_A = 5.5V, V_B = 5.5V, CLK = 500KHz$
V_{OUTA}, V_{OUTB}	Output voltage	6.0	-	-	V	$V_A = 3.15V, V_B = 3.15V, CLK = 0V, no load$
		5.0	-	-	V	$V_A = 3.15V, V_B = 3.15V, CLK = 500KHz, no load$
		6.0	-	-	V	$V_A = 3.15V, V_B = 3.15V, CLK = 2.0MHz, no load$
		10.0	-	-	V	$V_A = 4.5V, V_B = 4.5V, CLK = 0V, no load$
		8.0	-	-	V	$V_A = 4.5V, V_B = 4.5V, CLK = 500KHz, no load$
I_{ILA}	Logic low input A current	-	-	10	μA	$V_A = 0.5V, V_B = high$
I_{ILB}	Logic low input B current	-	-	10	μA	$V_A = high, V_B = 0.5V$
I_{ILQ}	Quiescent current	-	-	10	μA	$V_A = 0.5V, V_B = 0.5V$
V_{ISO}	Input to output isolation voltage	± 400	-	-	V	---
V_{CISO}	Output to output isolation voltage	± 700	-	-	V	---

AC Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$t_{d(\text{ON})}$	Turn-on delay time	-	-	50	μs	See timing diagram and test circuit CLK = 0V, CL = 600pF
t_r	Rise time	-	-	650	μs	
$t_{d(\text{OFF})}$	Turn-off delay time	-	-	150	μs	
t_f	Fall time	-	-	3.0	ms	

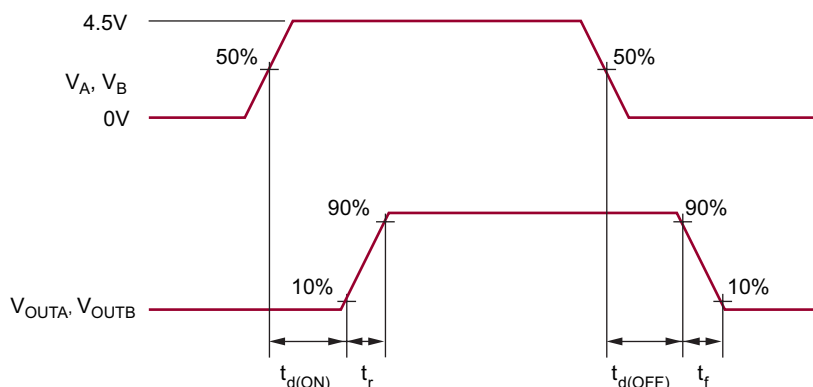
Recommended Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
CLK	External clock frequency	0.5	-	2.0	MHz	---
V_{IHCLK}	Clock input high voltage	3.15	-	5.5	V	---
V_{ILCLK}	Clock input low voltage	0	-	0.5	V	---
V_{IH}	Logic input high voltage	3.15	-	5.5	V	---
V_{IL}	Logic input low voltage	0	-	0.5	V	---
T_A	Operating temperature	-40	-	+85	$^\circ\text{C}$	---

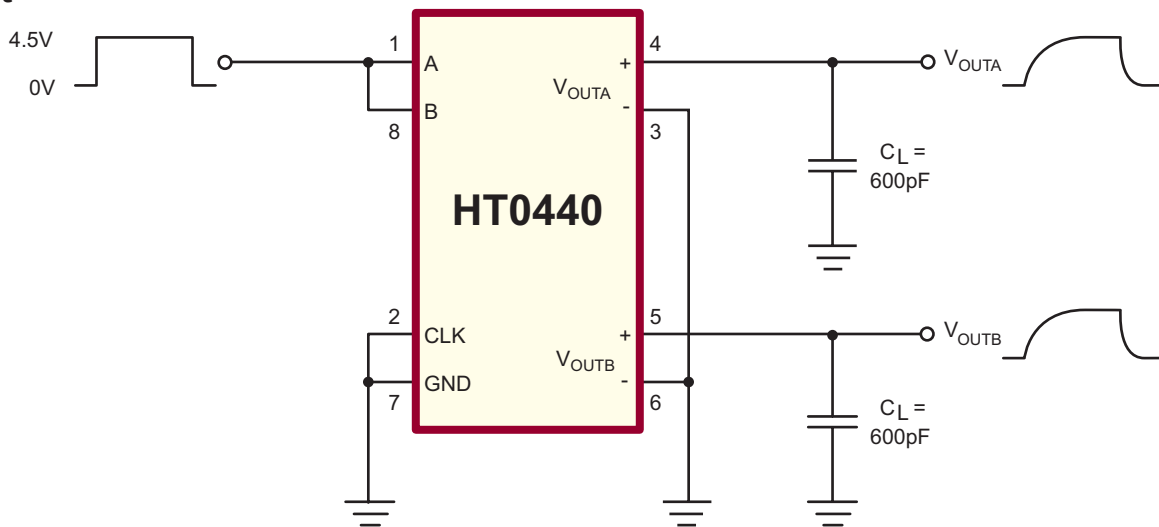
Truth Table

A	B	CLK	V_{OUTA}	V_{OUTB}	Internal Clock
0	0	0	Off	Off	Off
0	1	0	Off	On	On
1	0	0	On	Off	On
1	1	0	On	On	On
0	0	CLK	Off	Off	Off
0	1	CLK	Off	On	Off
1	0	CLK	On	Off	Off
1	1	CLK	On	On	Off

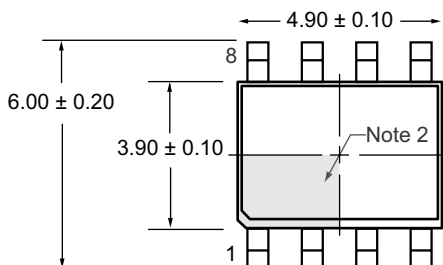
Timing Diagram



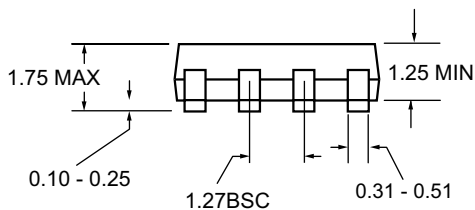
Test Circuit



8-Lead SOIC (Narrow Body) LG Package Outline



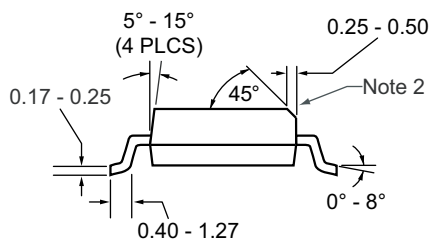
Top View



Side View

Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.



End View

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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