R&E International

RE46C109

Voltage Regulator, Voltage Converter and Piezoelectric Horn Driver

Product Specification

General Description

The RE46C109 is intended for use in applications where low voltage regulation and a high voltage horn driver are required. The circuit features a voltage boost converter/regulator and driver circuit suitable for driving a piezoelectric horn. The horn enable pin activates the boost converter and horn driver circuit. Supply current is 6.5uA maximum when the boost regulator and horn driver are not in use. A 3V regulator is also provided for microprocessor voltage regulation. Low battery detection and signaling are also available. Interconnect pins are provided to allow communication in multiple unit environments. A power good pin monitors the status of the regulator output.

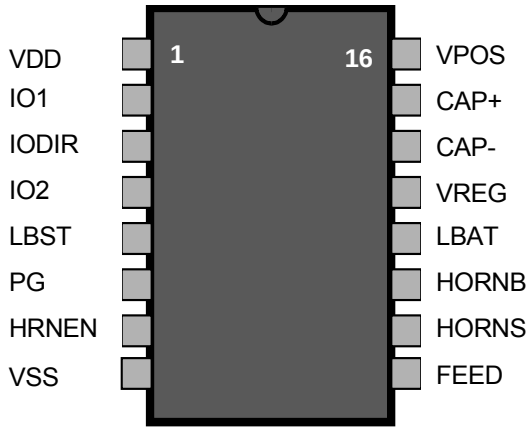
Applications

Smoke detectors
CO Detectors
Personal Security Products
Electronic Games
Hand Held Instruments

Features

- Low Quiescent Current
- 12V Boost Regulator
- Low Horn Driver Ron
- 3V Regulator, Other Options Available
- Low Battery Detection Interface
- Power Good and Brownout Circuits
- Device interconnection
- Available in DIP and SOIC packages
- Available in Standard Packaging or RoHS Compliant Pb Free Packaging

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{DD}	12	V
Input Voltage Range Except FEED, IO1, IO2	V_{in}	-.3 to V_{dd} +.3	V
FEED Input Voltage Range	V_{infd}	-10 to +22	V
IO2 Input Voltage Range	V_{io2}	-.3 to VREG+.3	V
IO1 (as input) Voltage Range	V_{io1}	-.3 to V_{dd} + 6	V
Input Current except FEED	I_{in}	10	mA
Operating Temperature	T_A	-40 to 85	°C
Continuous Operating Current (Horn or VPOS)	I_{con}	50	mA
Storage Temperature	T_{STG}	-55 to 125	°C
Maximum Junction Temperature	T_J	125	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation at these conditions for extended periods may affect device reliability.

This product utilizes CMOS technology with static protection; however proper ESD prevention procedures should be used when handling this product. Damage can occur when exposed to extremely high static electrical charges.

Electrical Characteristics at T_A=27°C, Vdd=9V, Vss=0V (unless otherwise noted).

Parameter	Symbol	Conditions	Limits			
			MIN	TYP	MAX	UNITS
Supply Voltage	Vdd	Operating	6		12	V
Quiescent Supply Current	Idd1	HRNEN, LBST, IODIR, FEED, REGSEL=VSS, No Loads		4.7	6.5	uA
Supply Current	Idd2	LBST, IODIR, FEED =VSS HRNEN=VDD, No Loads		350		uA
Input Leakage	Iin	All Inputs except FEED, Vin=VDD or VSS	-100		100	nA
	Iihf	FEED=+22V		20	50	uA
	Iilf	FEED=-10V	-50	-15		uA
Output Leakage	Iout	PG = 5.0v			1.0	uA
Input Voltage Low	Vil	All Inputs except FEED			1	V
Input Voltage High	Vih	All Inputs Except FEED	2.3			V
Output Low Voltage	Vol1	HORNB or HORNS; Iout=16mA;		.3	.5	V
	Vol2	IO2, Iout=100uA; IODIR=Vil , IO1=Vil		.3	.5	V
	Vol3	PG, Iout=5.0mA;		.5		V
Output High Voltage	Voh1	HORNB or HORNS; Iout=-16mA	Vpos-.5	Vpos-.3		V
	Voh2	IO2, Iout=-100uA; IODIR=Vil , IO1=Vih	Vreg -.5	Vreg -.3		V
VPOS RMS Output Voltage	V_{vpos}	VPOS; Iout=-16mA; HRNEN=VDD	10.7	11.8	12.7	V
Charge pump Oscillator Frequncy	CPf			150		kHz
Charge pump Power Efficiency	CPpe	VPOS; Iout=-16mA, C1=1uF C2=10uF; Vdd=6.5v		85		%
Charge pump Voltage Efficiency	CPve	VPOS; No Loads, C1=1uF C2=10uF; Vdd=6.0v	95	99		%
Low Battery Interface	Lbv	LBAT; LBST=Vdd	.17 *Vdd	.2*Vdd	.23*Vdd	V
VREG Voltage	Vreg	VREG; Iout<50mA; HRNEN=VSS	2.85	3	3.15	V
VREG Line Regulation	Vregln	VREG; Vdd=6V to 12V; VREG Iout=10mA; HRNEN = VSS; Note 3			50	mV
VREG Load Regulation	Vregld	VREG; Iout=0 to -50mA; HRNEN=VSS; Note 3			90	mV
Brownout Threshold	Vbvt	Falling Edge of VDD; Note 1	4.5	5.0	5.5	V
Brownout Pull Down Current	Ibt	Vdd=4.5V, Vreg=2v	15	25		mA

Electrical Characteristics at T_A=27°C, Vdd=9V, Vss=0V (unless otherwise noted).

Parameter	Symbol	Conditions	Limits			
			MIN	TYP	MAX	UNITS
VREG Over Voltage Clamp	Vcl	Iout>1mA; Note 2	3.7	4.0	4.3	V
VREG Over Voltage Clamp Current	Icl	VREG≥Vcl	0.5			mA
PG Trip Threshold	PGvtr	Vreg output rising	77	84	94	%Vreg
	PGvtf	Vreg output falling	72	80	88	%Vreg
PG Delay	PGtdly	Delay time with respect to PGvtr		500		usec
IO1 Output Current	IO1ih1	IODIR=Vil, IO1=Vdd-2V, Vdd=12V	25		60	UA
	IO1ih2	IODIR=Vil, IO1=17V, Vdd=12V			150	UA
	IO1ioh1	IODIR, IO2=Vih, Vdd=6.5V, IO1=4.5V	-4			mA
	IO1ioh2	IODIR, IO2=Vih, Vdd=12V, IO1=Vss			-16	mA
	IO1iol1	IO dump current IODIR= Vih, IO2=Vil, IO1=1V	10	15		mA
IO1 Alarm Voltage	IO1vih	IODIR=Vil	3			V
	IO1vil	IODIR=Vil			1.5	V

Unless noted the limits at room temperature are guaranteed and 100% production tested. Limits over temperature are guaranteed but not 100% tested.

Note 1: The brown-out threshold voltage is the Vdd voltage at which the regulator will be disabled and VREG (output) will be pulled to Vss.

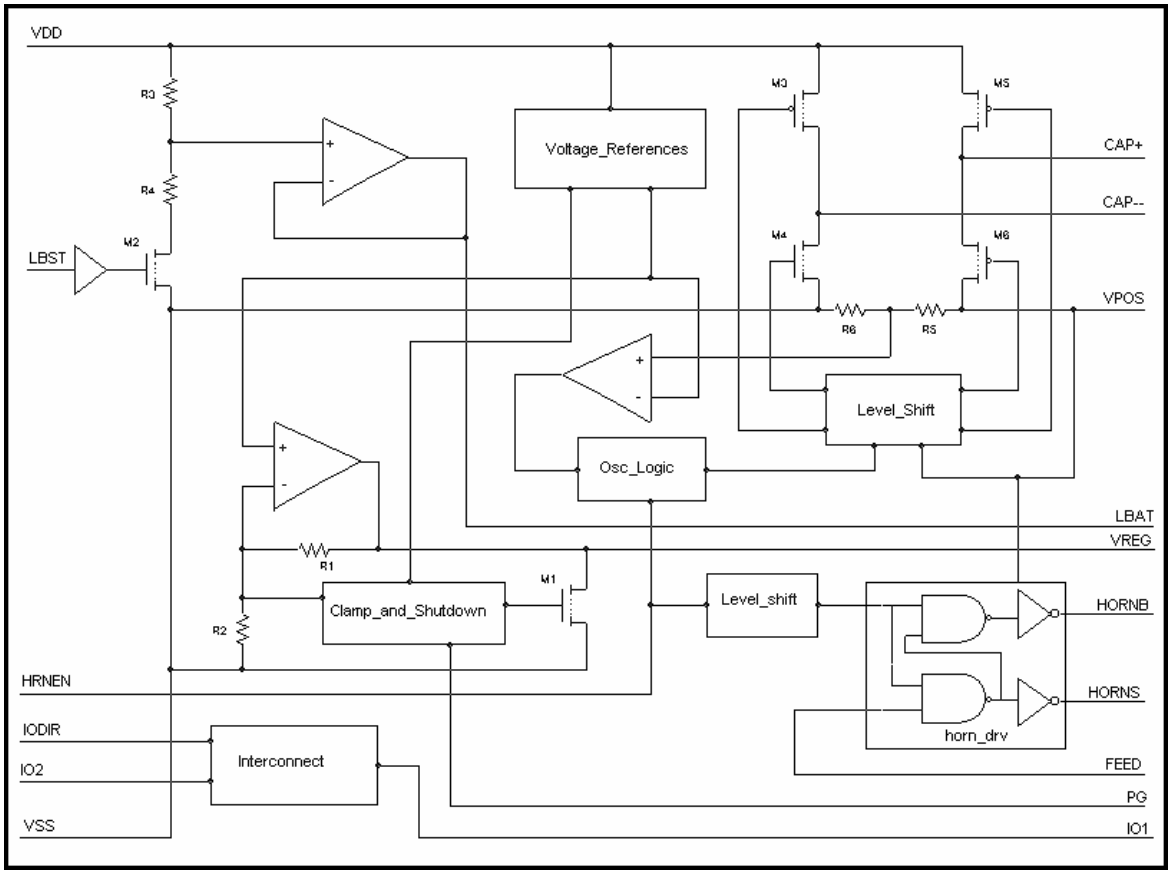
Note 2: In normal operation, the regulator will provide high-side current of up to 50mA, but current sinking capability is typically under 1uA. The overvoltage clamp, Vcl is intended to limit the voltage at VREG (output) when it is pulled up by an external source.

Note 3: Not 100% production tested but limits are guaranteed by design.

Interconnect Logic Truth Table

IODIR (pin 3)	IO2 (pin 4)		IO1 (pin 2)	
	Input	Output	Input	Output
1	0			0
1	1			1
0		0	0	
0		1	1	

Functional Block Diagram



PIN DESCRIPTIONS

VDD (Pin 1, Input) - Connect to the positive terminal of the supply voltage for the voltage regulator, charge pump voltage converter and bi-directional Interconnect block.

IO1 (Pin 2, Input/Output) - This bi-directional pin provides an interface to additional RE46C109 IO1 pins. This serves as a communication link between separate modules.

IODIR (Pin 3, Input) - This input provides control for the bi-directional pins IO1 and IO2.

IO2 (Pin 4, Input/Output) - This bi-directional pin provides an interface to a TTL/CMOS I/O of a *u*P or ASIC. Refer to the interconnect logic truth table.

LBST (Pin 5, Input) - This input provides an enable or strobe control for the analog low battery detection function.

PG (Pin 6, Output) - This open drain NMOS output provides a status indication of when the VREG output is above or below a specified voltage level.

HRNEN (Pin 7, Input) - This input provides activation control for the charge pump boost regulator and horn driver outputs.

VSS (Pin 8, Input) - This power pin is connected to the negative terminal of the supply voltage.

FEEDBACK (Pin9, Input) - Horn driver input.

HORNS (Pin10, Output) - Horn output driver which provides VPOS to VSS output voltage swing for the piezoelectric horn.

HORNB (Pin11, Output) - Horn output driver which provides VPOS to VSS output voltage swing for the piezoelectric horn.

LBAT (Pin12, Output) - Analog output voltage that is proportional to the VDD supply and functions as a low battery detection output.

VREG (Pin13, Output) - Voltage regulator output, requires an external capacitor.

VCAP- (Pin14, I/O) - Negative terminal for the external charge pump boost (fly) capacitor.

VCAP+ (Pin 15, I/O) - Positive terminal for the external charge pump boost (fly) capacitor.

VPOS (Pin 16, Output) - This output pin requires an external filter capacitor which supplies voltage for the horn driver outputs.

Device Operation

(Please refer to the functional block diagram)

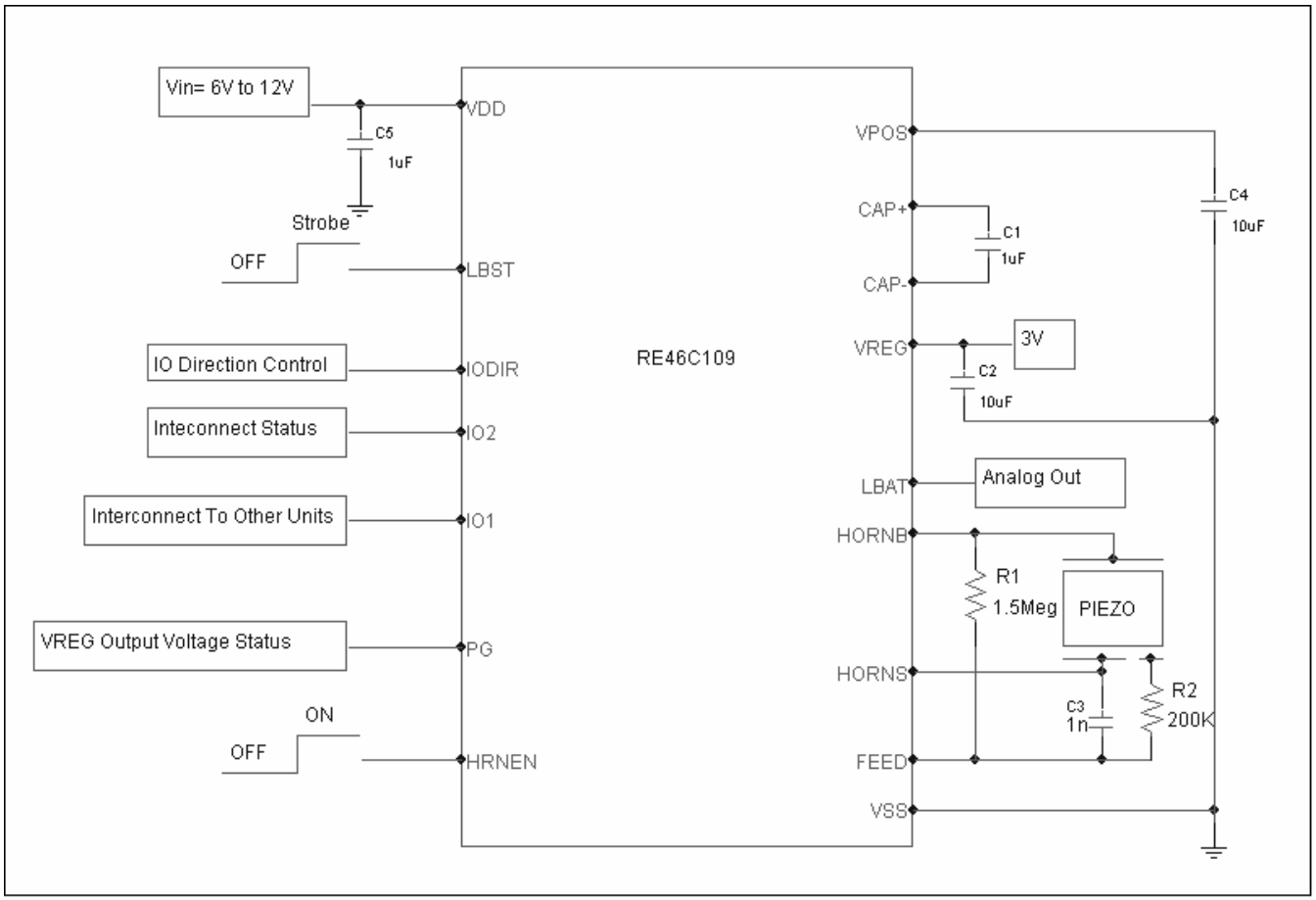
The RE46C109 consists of the following main functional blocks: band gap voltage reference, low drop-out voltage regulator (with over voltage clamp and power supply brownout protection), low battery detection, switched capacitor 12 volt boost regulator, horn driver and Interconnect logic.

When power is applied the band gap voltage reference and the voltage regulator output are initially enabled. The low battery detection, horn driver outputs and switched capacitor 12v boost regulator are enabled by TTL compatible positive logic control inputs.

When the HRNEN (Horn Enable) input is brought to a logic high level, the horn driver outputs as well as the 12v boost regulator become active. The 12v boost regulator supplies the horn driver outputs. The 12v boost regulator utilizes a charge pump to boost the Vdd supply input to a regulated 12-volt output. The charge pump consists of an internal oscillator that is controlled in a voltage comparator feedback configuration.

The low battery detection is enabled and strobed when the LBST input is brought to a logic high level. The LBAT output is a voltage follower amplifier whose input is determined by a resistor divider across the device supply rails.

Typical Application Circuit



Application Notes:

(see application circuit)

The efficiency of the switched capacitor charge pump regulator varies with the applied input voltage and the load current. The approximate voltage efficiency is given by:

$$\text{Efficiency (\%)} = [\text{VPOS}/(2\text{xVDD})]\text{x}100$$

Application Notes cont'd:

(see application circuit)

Capacitor Selection:
To achieve minimum output voltage ripple, the output capacitor C_4 (for VPOS) should have a low ESR (Effective Series Resistance) value with leads kept as short as possible. Capacitors with long leads increase ripple voltage due to lead inductance.

Like all Low-Dropout Regulators, the RE46C109 requires an output capacitor connected between VREG (output) and VSS to stabilize the internal control loop. The recommended capacitance is 10*u*F. Capacitor values larger than 10*u*F are acceptable.

PCB Layout Suggestions:
Due to large transient currents flow in the V_{DD}, V_{POS} and V_{SS} terminals, minimizing both input and output ripple is accomplished by placing capacitors as close as possible to the regulator using short direct circuit wiring or traces.