R&E International

RE46C107

DC to DC Converter, Voltage Regulator and Piezoelectric Horn Driver

Product Specification

General Description

The RE46C107 is intended for use in 3V or 4.5V battery or battery-backed applications. The circuit features a DC-to-DC up-converter and driver circuit suitable for driving a piezoelectric horn. A selectable 3.0V or 3.3V regulator is also provided for microprocessor voltage regulation. An LED driver and low battery detection and signaling are also available.

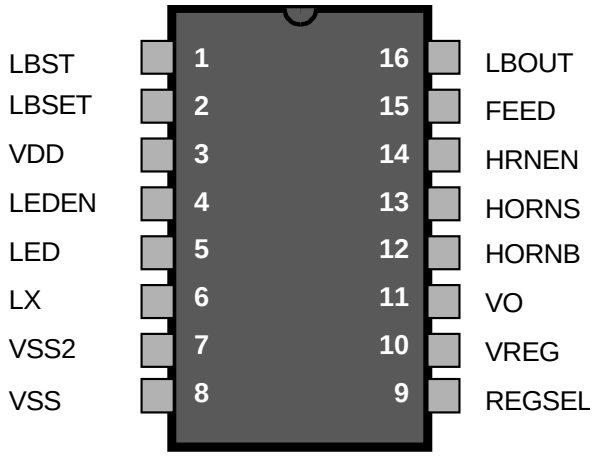
Applications

Smoke detectors
CO Detectors
Personal Security Products
Electronic Toys

Features

- Low Quiescent Current
- 10V Up Converter
- Low Horn Driver Ron
- Voltage Regulation to 3.0V or 3.3V
- Low Battery Detection
- Available in Standard Packaging or RoHS Compliant Pb Free Packaging

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{DD}	5	V
	V_{OUT}	12	V
Input Voltage Range Except REGSEL & FEED	V_{in}	-.3 to V_{reg} +.3	V
REGSEL Input Voltage Range	V_{inrs}	-.3 to V_{dd} +.3	V
FEED Input Voltage Range	V_{infd}	-10 to +22	V
Input Current except FEED	I_{in}	10	mA
Operating Temperature	T_A	0 to 50	°C
Storage Temperature	T_{STG}	-55 to 125	°C
Continuous Operating Current (HornS, HornB, Vreg, VO)	I_O	40	mA

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation at these conditions for extended periods may affect device reliability.

This product utilizes CMOS technology with static protection; however proper ESD prevention procedures should be used when handling this product. Damage can occur when exposed to extremely high static electrical charge

PIN DESCRIPTIONS

PIN#	PIN NAME	DESCRIPTION
1	LBST	Logic input used to activate low battery detection circuitry. Input is designed to interface with circuitry supplied by Vreg, so input voltage levels will scale with the Vreg voltage. Input is disabled during brown-out.
2	LBSET	Internally connected to the low battery comparator input used to sense the Vdd voltage divider. The internal reference to which this node is compared is nominally 0.9V. Nominal internal resistance to Vdd is 400kohm. Nominal resistance to Vss is 240kohm. The resistance to Vss is changed to a nominal of 220kohm once a low battery condition is detected. External resistances can be added in parallel to adjust the low battery threshold voltage.
3	VDD	Connect to the positive supply voltage
4	LEDEN	Logic input used to enable the LED driver. Input is designed to interface with circuitry supplied by Vreg, so input voltage levels will scale with the Vreg voltage. LED driver is disabled during brown-out.
5	LED	Open drain NMOS output used to drive a visible LED.
6	LX	Open drain NMOS output used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low resistance path.
7	VSS2	Internally connected to the source of the NMOS device used to drive the boost converter inductor. Connect to the negative supply voltage through a low resistance path.
8	VSS	Connect to the negative supply voltage.
9	REGSEL	Logic input used to set the Vreg output voltage level. This input should always be tied to either Vdd or Vss.
10	VREG	Regulated output voltage. Nominal output is 3.3V for REGSEL=Vdd and 3.0V for REGSEL=Vss.
11	VO	Boosted voltage produced by DC-DC converter, typically 4V or 10V.
12	HORNB	This pin is connected to the metal electrode (B) of a piezoelectric transducer.
13	HORNS	HS is a complementary output to HB and connects to the ceramic electrode (S) of the piezoelectric transducer.
14	HRNEN	Logic input for horn enable designed to interface with circuitry supplied by Vreg. Input voltage levels will scale with the Vreg voltage. Horn is disabled during brown-out.
15	FEED	Usually connected to the feedback electrode of the piezoelectric horn through a current limiting resistor. If not used, this pin must be connected to Vss.
16	LBOUT	Logic output used to signal a low battery condition. Output pulls to Vreg when LBST is high and a low battery condition is detected.

Electrical Characteristics

Limits apply at Vdd=3V, Vss=Vss2=0V, Creg=10uF, Cvo=10uF, T_A=0°C to 50°C, unless otherwise noted.
Typical values are at T_A=27°C.

Parameter	Symbol	Test Pin	Test Conditions	Limits Min	Limits Typ	Limits Max	Units
Supply Voltage	Vdd	3	Operating	2.0		5.0	V
Standby Supply Current	Iddstby		Inputs low; LBSET open; No loads; DC-DC Running		20		uA
Quiescent Supply Current	Iddq	3	Inputs low; LBSET open; No loads; VO=5V; Vlx=0.5V		7		uA
Quiescent Ivo	Ivoq	10	Same conditions as above for Iddq		9		uA
Input Leakage Low	Iil	1, 4, 14	LBST, LEDEN, HRNEN Inputs Vin= VSS			-100	nA
	Iilrs	9	REGSEL Input Vin= Vss			-100	nA
	Iilf	15	FEED=-10V; VO=10V		-15	-50	uA
Input Leakage High	Iih	1, 4, 14	LBST, LEDEN, HRNEN Inputs Vin=Vreg			100	nA
	Iihrs	9	REGSEL Input Vin=Vdd			100	nA
	Iihf	15	FEED=+22V; VO=10V		20	50	uA
Input Voltage Low	Vil	1, 4, 14	LBST, LEDEN, HRNEN Inputs			1	V
	Vilrs	9	REGSEL Input			1	V
	Vilf	15	FEED Input; VO=10V			3	V
Input Voltage High	Vih	1, 4, 14	LBST, LEDEN, HRNEN Inputs	Vreg-.7			V
	Vihrs	9	REGSEL Input	2.3			V
	Vihf	15	FEED Input; VO=10V	7			V
Output Low Voltage	Vol1	12,13	HORNB or HORNS; Iout=16mA; Vdd=3V; VO=10V		.3	.5	V
	Vol2	5	LED; Iout=10mA; VO=4V		.3	.5	V
	Vol3	16	LBOUT; Iout=100uA; Vdd=3V		.3	.5	V
Output High Voltage	Voh1	12,13	HORNB or HORNS; VO=10V; Iout=-16mA; HRNEN=Vreg	9.5	9.7		V
	Voh3	16	LBOUT; Iout=100uA; Vdd=2.1V	Vreg-.5	Vreg-.3		V
VO Output Voltage	Vvo1	11	Vdd=3V; HRNEN=Vreg; Iout=10mA		10		V
	Vvo2	11	Vdd=3V; HRNEN=0V; Iout=10mA		4		V

Electrical Characteristics (continued)

Limits apply at Vdd=3V, Vss=Vss2=0V, Creg=10uF, Cvo=10uF, T_A=0°C to 50°C, unless otherwise noted.
Typical values are at T_A=27°C.

Parameter	Symbol	Test Pin	Test Conditions	Limits Min	Limits Typ	Limits Max	Units
VO Efficiency	Voeff1		Iload= 10mA, Vdd=3V; HRNEN=0V		85		%
	Voeff2		Iload=100uA; Vdd=3V; HRNEN=0V		75		%
Low Battery Threshold	Vlbat	3	LBST=Vreg		2.4		V
LBST to LBOUT Propagation Delay	Tplhlb	16	Vdd=2.1; LBSET Cload=5pF		30		us
VREG Voltage	Vreg1	10	Iout<20mA; REGSEL=Vdd	3.1	3.3	3.5	V
	Vreg2	10	Iout<20mA; REGSEL=Vss	2.8	3.0	3.2	V
VREG Load Regulation	Vregld1	10	Iout=0 to 20mA; HRNEN=Vreg		50		mV
	Vregld2	10	Iout=0 to 20mA; HRNEN=0V		50		mV
Brownout Threshold	Vobvt	11	Falling edge of VO		3.6		V
VO-to-Brownout Margin	Vobvtm	11	Vv02 -Vobvt	100	400		mV
Brownout Pull down	Ibt	10	VO=3.0V; Vreg=2.0V	20	40		mA
VREG over voltage clamp	Vcl1	10	REGSEL=Vdd	3.75	4	4.25	V
	Vcl2	10	REGSEL=0V	3.35	3.6	3.85	V

Notes on Electrical Characteristics:

1/ DC-DC converter in high boost mode (nominal VO=10V) can draw current pulses of greater than 1 Amp and is therefore very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to the LX pin and from the Vss2 pin to the battery. In order to function properly under full load at Vdd=2V, the total of the inductor and interconnect resistances should not exceed 0.3 ohm. The internal battery resistance should be no more than 0.5 ohm and a low ESR capacitor of 10uF or more should be connected in parallel with the battery to average current draw over the boost converter cycle.

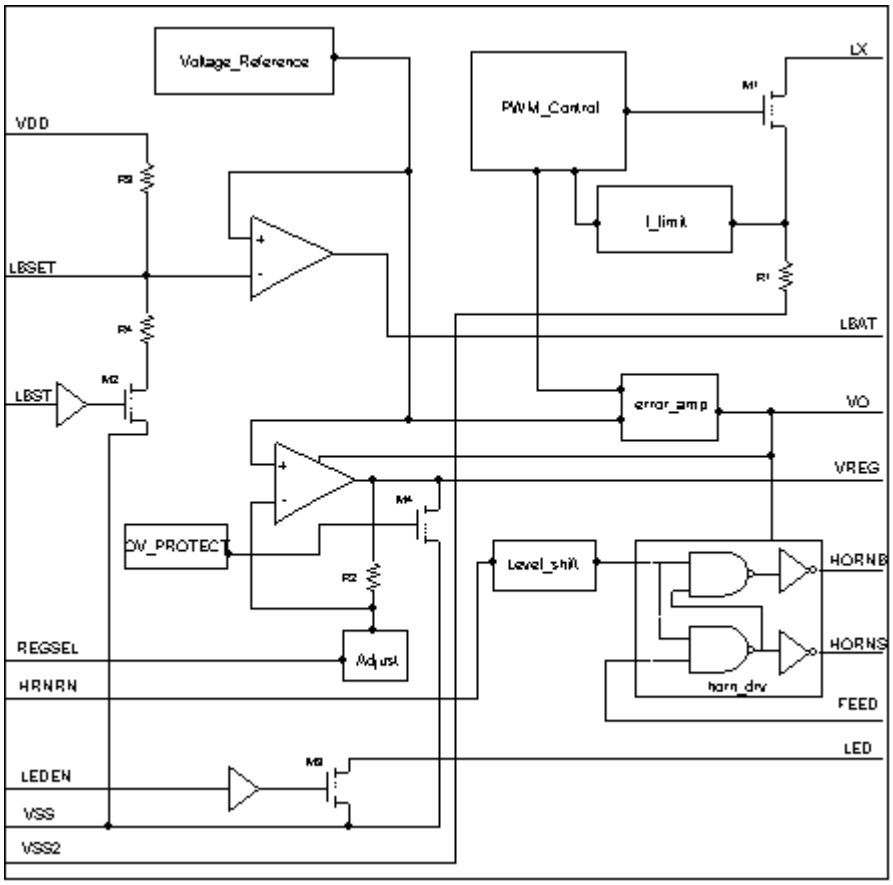
2/ In the Electrical Characteristics Table, wherever a specific VO value is listed under test conditions, the VO is forced externally with the inductor disconnected and the DC-DC converter is NOT running.

3/ The brown-out threshold voltage is the VO voltage at which the regulator and horn will be disabled. At VO voltages below the brown-out threshold Vreg will be pulled to Vss.

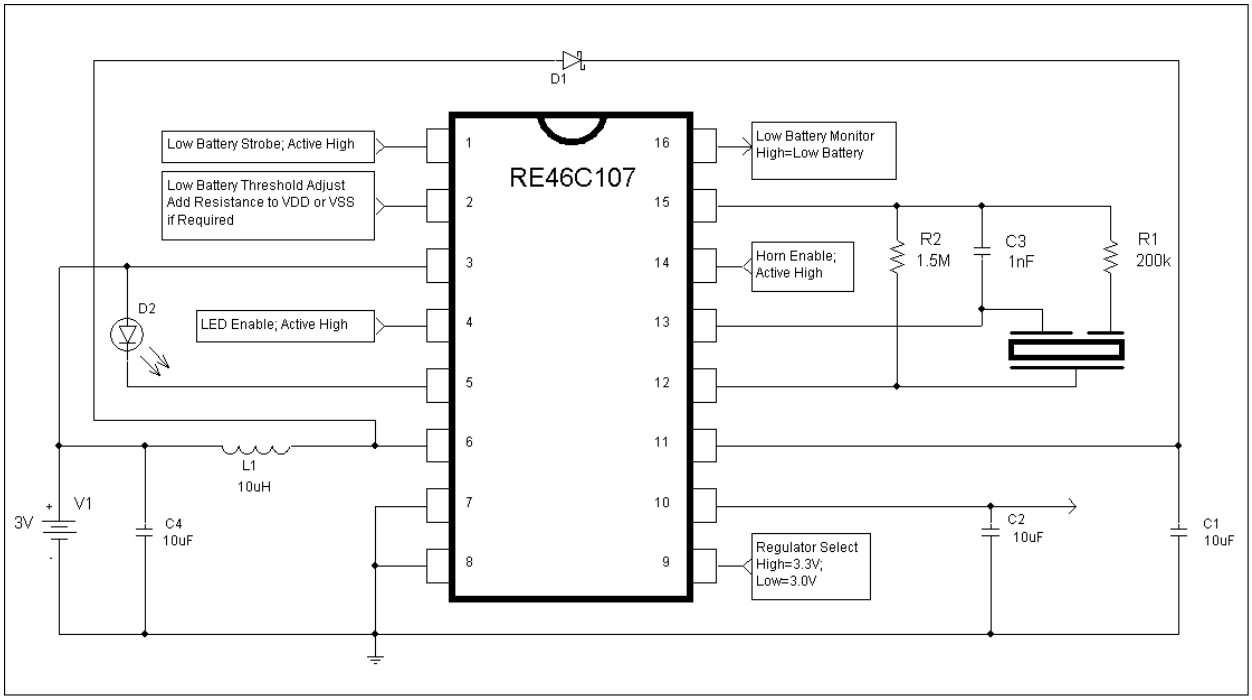
4/ In normal operation, the regulator will provide high-side current of up to 20mA, but current sinking capability is typically under 1uA. The overvoltage clamp is intended to limit the voltage at Vreg when it is pulled up by an external source.

5/ The limits shown are 100% tested at 25C only. Test limits are guard-banded based on temperature characterization to guarantee compliance at temperature extremes.

Functional Block Diagram



Typical Application Circuit



Notes:

1/ Schottky diode D1 must have maximum peak current rating of at least 1.5A and for best results should have forward voltage spec of less than 0.5V at 1 Amp.

2/ Inductor L1 must have maximum peak current rating of at least 1.5A and for best results should have DC resistance of less than 0.3 ohm.

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