

CRYSTAL CONTROLLED OSCILLATORS

SURFACE MOUNT 3.3V PECL CLOCK



EML5113

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-55	-	125	°C	
Supply Voltage	(Vcc)	-0.5	-	7.0	Vdc	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Center Frequency	(Fo)	19.44	-	164	MHz	
Total Frequency Tolerance		-25	-	25	ppm	1
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	-	60	mA	
Jitter (BW=10Hz to 20MHz)		-	-	5	ps rms	
Jitter (BW=12kHz to 20MHz)		-	-	1	ps rms	
SSB Phase Noise at 10Hz offset		-	-60	-	dBc/Hz	
SSB Phase Noise at 100Hz offset		-	-90	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-100	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-125	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-135	-	dBc/Hz	

PECL OUTPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	2
Voltage (High)	(Voh)	2.275	-	-	Vdc	
(Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle		45	50	55	%	3
Rise / Fall Time 20% to 80%		-	-	1	nS	

PACKAGE CHARACTERISTICS

TABLE 4.0

Package	Hermetically sealed, leadless ceramic package.
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Notes

- 1) Includes calibration, stability vs. temperature, supply and load variations, shock, vibration and aging (10 years).
- 2) Output must be terminated into 50 ohms to Vcc - 2V or Thevenin equivalent.
- 3) Duty Cycle measured at 1.977V

DESCRIPTION

The Connor-Winfield EML5113 is a fixed frequency surface mount Crystal Controlled Oscillator (XO) designed for applications requiring low jitter and tight Frequency stability. Operating at 3.3V supply voltage, the EML5113 provides LVPECL compatible outputs.

FEATURES

- 3.3V OPERATION
- LVPECL DIFFERENTIAL OUTPUTS
- LOW JITTER <1pS RMS
- OVERALL FREQUENCY TOLERANCE: ±25ppm
- TEMPERATURE RANGE: 0 to 70°C
- SURFACE MOUNT PACKAGE
- TAPE AND REEL PACKAGING

ORDERING INFORMATION

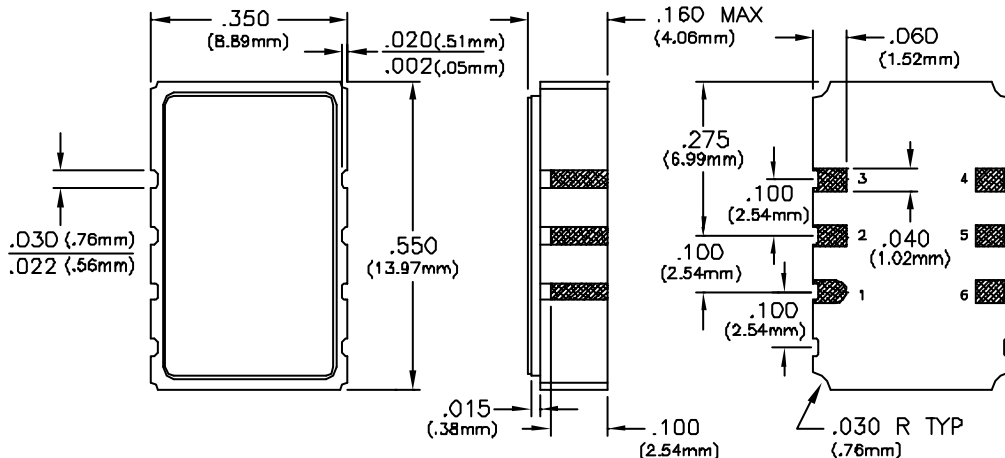
EML5113 - 125.00MHz

PECL
SERIES

CENTER
FREQUENCY

Specifications subject to change without notice.

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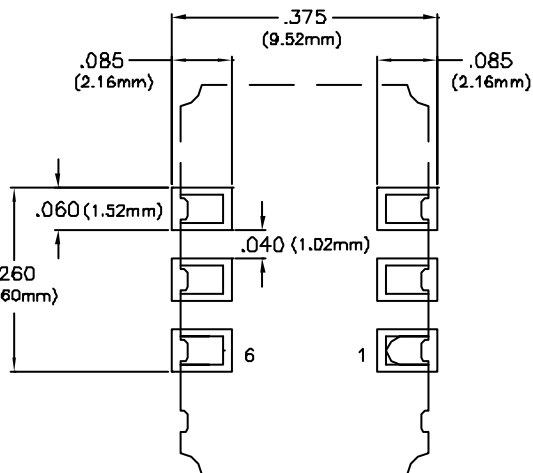
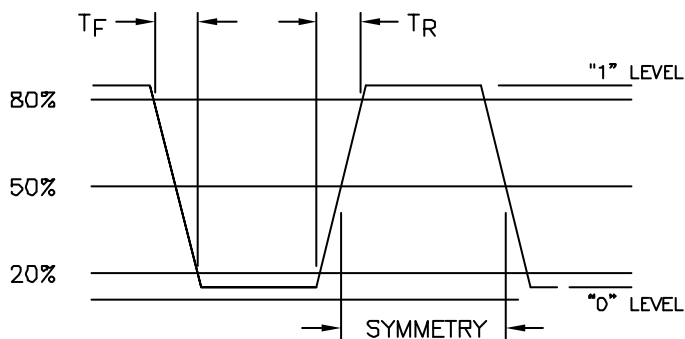


PIN	CONNECTION
1	Q̄ OUTPUT
2	N/C
3	GND
4	Q OUTPUT
5	N/C
6	Vcc

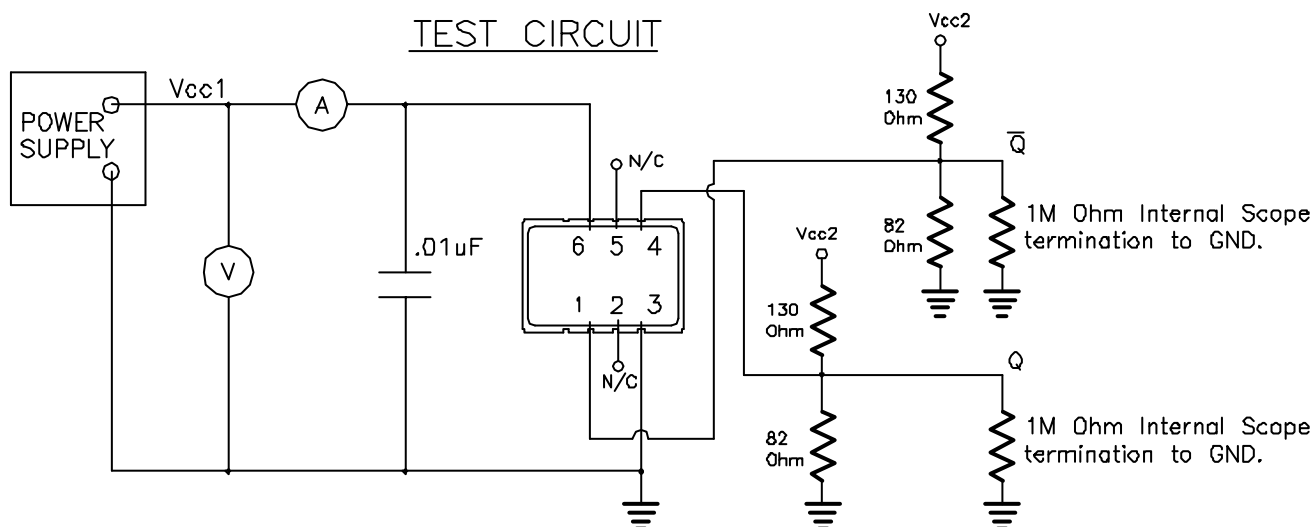
NOTE 1: Metal cover is tied to pin 3

NO LEADS SUGGESTED PAD LAYOUT

OUTPUT WAVEFORM



TEST CIRCUIT



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