### **DISCRETE SEMICONDUCTORS**

### DATA SHEET

**PEMD10**; **PUMD10** NPN/PNP resistor-equipped transistors; R1 = 2.2 kΩ, R2 = 47 kΩ

Product specification Supersedes data of 2003 Nov 04 2004 Apr 15





TYP. MAX. UNIT

 $\mathsf{k}\Omega$ 

### NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

PEMD10; PUMD10

### **FEATURES**

- Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- · Reduces pick and place costs.

### **APPLICATIONS**

- · Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- · Control of IC inputs.

V <sub>CEO</sub>	collector-emitter voltage	_	50	V
I <sub>O</sub>	output current (DC)	_	100	mA
TR1	NPN	_	_	_
TR2	PNP	_	_	_
R1	bias resistor	2.2	_	kΩ

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**PARAMETER** 

bias resistor

QUICK REFERENCE DATA

SYMBOL

R2

### **DESCRIPTION**

NPN/PNP resistor-equipped transistors (see "Simplified outline, symbol and pinning" for package details).

### **PRODUCT OVERVIEW**

TYPE NUMBER	PAC	KAGE	MARKING CODE	PNP/PNP	NPN/NPN
TIPE NOWBER	PHILIPS	EIAJ	WARKING CODE	COMPLEMENT	COMPLEMENT
PEMD10	SOT666	_	D1	PEMB10	PEMH10
PUMD10	SOT363	SC-88	D*0 <sup>(1)</sup>	PUMB10	PUMH10

### Note

- 1. \* = p: Made in Hong Kong.
  - \* = t: Made in Malaysia.
  - \* = W: Made in China.

### SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL		PINNING
I TPE NUMBER	SIMPLIFIED OUTLINE AND STMBOL	PIN	DESCRIPTION
PEMD10; PUMD10	6 5 4	1	emitter TR1
	6 5 4	2	base TR1
	R1 R2	3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1
	1 2 3		
	1 2 3 Top view MAM448		
	·		

### NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

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### **ORDERING INFORMATION**

TYPE NUMBER		PACKAGE	
NAME		DESCRIPTION	VERSION
PEMD10	<ul> <li>plastic surface mounted package; 6 leads</li> </ul>		SOT666
PUMD10	plastic surface mounted package; 6 leads		SOT363

### **LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor;	for the PNP transistor with negative	polarity		•	
V <sub>CBO</sub>	collector-base voltage	open emitter	_	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	_	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	_	10	V
VI	input voltage TR1				
	positive		_	+12	V
	negative		_	-5	V
VI	input voltage TR2				
	positive		_	+5	V
	negative		_	-12	V
Io	output current (DC)		-	100	mA
I <sub>CM</sub>	peak collector current		_	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C;	_	_	
	SOT363	note 1	_	200	mW
	SOT666	notes 1 and 2	_	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T <sub>amb</sub>	operating ambient temperature		-65	+150	°C
Per device	•	•	'	•	•
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C;	_	_	
	SOT363	note 1	_	300	mW
	SOT666	notes 1 and 2	_	300	mW

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### **Notes**

- 1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
- 2. Reflow soldering is the only recommended soldering method.

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# NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transis	stor			
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient			
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device	•	•		
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient			
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

### Notes

- 1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
- 2. Reflow soldering is the only recommended soldering method.

# NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

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### **CHARACTERISTICS**

 $T_{amb}$  = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transis	stor; for the PNP transistor with ne	gative polarity				
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	_	_	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	_	_	1	μΑ
		$V_{CE} = 30 \text{ V}; I_{B} = 0 \text{ A}; T_{j} = 150 ^{\circ}\text{C}$	_	_	50	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	_	_	180	μΑ
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 10 mA	100	_	_	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}$	_	_	100	mV
V <sub>i(off)</sub>	input-off voltage	$V_{CE} = 5 \text{ V}; I_{C} = 100 \mu\text{A}$	_	0.6	0.5	V
V <sub>i(on)</sub>	input-on voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 5 mA	1.1	0.75	_	V
R1	input resistor		1.54	2.2	2.86	kΩ
R2 R1	resistor ratio		17	21	26	
C <sub>c</sub>	collector capacitance					
	TR1 (NPN)	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	_	_	2.5	pF
	TR2 (PNP)		_	_	3	pF

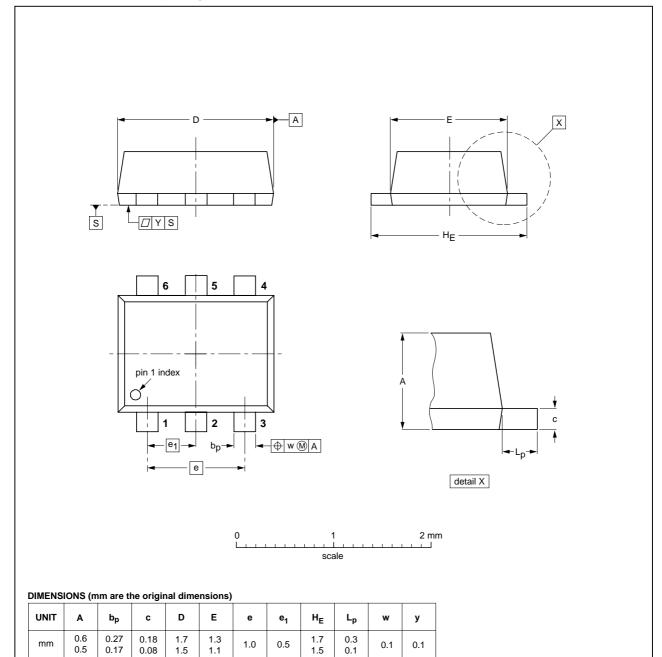
# NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

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### **PACKAGE OUTLINES**

### Plastic surface mounted package; 6 leads

SOT666



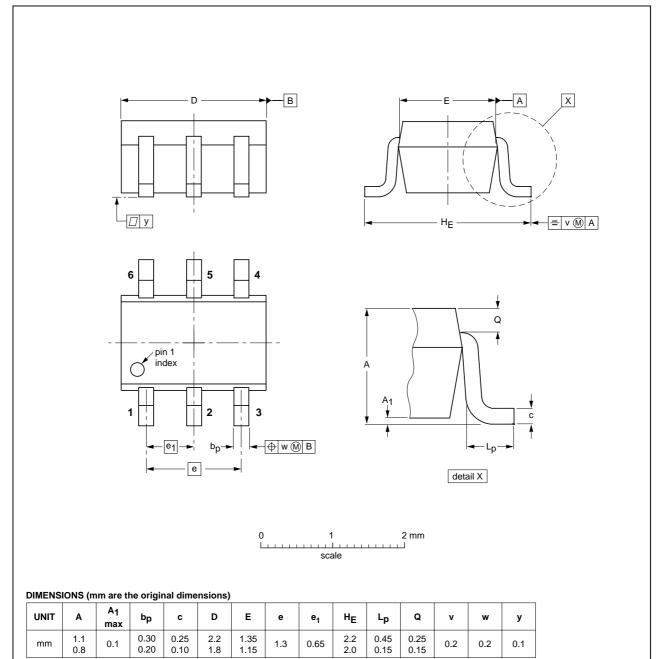
OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT666						<del>-01-01-04</del> 01-08-27

# NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

PEMD10; PUMD10

### Plastic surface mounted package; 6 leads

**SOT363** 



OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT363			SC-88			97-02-28

### NPN/PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

PEMD10; PUMD10

#### **DATA SHEET STATUS**

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