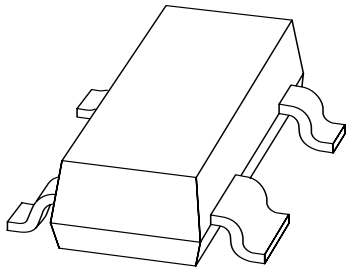


DATA SHEET



BCV62 PNP general purpose double transistor

Product specification
Supersedes data of 1997 Jun 18

1999 Apr 08

PNP general purpose double transistor

BCV62

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 30 V)
- Matched pair.

APPLICATIONS

- For use in applications where the working point must be independent of temperature
- Current mirrors.

DESCRIPTION

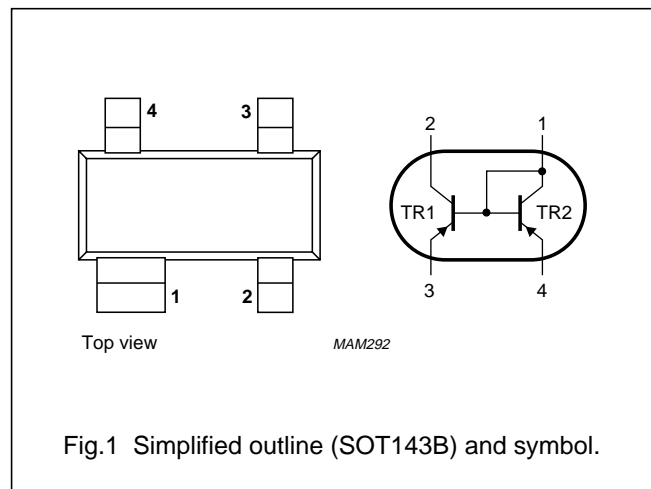
PNP double transistor in a SOT143B plastic package.
NPN complement: BCV61.

MARKING

TYPE NUMBER	MARKING CODE	TYPE NUMBER	MARKING CODE
BCV62	3Mp	BCV62B	3Kp
BCV62A	3Jp	BCV62C	3Lp

PINNING

PIN	DESCRIPTION
1	collector TR2; base TR1 and TR2
2	collector TR1
3	emitter TR1
4	emitter TR2



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage TR1	open emitter	–	–30	V
V_{CEO}	collector-emitter voltage TR1	open base	–	–30	V
V_{EBS}	emitter-base voltage	$V_{CE} = 0$	–	–6	V
I_C	collector current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–200	mA
I_{BM}	peak base current TR1		–	–200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

PNP general purpose double transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transistor TR1						
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -30\text{ V}$	–	–	–15	nA
		$I_E = 0; V_{CB} = -30\text{ V}; T_j = 150\text{ °C}$	–	–	–5	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -5\text{ V}$	–	–	–100	nA
h_{FE}	DC current gain	$I_C = -100\text{ }\mu\text{A}; V_{CE} = -5\text{ V}$	100	–	–	
		$I_C = -2\text{ mA}; V_{CE} = -5\text{ V}$	100	–	800	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}$	–	–75	–300	mV
		$I_C = -100\text{ mA}; I_B = -5\text{ mA}$	–	–250	–650	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}; \text{note 1}$	–	–700	–	mV
		$I_C = -100\text{ mA}; I_B = -5\text{ mA}; \text{note 1}$	–	–850	–	mV
V_{BE}	base-emitter voltage	$I_C = -2\text{ mA}; V_{CE} = -5\text{ V}; \text{note 1}$	–600	–650	–750	mV
		$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}; \text{note 2}$	–	–	–820	mV
C_C	collector capacitance	$I_E = I_E = 0; V_{CB} = -10\text{ V}$	–	4.5	–	pF
f_T	transition frequency	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	100	–	–	MHz
F	noise figure	$I_C = -200\text{ }\mu\text{A}; V_{CE} = -5\text{ V}; R_S = 2\text{ k}\Omega;$ $f = 1\text{ kHz}; B = 200\text{ Hz}$	–	–	10	dB
Transistor TR2						
V_{EBS}	base-emitter forward voltage	$I_E = 250\text{ mA}; V_{CB} = 0$	–	–	1.5	V
		$I_E = 10\text{ }\mu\text{A}; V_{CB} = 0$	400	–	–	mV
h_{FE}	DC current gain	$I_C = -2\text{ mA}; V_{CE} = -5\text{ V}$	125	–	250	
			220	–	475	
			420	–	800	

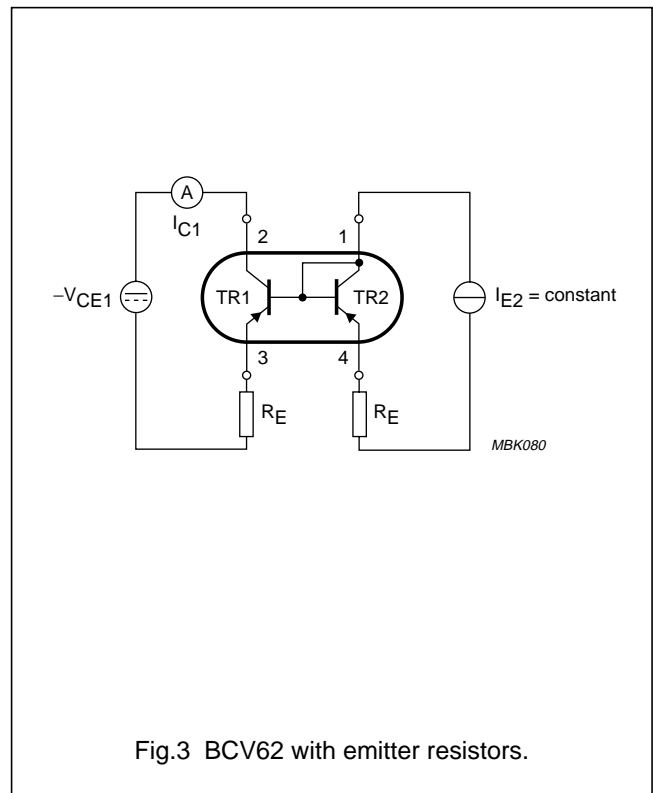
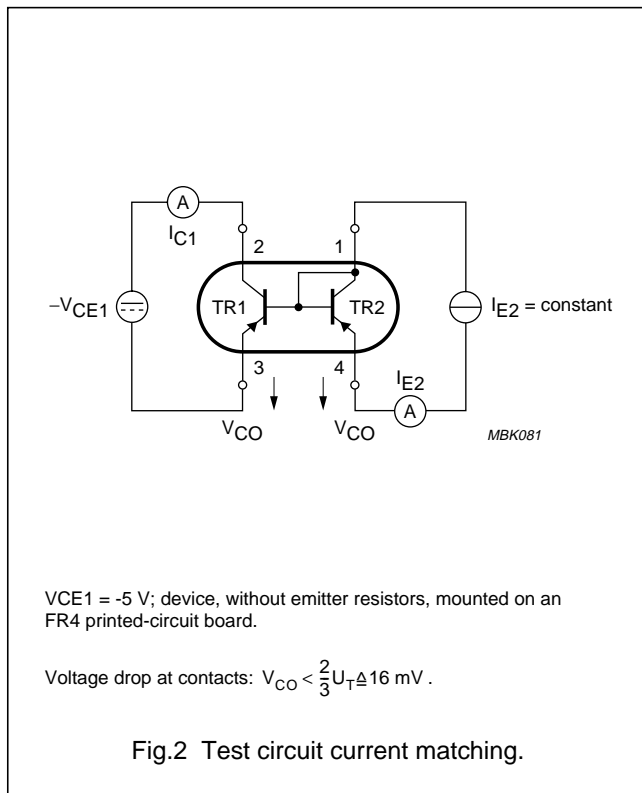
PNP general purpose double transistor

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transistors TR1 and TR2						
$\frac{I_{C1}}{I_{E2}}$	current matching of transistors TR1 and TR2	$I_{E2} = 0.5 \text{ mA}; V_{CE1} = -5 \text{ V}; T_{\text{amb}} \leq 25 \text{ }^\circ\text{C}$	0.7	–	1.3	
		$I_{E2} = 0.5 \text{ mA}; V_{CE1} = -5 \text{ V}; T_{\text{amb}} \leq 150 \text{ }^\circ\text{C}$	0.7	–	1.3	
I_{E2}	emitter current for thermal stability of $-I_{C1}$	$V_{CE1} = -5 \text{ V}; \text{note 3}; (\text{see Fig.2})$	–	–	5	mA

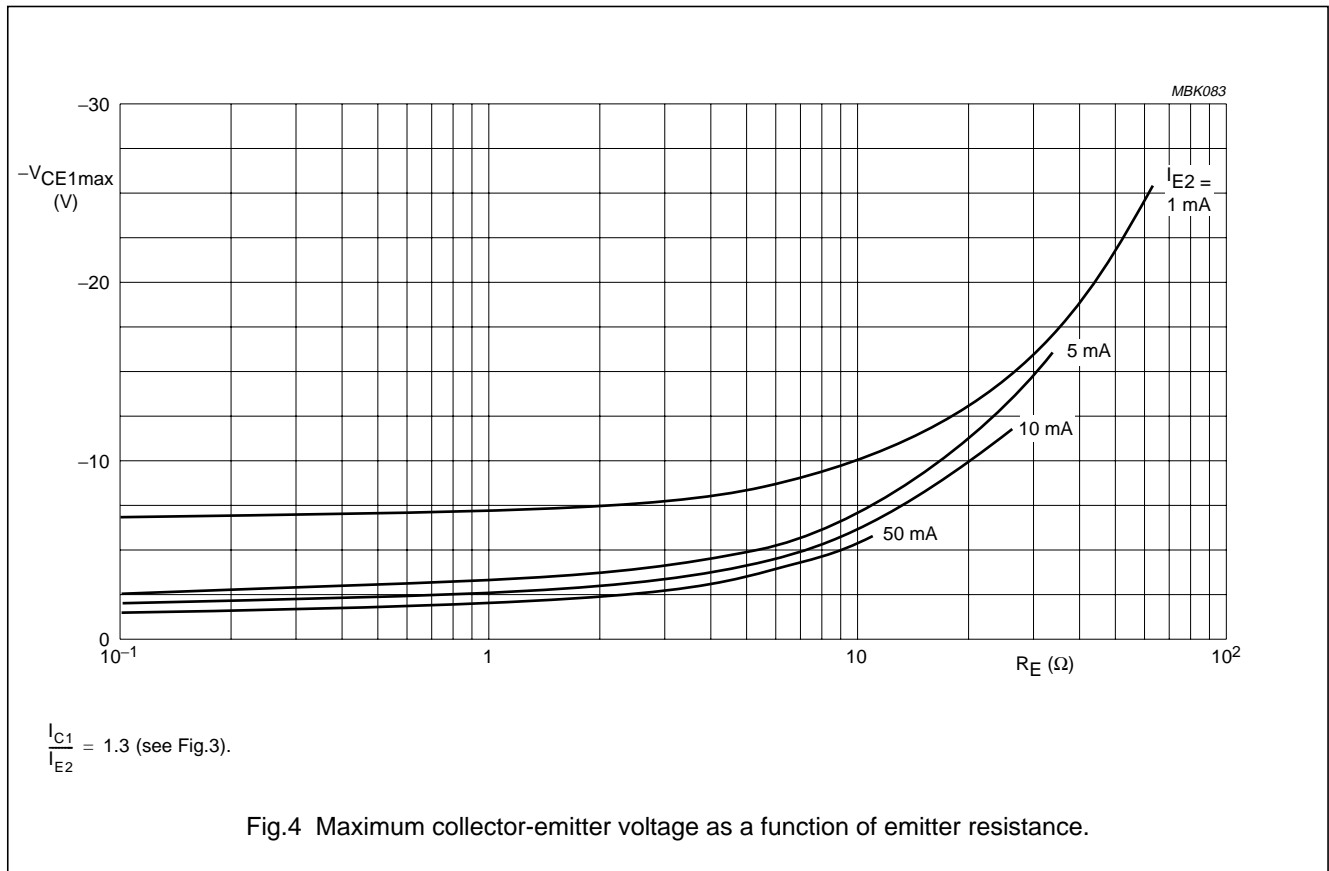
Notes

1. Decreasing $-1.7 \text{ mV}/^\circ\text{C}$ with increasing temperature.
2. Decreasing $-2 \text{ mV}/^\circ\text{C}$ with increasing temperature.
3. Device, without emitter resistors, mounted on an FR4 printed-circuit board.



PNP general purpose double transistor

BCV62



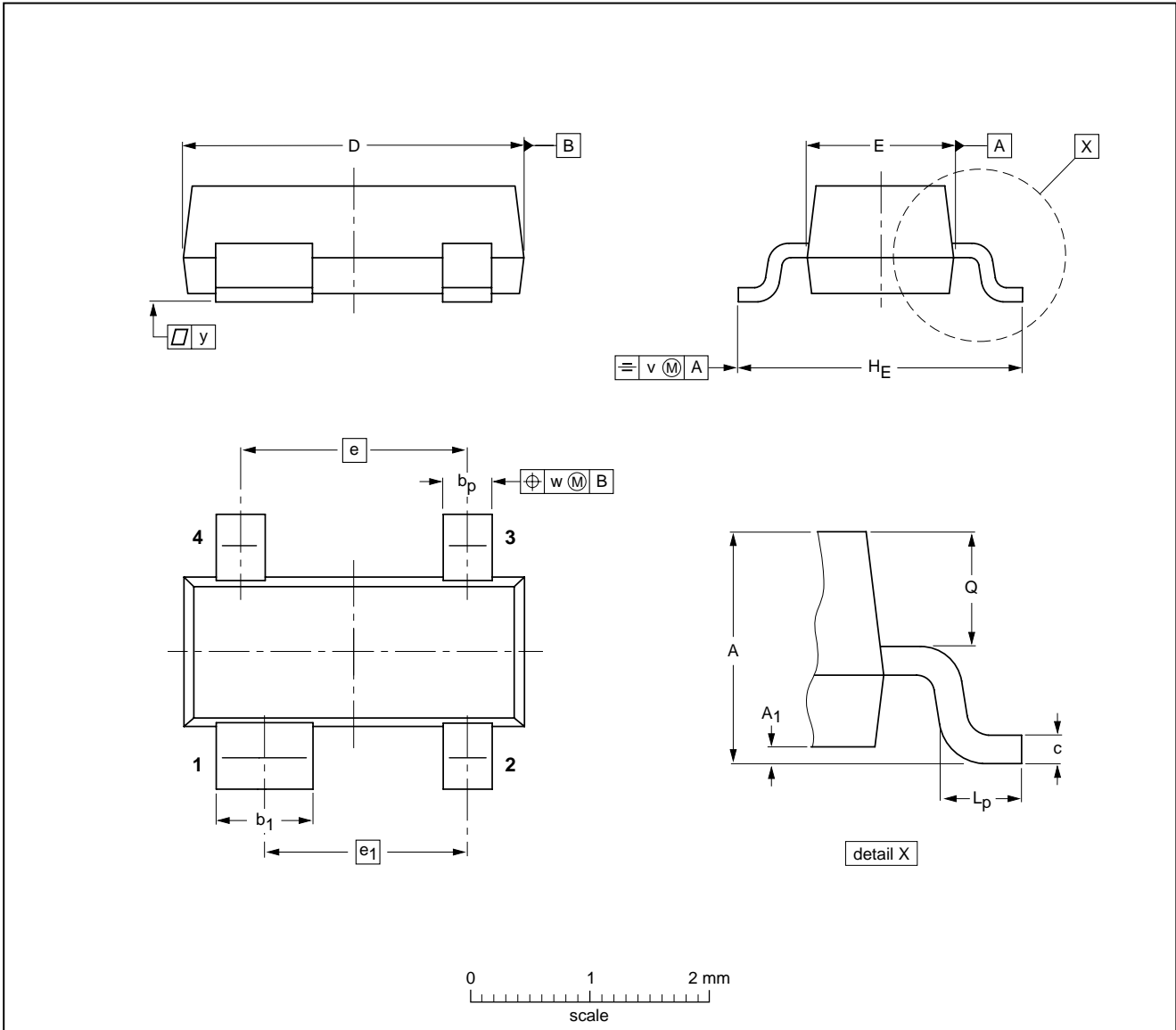
PNP general purpose double transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

PNP general purpose double transistor**BCV62**

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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