INTRODUCTION

48-BCC+-7.0×7.0

S1M8660A is CDMA/AMPS/GPS Triple Mode IF/ baseband IC which is divided into three main parts - IF frequency processing, basband processing , and digital interface. The receiver IC (S1M8660A)and transmitter IC (S1M8657) are provided as a KIT.
S1M8660A is a receiver IC, installed with a Rx AGC, Baseband Converter, Baseband analog filter, and A-D Converter. It can send a digital baseband signal to the digital baseband IC.

S1M8660A is fabricated on the Samsung's 0.5um high-speed, high frequency BICMOS processing and can achieve superior high frequency and low power digital operations.
Its operating voltage is 2.7 to 3.3V, and operating temperature -30 to +85°C .

FEATURES

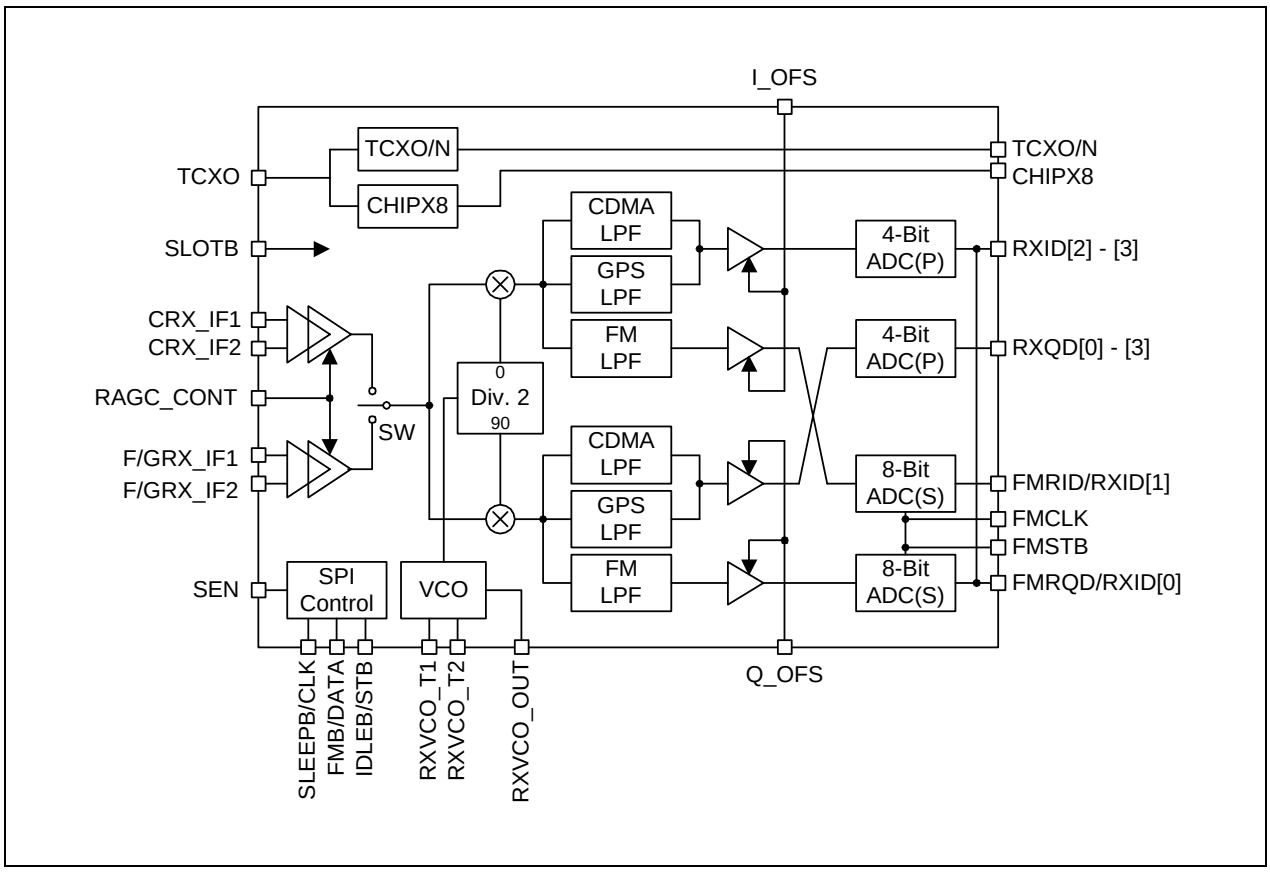
- CDMA/AMPS/GPS Triple Mode
- AGC input signal range : 90dB
- QPSK Baseband Converter
- Built-in I ,Q Baseband signal extractor LPF
- Built-in 4-bit ADC for converting I and Q CDMA analog baseband signals to digital baseband signals
- Built-in 8-bit ADC for converting I and Q FM analog baseband signals to digital baseband signals
- Adopts the Rx SLOT function to minimize the AMPS Mode consumption power
- Built-in VCO for baseband conversion
- Built-in Modem PDM control circuit to compensate the I and Q offsets
- 3-Line Serial Port Interface (SPI)
- Operating Voltage : 2.7 to 3.3V
- 48BCC+(7mm * 7mm * 0.8mm) Package

ORDERING INFORMATION

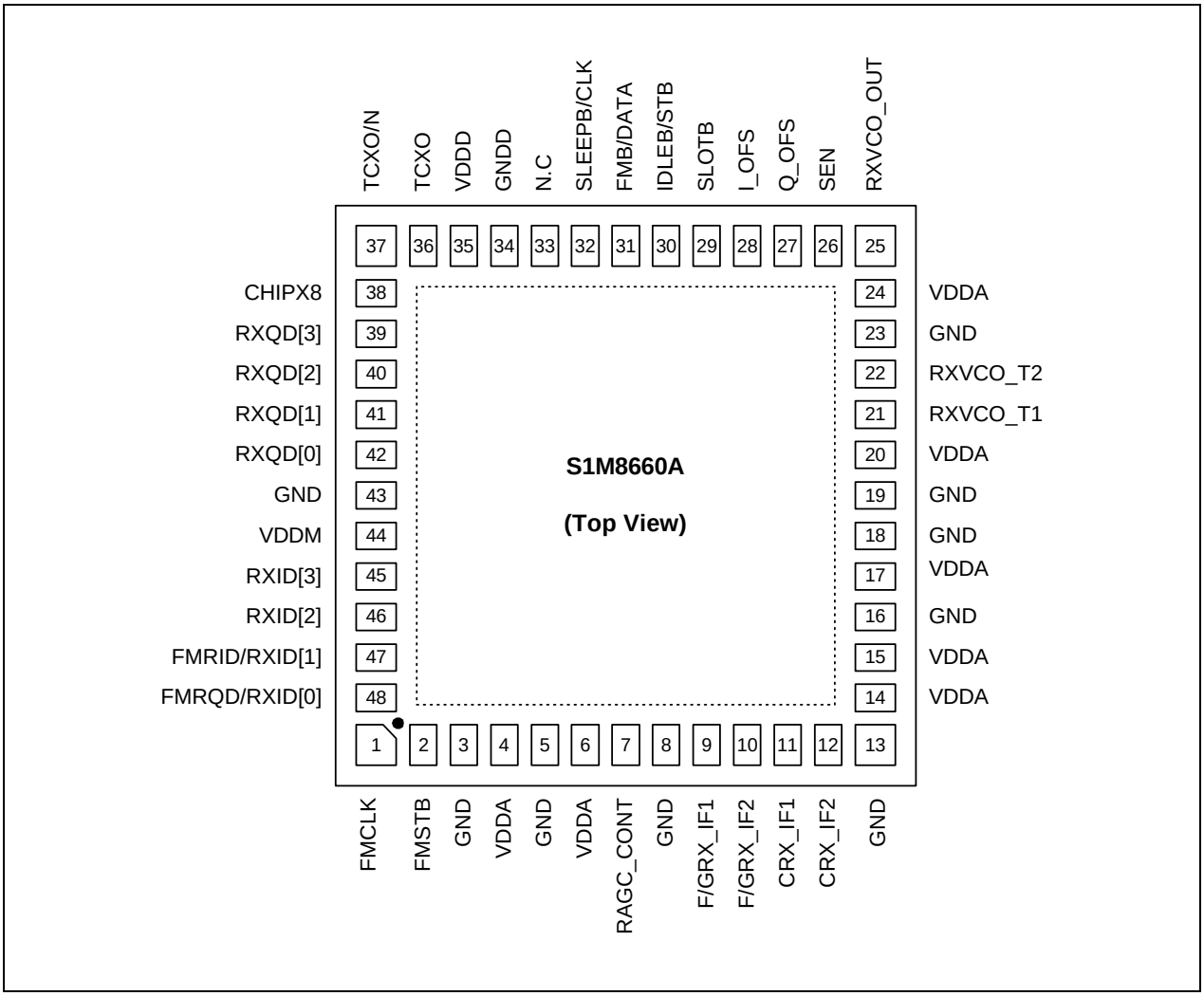
Device	Package	Operating Temperature
++ S1M8660AX01-F0T0	48-BCC+-7.0×7.0	-30 to +85°C

++ : Under Development

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	FMCLK	SEN	FM ADC clock input ,received from the modem. Signal frequency is 360kHz; if unconnected, it becomes LOW.
2	FMSTB	DI	FM STROBE input. Signal that controls the FM ADC initialization and A-D conversion start. CLOCK frequency is 40kHz, which is received from the MODEM; if unconnected, it remains at LOW.
7	RAGC_CONT	AI	AGC gain control input. The input voltage is allowed up to VDDA. It remains at High impedance during SLEEP.
9 10	F/GRX_IF1 F/GRX_IF2	AI	FM/GPS IF input terminals, which have an input impedance of about 865Ω; generally, the FM IF SAW filter is connected to them. Usually, the IF SAW output is single-ended. When these terminals are not used, they remain at High impedance.
11 12	CRX_IF1 CRX_IF2	AI	CDMA IF input terminals, which have an input impedance of about 865Ω; generally, the CDMA IF SAW filter is connected to them. Usually, the IF SAW output is differential. When these terminals are not used, they remain at High impedance.
21 22	RXVCO_T1 RXVCO_T2	AI	Very sensitive terminal, which is connected to the oscillation L-C resonance circuit. Their impedance are about 2kΩ
25	RXVCO_OUT	AO	Output for the PLL, able to output about -12dBm. When this is not used, it remains at high impedance.
26	SEN	D	Input that permits/not permits SPI BUS control. If the input is high, SPI control is allowed, and its related 3-pins, STB, DATA, and CLK, perform their functions; if Low, related 3-pins, IDLEB, FMB, and SLEEPB, are allowed to perform parallel control. When this is not used, it remains at Low.
27 28	Q_OFS I_OFS	AI	Control DC input for removing the DC offset generated in the S1M8660A and system during CDMA and AMPS Mode. The control DC is generated in the modem in PDM form, passes through the R-C filter and is converted to DC, which is sent to this input terminal.
29	SLOTB	DI	This pin becomes Low during CDMA SLEEP Mode or FM RX Mode, the system is assumed to be in the Rx SLOT mode, and all functions are stopped except for the VCO, VCO buffer and TCXO/N. No external clock inputs are not required in this product with this function.
30	IDLEB/STB	DI	When SEN is high, this pin becomes the STROBE input with the permit of the 3-LINE Serial control input. When SEN is low, parallel control input is allowed and this pin executes the IDLEB function. If this pin is opened, it remains at Low.
31	FMB/DATA	BI	When SEN is high, this pin inputs and outputs data with the permit of the 3-line serial control input. When SEN is low, parallel control input is allowed and this pin performs IDLEB. If this pin is opened, it remains at Low.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
32	SLEEPB/CLK	DI	When SEN is high, this pin inputs the clock with the permit of the 3-line serial control input. When SEN is low, parallel control input is allowed and this pin performs SLEEPB. If this pin is opened, it remains at Low.
36	TCXO	AI	Reference frequency input terminal connected to the VCTCXO output. When this pin stops, only DC bias is delivered to maintain the DC charge value of the capacitor connected externally.
37	TCXO/N	DO	Division output of the TCXO Reference frequency input. 3-different division ratio and 2- output drive capacities can be selected through the SPI bus control. Default : 4.92MHz, Weak OUT *division ratio : 1, 1/4, 1/16
38	CHIPx8	BI	CHIPx8 CLOCK output terminal. It has a division ratio of 512/1025 for the TCXO reference frequency. Therefore, it cannot have a perfect 50% duty. When this terminal is not used (CDMA SLEEP, FM IDLE), it remains at Low. This pin can be used exclusively for the externally generated CHIPx8 CLOCK input using the SPI BUS control.
39 40 41 42 45 46 47 48	RXQD3 RXQD2 RXQD1 RXQD0 RXID3 RXID2 RXID1/FMRID RXID0/FMRQD	DO	CDMA A-D Converter's digital outputs, which are connected to the modem data input pins. These data are synchronized at CHIP×8's rising edge and output. Because they are valid at the falling edge, the data are latched at the falling edge in the modem. Because the number of 48-pins are restricted in this product, pins 47 and 48 are shared with the FMDATA pin.
4, 6, 14, 15, 17, 20, 24	VDDA	AI	Power input terminal for the analog circuit.
35	VDDD	DI	Power for the digital logic.
44	VDDM	DI	Power source for a logic circuit, related to the digital input /output, connected to an external digital logic such as the modem.
3, 5, 8, 13, 16, 18, 19, 23, 43	GND	AI	Analog circuit ground. Pin-18 is N.C. in the product.
34	GNDD	DI	Digital logic circuit ground.
33	NC	-	This pin is used for internal testing only and is not connected to anything.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value
Power supply	V_{CC}	-0.5 to 3.6V
Storage temperature	T_{STG}	-55 to +125°C
Operating temperature	T_{OPR}	-30 to +85°C
Storage temperature	HBM	TBD
Electrostatic discharge rating	MM	TBD

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value
Power supply	V_{DDA}, V_{DDD}	2.7 to 3.3V
	V_{DDM}	2.4 to 3.5V
Ambient operating temperature	Ta	-30 to +85°C

ELECTRICAL CHARACTERISTICS

Electrical Characteristics(V_{CC} = 3.3V, Ta = 25°C)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Units
Current consumption	CDMA idle mode	I_{CRX}	-	26	34	mA
Current consumption	CDMA sleep mode	I_{CSLP}	-	300	650	uA
Current consumption	FM idle mode	I_{FRX}	-	19	25	mA
Current consumption	FM slot mode	I_{FSLT}	-	5.5	7.0	mA
Current Consumption	GPS idle mode	I_{GPS}	-	26	34	mA
Current consumption	Power down	I_{DWN}	-	10	100	uA
Logic high input		V_{IH}	V_{DDM}-0.4	-	-	V
Logic low input		V_{IL}	-	-	0.4	V
Logic high output		V_{OH}	V_{DDM}-0.4	-	-	V
Logic low output		V_{OL}	-	-	0.4	V
Digital input capacitance		C_{DI}	-	-	5	pF
Digital output load capacitance		C_{DOL}	-	-	10	pF
TCXO input impedance	Attach C = 2pF	Z_{TCXO}	10	-	-	kΩ
CDMA IF input resistance	IF differential	R_{IFINC}	-	1	-	kΩ
FM IF input resistance	IF single-ended	R_{IFINF}	-	850	-	Ω
IF input capacitance	CDMA, FM IF differential	C_{IFIN}	-	-	2	pF
VCO input resistance	IF VCO differential	R_{VCO}	-	2.5	-	kΩ
VCO input capacitance	IF VCO differential	C_{VCO}	-	-	2	pF

AC CHARACTERISTIC

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CDMA Performance						
Input sensitivity	Maximum AGC gain. Control input signal so that output corresponding to 3LSB is output from ADC.	VCSEN	-102	-	-	dBm
Maximum input signal	Minimum AGC gain. Control input signal so that output corresponding to 3LSB is output from ADC.	VCMAX	-	-	-12	dBm
AGC gain slope	PDM 3.3V Mode	GSLOPE	33	45	53	dB/V
AGC gain error over temperature	-30°C to +85°C.	GVAR	-3	-	3	dB
IF input frequency range	Cin < 2pF	Fin	-	85.38	-	MHz
IF input Impedance		Zin	0.8	1.0	1.2	kΩ
Noise figure	Input power = -102dBm	NFmin	-	-	7	dB
	Input power = -75dBm	NFmid	-	-	20	dB
	Input power = -25dBm	NFmax	-	-	72	dB
IIP3	AGC gain Max.	IIP3max	-53	-	-	dBm
	AGC gain Min.	IIP3min	-10	-	-	dBm
Spurious contents	ADC generated harmonic frequency component. Two signals in the in-band are each mixed with signals which will allow ADC to produce -7dB output signals. The harmonic and non-harmonic components of the ADC output signals between 1kHz to 20MHz are extracted and added. The AGC control voltage is controlled so that ADC output is full scale when the input signal is -80dBm.	TSpur	-	-	-25	dBc
Spurious content related to jammer	In-band spurious peak value produced by IMD based on 2 jammer signals. One in-band signal(@50kHz,0.5*F/S) and two jammers(@900kHz, 22dB*F/S and @1.7MHz, 21dB*F/S)are simultaneously input. AGC control voltage is controlled so that ADC output is F/S when the input signal is -80dBm.	Jspur	-	-	-18.4	dBc

AC CHARACTERISTICS (Continued)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Single-tone jammer desense	Overall gain reduction due to one jammer. The in-band signal at -97dBm (control the AGC control voltage to 0.5*F/S)and the jammer signal at 900kHz and -57dBm are simultaneously input.	Jdsen	-	-	1.0	dB
Residual Sideband	$RSB = 20\log\sqrt{\frac{1+k^2+2k\cos\theta}{1+k^2-2k\cos\theta}}$ *k* : Linear Gain Mismatch θ : Phase Mismatch in Deg.	RSB	22			dB
Crosstalk FM to CDMA	Leakage ratio between CDMA input and FM input.	CTFC	30	-	-	dB
Offset gain slope	Amount of code change of the voltage ADC output at the I/Q offset control	GOFS	-	250	-	%FS/V
Offset adjust input impedance	-	Zoff	100	-	-	kΩ
Out-band attenuation	≥ 900kHz	ATC9	46	-	-	dB
	≥ 1.2MHz	ATC12	48	-	-	dB
Gain flatness	Amount of gain change along I and Q paths between 1kHz to 615kHz	Gft	-1		1	dB
FM Performance						
Input sensitivity	Maximum AGC gain. Control input signal so that ADC outputs 0.5*F/S.	VSEN	-98.3	-	-	dBm
Maximum input signal	Minimum AGC gain. Control input signal so that ADC outputs 0.5*F/S.	VMAX	-	-	-8.3	dBm
AGC gain slope	PDM 3.3V Mode	GSLOPE	33	45	53	dB/V
AGC gain error over temperature	-30 to +85°C.	GVAR	-3	-	3	dB

AC CHARACTERISTICS (Continued)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
IF input frequency range	Cin < 2pF	Fin	-	-	250	MHz
Noise figure	Input power = - 98dBm	NFmin	-	-	7	dB
	Input power = - 75dBm	NFmid	-	-	12	dB
	Input power = - 25dBm	NFmax	-	-	58	dB
IIP3	AGC gain Max.	IIP3max	-53	-	-	dBm
	AGC gain Min.	IIP3min	-25	-	-	dBm
Spurious contents	ADC generated harmonic frequency component. ADC generated Two signals in the in-band are each mixed with signals which will allow ADC to produce -7dB output signals. The harmonic and non-harmonic components of the ADC output signals between 1kHz to 20MHz are extracted and added. The AGC control voltage is controlled so that ADC output is full scale when the input signal is -80dBm.	TSpur	-	-	-42	dBc
Spurious content related to jammer	In-band spurious peak value produced by IMD based on 2 jammer signals. One in-band signal(@1kHz,0.5*F/S) and two jammers(@60kHz, 22dB*F/S and @122kHz, 4dB*F/S)are simultaneously input. AGC control voltage is controlled so that ADC output is F/S when the input signal is -80dBm.	Jspur	-	-	-18.4	dBc
Single-tone jammer desense	Overall gain reduction due to one jammer. The in-band signal at -93dBm (control the AGC control voltage to 0.5*F/S)and the jammer signal at 900kHz and -53dBm are simultaneously input. The gain reduces if the input/output range is small in BBA.	Jdsen	-	-	1.0	dB
Crosstalk CDMA to FM	The leak ratio between the CDMA input and FM input.	CTCF	30	-	-	dB
Offset gain slope	Amount of code change of the voltage ADC output at the I/Q offset control	GOFS		250		%FS/V
Offset adjust input impedance	-	Zoff	100	-	-	kΩ
Out-band attenuation	≥ 45kHz	ATC9	48	55	-	dB
	≥ 60MHz	ATC12	60	69	-	dB
Residual Sideband	$RSB = 20\log\sqrt{\frac{1+k^2+2k\cos\theta}{1+k^2-2k\cos\theta}}$ k : Linear Gain Mismatch θ : Phase Mismatch in Deg.	RSB	28	-	-	dB

AC CHARACTERISTICS (Continued)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Gain flatness	Amount of gain change along I and Q paths between 1kHz to 615kHz	Gft	-1	-	1	dB
IF VCO perormance						
VCO and buffered output frequency range	VCO external time constant and PLL value	Fvco	-	170	500	MHz
VCO phase noise	Tank LC's Q value should be above 20. Measure @100kHz away from the mid-frequency.	Pvco	-	-	-104	dBc/ Hz
RXVCO_OUT output power	Select a VCO buffer output value reduced by -2dB. Connect output load to 50Ω.	Ovco	-15	-	-	dBm
GPS Performance						
Input sensitivity	Maximum AGC gain. Control input signal so that ADC outputs 0.5*F/S.	VCSEN	-98.3	-	-	dBm
Maximum input signal	Minimum AGC gain Control input signal so that ADC outputs 0.5*F/S.	VCMAX	-	-	-8.3	dBm
AGC gain slope	PDM 3.3V Mode	GSLOPE	33	45	53	dB/V
AGC gain error over temperature	-30 to +85°C.	GVAR	-3	-	3	dB
IF input frequency range	Cin < 2pF	Fin	-	85.38	150	MHz
IF input Impedance		Zin	0.8	1.0	1.2	kΩ
Noise figure	Input power = -98dBm	NFmin	-	-	7	dB
	Input power = -75dBm	NFmid	-	-	12	dB
	Input power = -25dBm	NFmax	-	-	58	dB
IIP3	AGC gain Max.	IIP3max	-53	-	-	dBm
	AGC gain Min.	IIP3min	-25	-	-	dBm
Offset gain slope	Amount of code change of the voltage ADC output at the I/Q offset control	GOFS		250		%FS/ V
Offset adjust input impedance	-	Zoff	100	-	-	kΩ
Out-band	≥ 1.3MHz	ATC13	46	-	-	dB
attenuation	≥ 1.7MHz	ATC17	48	-	-	dB
Residual Sideband	$RSB = 20\log\sqrt{\frac{1+k^2+2k\cos\theta}{1+k^2-2k\cos\theta}}$ *k : Linear Gain Mismatch* θ *: Phase Mismatch in Deg.*	RSB	22	-	-	dB
Gain flatness	Amount of gain change along I and Q paths between 1kHz to 800kHz	Gft	-1.5		1.5	dB

TIMING DIAGRAMS

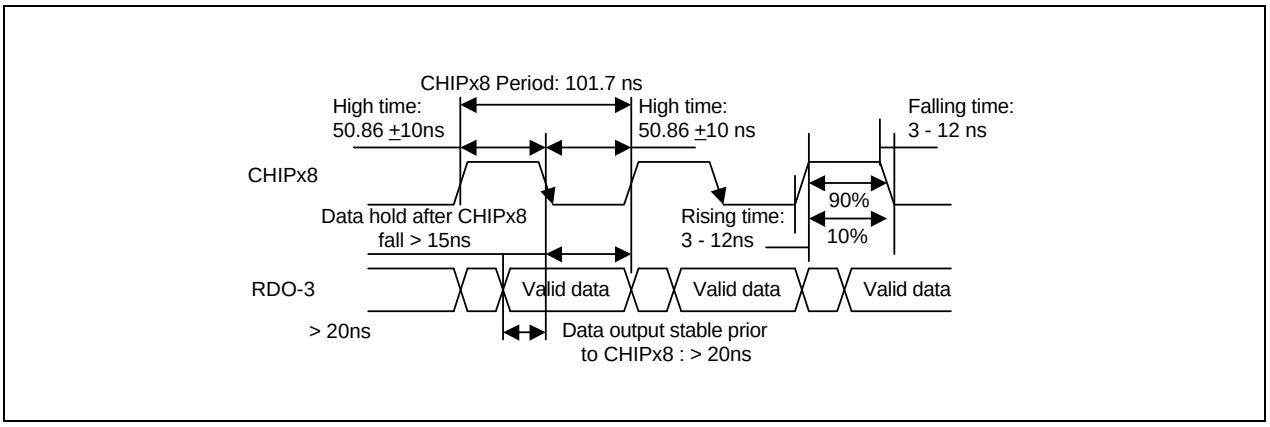


Figure 1. CDMA / GPS Receive ADC Timing

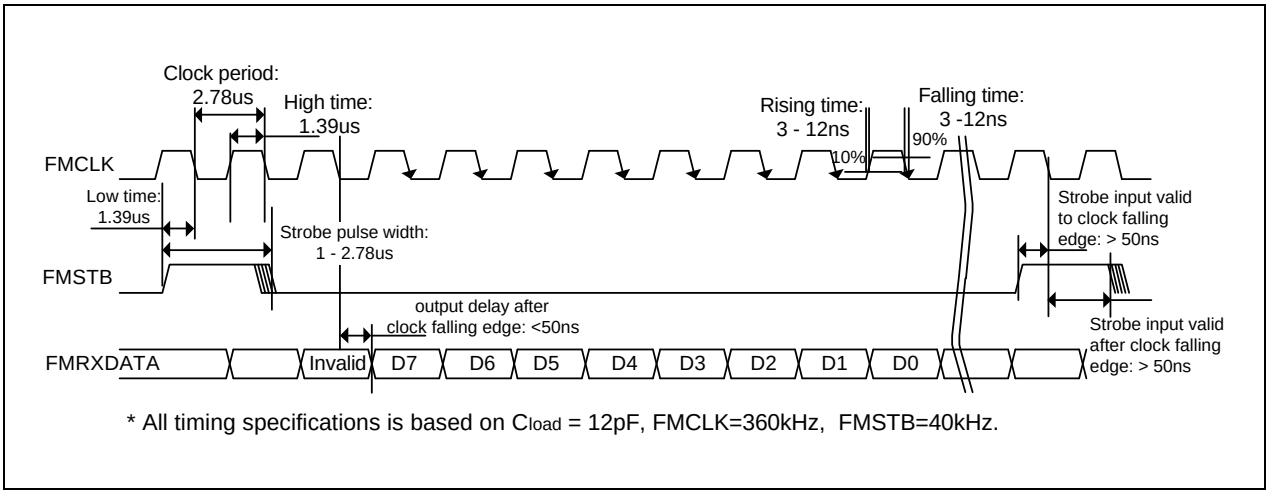


Figure 2. FM Receive ADC Timing

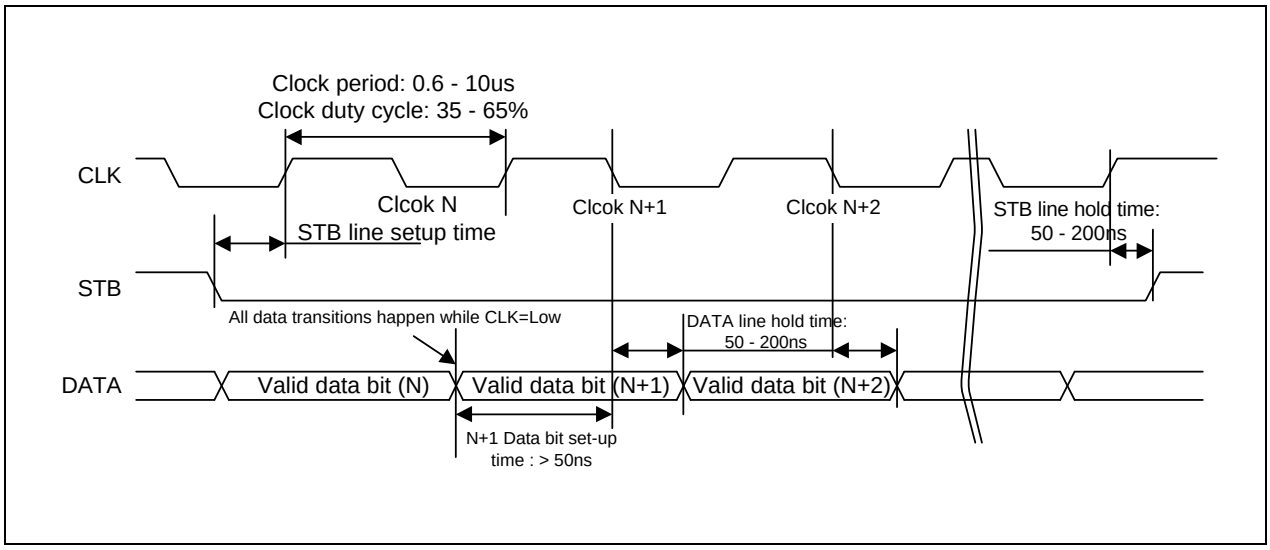


Figure 3. 3-Line Serial Port Interface Timing

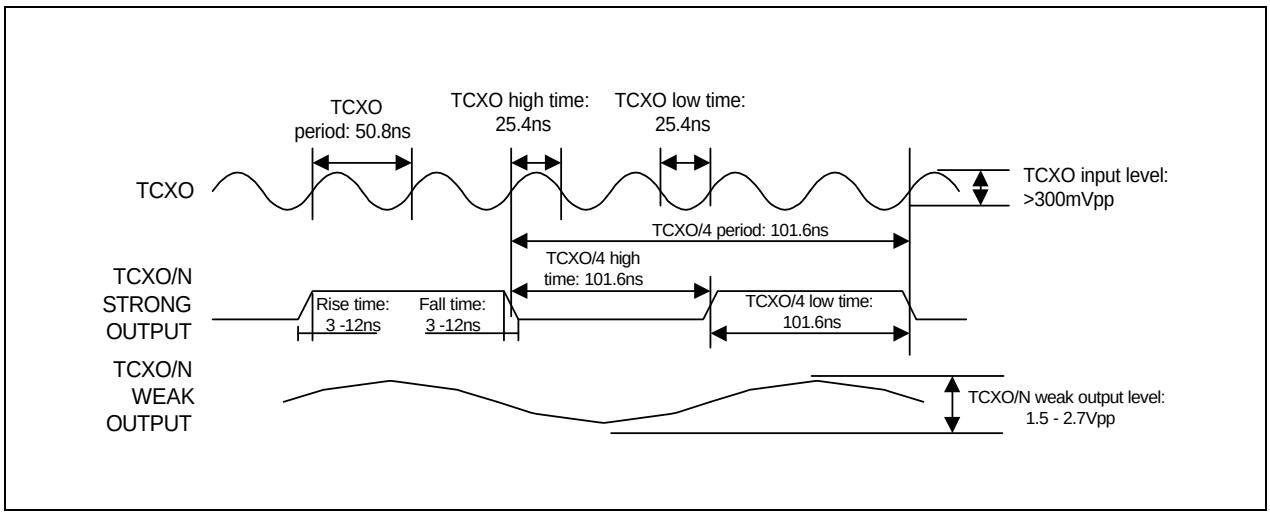


Figure 4. TCXO and TCXO/N Timing

FUNCTIONAL DESCRIPTION

S1M8660A is a CDMA/AMPS/GPS receive-only baseband analog IC, located between the RF mid-frequency processing terminal and baseband processing terminal. The RF analog mid-frequency signal terminal(IF SAW filter output), directly connected to the S1M8660A mid-frequency input pin, converts and processes the baseband signal and sends the corresponding digital signal to the modem IC. Baseband analog processing uses QPSK modulation, LPF, and A-D converter and the modem IC performs digital CDMA/AMPS/GPS baseband modulation on the digitalized analog baseband signal it receives.

S1M8660A uses a 0.5um BiCMOS, equipped with high-frequency bipolar and low power standardized CMOS logic, to operate safely in the low power range, consisting of power voltage between 2.7 to 3.3V and operating temperature between -30 to +85°C.

CDMA Receive Signal Path

S1M8660A is composed of a receive circuit, installed with TCXO/N, CHIP×8 like clock generator, mode conversion switch and serial I/F apparatus. The receive circuit has the Rx AGC, an automatic gain controller, and baseband LPF and output terminal with the A-D converter, and VCO and mixer etc. The input signal is received as a differential signal, which is modulated to 1.23 MHz spread-spectrum for CDMA. The mid-frequency is 220.38MHz for Korea-PCS, 1.23MHz for US-PCS, and 85.38MHz for cellular; they are set based on the time constants of the components involved with the external VCO and external Rx PLL. Rx AGC , connected to both the IF SAW filter and matching component in the RF-IF converter output located in the RF block, amplifies or reduces according to the signal size. It takes its orders from the modem chip when it sets the appropriate receive level as required by the CDMA system. Gain is controlled by applying a DC voltage to the RAGC_CONT pin. The applied DC is produced when the PDM signal, generated as a control signal in the modem, passes through the R-C filter. The control band of this AGC is approx. 90dB. The QPSK Baseband modulator separates and modulates the IF signal sent by the AGC using I(In-phase) and Q(Quad-phase) baseband signal. Essentially, two signals, I-LO and Q-LO (Local oscillator), are mixed with AGC's IF output signals, respectively. The LO(local oscillator) signal is generated by the internal oscillating components, externally connected tank coil, and Varactor, and the externally independent PLL device is used to generate its exact oscillation mid-frequency.

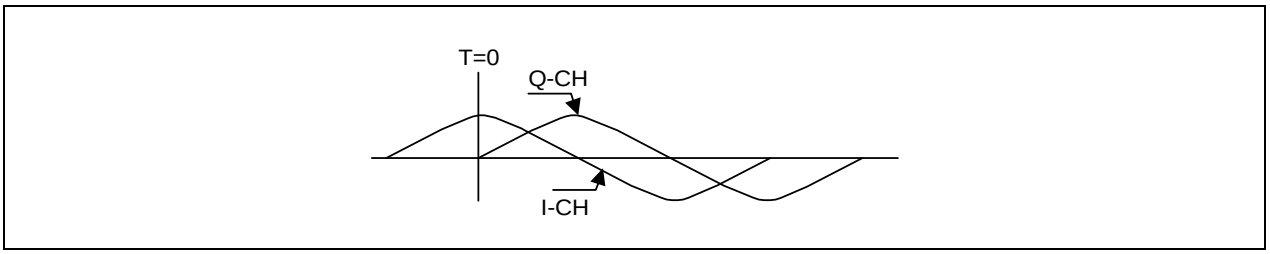


Figure 5. Received I/Q Phase in S1M8660A

Defining of the I-Phase and Q-Phase receive path is very important to its design. The polarities of these paths are also important to digital baseband modulation. Therefore, the output of the QPSK baseband modulation determines the I and Q phases; I-phase is defined as the phase leading the Q-phase by exactly 90°, but it simpler to think of I as Cosin and Q as Sin. The figure related to this is shown in Figure 5. This definition is valid only when the QPSK IF input signal is higher than the IF mid-frequency. The baseband signal, output by the QPSK modulator, includes various other unnecessary surrounding band noises, which are removed by the use of the LPF(Low-Pass-Filter).

Ultimately, I and Q filtered signals are converted to digital signals by the 4-bit A-D converter and sent to the modem. The A-D converter used is a parallel output type and its outputs are synchronized at the CHIPx8 rising edge. The modem chip captures the data on the CHIPx8 falling edge. The CHIPx8 clock used in the A-D converter can change the CHIP×8 output to input so that the clock can be used in systems with different TCXO reference frequency.

FM Rx Signal Path

S1M8660A FM signal path is the same as that of the CDMA with the exception of a different LPF and A-D converter, which meet the system specification. Basically a FM modulated signal between IF mid-frequency to ±15kHz is input so that the baseband LPF, unlike CDMA, has the 12kHz cut-off frequency characteristic. A-D Converter has 8-bit resolution, characteristic of AMPS, and processing speed of approx. 40kHz. It does not adopt the power consuming parallel configuration but rather the series configuration to minimize the consumption power.

Rx AGC , connected to both the IF SAW filter and matching component in the RF-IF converter output located in the RF block, amplifies or reduces according to the signal size. It takes its orders from the modem chip when it sets the appropriate receive level as required by the CDMA system. Gain is controlled by applying a DC voltage to the RAGC_CONT pin. The applied DC is produced when the PDM signal, generated as a control signal in the modem, passes through the R-C filter. The control band of this AGC is approx. 90dB. The QPSK Baseband modulator separates and modulates the IF signal sent by the AGC using I(In-phase) and Q(Quad-phase) baseband signals. Essentially, two signals, I-LO and Q-LO (Local oscillator), are mixed with AGC's IF output signals, respectively. The LO(local oscillator) signal is generated by the internal oscillating component, externally connected tank coil, and Varactor, and the externally independent PLL device is used to generate its exact oscillation mid-frequency. Defining of the I-Phase and Q-Phase receive path is very important to its design. The polarities of these paths are also important to digital baseband modulation. Therefore, the output of the QPSK baseband modulation determines the I and Q phases; I-phase is defined as the phase leading the Q-phase by exactly 90°, but it simpler to think of I as Cosin and Q as Sin.

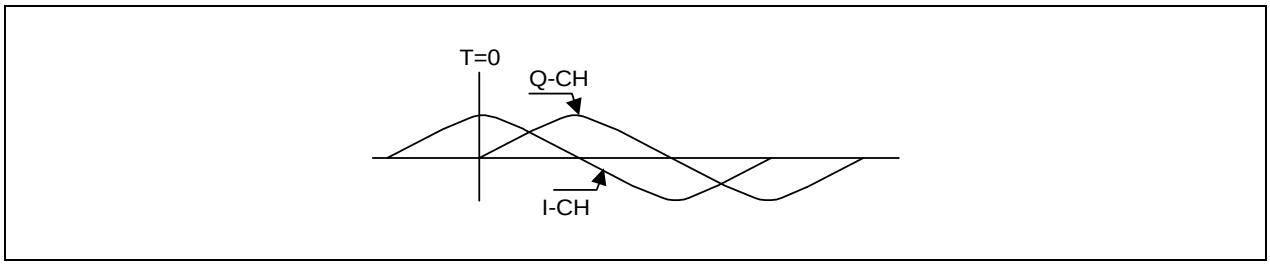


Figure 6. Received I/Q Phase in S1M8660A

The figure related to this is shown in Figure 6. This definition is valid only when the QPSK IF input signal is higher than the IF mid-frequency. The baseband signal, output by the QPSK modulator, includes various other unnecessary surrounding band noises, which are removed by the use of the LPF(Low-Pass-Filter). The filter pole is barely 12kHz , merely in the audible range, for AMPS considering that the CDMA is 630kHz. Ultimately, I and Q filtered signals are converted to digital signals by the 4-bit A-D converter and sent to the modem. The A-D converter used is a parallel output type ;its outputs are synchronized at the FMCLK and output in the order that it was synchronized. The modem chip captures the data by matching the FMDATA to the FMCLK clock. The CHIPx8 clock used in the A-D converter can change the CHIP×8 output to input so that the clock can be used in systems with different TCXO reference frequency. The clock used by the A-D converter is provided by the modem chip. It has a 360kHz frequency but can have 40kHz cycle when converting an 8-bit data.

GPS Rx Signal Path

The difference of the S1M8660A from the S1M8656A is that S1M8660A provides GPS receiving operation. While GPS receiving path shares function blocks with FM and CDMA modes, it needs independent low pass filter.

GPS IF signal from GPS RF-IF mixer is applied to S1M8660A via GPS SAW filter. Because both outputs of FM SAW filter and GPS SAW filter are generally single ended signals, differential input pins of FM AGC are designed to be shared with GPS block. And as a consequence of this sharing, external circuit is necessary for switching of input signal. A recommended circuit for this is in Figure. 8.

The operation of I/Q demodulator is the same in CDMA/FM/GPS modes and the phase relation of I/Q signal of the output is the same as depicted in Figure . 7.

GPS low pass filter of S1M8660A has its cut off frequency at around 800kHz.

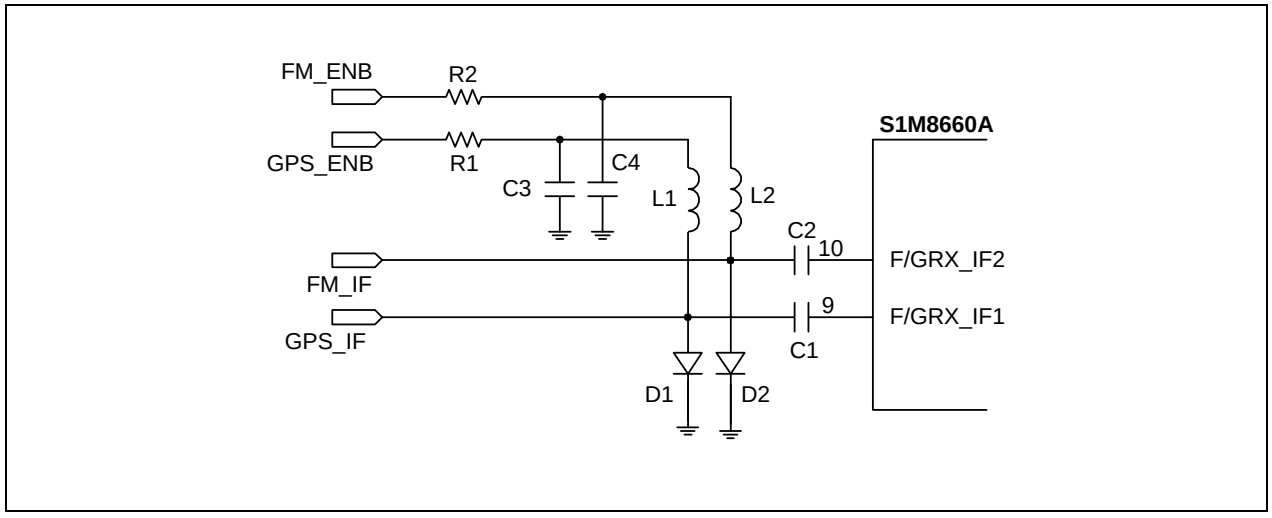


Figure 7. FM/GPS IF Input Application

A-D converter, as output of GPS path, is the 4bit parallel converter which is the same one used in CDMA path. But the sampling frequency is different from that of CDMA mode. And in operating in GPS mode, sampling clock of A-D converter should be supplied from the modem.

Rx Low-Pass Filters

The CDMA baseband signal frequency can range between 1kHz to 630kHz. Normally, the range between 1kHz to 615kHz is called the In-band, between 630kHz to 750kHz Band-edge, and anything outside of these ranges out band. Very precise characteristics are required in the in-band range. The ripple, I/Q gain-phase error are critical factors that lead to noise in the in-band. FM Baseband signal ranges between 100Hz to 15kHz. Normally, the frequency range between 100Hz to 12kHz is called the in-band, between 12kHz to 18kHz the band-edge, and anything outside of these ranges the out-band. As for the CDMA, the ripple, I/Q gain-phase error are critical factors that lead to noise in the in-band.

The LPF characteristic required by these three systems are shown in Figures.

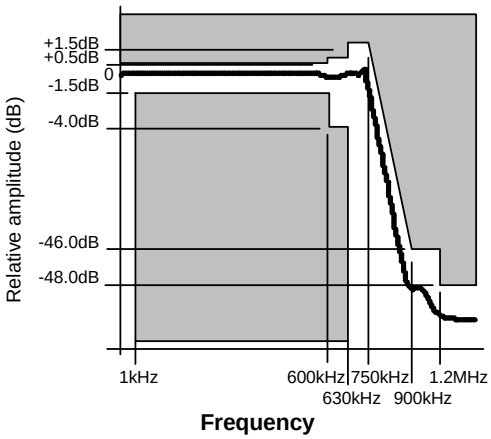


Figure 8. CDMA Rx Low-Pass Filter Masks

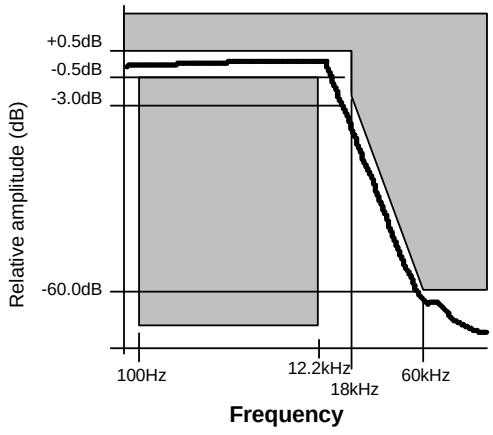


Figure 9. FM Rx Low-Pass Filter Masks

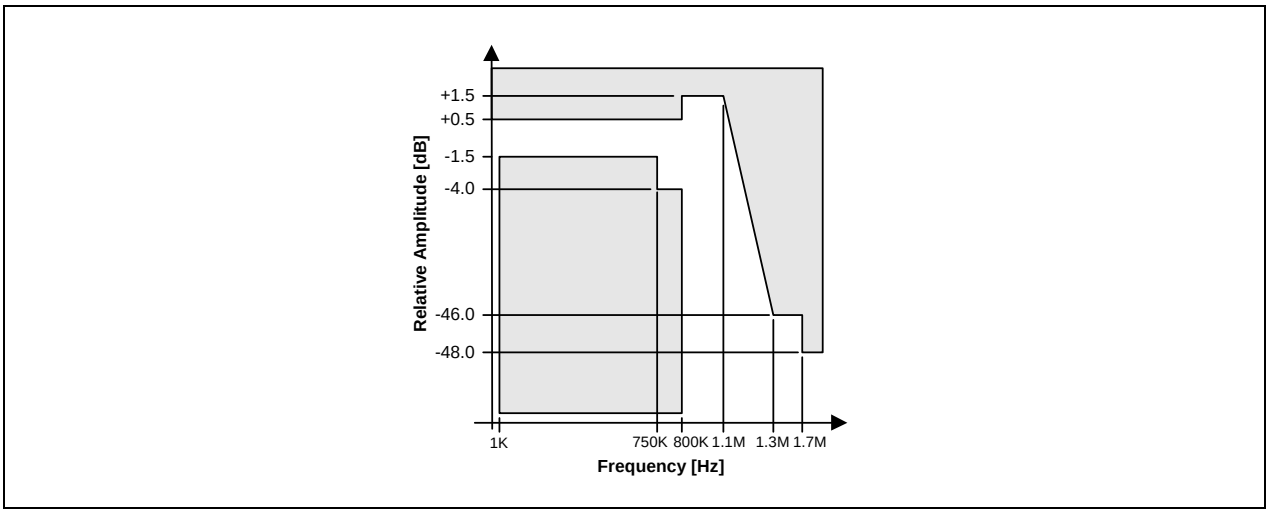


Figure 10. GPS Rx Low Pass Filter Mask

CHIP×8 Clock Generator

CHIP×8 CLOCK is a digital division that divides the 19.68MHz TCXO by 512/1025. It holds the TCXO clock by half cycle every 512th TCXO cycle and strictly speaking it does not generate 9.8304MHz precisely. The 9.8304MHz is the mean on the 1025TCXO cycle, where 9.84MHz of 50% duty is obtained from 1 to 512 and 513 to 1024. The timing diagram in Figure 9 explains this. The CHIP×8 CLOCK output is held at low when the CDMA is asleep and FM is idle. Moreover, it can use three division ratios(19.68MHz, 9.84MHz, 9.8304MHz) through the serial I/F. Various external chip clocks can be used by converting them to inputs. In operating in GPS mode, input should be changed in order that the signal of GPS sampling frequency can be applied.

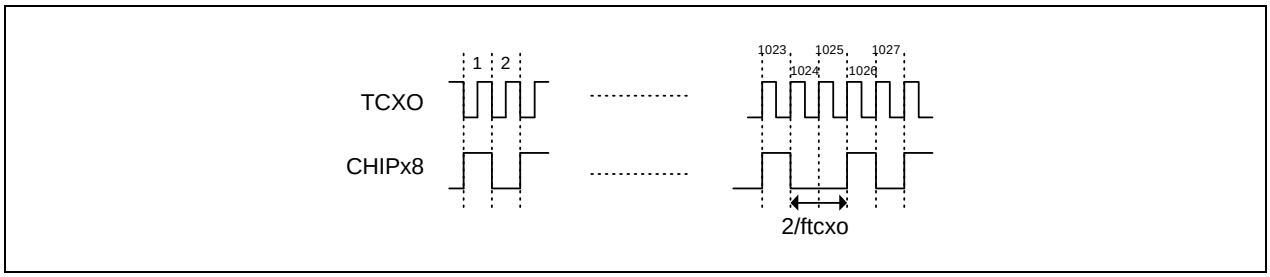


Figure 11. CHIP×8 Clock form

Rx Voltage Controlled Oscillator(VCO)

S1M8660A includes the Rx LO block having the VCO and quad-phase generator. The quad-phase generator outputs I-phase and Q-phase clocks with 1/2 the VCO frequency and sends them to the QPSK modulator. The VCO buffer is used when the VCO output is sent to the external RX PLL. Although the allowable VCO frequency is determined based on an external time constant, it can only range between approx. 100MHz to 500MHz, suggesting that the maximum input IF frequency is 250MHz.

Serial Port Interface(SPI)

S1M8660A is equipped with the Serial I/F. All internal functions can be controlled through a common bus using an external controller. The serial I/F can be used by setting pin 26(SEN) high, the pin which permits/ not permit the SPI. If the SEN becomes low, the SPI cannot be used and the S1M8660A must be used DC control mode. (All the internal registers are default value) In GPS mode, for the compatibility with the former products, it is designed to be uncontrollable with DC control. So, in case of GPS mode, the SEN pin should be set high and then it can be controlled through serial interface. S1M8660A is designed to be completely compatible with MSM series of Qualcomm, and compatible with S1M8656A except for GPS function. Here, the modem is the master and S1M8660A the slave.

Each pin which uses the SPI bus has the following common functions.

- The STB(STROBE) for the serial bus start signal is used to initialize serial data transmission. This pin is used with the IDLEB function in manual mode and designated the IDLEB/STB pin.
- Serial BUS DATA is used for the bi-direction data input /output at serial data transmission. This pin is used with the FMB function in parallel mode and designated the FMB/DATA pin. Because it is an open drain type pin, it requires the pull-up resistance of approx. 8kΩ.
- Serial BUS CLK is used to synchronize the data input/output at serial data transmission. This pin is used with the SLEEPB function in manual mode and designated the SLEEPB/CLK pin.

S1M8660A can be used to power down the TCXO/N block using the SPI bus when the CDMA is asleep (CDMA SLEEP). This mode, installed to minimize the product consumption power, is entered by setting a specific bit (PWRDWN) in the CLK_GEN_MODE register to '1'. The current in the sleep mode reduces from 300uA to 10uA. The SEN(PIN26) pins decide on whether the product will used the SPI bus or parallel control inputs; if it is in low, then the pins the parallel control input functions, IDLEB, FMB, and SLEEPB, but if in high then these pins execute the SPI bus functions, STB, DATA, and CLK. This product does not require any external time constants in initializing the internal register because it can use the internal reset function. In Qualcomm's devices, time delay using R and C in the figure blow is applied for the initiation of the chip. The R is used to set SEN high and then the device can be controlled by SPI. If DC control mode is necessary, C should be replaced with R. Figure. 10 shows the serial bus connection.

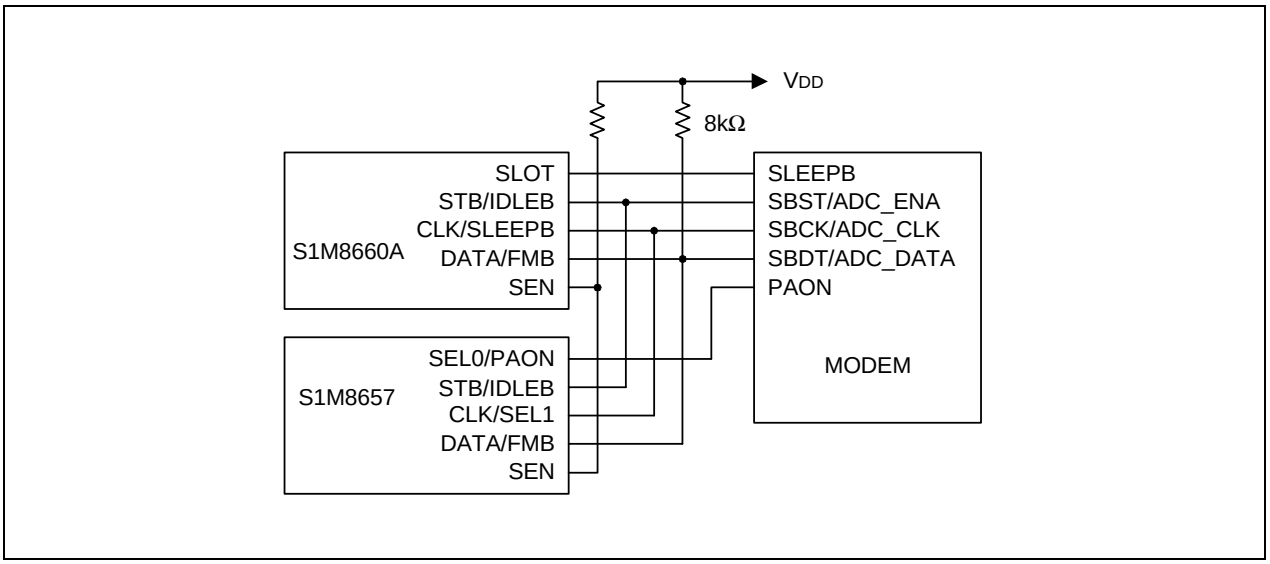


Figure 12. Serial Bus connection

The advantage of using the SPI bus is the opportunity given to use all the various functions in the product, thus allowing more flexibility. Moreover, by tieing all the products using a common bus and controlling them together, the PCB application area and the number of control pins for the master can be simultaneously reduced, as compared to controlling the products independently.

Serial Port Interface Operation

The modem, the master, controls slaves such as S1M8660A using the SPI bus.
The STB falling edge indicates the start of the serial I/F data transmission. The STB becomes high to mark the end of the data transmission.
(Data sent after the STB turns high are not valid.)
Serial line data is captured and stored as soon as the slave or the master places the clock on the falling edge.
The SPI 3-line must remain high for at least 1-clock cycle in order to sent new data.
The MSB always outputs the data line data.
After 9-clocks, which is required to send data, the data line driver opens the data line, at which time the data line becomes high because of the external pull-up resistance.

Serial Data Transfer format

S1M8660A and S1M8657 are all slave devices with the SPI bus. What differentiate them from one another is their different device IDs. Each company has its own characteristic SPI bus configuration , but normally the 3-line bus is most often used and sometimes the 2-line bus such as the IIC bus. Figure 13. shows the serial data transfer format.

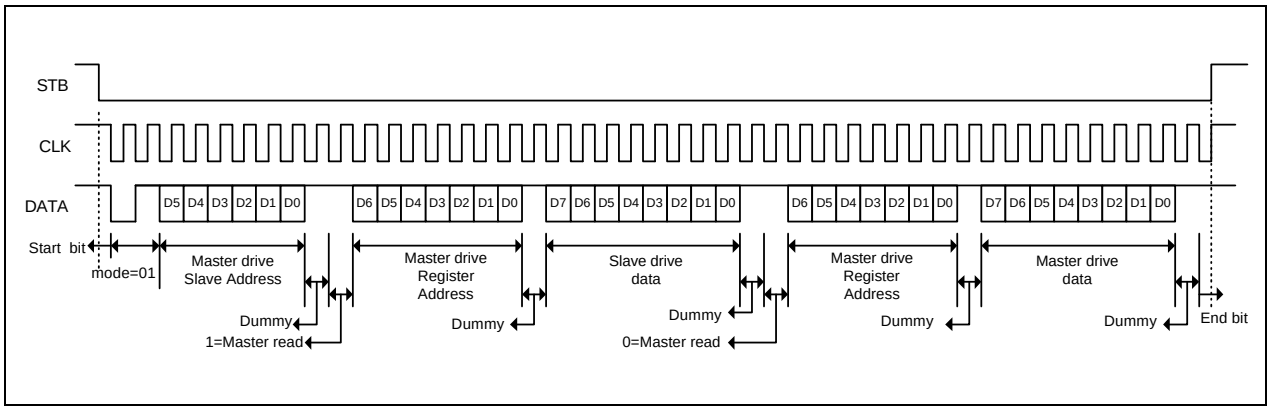


Figure 13. Serial Data Transfer Format

(1) The first 2-BITs are for transmission only and this product must send '01'.(Others are not permitted.)

(2) The following 6-bit data specifies the slave device, which is connected to the SPI bus and has its own ID.

(3) The following 1-bit is a dummy bit, which marks the end of the 8-bit data transmission and the beginning of the next data to be sent.

(4) The following 1-bit decides on whether the master will drive the data line or the slave will. If this bit is '1', the master will drive , but if '0' the slave will drive the data line.

(5) The following 7-bit data is the register address of the specified slave device; the 7-bits for an address allows 128 register addresses for slaves.

(6) The following high 1-BIT data is a dummy data.

(7) The following 8-BIT data is the data in the device to be driven.

(8) The following 1-BIT data is a dummy data, which marks the end of the 8-bit data transmission and beginning of the next data to be sent.

(9) The following 1-bit decides on whether the master will drive the data line or the slave will. If this bit is '1', the master will drive , but if '0' the slave will drive the data line.

(10) The following 7-bit data is the register address of the specified slave device.

(11) The following high 1-BIT data is a dummy data.

(12) The following 8-BIT data is the data in the device to be driven.
(Continous data transmission such as this can be ended with a 1-byte transmission or can be read/written repeatedly.)

(13) After the last data is sent, the data line opens and becomes high;

(14) the CLK continues for half the 1-clock cycle and then becomes high;

(15) and the STB becomes high as soon as the clock becomes high and this marks the end of data transmission.

Modes of Operation

S1M8660A can be controlled by existing DC control inputs such as S1M8656A or by the SPI bus.
The modes of DC operation consists of state FMB, IDLEB, and SLEEPB modes; Table 2 shows the various modes.

In GPS mode, it can be controlled only by SPI bus.

Table 2. Mode control in the DC control mode

Mode	FMB	IDLEB	SLEEPB	CHIPx8	TCXO/N
CDMA talk	H	H	H	On	On
CDMA idle	H	L	H	On	On
CDMA sleep	H	L	L	Off	On
FM talk	L	H	X	On	On
FM idle	L	L	H	Off	On
Rx slot	L	L	L	Off	On

CONTROL REGISTERS

S1M8660A has various registers which can be programmed by the SPI bus. These registers have their own function which are described below.

Table 3. S1M8660A Control Registers

Register name	Address	R/W	Default vale	Description
RESET	0x00	W	-	Reset. Reset S1M8660A and all the register values are returned to their default value.
SPI_ID	0x01	R	0x1F	SPI_ID. Each slave device has its own, independent code; S1M8660A code is 1Fh.
BLOCK_CTL	0x04	R/W	0x3C	BLOCK_CTL Decides on the S1M8660A operation and performs the same functions as IDLEB, FMB and SLEEPB in the parallel control mode.
CLK_GEN_ MODE	0x09	R/W	0x0C	CLK_GEN_MODE Changes the internal divider(TCXO,CHIPx8) conditions; controls the output drive.
FILTER_SEL	0x0A	R/W	0x0A	FILTER_SEL Lowpass filter selection
AGC_DCONV	0x0C	R/W	0x0B	AGC_DCONV Controls the AGC gain control range and VCO output.
Reserved	0x10 - 0x15	Absolutely not permitted.		

W : MODEM is recorded in the S1M8660A register R : When S1M8660A sends data to the modem

Table 4. Description Of Control Registers

Address	Name	Type	Bits	Description
00(h)	RESET	W	-	When the master uses this register, the S1M8660A returns all the programmed register values to their initial value.
01(h)	SPI_ID	R	[5:0]	This read-only register is used to confirm the type of slave connected to the master. It is set to 1Fh and all S1M8660A has the same value. This is the ID absolutely required to differentiate the controller from the data, when there are many slaves connected to the SPI bus.

Table 4. Description Of Control Registers(Continued)

Address	Name	Type	Bits	Description
04(h)	Block_CTL [7], [2:0]	R/W	[7]	Identifies the S1M8660A 0 = S1M8656A, 1 = S1M8660A
			[6:3]	Default = 0111 Reserved Registers
			[2]	FMB. Default = 1 1: CDMA Mode, 0: FM Mode CDMA Mode or FM Mode select bit.
			[1]	IDLEB. Default = 0 1: RxTx Mode, 0: Idle Mode Talk Mode or idle Mode select bit.
			[0]	SLEEPB. Default = 0 1: follows the IDLEB state. 0: SLEEP Mode SLEEP or None-SLEEP select bit.
		When [2:0] = 001 and SLOTB(Pin29)=0, FM SLOT Mode; if SLOTB = 1,FM Rx Mode. If [2:0]=000, becomes FM SLOT Mode, regardless of SLOTB. Operates in the CDMA Mode, regardless of the SLOTB state.		
09(h)	CLK_GEN_ MODE [4:0]	R/W	[7:5]	Default = 000 Reserved Registers
			[4]	TCXO_PWR. Default = 0 1: TCXO/N output not allowed 0: TCXO/N output allowed TCXO/N division and output permit/not permit select bit.
			[3]	TCXO_DRV. Default = 1 1: TCXO/N Weak CMOS output 0: TCXO/N is STRONG CMOS output TCXO/N DRIVE select bit according to conditions of use.
			[2]	TCXO_N. Default = 1 1: TXCO/N ; N = 4 0: TCXO/N ; N = 1 TCXO/N output division ratio selection parameter.
			[1:0]	CHIP×8. Default = 00 00: In the Normal Mode, it has the TCXO*512/1025 ratio. 01: CHIP×8 output is converted to external clock input. 10: Half the TCXO is output. 11: CHIP×8 division and output are not allowed. Select bit on whether to use the CHIP×8 division ratio with the input mode or output mode.
0A(h)	FILT_SEL [1:0]	R/W	[7:2] [1:0]	Default = 000111 Reserved Registers. FILT_SEL Default = 00 00 : CDMA LPF, 01 : GPS LPF

Table 4. Description Of Control Registers (Continued)

Address	Name	Type	Bits	Description
0C(h)	AGC_RVCO [7:5], [2:0]	R/W	[7]	GPS_SEL, Default = 0
			[6:5]	AGCPDM. Default=00. AGC PDM control range 00: PDM 3.3V : Use when VDDM = 3.3V 01: PDM 2.4V : Use when VDDM = 2.4V 10: PDM 2.7V : Use when VDDM = 2.7V 11: Reserved : not allowed. Reserved bit for changes to PDM voltage according to the MODEM power voltage BIT.
			[4:3]	Reserved Registers. Default = 01
			[2:0]	IF_PWRDN. Default = 011. 000 : I/Q Demod, RxVCO, VCO Buffer Power down 100 : Reserved X01 : Reserved X10 : Reserved 011 : I/Q Demod, RxVCO, VCO Buffer Power up RXVCO_OUT Weak Mode 111 : I/Q Demod, RxVCO, VCO Buffer Power up RXVCO_OUT Strong Mode

CHARACTERISTIC GRAPH

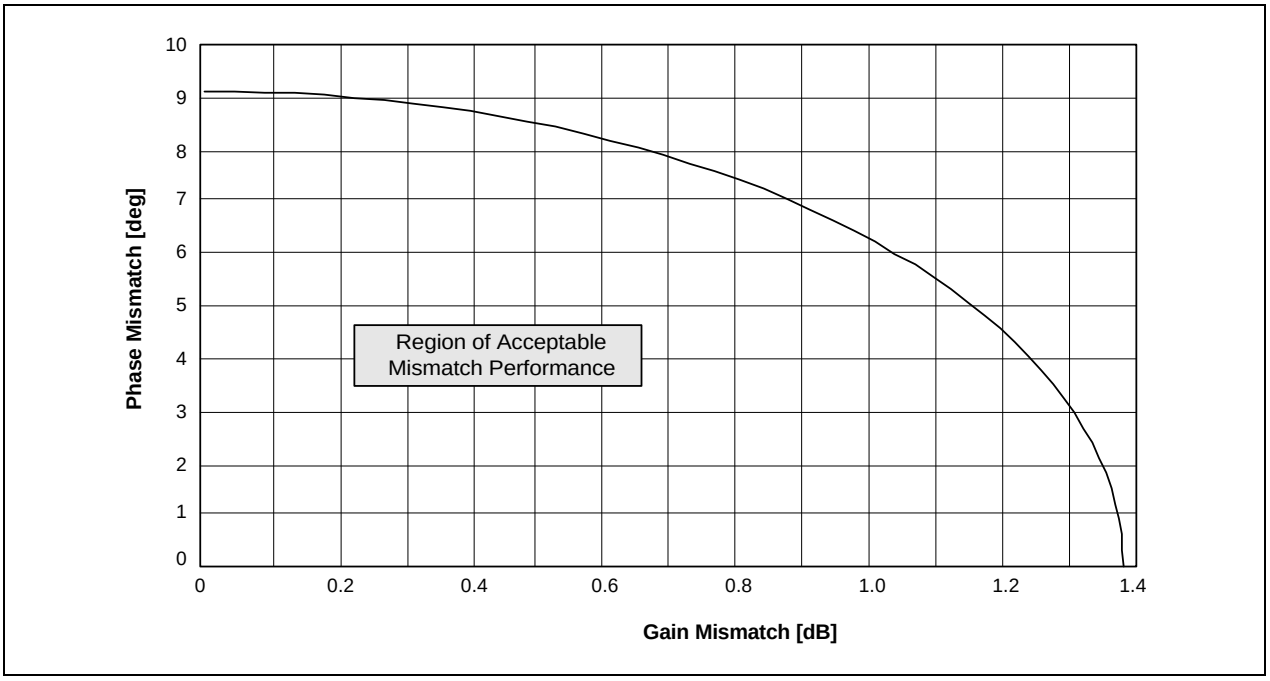


Figure 14. CDMA Rx Gain/Phase Mismatch Specification

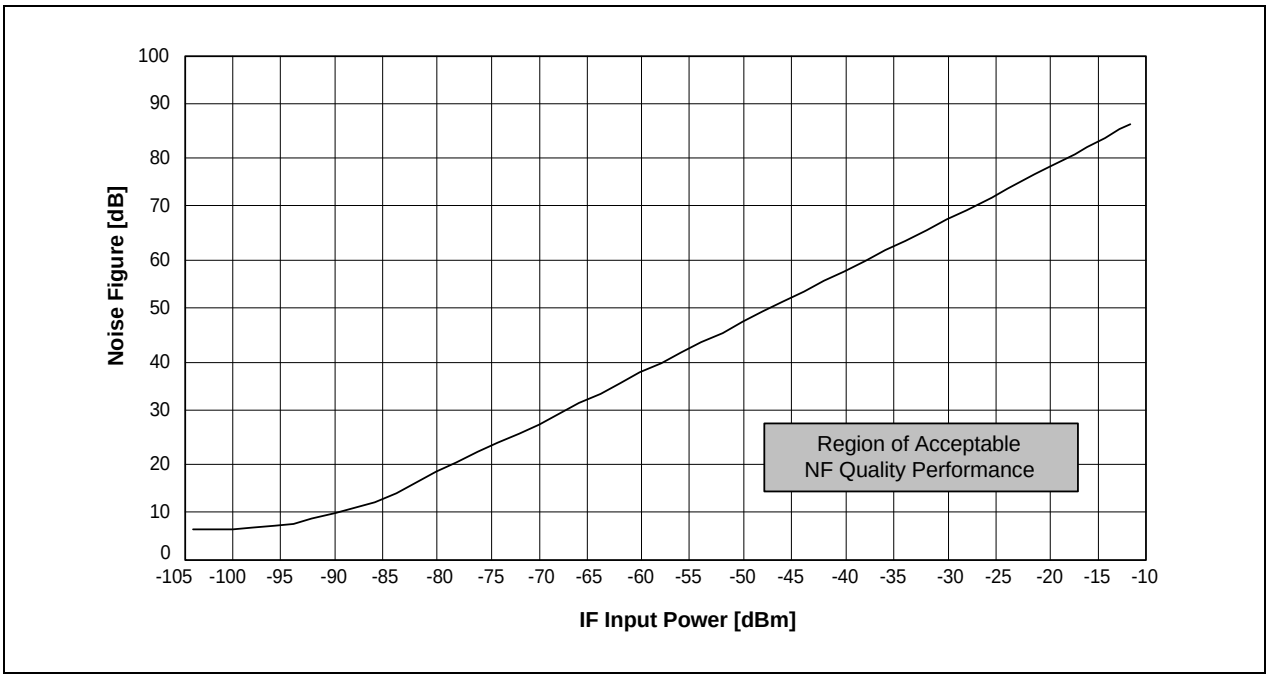


Figure 15. CDMA Rx Mode Noise Figure Specification

CHARACTERISTIC GRAPH (Continued)

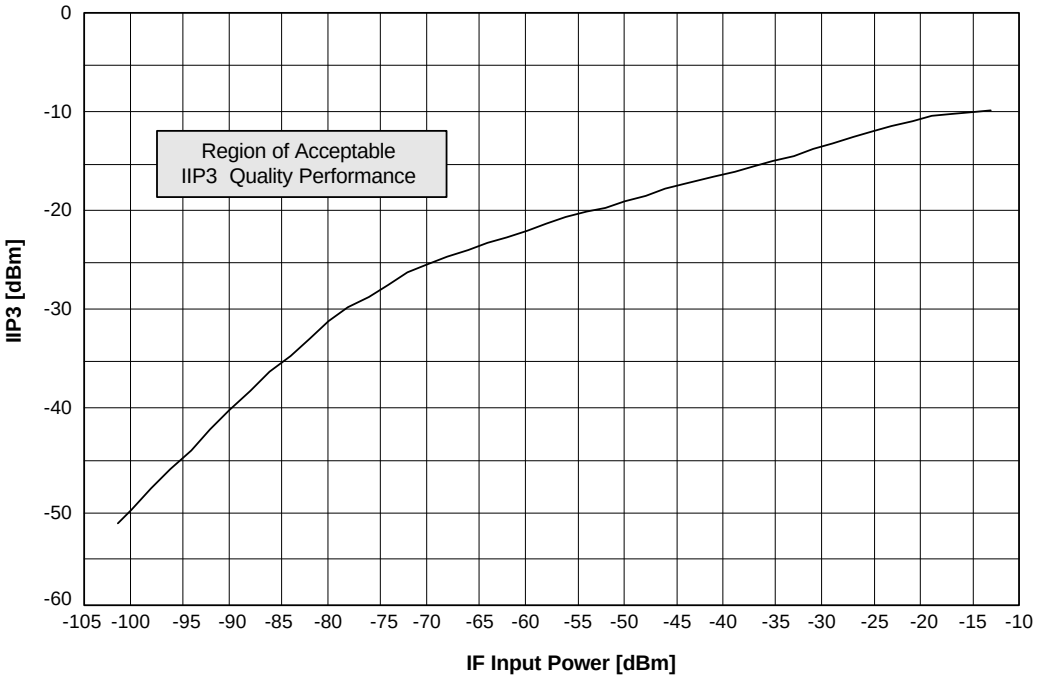


Figure 16. CDMA Rx Mode IIP3 Specification

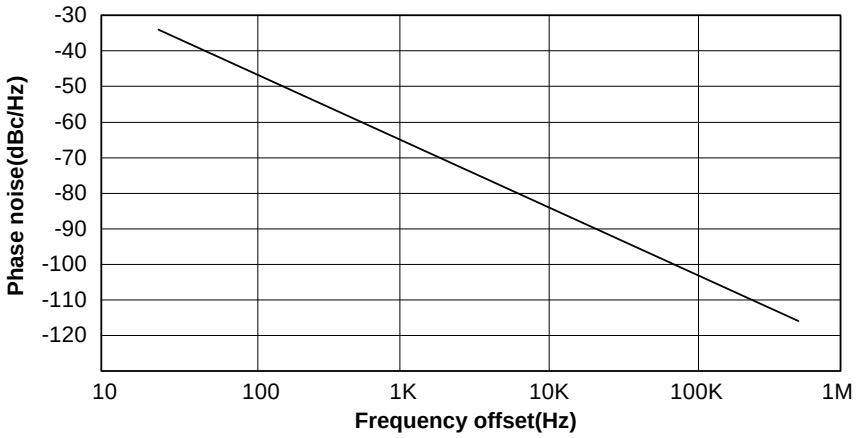


Figure 17. S1M8660A IF VCO Open Loop Phase Noise

CHARACTERISTIC GRAPH (Continued)

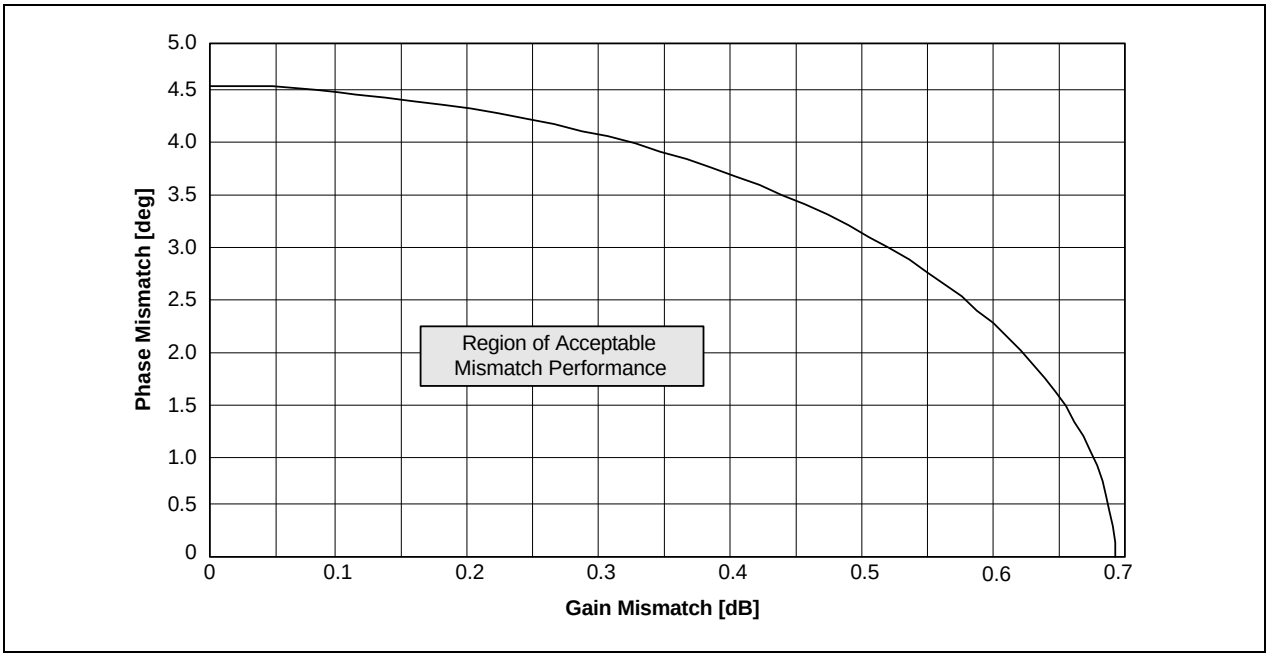


Figure 18. FM Rx Gain/Phase Mismatch Specification

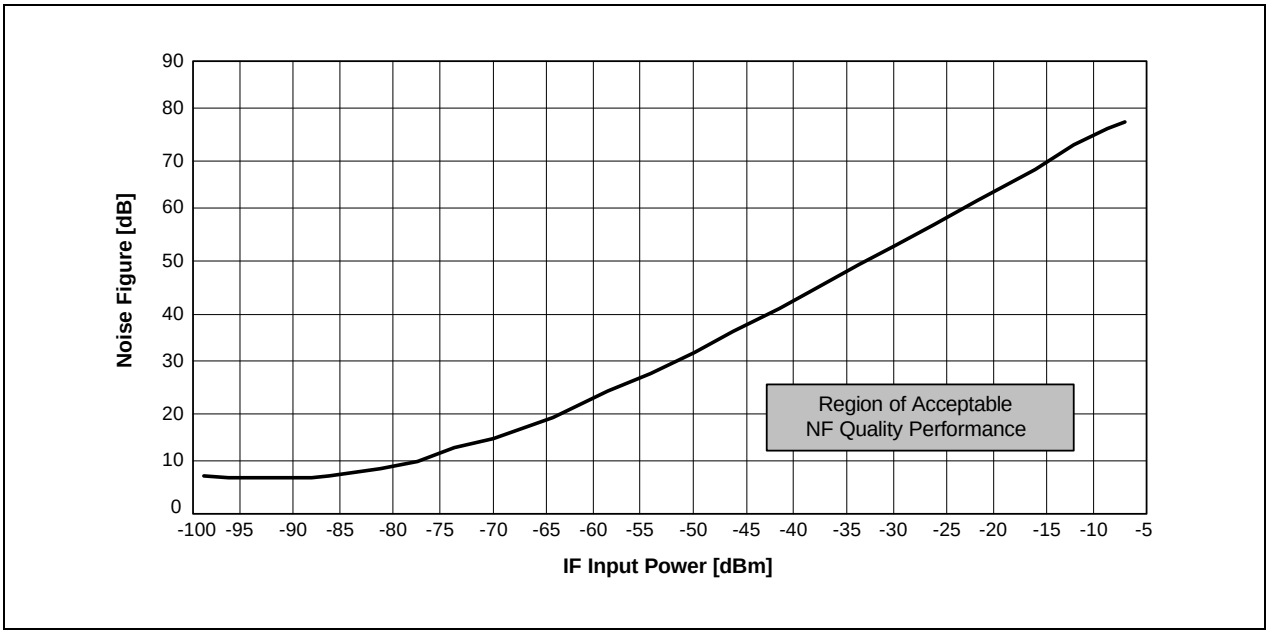


Figure 19. FM Rx Mode Noise Figure Specification

CHARACTERISTIC GRAPH (Continued)

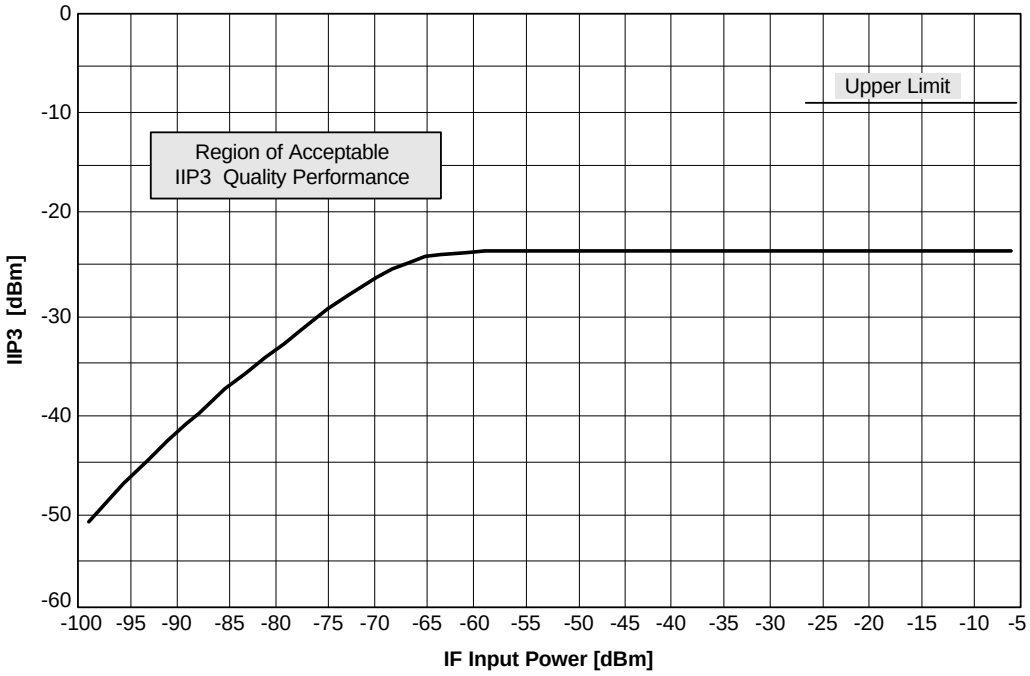


Figure 20. FM Rx Mode IIP3 Specification

CHARACTERISTIC GRAPH (Continued)

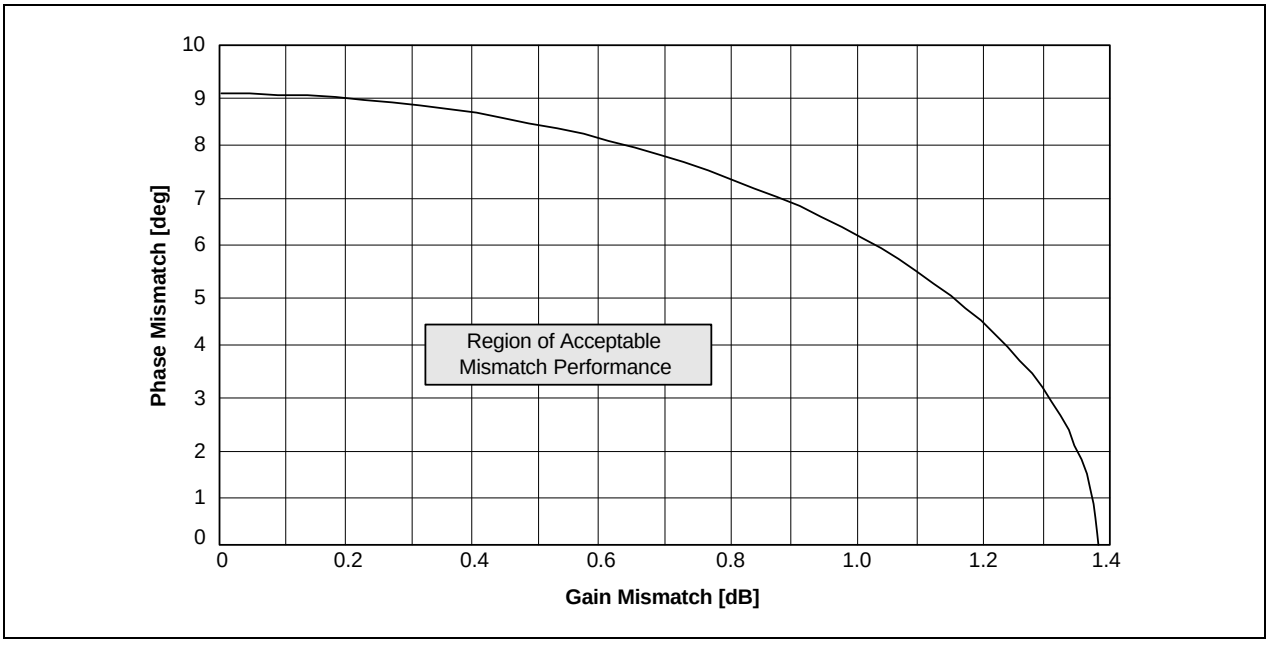


Figure 21. GPS Rx Gain/Phase Mismatch Specification

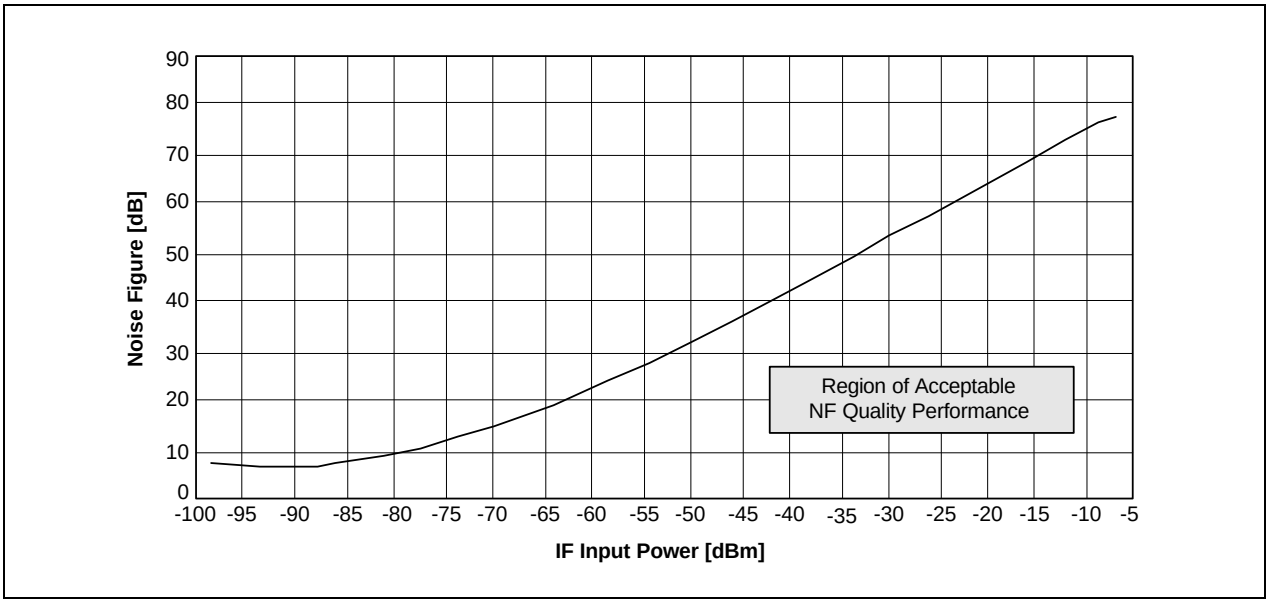


Figure 22. GPS Rx Mode Noise Specification

CHARACTERISTIC GRAPH (Continued)

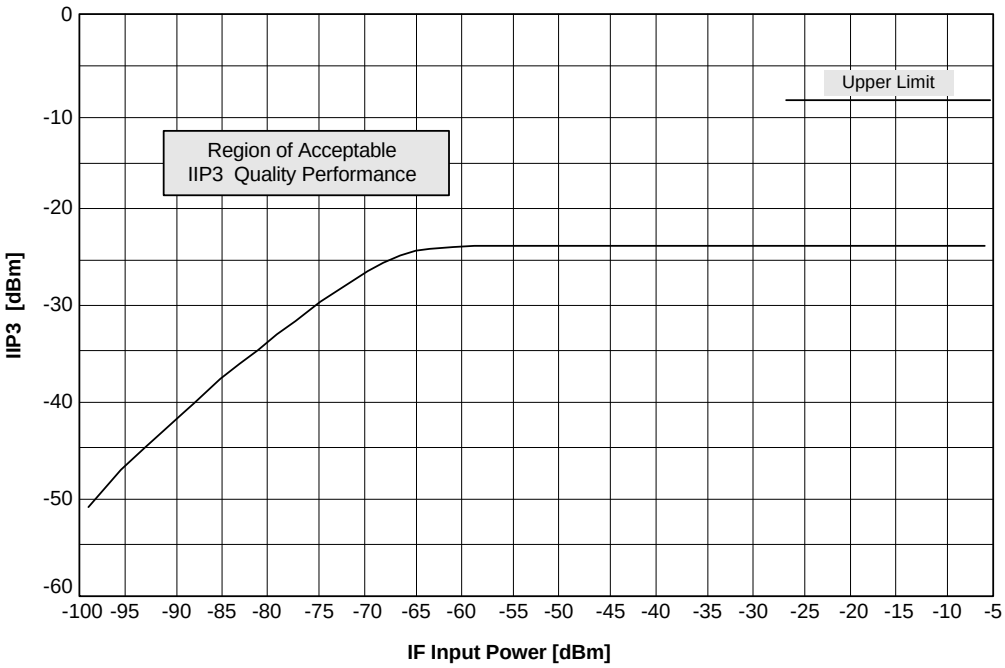


Figure 23. GPS Rx Mode IIP3 Specification

TEST CIRCUIT

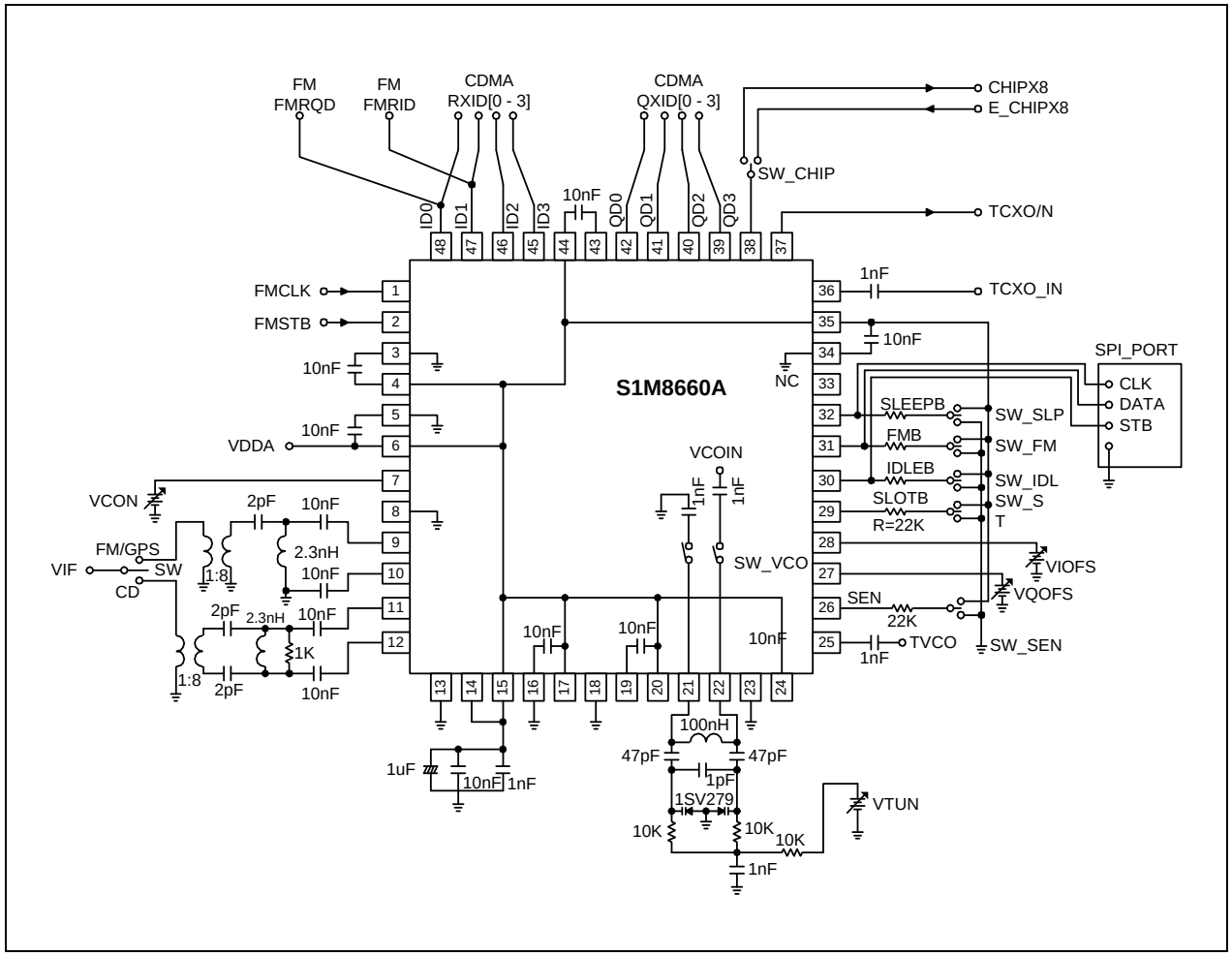


Figure 24. Test Circuit

PACKAGE DEMENSION

48BCC+ Package Outline