

S1D13711 Mobile Graphics Engine

March 2003

The S1D13711 is an LCD controller solution providing support for the digital video revolution in mobile products. The S1D13711 is designed specifically for the GSM cellular phone market where multimedia messaging (MMS) is required. The rich feature set was chosen to off-load the host processor from graphics intensive drawing functions as well as streaming video.

Supporting both an integrated camera interface and serial μ Wire interface, the S1D13711 provides the highest possible integration for the system designer. The Host interface is SRAM "like" and requires no handshaking signals.

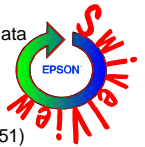
The S1D13711 contains 160K bytes of embedded SRAM used as the image and video buffer. The S1D13711 supports up to two parallel (RAM Integrated) LCD panels to be connected simultaneously. This level of integration provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13711 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

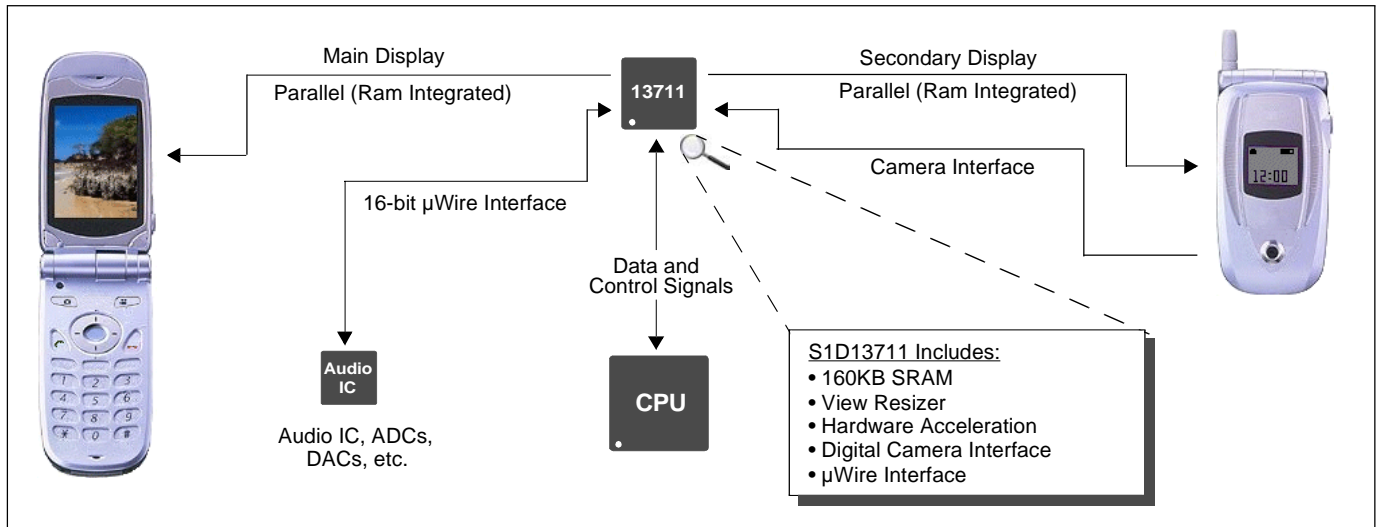
The S1D13711 provides impressive support for cellular and other mobile solutions requiring Digital Video support.

FEATURES

- Embedded 160K byte SRAM Display Buffer
- Low Operating Voltage
- 8-Bit CPU interface
- Support for 2 Parallel I/F Panels
- Programmable resolutions and color depths
- LCD Panel register read capability
- Digital clock input
- μ Wire interface
- YUV to RGB converter
 - Converter can be bypassed to allow storage of 'raw' camera data
- SwivelView™ (90°, 180°, 270° hardware rotation of displayed image)
 - (Patent # 5,734,875 - Patent # 5,956,049 - Patent #6,262,751)
- "Picture-in-Picture Plus"
- 2D Hardware Acceleration Engine
- Software Initiated Power Save Mode



SYSTEM BLOCK DIAGRAM



S1D13711

DESCRIPTION

Integrated Display Buffer

- 160K bytes of embedded SRAM
- Addressable as a single linear address space

CPU Interface

- 8-bit CPU interface
- 13 MHz operation
- Direct addressing

Panel Support

- Supports up to 2 8/16-bit Parallel panels (Ram integrated)
- Maximum resolution of:
 - up to 320x480 at 8 bpp
 - up to 320x240 at 16 bpp

Acceleration

- 2D BitBLT Engine
- SwivelView: 90°, 180°, 270° hardware rotation of displayed image

Display Features

- 8/16 bit-per-pixel (bpp) support
- Picture-in-Picture Plus: displays a variable size window overlaid over the background image
- Overlay Functions
- Pixel Doubling: doubles the effective resolution
- Video Invert: inverts display data
- Virtual Display Support: displays images larger than the panel size through the use of panning

Digital Video

- Camera Interface: YUV 4:2:2 (ITU-R-BT656 compatible) w/resize function
- View hardware resizer with trimming functions
- YUV to RGB converter

Miscellaneous

- Software initiated power save mode
- Multiple General Purpose IO pins
- CORE_{VDD} and HIO_{VDD} 1.8 volts, all other IO_{VDD} 2.75 volts
- FCBGA 120-pin package

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13711 Technical Documentation
- S1D13711 Evaluation Boards
- CPU Independent Software Utilities
- Royalty Free source level driver code



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