

S1D13710 Mobile Graphics Engine

March 2003

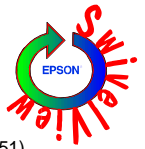
The S1D13710 is an LCD solution designed with support for the digital video revolution in mobile products. The S1D13710 contains an integrated dual port camera interface and hardware JPEG Codec (encoder/decoder). It offers connectivity to both V85E based and 16-bit Generic Asynchronous CPUs. Providing support for up to two LCD panels, the LCD controller supports all standard TFT panel types and parallel/serial ram integrated panels. The S1D13710 with it's 224K bytes of embedded SRAM and rich feature set provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PCs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13710 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

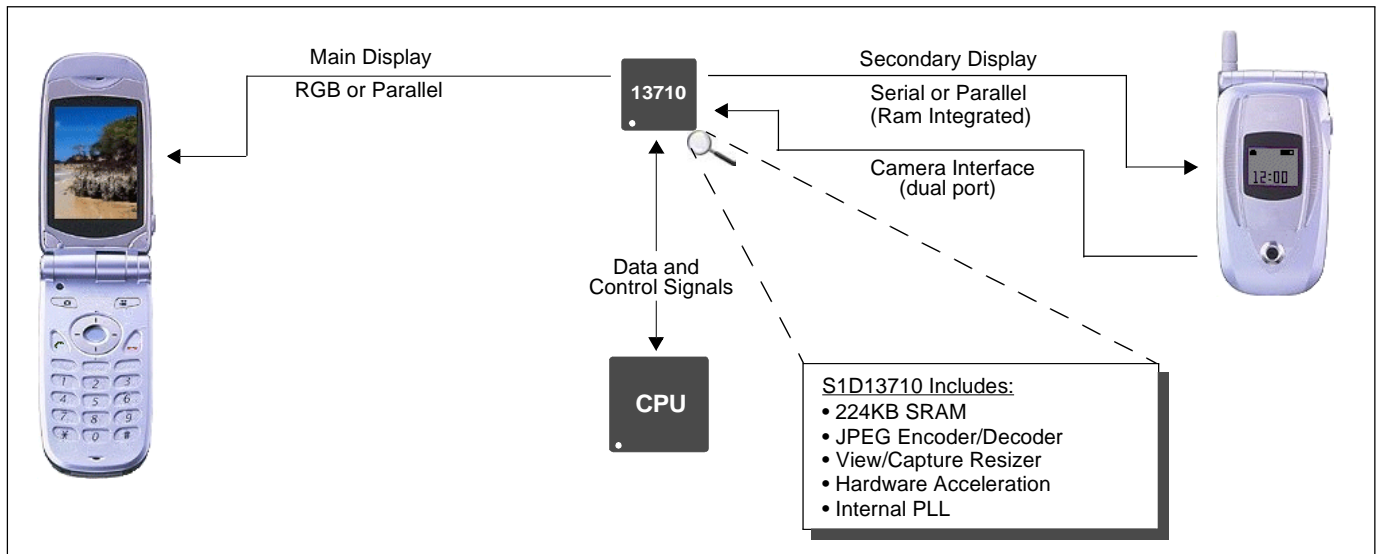
The S1D13710 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to operating system makes it an ideal display solution for a wide variety of applications.

■ FEATURES

- Embedded 224K byte SRAM Display Buffer
- Low Operating Voltage
- Direct V85E and 16-bit Generic CPU interfaces
- Programmable resolutions and color depths
- Support for 2 panels (LCD2 must be RAM integrated)
- Support for RGB, Serial and Parallel interface panels
- Serial Video Interface
- Internal PLL or digital clock input
- Dual port Camera interface w/resize function
- Hardware JPEG encoder/decoder
- YUV to RGB converter
- SwivelView™ (90°, 180°, 270° hardware rotation of displayed image)
 - (Patent # 5,734,875 - Patent # 5,956,049 - Patent #6,262,751)
- "Picture-in-Picture Plus"
- Overlay with Half Transparency
- Mirror Display
- 2D Hardware Acceleration Engine
- Software Initiated Power Save Mode



■ SYSTEM BLOCK DIAGRAM



S1D13710

DESCRIPTION

Integrated Display Buffer

- 224K bytes of embedded SRAM
- Addressable as a single linear address space

CPU Interface

- 16-bit Generic Asynchronous CPU interface
- Direct V85E interface
- Little Endian

Panel Support

- Supports up to 2 LCD panels
 - LCD1: 9/12/18-bit RGB panel
LCD2: 8/9-bit Serial Ram integrated panel
 - LCD1: 8/16/18-bit Parallel Ram integrated panel
LCD2: 8/9-bit Serial Ram integrated panel
 - LCD1: 8/16/18-bit Parallel Ram integrated panel
LCD2: 8/16/18-bit Parallel Ram integrated panel
- Programmable resolutions and color depths
- Typical resolution of 176x240 at 16 bpp with JPEG function enabled

Acceleration

- 2D BitBLT Engine
- SwivelView: 90°, 180°, 270° hardware rotation of displayed image
- Mirror Display

Display Features

- 8/16 bit-per-pixel (bpp) support
- Picture-in-Picture Plus: displays a variable size window overlaid over the background image
- Overlay Function w/ half transparency
- Serial Video Interface
- Video Invert: inverts display data

Digital Video

- Dual port Camera Interface (YUV 4:2:2)
- Hardware JPEG Encoder (YUV 4:2:2)
- Hardware JPEG Decoder (YUV 4:4:4, 4:2:2, 4:1:1, 4:2:0)
- YUV Data Capture (YUV 4:2:2, 4:2:0)
- YUV to RGB converter
- View and Capture hardware resizer with trimming and reduction functions

Miscellaneous

- Internal PLL or digital clock input
- Software initiated power save mode
- Bus Timeout Function
- CORE_{VDD} 1.8 volts and IO_{VDD} 3.0 volts
- FCBGA 161-pin

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13710 Technical Documentation
- S1D13710 Evaluation Boards
- CPU Independent Software Utilities
- Royalty Free source level driver code



Japan
Seiko Epson Corporation
Electronic Devices Marketing Division
421-8, Hino, Hino-shi
Tokyo 191-8501, Japan
Tel: 042-587-5812
Fax: 042-587-5564
<http://www.epson.co.jp/>

Hong Kong
Epson Hong Kong Ltd.
20/F., Harbour Centre
25 Harbour Road
Wanchai, Hong Kong
Tel: 2585-4600
Fax: 2827-4346
<http://www.epson.com.hk/>

North America
Epson Electronics America, Inc.
150 River Oaks Parkway
San Jose, CA 95134, USA
Tel: (408) 922-0200
Fax: (408) 922-0238
<http://www.eea.epson.com/>

Europe
Epson Europe Electronics GmbH
Riesstrasse 15
80992 Munich, Germany
Tel: 089-14005-0
Fax: 089-14005-110
<http://www.epson-electronics.de/>

Taiwan
Epson Taiwan Technology & Trading Ltd.
10F, No. 287
Nanking East Road
Sec. 3, Taipei, Taiwan
Tel: 02-2717-7360
Fax: 02-2712-9164
<http://www.epson.com.tw/>

Singapore
Epson Singapore Pte., Ltd.
No. 1
Temasek Avenue #36-00
Millenia Tower
Singapore, 039192
Tel: 337-7911
Fax: 334-2716
<http://www.epson.com.sg/>

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