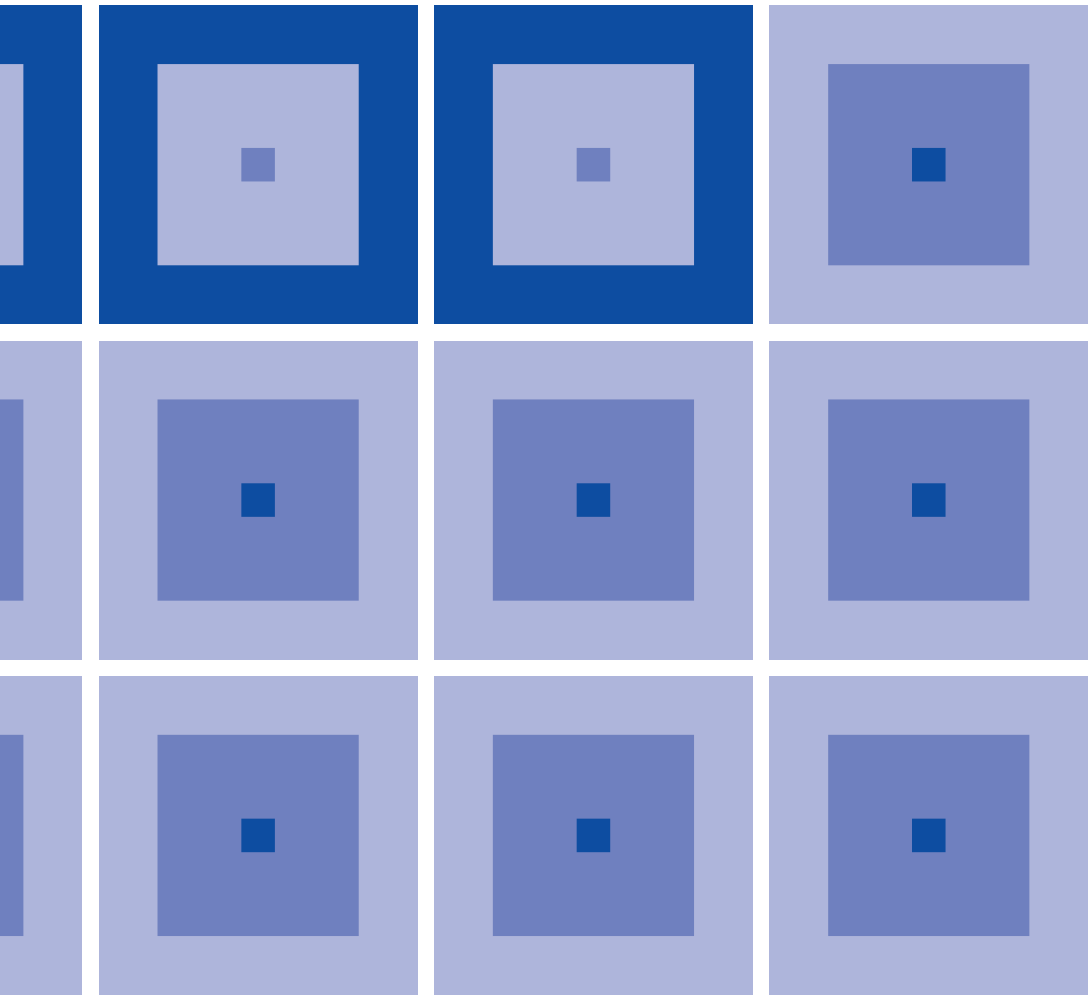
EPSON

ER IC
L2000 Series
nical Manual



ENERGY SAVING EPSON

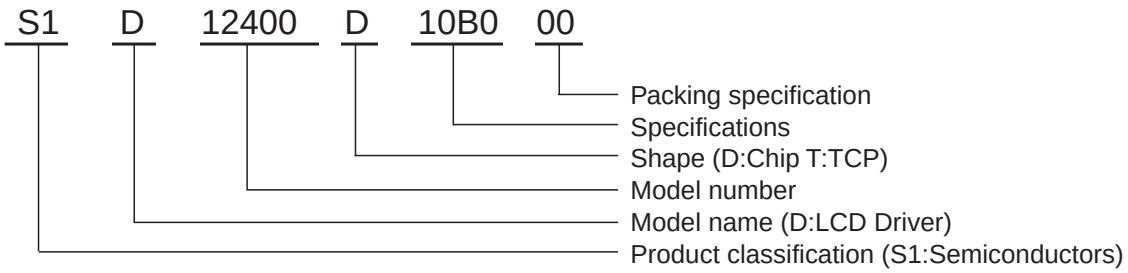
SEIKO EPSON CORPORATION

The information of the product number change

Starting April 1, 2001 the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

●DEVICES



Comparison table between new and previous number

Previous number	New number
SED122*D*A	S1D122**D**A*
SED122*D*B	S1D122**D**B*
SED122*DA*	S1D122**D10**
SED122*T**	S1D122**T****
SED1220	S1D12200
SED1221	S1D12201
SED1222	S1D12202
SED1220D**	S1D12200D****
SED1220DAB	S1D12200D10B*
SED1220DB*	S1D12200D11**
SED1220DG*	S1D12200D16**
SED1221D**	S1D12201D****
SED1222D**	S1D12202D****
SED1222D*A	S1D12202D**A*
SED122A	S1D12210
SED1225	S1D12205 Series
SED1225D**	S1D12205D****
SED1225D*B	S1D12205D**B*
SED1225DAB	S1D12205D10B*
SED1225DBB	S1D12205D11B*
SED1225DGB	S1D12205D16B*
SED1225T**	S1D12205T****
SED123*	S1D123**
SED123*D**	S1D123**D****

Previous number	New number
SED123*D*A	S1D123**D**A*
SED123*D*B	S1D123**D**B*
SED123*D*C	S1D123**D**C*
SED123*D*E	S1D123**D**E*
SED123*D*F	S1D123**D**F*
SED123*D*G	S1D123**D**G*
SED123*DA*	S1D123**D10**
SED123*DB*	S1D123**D11**
SED123*DG*	S1D123**D16**
SED123*T**	S1D123**T****
SED1230	S1D12300
SED1230D**	S1D12300D****
SED1230DBB	S1D12300D11B*
SED1230DGB	S1D12300D16B*
SED1230DGE	S1D12300D16E*
SED1230DJB	S1D12300D19B*
SED1230DRE	S1D12300D27E*
SED1230T01	S1D12300T001*
SED1230T0A	S1D12300T00A*
SED1230T0B	S1D12300T00B*
SED1231	S1D12301
SED1231D**	S1D12301D****
SED1231DAB	S1D12301D10B*
SED1231DBE	S1D12301D11E*

Previous number	New number
SED1231DJB	S1D12301D19B*
SED1231DMB	S1D12301D22B*
SED1231T01	S1D12301T001*
SED1231T02	S1D12301T002*
SED1231T0B	S1D12301T00B*
SED1232	S1D12302
SED1232D**	S1D12302D****
SED1232DAB	S1D12302D10B*
SED1232DBB	S1D12302D11B*
SED1232DGB	S1D12302D16B*
SED1232DMB	S1D12302D22B*
SED1233	S1D12303
SED1233D**	S1D12303D****
SED1233D2E	S1D12303D02E*
SED1233D3E	S1D12303D03E*
SED1233DAE	S1D12303D10E*
SED1233DBB	S1D12303D11B*
SED1233DBE	S1D12303D11E*
SED1233DGB	S1D12303D16B*
SED1233DGE	S1D12303D16E*
SED1233DMB	S1D12303D22B*
SED1233DRA	S1D12303D27A*
SED1233T0A	S1D12303T00A*
SED1233T0B	S1D12303T00B*
SED123*D*A	S1D123**D**A*
SED123*D*B	S1D123**D**B*
SED123*D*C	S1D123**D**C*
SED123*D*F	S1D123**D**F*
SED123*D..	S1D123**D****
SED123*DA*	S1D123**D10**
SED123*DB*	S1D123**D11**
SED123*DG*	S1D123**D16**
SED1234	S1D12304
SED1234D**	S1D12304D****
SED1234DBA	S1D12304D11A*
SED1235	S1D12305
SED1235D2C	S1D12305D02C*
SED1235DAA	S1D12305D10A*
SED1235DBA	S1D12305D11A*
SED1235DGA	S1D12305D16A*
SED124*D**	S1D124**D****
SED124*T**	S1D124**T****
SED1240	S1D12400

Previous number	New number
SED1240D0A	S1D12400D00A*
SED1240DAB	S1D12400D10B*
SED1240DBB	S1D12400D11B*
SED1240DGB	S1D12400D16B*
SED1240T0A	S1D12400T00A*
SED1240T0B	S1D12400T00B*
SED1240T0G	S1D12400T00G*
SED1241	S1D12401
SED1241DAB	S1D12401D10B*
SED1241DBB	S1D12401D11B*
SED1241DGB	S1D12401D16B*
SED1241T0A	S1D12401T00A*
SED1241T0B	S1D12401T00B*
SED1241T0G	S1D12401T00G*
SED1242	S1D12402
SED1242DAB	S1D12402D10B*
SED1242DBB	S1D12402D11B*
SED1242DGB	S1D12402D16B*
SED1242T0A	S1D12402T00A*
SED1242T0B	S1D12402T00B*
SED1242T0G	S1D12402T00G*
SED1242TXX	S1D12402T****

CONTENTS

S1D12000 series
Selection Guide

■ LCD controller-drivers for small-sized displays

Built-in character generators together with segment and common drivers simplify the task of displaying microprocessor messages on small LCDs.

S1D12000 (SED1200) Series

Part number	Supply voltage	LCD voltage range (V)	Duty	Segment	Common	Display RAM (characters)	MPU interface	Extension display output	Package	Comment
S1D12200D (SED1220D)	2.4 to 3.6	4.0 to 7.0	1/26	64	26	36	4 or 8-bit serial	—	Au bump chip	Built-in power circuit for LCD Three standard characters (JIS,ASCII,Cellular) LCD static drive allowed
S1D12200T (SED1220T)									TCP	
S1D12201D (SED1221D)	2.4 to 3.6	4.0 to 7.0	1/18	64	18	36	4 or 8-bit serial	—	Au bump chip	
S1D12201T (SED1221T)									TCP	
S1D12202D (SED1222D)	2.4 to 3.6	4.0 to 7.0	1/18	60	18	36	4 or 8-bit serial	—	Al pad chip	
S1D12210D** (SED122AD*)	2.4 to 3.6	4.0 to 7.0	1/18	64	18	36	4 or 8-bit serial	—	Au bump chip	
S1D12205D (SED1225D)	1.7 to 3.6	3.0 to 6.0	1/18,1/26	64	26	36	4 or 8-bit serial	—	Au bump chip	
S1D12205T (SED1225T)									TCP	
S1D12300D (SED1230D)	2.4 to 3.6	4.5 to 11.0	1/30	65	30	48	4 or 8-bit serial	—	Au bump chip	
S1D12300T (SED1230T)									TCP	
S1D12301D (SED1231D)	2.4 to 3.6	4.5 to 11.0	1/23	65	23	48	4 or 8-bit serial	—	Au bump chip	
S1D12301T (SED1231T)									TCP	
S1D12302D (SED1232D)	2.4 to 3.6	4.5 to 11.0	1/16	65	16	48	4 or 8-bit serial	—	Au bump chip	
S1D12302T (SED1232T)									TCP	
S1D12303D (SED1233D)	2.4 to 3.6	4.5 to 11.0	1/16	80	16	48	4 or 8-bit serial	—	Au bump chip	
S1D12303T (SED1233T)									TCP	
S1D12304D (SED1234D)	2.4 to 3.6	4.5 to 11.0	1/30	62	30	48	4 or 8-bit serial	—	Al pad chip	Built-in power circuit for LCD Three standard characters (JIS,ASCII,Cellular) LCD dynamic drive only
S1D12305D (SED1235D)	2.4 to 3.6	4.5 to 11.0	1/16	62	16	48	4 or 8-bit serial	—	Al pad chip	
S1D12400D (SED1240D)	1.8 to 5.5	4.0 to 16.0	1/34	80	34	80	4 or 8-bit serial	—	Au bump chip	Line Blink, Vertical Scroll
S1D12400T (SED1240T)									TCP	
S1D12401D (SED1241D)	1.8 to 5.5	4.0~16.0	1/26	80	26	80	4 or 8-bit serial	—	Au bump chip	
S1D12401T (SED1240T)									TCP	
S1D12402D (SED1242D)	1.8 to 5.5	4.0 to 16.0	1/18	80	18	80	4 or 8-bit serial	—	Au bump chip	
S1D12402T (SED1242T)									TCP	

S1D12200 Series

Rev. 1.4

Contents

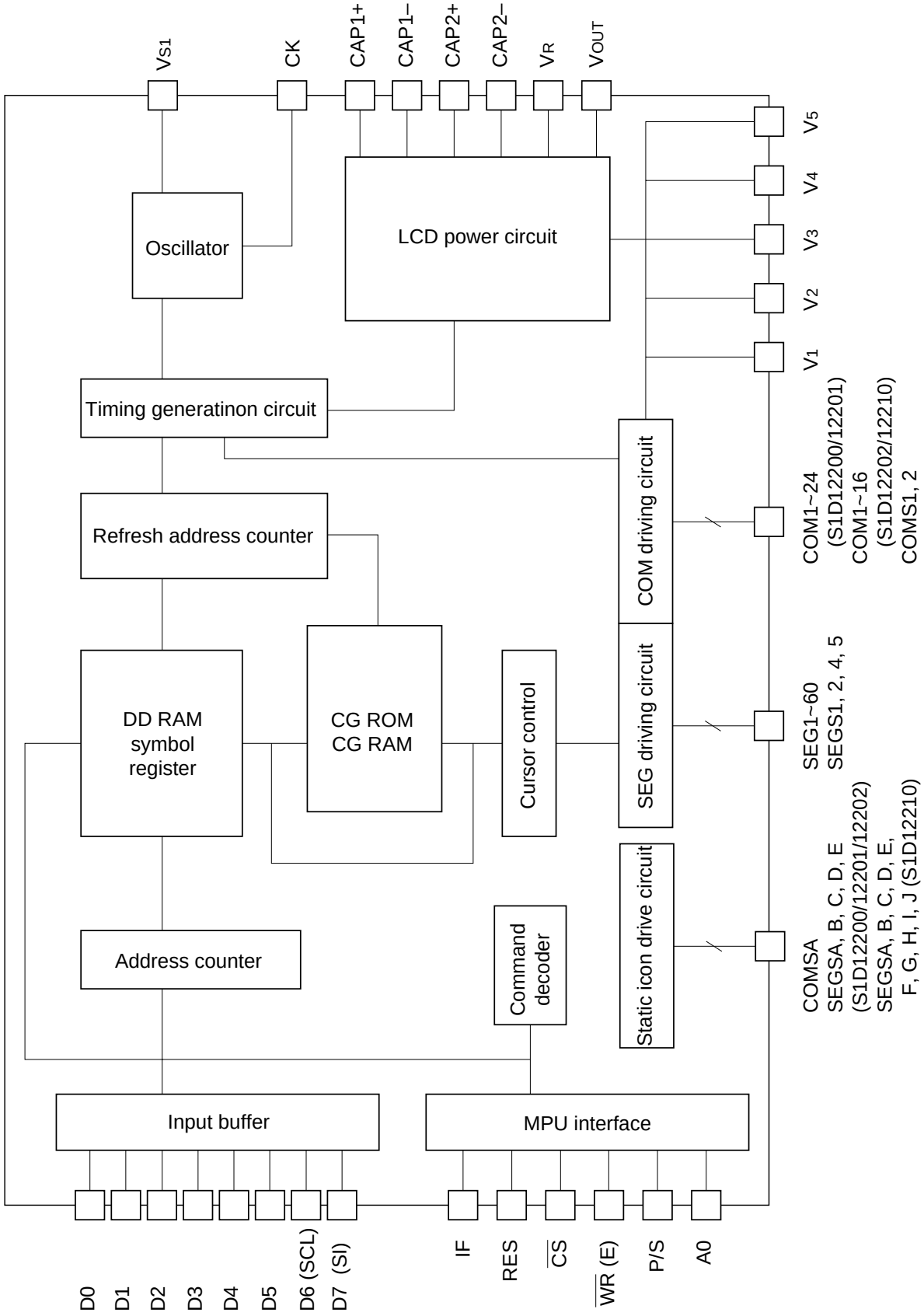
1. DESCRIPTION

S1D12200 Series is a dot matrix LCD controller/driver for character display. Using 4bits data, 8bits data or serial data being provided from the micro computer, it displays up to 36 characters, 4 user defined characters and up to 120 symbols.
Up to 256 types of built-in character generator ROMs are prepared. Each character font is consisted of 5 × 8 dots. It also contains the RAM for displaying 4 user defined characters each font consisting of 5 × 8 dots. It is symbol register allows character display with high degree of freedom. This handy equipment can be operated with minimum power consumption with its low power consumption design, standby and sleeping mode.

2. FEATURES

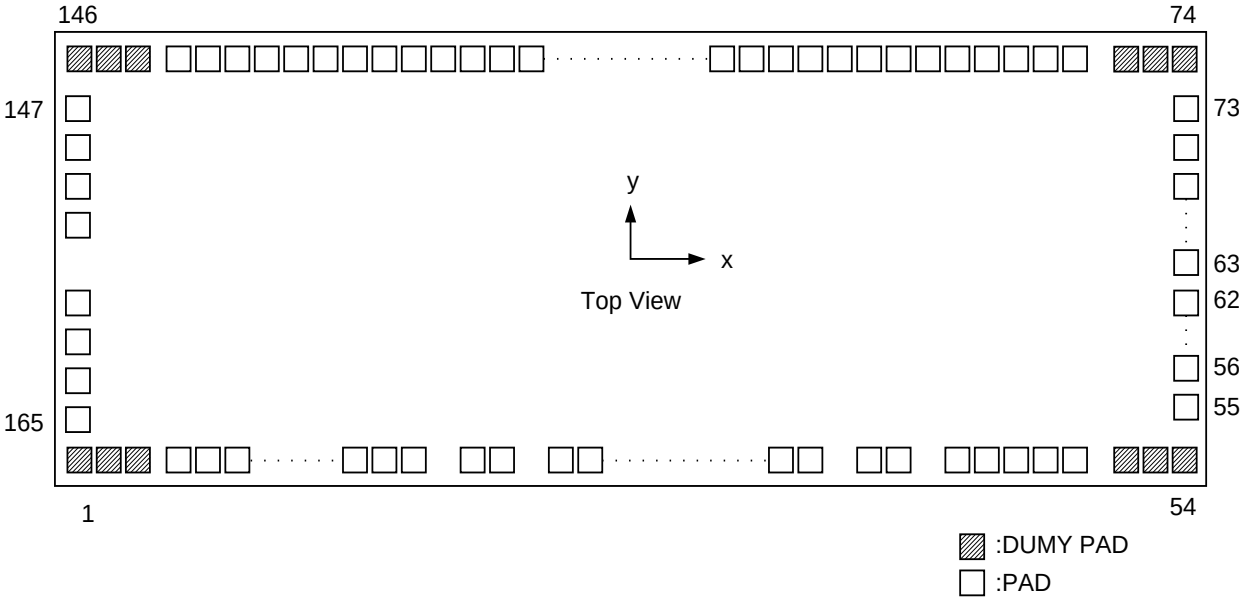
- Built-in data display RAM – 36 characters + 4 user defined characters + 120 symbols.
- CG ROM (For up to 256 characters), CG RAM (for 4 characters) and symbol register (for 120 symbols).
- No. of display digit and lines
  < In normal mode >
  ① (12 digits + 4 segments for signal) × 3 lines + 120 symbols + 5 static symbols (S1D12200D∗∗∗∗)
  ② (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 5 static symbols (S1D12201D∗∗∗∗)
  ③ 12 digits × 2 lines + 120 symbols + 5 static symbols (S1D12202D∗∗∗∗)
  ④ (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 10 static symbols (S1D12210D∗∗∗∗)
  < In standby mode >
  ① 5 static symbols
  ② 5 static symbols
  ③ 5 static symbols
  ④ 10 static symbols
- Built-in CR oscillation circuit (C and R contained)
- Accepts external clock input
- High-speed MPU interface
  Affords interface with both 68/80 system MPUs
  Affords interface through 4 bits and 8 bits
- Affords serial interface
- Character font consists of 5 × 8 dots
- Duty ratio ① 1/26 (S1D12200D∗∗∗∗)
  ② 1/18 (S1D12201D∗∗∗∗, S1D12202D∗∗∗∗)
- Simplified command setting
- Built-in power circuit for driving liquid crystal
  Power amplifier circuit, power regulation circuit and voltage followers × 4
- Built-in electronic volume function
- Low power consumption
  80 µA max. (In normal operation, including operating current of the power supply).
  20 µA max. (In standby mode for displaying static icon).
  5 µA max. (In sleeping mode when display is turned off).
- Power supply
  V_{DD} - V_{SS} – 2.4 V ~ – 3.6 V
  V_{DD} - V_5 – 4.0 V ~ – 6.0 V
- Temperature range for wide range operation
  Ta = – 30 ~ 85°C
- CMOS process
- Shipping form
  Chip (Al pad product) S1D12202D∗∗A∗
  Chip (Au bump product) S1D122∗∗D∗∗B∗
  TCP S1D122∗∗T∗∗∗∗
- These chips are not designed for resistance to light or resistance to rediation

3. BLOCK DIAGRAM



4. CHIP SPECIFICATION

S1D12200D****/S1D12201D****/S1D12210D****



S1D122∗∗D∗∗∗∗

Digits prepared for CGROM pattern changes

Chip size:	7.70 × 2.77 mm
Pad pitch:	100 µm (Minimum)
Chip thickness (for reference):	625 ± 25 µm (S1D122∗∗D∗∗A∗)
	(S1D122∗∗D∗∗B∗)

1) A1 pad specifications

Pad size on Y side:	135 µm × 75 µm
Pad size on X side:	75 µm × 135 µm

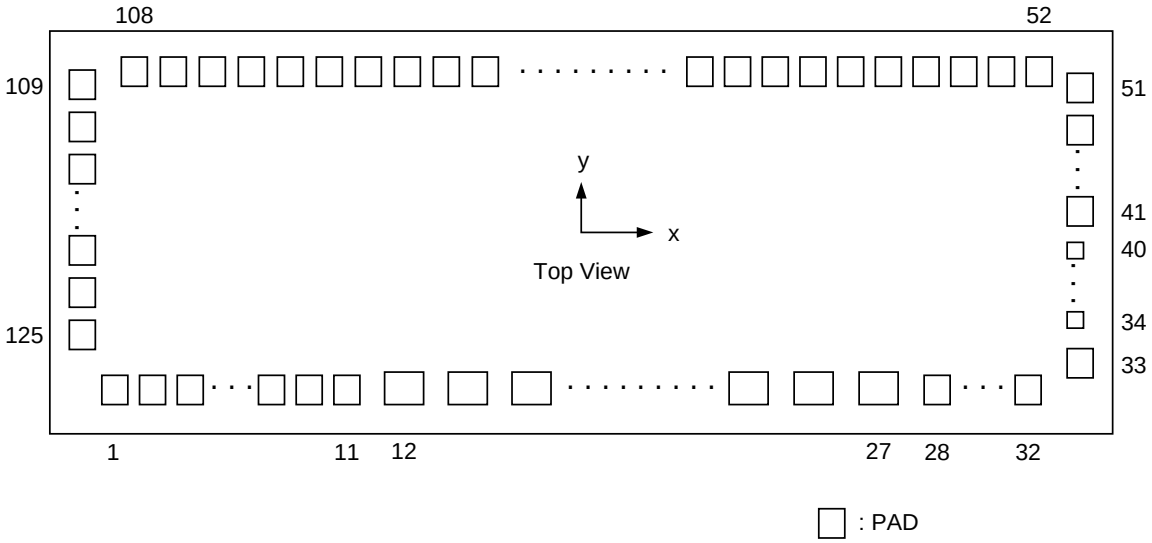
2) Au bump specifications

Bump size on Y side:	129 µm × 69 µm
Bump size on X side:	69 µm × 129 µm
Bump height (for reference)	22.5 µm ± 5.5 µm

<Fuse Pines>

1) Al pad. pad size 86 µm × 75 µm
2) Au bump
   Bump size 80 µm × 69 µm

S1D12202D****



S1D12202D****
↑
Digits prepared for CGROM pattern changes

Chip size: 7.70 × 2.77 mm
Pad pitch: 124 µm (Minimum)
Chip thickness (for reference): 625 ± 50 µm (S1D12202D**A*)

1) A1 pad specifications
Pad size on Y side: 90 µm × 96 µm
Pad size on X side: 96 µm × 90 µm (PAD. No. 1 ~ 11, 28 ~ 32, 52 ~ 108)
175 µm ×135 µm (PAD. No. 12 ~ 27)

<Fuse Pines>
1) Al pad. pad size 86 µm × 75 µm

<S1D12200D**/S1D12201D****>**

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	NC	–3700	–1204	55	V_{DD}	3670	–910
2	NC	–3600	↑	56	(FSA)	3603	–796
3	NC	–3500	↑	57	(FSB)	↑	–696
4	$\overline{A0}$	–3252	↑	58	(FSC)	↑	–596
5	$\overline{WR}$	–3132	↑	59	(FS0)	↑	–496
6	$\overline{CS}$	–3012	↑	60	(FS1)	↑	–396
7	D7	–2892	↑	61	(FS2)	↓	–296
8	D6	–2772	↑	62	(FS3)	3603	–196
9	D5	–2652	↑	63	V_{DD}	3670	–82
10	D4	–2532	↑	64	COMSA	↑	61
11	D3	–2412	↑	65	COMS1	↑	203
12	D2	–2292	↑	66	COM1	↑	303
13	D1	–2172	↑	67	COM2	↑	403
14	D0	–2052	↑	68	COM3	↑	503
15	V_{DD}	–1836	↑	69	COM4	↑	603
16	V_{DD}	–1736	↑	70	COM5	↑	703
17	V_{SS}	–1556	↑	71	COM6	↑	803
18	V_{SS}	–1456	↑	72	COM7	↓	903
19	V_5	–1276	↑	73	COM8	3670	1003
20	V_5	–1176	↑	74	NC	3700	1204
21	V_4	–996	↑	75	NC	3600	↑
22	V_4	–896	↑	76	NC	3500	↑
23	V_3	–716	↑	77	SEGS1	3319	↑
24	V_3	–616	↑	78	SEGS2	3219	↑
25	V_2	–436	↑	79	SEG1	3119	↑
26	V_2	–336	↑	80	SEG2	3019	↑
27	V_1	–156	↑	81	SEG3	2919	↑
28	V_1	–56	↑	82	SEG4	2819	↑
29	V_0	124	↑	83	SEG5	2719	↑
30	V_0	224	↑	84	SEG6	2619	↑
31	V_R	404	↑	85	SEG7	2519	↑
32	V_R	504	↑	86	SEG8	2419	↑
33	V_{OUT}	684	↑	87	SEG9	2319	↑
34	V_{OUT}	784	↑	88	SEG10	2219	↑
35	CAP2–	964	↑	89	SEG11	2119	↑
36	CAP2–	1064	↑	90	SEG12	2019	↑
37	CAP2+	1244	↑	91	SEG13	1919	↑
38	CAP2+	1344	↑	92	SEG14	1819	↑
39	CAP1–	1524	↑	93	SEG15	1719	↑
40	CAP1–	1624	↑	94	SEG16	1619	↑
41	CAP1+	1804	↑	95	SEG17	1519	↑
42	CAP1+	1904	↑	96	SEG18	1419	↑
43	V_{SS}	2084	↑	97	SEG19	1319	↑
44	V_{SS}	2184	↑	98	SEG20	1219	↑
45	V_{DD}	2364	↑	99	SEG21	1119	↑
46	V_{DD}	2464	↑	100	SEG22	1019	↑
47	CK	2693	↑	101	SEG23	919	↑
48	VS1	2821	↑	102	SEG24	819	↑
49	P/S	2949	↑	103	SEG25	719	↑
50	I/F	3077	↑	104	SEG26	619	↑
51	RES	3205	↑	105	SEG27	519	↑
52	NC	3500	↑	106	SEG28	419	↑
53	NC	3600	↓	107	SEG29	319	↓
54	NC	3700	–1204	108	SEG30	219	1204

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG31	119	1204
110	SEG32	19	↑
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	COM24	–3081	
142	COM23	–3181	
143	COM22	–3281	
144	NC	–3500	
145	NC	–3600	↓
146	NC	–3700	1204
147	COM21	–3670	1000
148	COM20	↑	900
149	COM19		800
150	COM18		700
151	COM17		600
152	COM16		500
153	COM15		400
154	COM14		300
155	COM13		200
156	COM12		100
157	COM11		0
158	COM10		–100
159	COM9		–200
160	COMS2		–300
161	SEGSA		–433
162	SEGSB		–533
163	SEGSC		–633
164	SEGSD	↓	–733
165	SEGSE	–3670	–833

<S1D12202D**>**

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	$\overline{A0}$	–3312	–1228	55	SEG4	3100	1228
2	$\overline{WR}$	–3180	↑	56	SEG5	2976	↑
3	CS	–3048		57	SEG6	2852	
4	D7	–2916		58	SEG7	2728	
5	D6	–2784		59	SEG8	2604	
6	D5	–2652		60	SEG9	2480	
7	D4	–2520		61	SEG10	2356	
8	D3	–2388		62	SEG11	2232	
9	D2	–2256		63	SEG12	2108	
10	D1	–2124	↓	64	SEG13	1984	
11	D0	–1992	–1228	65	SEG14	1860	
12	V_{DD}	–1786	–1204	66	SEG15	1736	
13	V_{SS}	–1506	↑	67	SEG16	1612	
14	V_5	–1226		68	SEG17	1488	
15	V_4	–946		69	SEG18	1364	
16	V_3	–666		70	SEG19	1240	
17	V_2	–386		71	SEG20	1116	
18	V_1	–106		72	SEG21	992	
19	V_0	174		73	SEG22	868	
20	V_R	454		74	SEG23	744	
21	V_{OUT}	734		75	SEG24	620	
22	CAP2–	1014		76	SEG25	496	
23	CAP2+	1294		77	SEG26	372	
24	CAP1–	1574		78	SEG27	248	
25	CAP1+	1854		79	SEG28	124	
26	V_{SS}	2134	↓	80	SEG29	0	
27	V_{DD}	2414	–1204	81	SEG30	–124	
28	$\overline{CK}$	2692	–1228	82	SEG31	–248	
29	VS1	2836	↑	83	SEG32	–372	
30	P/S	2980		84	SEG33	–496	
31	I/F	3124	↓	85	SEG34	–620	
32	RES	3268	–1228	86	SEG35	–744	
33	V_{DD}	3694	–919	87	SEG36	–868	
34	(FSA)	3603	–796	88	SEG37	–992	
35	(FSB)	↑	–696	89	SEG38	–1116	
36	(FSC)		–596	90	SEG39	–1240	
37	(FS0)		–496	91	SEG40	–1364	
38	(FS1)		–396	92	SEG41	–1488	
39	(FS2)	↓	–296	93	SEG42	–1612	
40	(FS3)	3603	–196	94	SEG43	–1736	
41	V_{DD}	3694	–73	95	SEG44	–1860	
42	COMSA	↑	63	96	SEG45	–1984	
43	COMS1		199	97	SEG46	–2108	
44	COM1		323	98	SEG47	–2232	
45	COM2		447	99	SEG48	–2356	
46	COM3		571	100	SEG49	–2480	
47	COM4		695	101	SEG50	–2604	
48	COM5		819	102	SEG51	–2728	
49	COM6		943	103	SEG52	–2852	
50	COM7	↓	1067	104	SEG53	–2976	
51	COM8	3694	1191	105	SEG54	–3100	
52	SEG1	3472	1228	106	SEG55	–3224	
53	SEG2	3348	1228	107	SEG56	–3348	↓
54	SEG3	3224	1228	108	SEG57	–3472	1228

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG58	–3694	1191
110	SEG59		1067
111	SEG60		943
112	COM16		819
113	COM15		695
114	COM14		571
115	COM13		447
116	COM12		323
117	COM11		119
118	COM10		75
119	COM9		–49
120	COMS2		–173
121	SEGSA		–335
122	SEGSB		–459
123	SEGSC		–583
124	SEGSD		–707
125	SEGSE	–3694	–831

<S1D12210D**>**

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	NC	–3700	–1204
2	NC	–3600	
3	NC	–3500	
4	A0	–3252	
5	WR	–3132	
6	CS	–3012	
7	D7	–2892	
8	D6	–2772	
9	D5	–2652	
10	D4	–2532	
11	D3	–2412	
12	D2	–2292	
13	D1	–2172	
14	D0	–2052	
15	V_{DD}	–1836	
16	V_{DD}	–1736	
17	V_{SS}	–1556	
18	V_{SS}	–1456	
19	V_5	–1276	
20	V_5	–1176	
21	V_4	–996	
22	V_4	–896	
23	V_3	–716	
24	V_3	–616	
25	V_2	–436	
26	V_2	–336	
27	V_1	–156	
28	V_1	–56	
29	V_0	124	
30	V_0	224	
31	V_R	404	
32	V_R	504	
33	V_{OUT}	684	
34	V_{OUT}	784	
35	CAP2–	964	
36	CAP2–	1064	
37	CAP2+	1244	
38	CAP2+	1344	
39	CAP1–	1524	
40	CAP1–	1624	
41	CAP1+	1804	
42	CAP1+	1904	
43	V_{SS}	2084	
44	V_{SS}	2184	
45	V_{DD}	2364	
46	V_{DD}	2464	
47	CK	2693	
48	VS1	2821	
49	P/S	2949	
50	I/F	3077	
51	RES	3205	
52	NC	3500	
53	NC	3600	
54	NC	3700	–1204

PAD		COORDINATES	
No.	Name	X	Y
55	V_{DD}	3670	–910
56	(FSA)	3603	–796
57	(FSB)		–696
58	(FSC)		–596
59	(FS0)		–496
60	(FS1)		–396
61	(FS2)		–296
62	(FS3)	3603	–196
63	V_{DD}	3670	–82
64	COMSA		61
65	COMS1		203
66	COM1		303
67	COM2		403
68	COM3		503
69	COM4		603
70	COM5		703
71	COM6		803
72	COM7		903
73	COM8	3670	1003
74	NC	3700	1204
75	NC	3600	
76	NC	3500	
77	SEGS1	3319	
78	SEGS2	3219	
79	SEG1	3119	
80	SEG2	3019	
81	SEG3	2919	
82	SEG4	2819	
83	SEG5	2719	
84	SEG6	2619	
85	SEG7	2519	
86	SEG8	2419	
87	SEG9	2319	
88	SEG10	2219	
89	SEG11	2119	
90	SEG12	2019	
91	SEG13	1919	
92	SEG14	1819	
93	SEG15	1719	
94	SEG16	1619	
95	SEG17	1519	
96	SEG18	1419	
97	SEG19	1319	
98	SEG20	1219	
99	SEG21	1119	
100	SEG22	1019	
101	SEG23	919	
102	SEG24	819	
103	SEG25	719	
104	SEG26	619	
105	SEG27	519	
106	SEG28	419	
107	SEG29	319	
108	SEG30	219	1204

(FS*) : This is a fuse adjusting terminal. Set it to floating state.
CK pins : Set it to V_{DD} when not used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG31	119	1204
110	SEG32	19	↑
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	NC	–3081	
142	NC	–3181	
143	NC	–3281	
144	NC	–3500	
145	NC	–3600	↓
146	NC	–3700	1204
147	COM16	–3670	1000
148	COM15	↑	900
149	COM14		800
150	COM13		700
151	COM12		600
152	COM11		500
153	COM10		400
154	COM9		300
155	COMS2		200
156	SEGSA		67
157	SEGSB		–33
158	SEGSC		–133
159	SEGSD		–233
160	SEGSE		–333
161	SEGSF		–433
162	SEGSG		–533
163	SEGSH		–633
164	SEGSI	↓	–733
165	SEGSJ	–3670	–833

5. PIN DESCRIPTION

Power Supply Pins

Pin name	I/O	Description	No. of Pins
V_{DD}	Power supply	Connected to logic supply. Common with MPU power terminal V_{CC}.	1
V_{SS}	Power supply	0V power terminal connected to system ground.	1
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ (1/4 V_5) $V_2 = 2/5\ V_5$ (2/4 V_5) $V_3 = 3/5\ V_5$ (3/4 V_5) $V_4 = 4/5\ V_5$ (4/4 V_5) voltage ratings in ( ) are for optinal choices.	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit, and DC/DC source. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	No. of Pins
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{DD} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = LOW, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><th>P/S</th><th>RES</th><th>I/F</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3-D0</th><th>$\overline{CS}$</th><th>A0</th><th>$\overline{WR}$</th></tr>
<tr><td>LOW</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>—</td><td>—</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LOW</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
RES: Indicates the active potential.
OPEN: Though “OPEN” is available, fixing the potential is recommended for noise-withstnading characteristical reason.
—: Indicates that it can be set at either HIGH or LOW, but fixing the potential is required.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ↓. In case of an 80 series MPU, initialization can be performed by changing ↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
LOW : 68 series MPU interface
HIGH : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the LOW level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active LOW. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
<When connecting a 68 series MPU>
Active HIGH. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>–</td></tr>
<tr><td>LOW</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
HIGH: 8-bit parallel input
LOW: 4-bit parallel input
When P/S = LOW, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
<tr><td>CK</td><td>I</td><td>External input terminal
It must be fixed to HIGH when the internal oscillation circuit is used.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic drive terminal (S1D12200D✱✱✱✱/S1D12201D✱✱✱✱/S1D12210D✱✱✱✱)

Pin name	I/O	Description	No. of Pins
COM1 to COM24	O	Common signal output pin (for characters)	24
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1 to SEG60	O	Segment signal output pin (for characters)	60
SEGS1, 2 4, 5	O	Segment signal output pin (except for characters) SEGS1, SEGS2: Segment output for signal output	4

Dynamic drive terminal (S1D12202D✱✱✱✱)

Pin name	I/O	Description	No. of Pins
COM1 to COM16	O	Common signal output pin (for characters)	16
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1 to SEG60	O	Segment signal output pin (for characters)	60

Static drive terminal

Pin name	I/O	Description	No. of Pins
COMSA	O	Common signal output pin (for icon)	1
SEGSA, B C, D, E F, G, H, I, J	O	Segment signal output pin (for icon) SEGSF, G, H, I, J (only S1D12210✱✱✱✱)	5 to 10

Note: For the electrode of liquid crystal display panel to be connected to the static drive terminal, we recommend you to use a pattern in which it is separated from the electrode connected to the dynamic drive terminal. When this pattern is too close to the other electrode, both the liquid crystal display and electrode will be deteriorated.

6. FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the S1D12200 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting HIGH or LOW as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0 to D7
HIGH	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0 to D7
LOW	Serial Input	$\overline{CS}$	A0	HIGH, LOW	SI	SCL	—

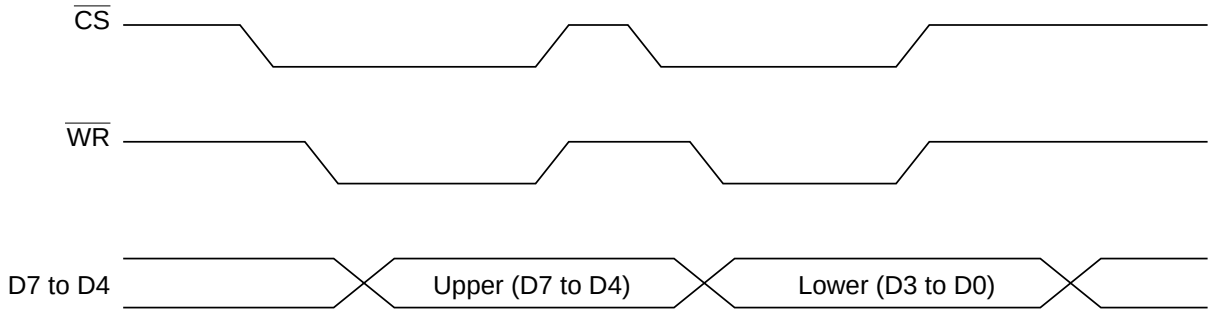
Parallel Input
In the S1D12200 Series, when parallel input is selected (P/S = HIGH), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either HIGH or LOW is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
↓ active	68 series	A0	E	$\overline{CS}$	D0 to D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0 toD7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = LOW)

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = LOW).
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = HIGH, it is regarded as display data. When A0 = LOW, it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

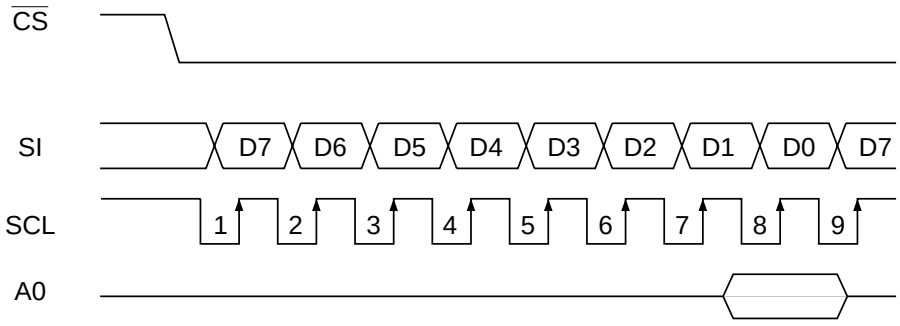


Fig. 1

Identification of data bus signals

The S1D12200 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The S1D12200 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = LOW, MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the S1D12200 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

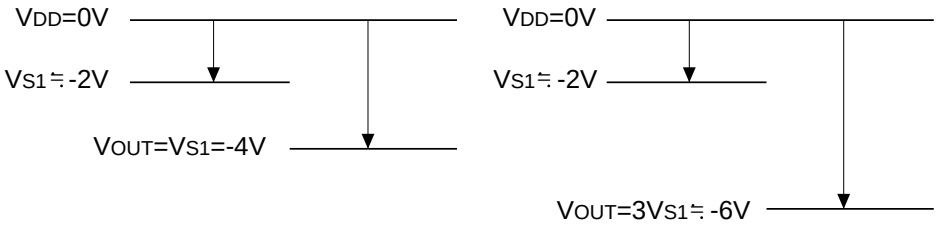
A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Booster circuit	Voltage regulating circuit	Voltage follower	External voltage input	Booster system pin
	○	○	○	—	Per specification
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Voltage Tripler Circuit

If capacitors are connected between CAP+1 – CAP–1 and CAP2+,CAP2– and VSS VOUT, VDD– VSS potential is negatively tripled and generated at VOUT terminal. When the voltage is boosted double, open CAP2+ and connect CAP2– to VOUT terminal.
At this time, the oscillating circuit must be operating since the amplifying circuit utilize the signal from the oscillation output.



Potential relationship of amplified voltage

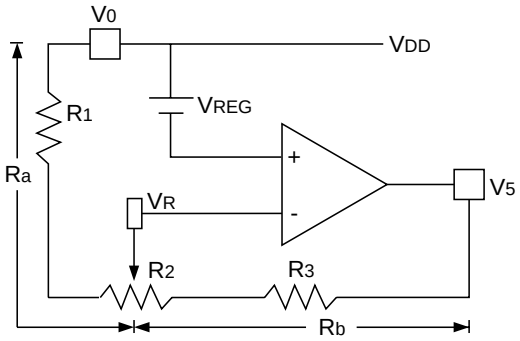
Voltage regulating circuit

Amplified voltage generated at VOUT outputs liquid crystal drive voltage V5 through the voltage regulation circuit.V5 voltage can be obtained from the expression ① below by adjusting the resistors Ra and Rb within the range of V5<VOUT.calculated by the following formula:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

Where, VREG is the constant power supply within IC. VREG is maintained constantly at VREG ≒ 2.0V. Voltage regulation of V5 output is done by connecting to a variable register between VR, VDD and V5. It is recommended to combine fixed registers R1 and R3 with variable resistor R2 for fine adjustment of V5 voltage.

[Sample setting on R1, R2 and R3]
- R1 + R2 + R3 = 1.2 M ohm (decided from the current value I05 passed between VDD – V5. Where, I05≤5 µA is supposed).
- Variable voltage range provided by R2 is from –4V to –6V (to be decided considering charecteristics of the liquid crystal).
- Since VREG = 2.0V, if the electronic volume register is set at (0, 0, 0, 0, 0), followings are derived from above conditions and expression ① :



R1 = 400KΩ
R2 = 200KΩ
R3 = 600KΩ

The voltage regulation circuit outputs VREG with the temperature gradient of approximately –0.04%/°C.
Since VR terminal has high input impedance, anti-noise measures must be considered including use of shortened wiring distance and shield wire.

● Voltage Regulation Circuit Using Electronic Volume Function

The electronic volume function allows to control the liquid crystal drive voltage V_5 with the commands and thus to adjust density of the liquid crystal display. Liquid crystal drive voltage V_5 can have one of 32 voltage values if 5-bit data is set to the electronic volume register.

When using the electronic volume function, you need to turn the voltage regulation circuit on using the supply control command.

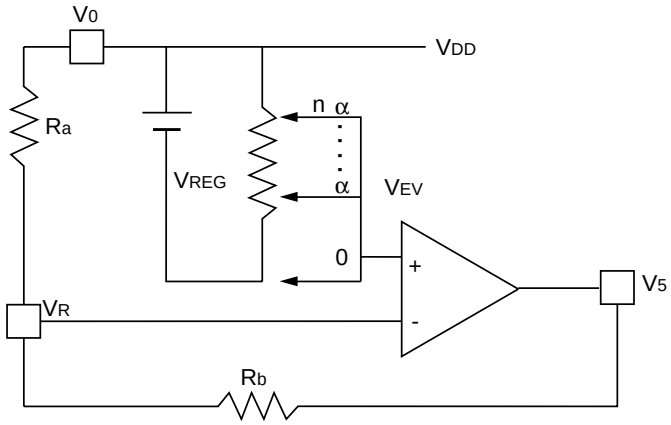
[Sample constants setting when electronic volume function is used]

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \textcircled{2}$$

Where $V_{EV} = V_{REG} - x$

$x = n\alpha$ (n = 0.1 – 31)

$\alpha = V_{REG} / 150$



No.	Electronic volume register	x	V5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	30α	•
31	(1, 1, 1, 1, 1)	31α	Small

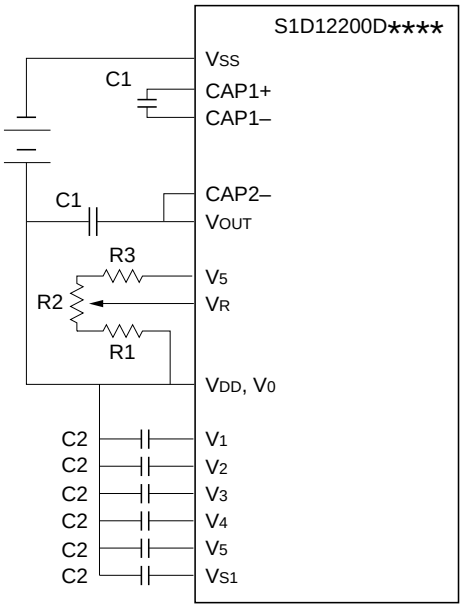
When the electronic volume function is not used, select (0, 0, 0, 0, 0) for the electronic volume register.

Liquid crystal voltage generating circuit

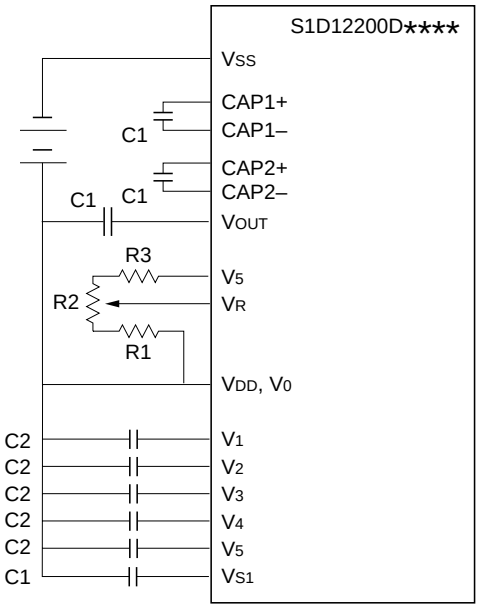
V_5 potential is resistive divided within IC to produce V_1, V_2, V_3 and V_4 potentials required for driving the liquid crystal. V_1, V_2, V_3 and V_4 potentials are then subject to impedance conversion and provided to the liquid crystal drive circuit.

The liquid crystal drive voltage is fixed to 1/5 (1/4) bias. The liquid crystal power terminals V_1 – V_5 must be externally connected with the voltage regulating capacitor C2.

When a built-in supply is used
When voltage is doubled



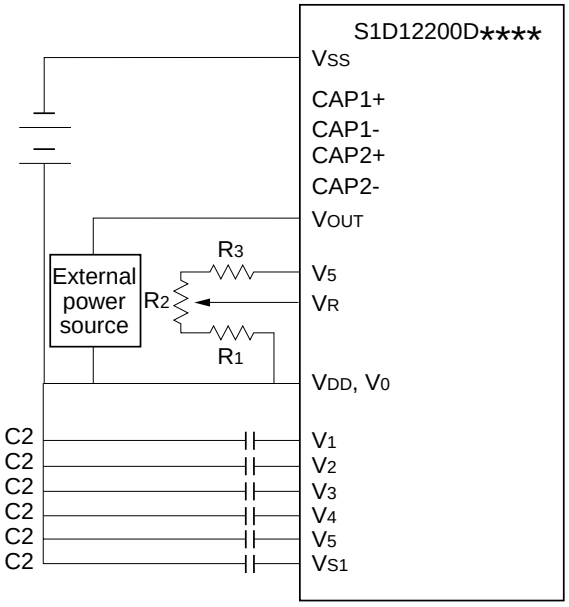
When voltage is tripled



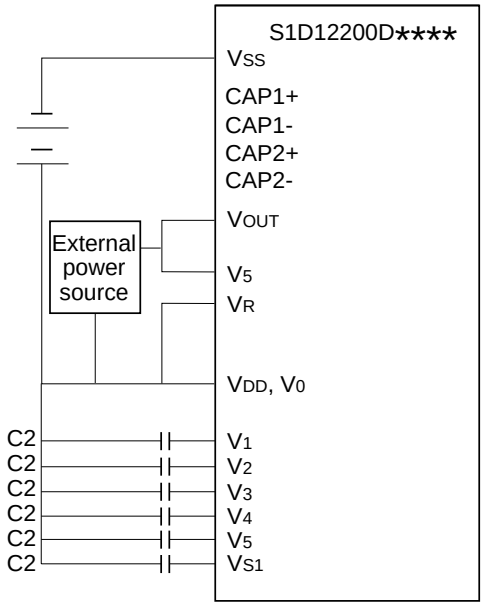
Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Example 2: When using the built-in power source
(VC, VF, P) = (1, 1, 0)



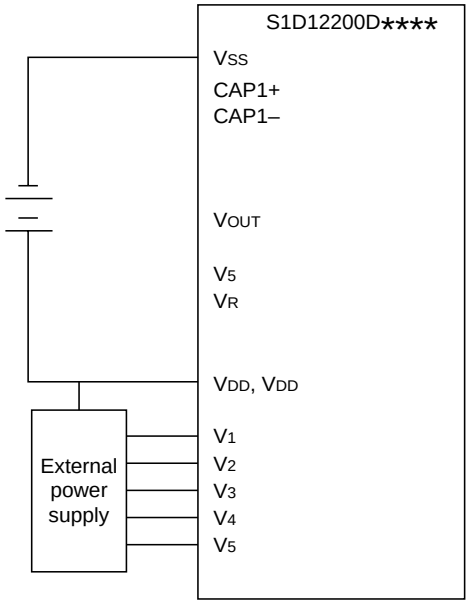
Example 3: When using the built-in power source
(VC, VF, P) = (0, 1, 0)



Reference setting values: C1: 0.47 - 4.7 µF
C2: 0.1 - 4.7 µF

We suggest you to determine the most appropriate capacitance values, fitting to the panel size, for respective capacitors C1 and C2 in consideration of the liquid crystal display and drive waveforms.

When a built-in supply is used



Low Power Consumption Mode

S1D12200 Series is provided with standby mode and sleep mode for saving power consumption during standby period.

● Standby Mode

Switching between on and off of the standby mode is done using the power save command.
In the standby mode, only static icon is displayed.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : V_{DD} level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : V_{DD} level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be turned on by static drives.
   Use the static icon RAM for controlling the static icon display done with SEGSA, B, C, D, E, COMSA.
2. DD RAM, CG RAM and symbol register
   Written information is saved as it is irrespective of on or off of the stand-by mode.
3. Operation mode is retained the same as it was prior to execution of the standby mode.
   The internal circuit for the dynamic display output is stopped.
4. Oscillating circuit
   The oscillation circuit for the static display must be remained on.

● Sleep Mode

To enter the sleep mode, turning off the power circuit and oscillation circuit using the commands, and then execute power save command. This mode helps to save power consumption by reducing current to almost resting current level.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : V_{DD} level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : V_{DD} level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Clear all the data of the static icon registers to “0”.
2. DD RAM, CG RAM and symbol register
   Written information is saved at it is irrespective of on or off the sleep mode.
3. Operation mode mode is retained the same at it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power circuit and oscillation circuit
   Turn off the built-in supply circuit and oscillation circuit using the power save command and supply control command.

Reset Circuit

Upon activation of the RES input, this LSI will be initialized.

● Initial State

1. Display on/off control
   C = 0 : Cursor off
   B = 0 : Blink off
   D = 0 : Display off
2. Power save
   O = 0 : Oscillation off
   PS = 0 : Power save off
3. Supply control
   VC = 0 : Voltage regulation circuit off
   VF = 0 : Voltage follower off
   P = 0 : Amplifying circuit off
4. System setting
   N2, N1 = 0 : 2 lines
   S = 0 : Left-hand shift
   CG = 0 : “CGRAM” blank
5. Electronic volume control
   Address : 28H
   Data : (0, 0, 0, 0, 0)
6. Static icon
   Address : 20H
   Data : (0, 0, 0, 0, 0)
   Address : 21H
   Data : (0, 0, 0, 0, 0)
   Address : 22H
   Data : (0, 0, 0, 0, 0)
   Address : 23H
   Data : (0, 0, 0, 0, 0)

As explained in the Section “MPU interface”, the RES terminal connects to the reset terminal of the MPU and initialization is being effected together with the MPU. However, when the bus, port, etc. of the MPU maintains high-impedance for a certain duration of time after resetting, make the resetting input to the S1D12200 Series after the inputs to the S1D12200 Series have become definite.
As the resetting signal, like explained in the Section “DC characteristics”, active level pulses of minimum 10us or more should be used. Normal operation status can be obtained after 1us from the edge of the RES signal.
By making the RES terminal active, respective registers can be cleared and the aforesaid setting state can be obtained.
If initialization is not effected by the RES terminal when the supply voltage is applied, it may go into a state where cancellation is unworkable.
In case the built-in liquid crystal power circuit will not be used, it becomes necessary that the RES input be active when the external liquid crystal power is being applied.

7. COMMAND

Table 4 lists the commands. S1D12200 Series identifies the data bus signal using different combinations of A0 and $\overline{WR}$ (E). High speed command interpretation and execution are possible since only the internal timing is used.

- **Command Overview**

Command type	Command name	A0	$\overline{WR}$
Display control instruction	Cusor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System set	System set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

Instruction execution duration of dependents on the internal process time of S1D12200 Series, therefore it is neces-sary to provide a duration larger than the system cycle time (t_{CYC}) between execution of two successive in-struction.

- **Description of Commands**

(1) Cursor Home
This command presets the address counter to 30H and moves the cursor, when it is present, to the first digit of the first line.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

*: Don't Care

(2) Display ON/OFF Control
This command performs on or off of display and cursor setting.

Note: Symbols driven by COMSA and SEGSA – E must be controlled through the static icon RAM.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	*	D

D = 0 : Display off
1 : Display on

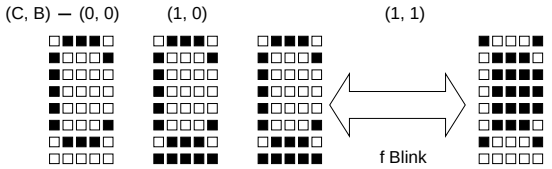
B = 0 : Cursor blink off
1 : Cursor blink on

Blink displays characters in black and white, alternately. The alternating display will be repeated with approx. 1 second interval.

C = 0 : Display of cursor
1 : Does not display

Following table shows relationship between B and C registers and the cursor.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Underbar cursor
1	1	Alternate display of display characters in black and white. The cursor position indicates the position of address



The cursor position indicates the position of address counter.

Therefore, whenever moving the cursor, change the address counter value using the RAM address set command or the auto increment done by writing the RAM data.

ISelective flashing symbol display is possible by selecting (C, B) = (1, 0) and thus locating the address counter to the position of the symbol register through selecting (since the symbol is corresponding to the character at each 5 dots).

(3) Power Save
This command is used to controlling the oscillation circuit and setting or resetting the sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

*: Don't Care

PS = 0 : Power save off (reset)
1 : Power save on (set)

O = 0 : Oscillating circuit off (stop of oscillation)
1 : Oscillating circuit on (oscilla tion)

(4) Supply Control
This command is used for controlling operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Amplifying circuit off
1 : Amplifying circuit on

Note: The oscillation circuit must be turned on for the amplitying circuit to be active.

VF = 0 : Voltage follower off
1 : Voltage follower on

VC = 0 : Voltage regulation circuit off
1 : Voltage regulation circuit on

(5) System Set
This command is used for selecting display line, common shift direction and use/non-use of CR RAM.
When power on or resetting is done, execute this command first.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	N1	N2	S	CG

∗: Don't Care

N2, N1 = 0, 0 : 2lines
N2, N1 = 0, 1 : 3lines

S = 0 : COM left shift
= 1 : COM right shift

CG = 0 : Use CG RAM
1 : Does not use RAM

(6) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DD RAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	CGRAM (0 0 H)							–	CGRAM (0 1 H)							–
1 0 H	CGRAM (0 2 H)							–	CGRAM (0 3 H)							–
2 0 H	SI	unused						–	EV	Test	unused					–
3 0 H	DDRAM line 1							For signals							Unused	
4 0 H	DDRAM line 2														"	
5 0 H	DDRAM line 3														"	
6 0 H	Symbol register														"	
7 0 H	Symbol register														"	

– :Unused
For signals :Output from SEGS1 to SEGS2, SEGS4, SEGS5
For symbol register :Output from COMS1 to COMS2.

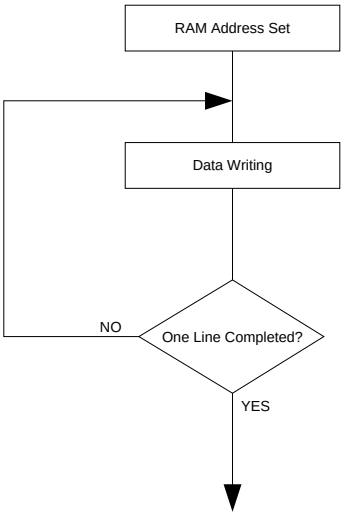
SI :Static icon register
EV :Electronic volume register
Test :Test register (Do not use)

(7) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data the DD RAM, CG RAM or symbol register.
② This command automatically increases the address counter by +1, thus enabling continuous writing of data.

<Example of Data Writing>
Following figures illustrates an example of continuous writing of one line data to DD RAM.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 S1D12200 Series Command List

Command	Code										Function
	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	*	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	S	CG	Sets the use or non-use of CG RAM and shifting direction of display line (N1, N2) and COM CG = 1 (use of CG RAM), 0 = (Does not use CG RAM), M2, N1 = 0, 0 (2 lines) 0, 1 (3 lines). S = 0 (left shift), 1 (right shift).
(6) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(7) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(8) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	Command for IC chip test. Don't use this command.

8. CHARACTER GENERATOR

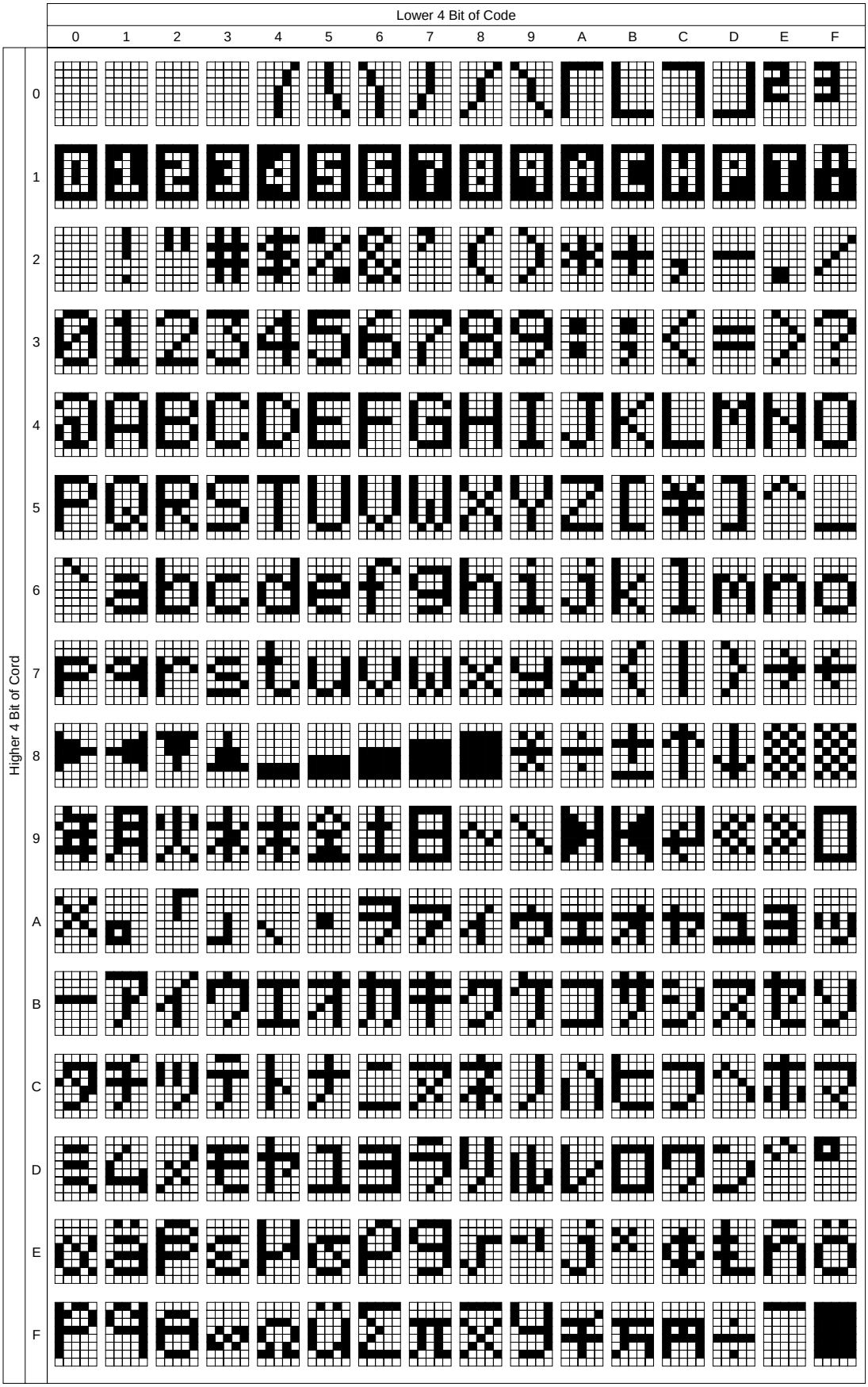
Character Generator ROM (CG ROM)

Character Generator ROM (CG ROM)
S1D12200 Series cntains the character generator ROM (CG ROM) consisted of up to 256 types of characters.
Character size is 5×8 dots.
Tables 5 though 7 show the S1D12200D∗∗∗∗ character code.

Concerning the 4 characters from 00H through 03H, the system command selects on which of CG ROM and CG RAM they are to be used.
S1D12200 Series CG ROM is mask ROM and compatible with customized ROM. Contact us for its use in your system.
Product name of modified CG ROM is defined as below:

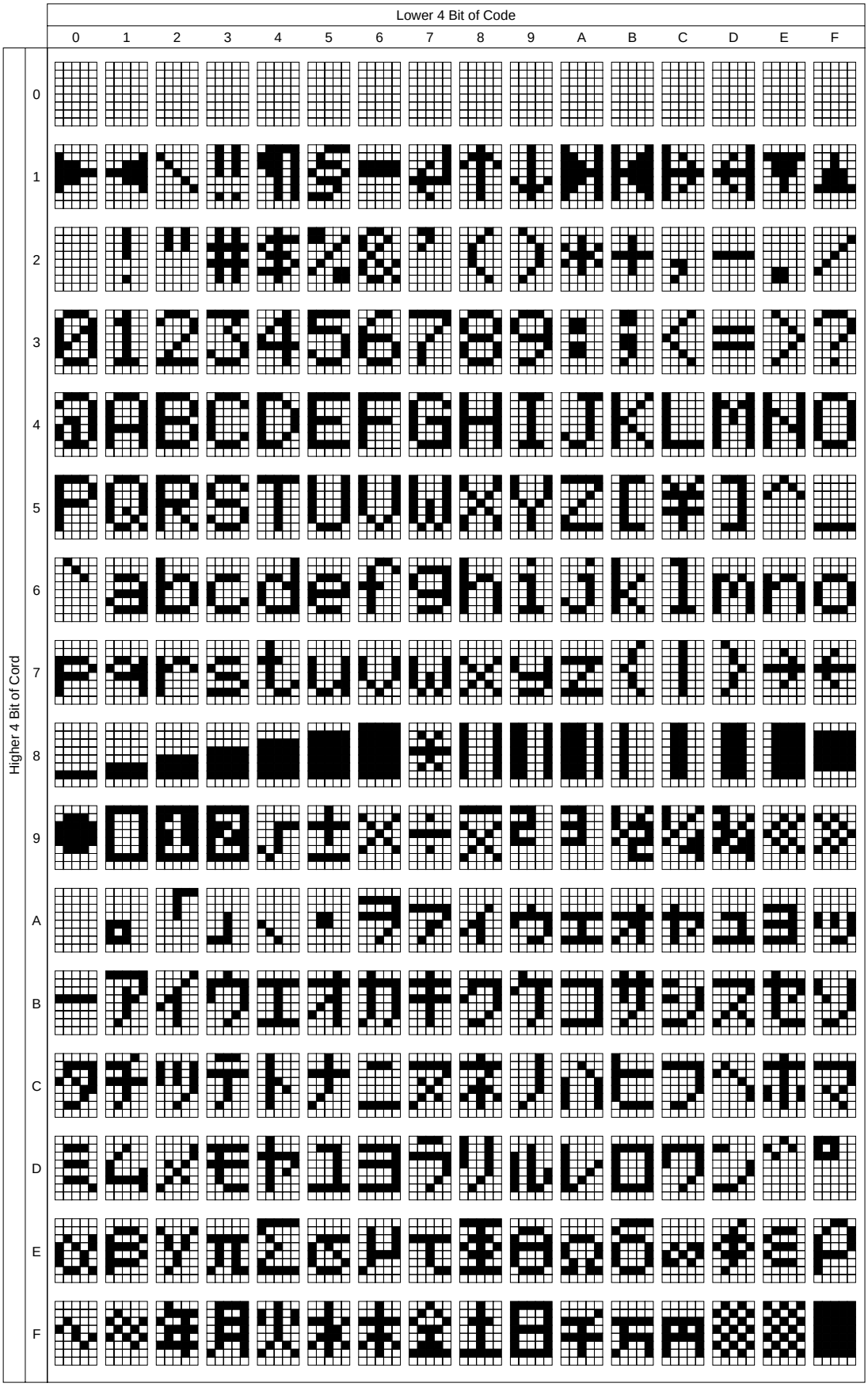
(Example) S1D12200D00B∗
↑
Digit for CG ROM pattern change

S1D12200D10**



S1D12200D11**

S1D12200D16**



Character Generator RAM (CG ROM)

CGRAM contained in S1D12200 Series enables user programming of character patterns for display signals with higher degrees of freedom.

When using CGRAM, select it using the system command.

Capacity of CGRAM is 160 bits and accepts registration of any 4 5 ×8 dots patterns.

Following shows relationship between the CGRAM characters, CGRAM addresses and character code.

Character code	RAM address		CGRAM data (character pattern) D7 D0								Character display SEG	Signal display SEGS 1 2 4 5
00H	00H to 07H	0	*	*	*	0	1	1	1	1	■■■■	■■ ■■
02H	10H to 17H	1	*	*	*	1	0	0	0	0	■ ■ ■ ■	■ ■ ■
		2	*	*	*	1	0	0	0	0	■ ■ ■ ■	■ ■ ■
		3	*	*	*	0	1	1	1	1	■■■■	■■ ■■
		4	*	*	*	0	0	0	0	1	■	■ ■
		5	*	*	*	0	0	0	0	1	■	■ ■
		6	*	*	*	1	1	1	1	0	■■■■	■■ ■
		7	*	*	*	0	0	0	0	0		
01H	08H to 0FH	8	*	*	*	0	0	1	0	0	■	
03H	18H to 1FH	9	*	*	*	0	0	1	0	0	■	
		A	*	*	*	0	1	1	1	0	■■■■	■■ ■
		B	*	*	*	0	1	1	1	0	■■■■	■■ ■
		C	*	*	*	0	1	1	1	0	■■■■	■■ ■
		D	*	*	*	1	1	1	1	1	■■■■	■■ ■■
		E	*	*	*	0	0	0	0	0	■■■■	■■ ■■
		F	*	*	*	0	0	0	0	0		

Unused

Character data
1: Display
0: Non-display

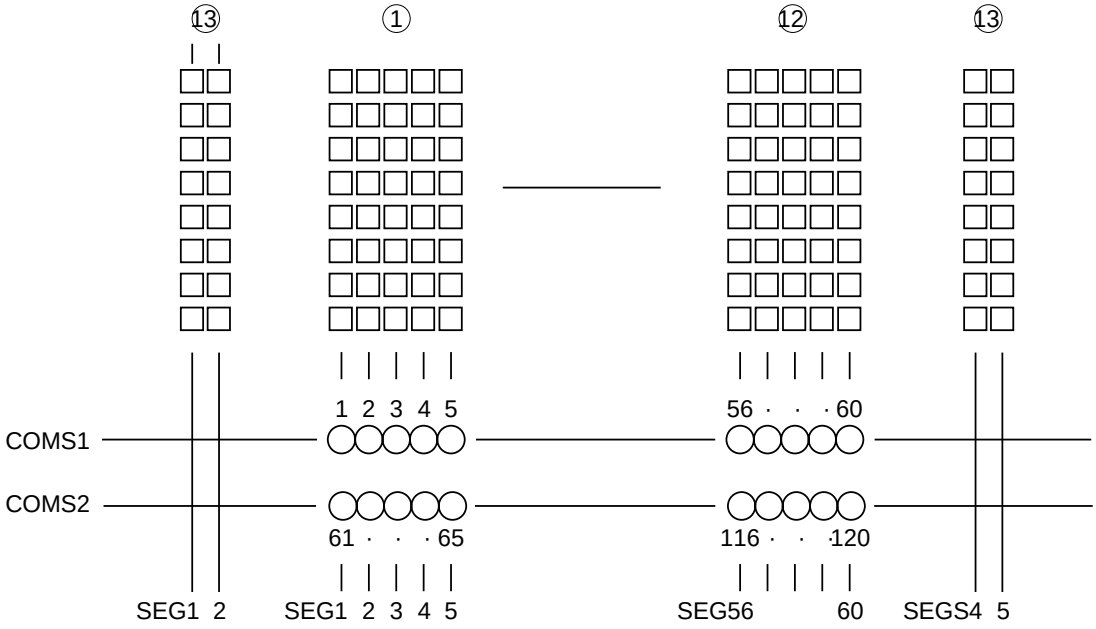
It is possible to set a 5 × 8 character size in this system. In this case, use the ∗7H/∗FH RAM. Note that the ∗7H/∗FH data is inverted when a under-bar cursor is used.

Symbol Register

S1D12200 Series contains the symbol register which enable individual symbol setting for displaying on the screen.

Capacity of the symbol register is 120 bits and is capable of displaying up to 120 symbols.

Following shows relationship between the symbol register display patterns, RAM addresses and written data.



RAM address		Symbol Bits D7 — D0							
60H~6BH	0	*	*	*	1	2	3	4	5
	1	*	*	*	6	7	8	9	10
	:	:							
	B	*	*	*	56	57	58	59	60
70H~7BH	0	*	*	*	61	62	63	64	65
	1	*	*	*	66	67	68	69	70
	:	:							
	B	*	*	*	116	117	118	119	120

Note: When the symbol is 1.5 times or more than the character, it is recommended to drive it using both COMS1 and COMS2.

Static Icon Ram

S1D12200 Series contains the static icon RAM for displaying the static icons in addition to the dynamic icons.
Capacity of static icon RAM is 10 bits (S1D12200/12201/12202) or 20 bit (S1D12210) and is capable of displaying up to 5 icons (S1D12200/12201/12202) or 10 icons (S1D12210).
Following shows relationship between the static icons functions, static icon RAM addresses and written data.

< SEGSA, B, C, D, E >

Function	RAM address	Static icon data D7							D0	Display S E G S A B C D E
Display On/Off	20H	*	*	*	0	0	1	1	1	□□■■■ / □□■■■
Blink On/Off	21H	*	*	*	1	0	0	0	1	f BLINK / ■□■■□

< SEGSF, G, H, I, J >

Function	RAM address	Static icon data D7							D0	Display S E G S F G H I J
Display On/Off	22H	*	*	*	0	0	1	1	1	□□■■■ / □□■■■
Blink On/Off	23H	*	*	*	1	0	0	0	1	f BLINK / ■□■■□

*: Blank
1: Display or blink on
0: Display or blink off
f_{BLINK}: 1–2 Hz

Electronic Volume RAM (register)

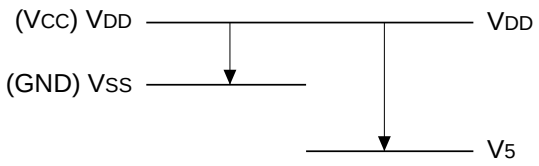
S1D12200 Series contains the electronic volume function for controlling the liquid crystal drive voltage V5 and density of liquid crystal display. The electronic volume function enables to select one of 32 voltage status of the liquid crystal drive voltage V5 by writting 5-bit data to the electronic volume RAM.
Following shows relationship between RAM addresses set by the electronic volume and written data.

Function	RAM address	Electronic volume data D7							D0	Condition	V_{EV}
Electronic volume data	28H	*	*	*	0	0	0	0	0	0	V_{REG}–0
		*	*	*	0	0	0	0	1	1	V_{REG}–α
		*	*	*	0	0	0	0	0	2	V_{REG}–2α
							:			:	
							:			:	
		*	*	*	1	1	1	0	1	29	V_{REG}–29α
		*	*	*	1	1	1	1	0	30	V_{REG}–30α
		*	*	*	1	1	1	1	1	31	V_{REG}–31α
	29H	*	*	*	*	*					For testing

* : Blank
Note : Do not use the address “29H”. It is for testing
$\alpha = V_{REG}/150$

9. ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0 to +0.3	V
Power supply voltage (2)		V_5, V_{out}	–7.0 to +0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes:
1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

10. DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Operatable	V_{SS}		–3.6	–3.0	–2.4	V	V_{SS} *1
	Data retain voltage			–3.6		–2.0		
Power supply voltage (2)	Operatable	V_5		–7.0		–4.0	V	V_5 *2
	Operatable	V_1, V_2		0.6×V_5		V_{DD}	V	V_1, V_2
	Operatable	V_3, V_4		V_5		0.4×V_5	V	V_3, V_4
HIGH-level input voltage		V_{IHC}		0.2×V_{SS}		V_{DD}	V	*3
LOW-level input voltage		V_{ILC}		V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	Display state	V_5 = –6 V without load			80	µA	V_{DD} *5
		Standby state	Oscillation ON, Power OFF, V_{SS} = –3V without load			20	µA	V_{DD}
		Sleep state	Oscillation OFF, Power OFF, V_{SS} = –3.0V			5	µA	V_{DD}
		Access state	f_{cyc}=200KHz, V_{SS} = –3.0V			500	µA	V_{DD} *6
Input pin capacity		C_{IN}	Ta=25°C f=1MHz		5.0	8.0	pF	*3

Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{ck}	Display of 2 lines		23.4		KHz	*10 *11
	f_{ck}	Display of 3 lines		33.8		KHz	*10 *11

Reset time	t_R		1.0			µs	*7
Reset pulse width	t_{RW}		10			µs	*8
Reset start time	t_{RES}		50			ns	*8

Dynamic system

Built-in power supply	Input voltage	V_{S1}		–2.3	–2.1	–1.9	V	*9
	Amplified voltage output voltage	V_{OUT}	When voltage is tripled	–6.9	–6.3	–5.7	V	V_{OUT}
	Voltage follower operating voltage	V_5		–7.0		–4.0	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.06	–2.0	–1.94	V	

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

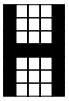
*2: When the voltage is Tripled, care must be paid to supply the voltage V_{SS} so that operating voltage of V_{OUT} and V_5 may not be exceeded.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, $\overline{RES}$, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

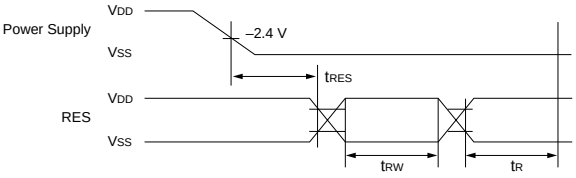
(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Applied if not access by the MPU during chara display and if the built-in power circuit and oscillator are operating.
Display character: 

*6: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*7: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the S1D12200 usually enters the operating state after t_R.

*8: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.



All signal timings are based on 20% and 80% of V_{SS} signals.

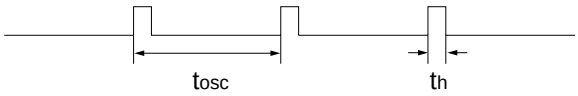
*9: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*10: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

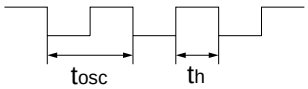
f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}

*11: When performing the operations using an external clock, not taking advantage of the built-in oscillation circuit, input the waveforms indicated below. Meanwhile, while using an external clock but when clock inputs are not being made, fix it to "H". (Normal HIGH)

<Incase the external clock = fosc>
- Duty = (th/tosc) × 100 = 20 ~ 30%
- fosc = 1/tosc

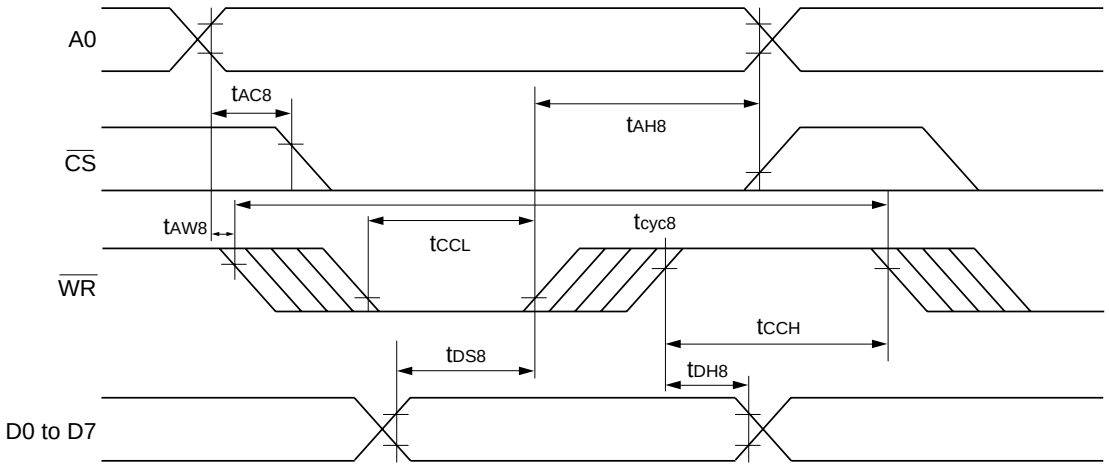


<Incase the external clock = 4 × fosc>
- Duty = (th/tosc) × 100 = 50%
- fosc = 1/tosc



11. TIMING CHARACTERISTICS

(1) MPU Bus Write Timing (80 series)



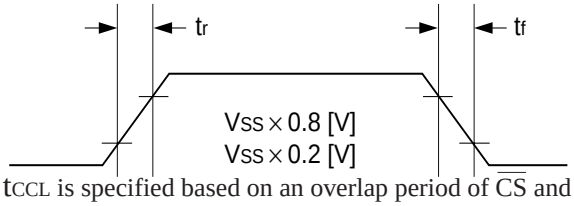
[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	tAH8	Every timing is specified on the basis of 20% and 80% of VSS.	30	–	ns
Address setup time		tAW8		60	–	ns
$\overline{CS}$ setup time		tAC8		0	–	ns
System cycle time	$\overline{WR}$	tCYC8		650	–	ns
Write LOW pulse width (Write)		tCCL		150	–	ns
Write HIGH pulse width (Write)		tCCH		450	–	ns
Data setup time	D0 to D7	tDS8		100	–	ns
Data hold time		tDH8		50	–	ns

[Ta = –30 to 85°C, VSS = –3.3 V to –2.7 V]

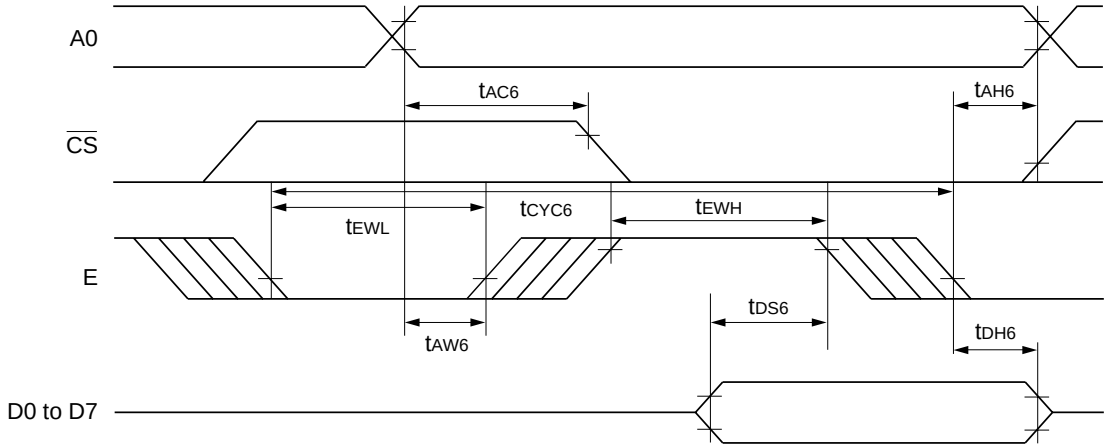
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	tAH8	Every timing is specified on the basis of 20% and 80% of VSS.	10	–	ns
Address setup time		tAW8		60	–	ns
$\overline{CS}$ setup time		tAC8		0	–	ns
System cycle time	$\overline{WR}$	tCYC8		500	–	ns
Write LOW pulse width (Write)		tCCL		100	–	ns
Write HIGH pulse width (Write)		tCCH		350	–	ns
Data setup time	D0 to D7	tDS8		100	–	ns
Data hold time		tDH8		20	–	ns

*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



*2: tCCL is specified based on an overlap period of $\overline{CS}$ and $\overline{WR}$ LOW levels.

(2) MPU Bus Write Timing (68 series)



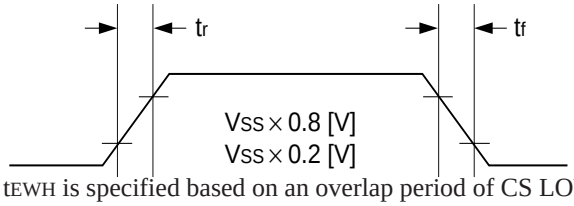
[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	tAW6	Every timing is specified on the basis of 20% and 80% of VSS.	60	–	ns
Address hold time		tAH6		30	–	ns
$\overline{CS}$ setup time		tAC6		0	–	ns
System cycle time	$\overline{WR}$	tCYC6		650	–	ns
Enable LOW pulse width (Write)		tEWL		150	–	ns
Enable HIGH pulse width (Write)		tEWH		450	–	ns
Data setup time	D0 ~ D7	tDS6		100	–	ns
Data hold time		tDH6		50	–	ns

[Ta = –30 to 85°C, VSS = –3.3 V to –2.7 V]

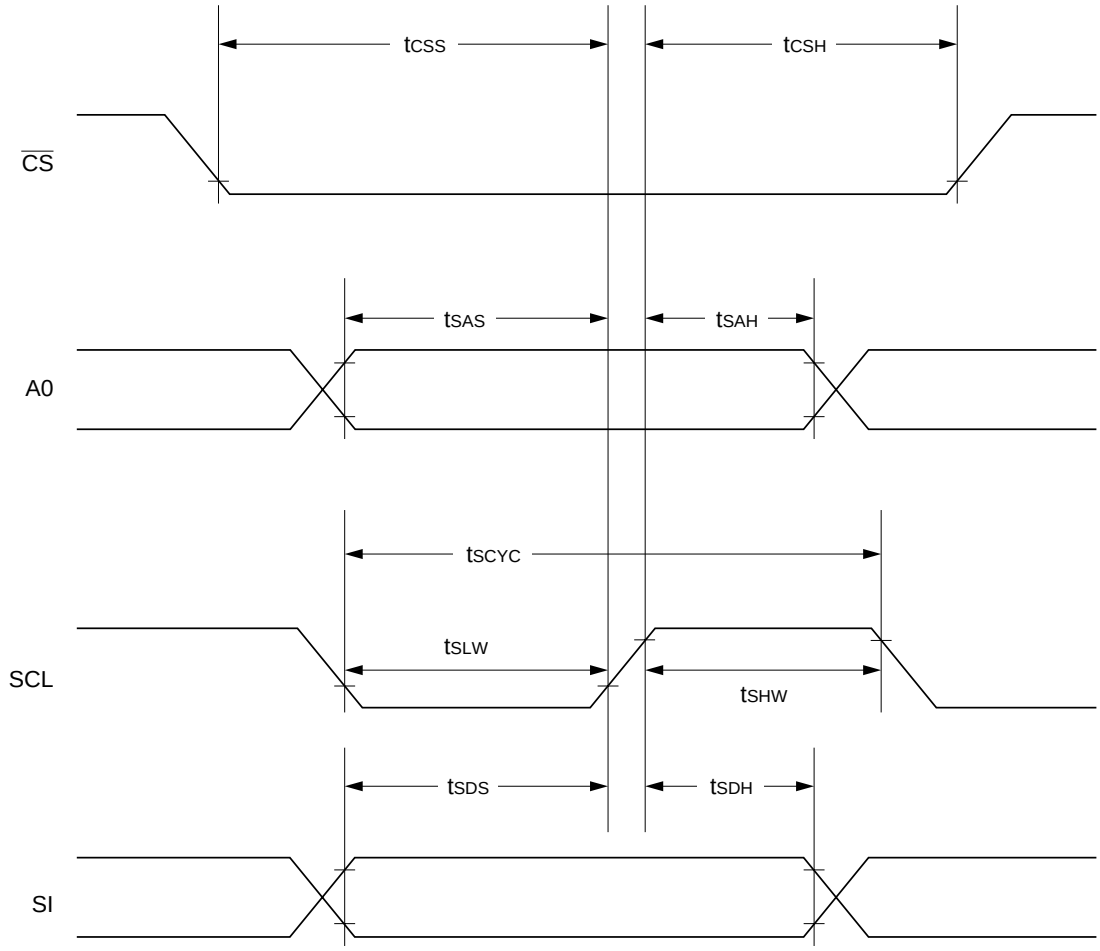
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	tAW6	Every timing is specified on the basis of 20% and 80% of VSS.	60	–	ns
Address hold time		tAH6		10	–	ns
$\overline{CS}$ setup time		tAC6		0	–	ns
System cycle time	$\overline{WR}$	tCYC6		500	–	ns
Enable LOW pulse width (Write)		tEWL		100	–	ns
Enable HIGH pulse width (Write)		tEWH		350	–	ns
Data setup time	D0 to D7	tDS6		100	–	ns
Data hold time		tDH6		20	–	ns

*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



*2: tEWH is specified based on an overlap period of CS LOW and E HIGH levels.

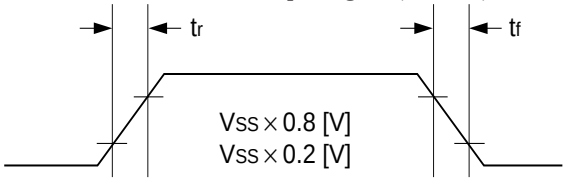
(3) Serial Interface



[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	Every timing is specified	1000		ns
SCL HIGH pulse width		tSHW	on the basis of 20% and	300		ns
SCL LOW pulse width		tSLW	80% of VSS.	300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH		300		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
CS-SCL time	CS	tCSS		150		ns
		tCSH		700		ns

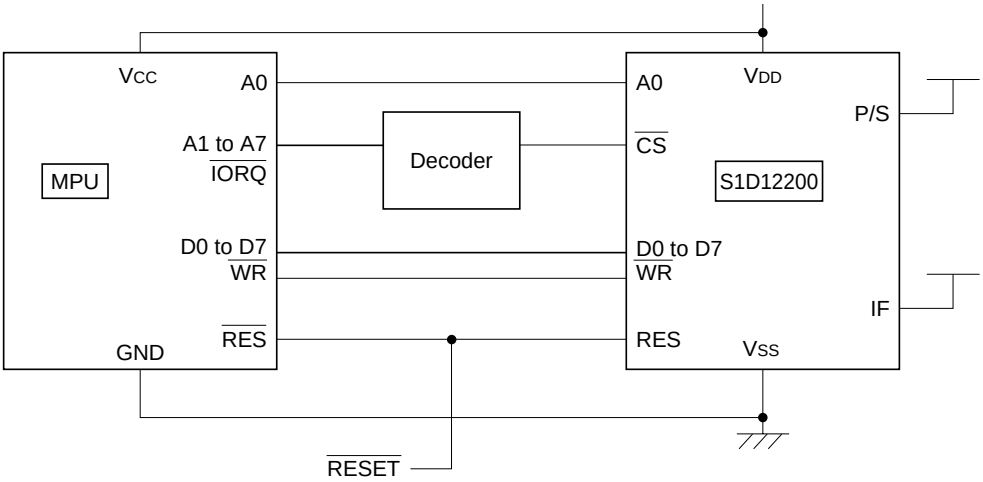
*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



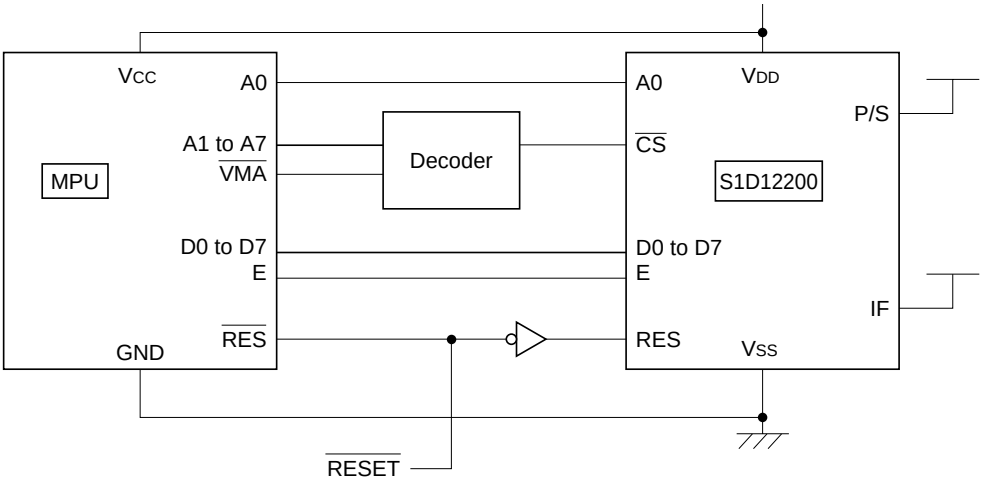
12. MPU INTERFACE (REFERENCE EXAMPLES)

The S1D12200 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the S1D12200 Series can be operated by less signal lines.

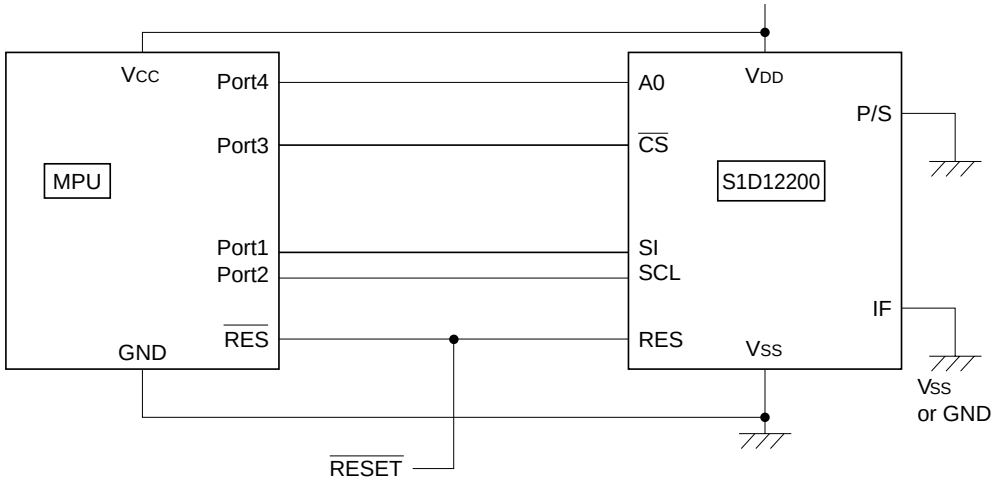
80 Series MPU



68 Series MPU

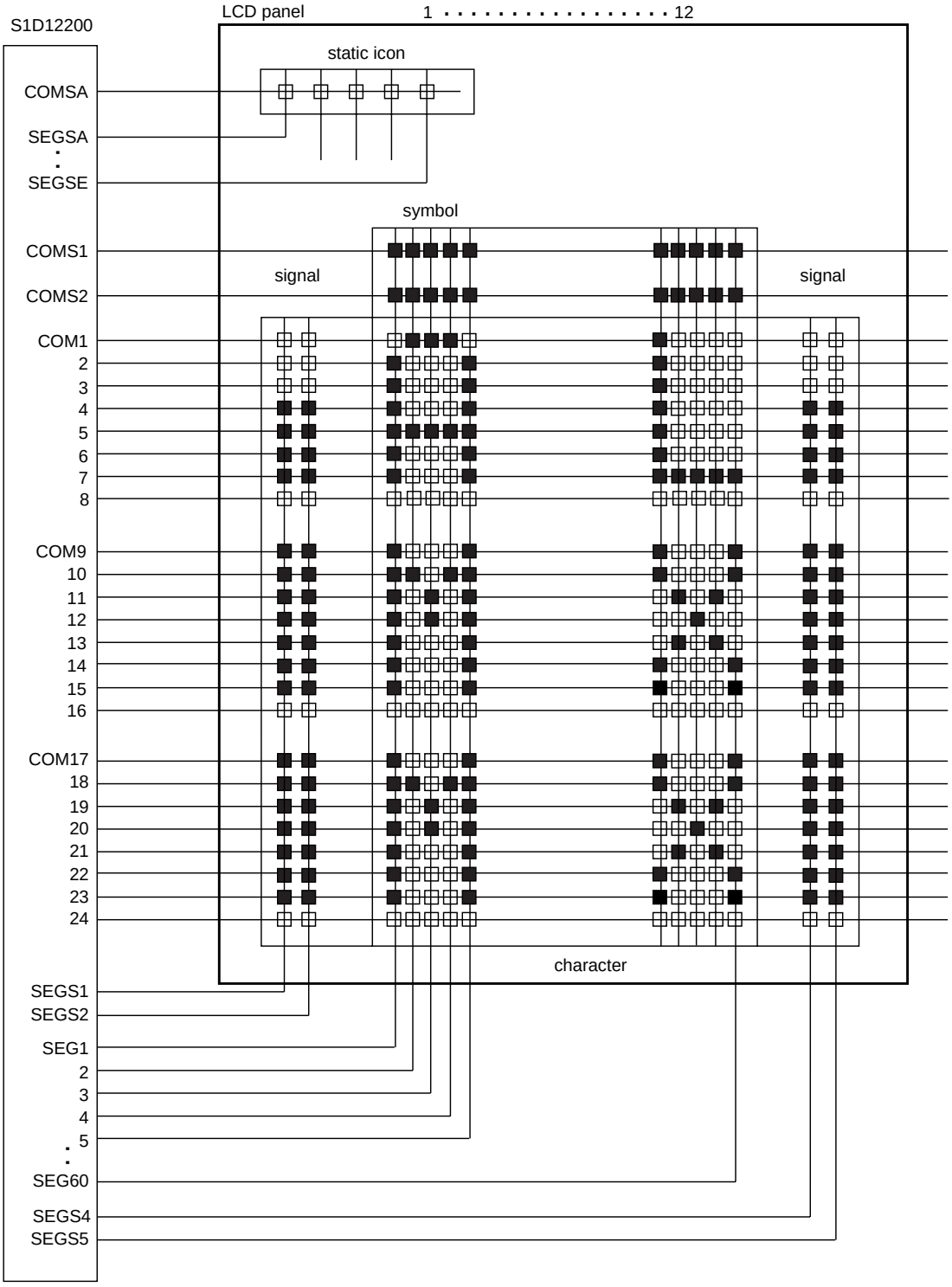


Serial Interface

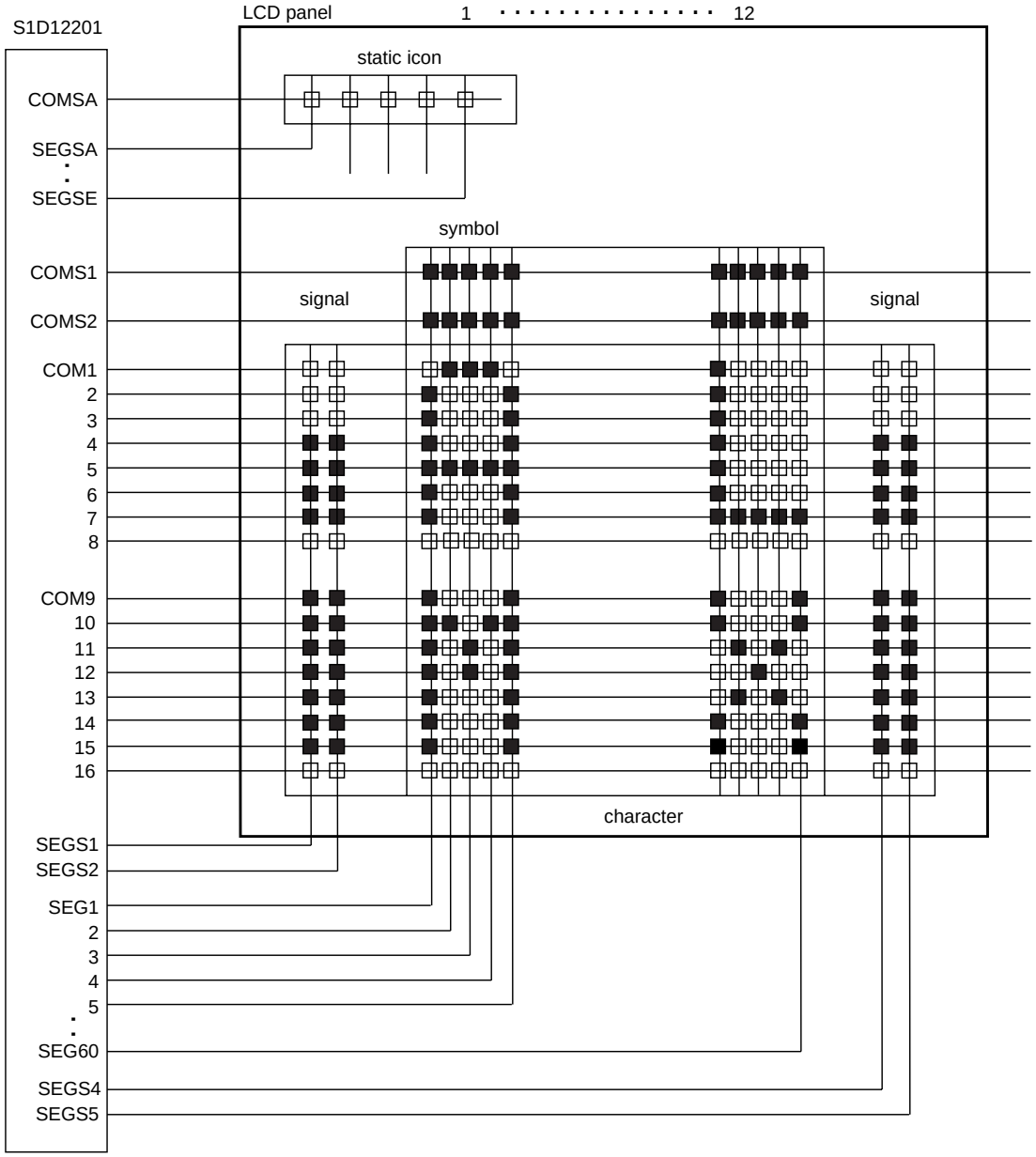


13. LCD CELL INTERFACE (REFERENCE)

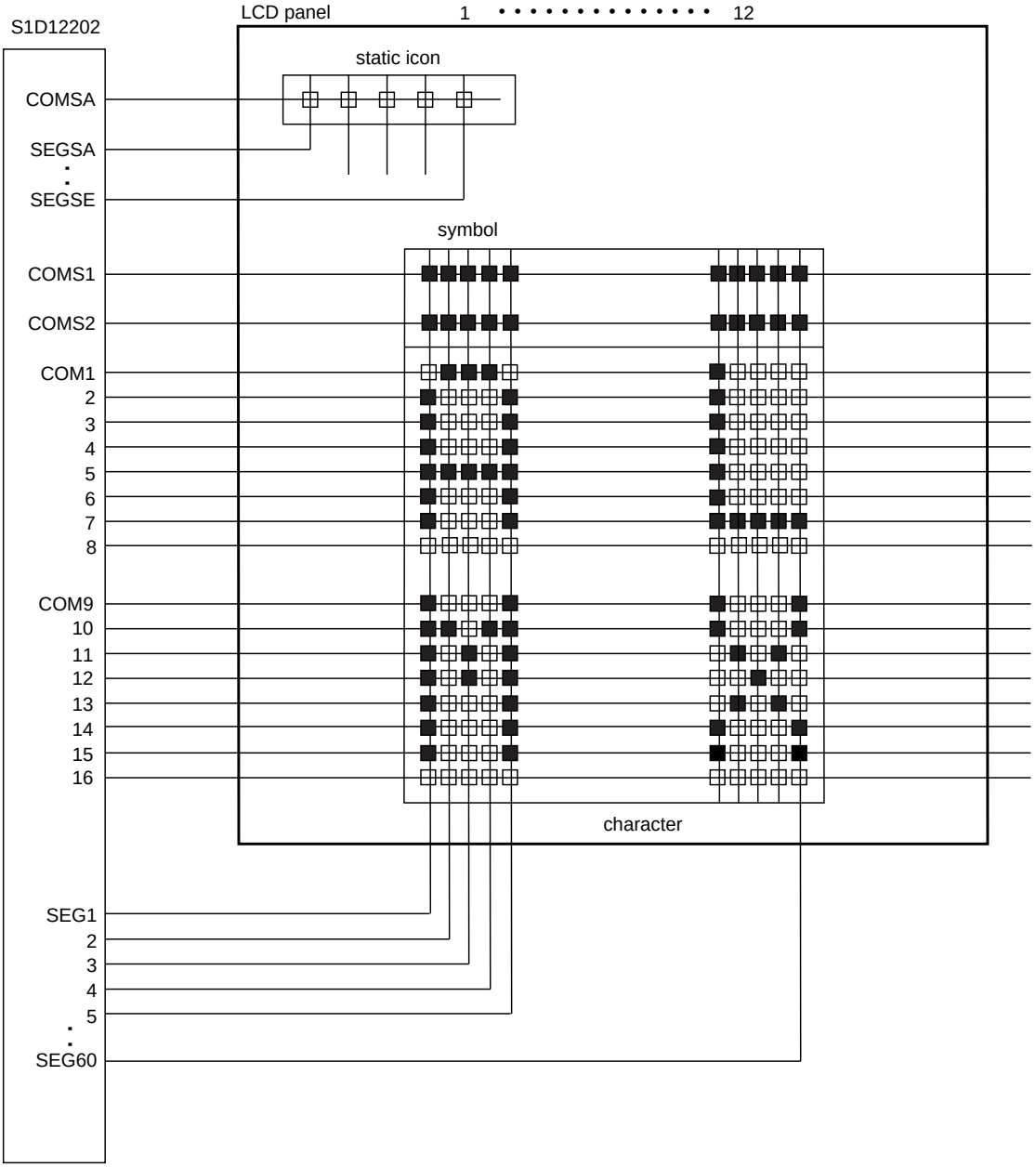
12 columns by 3 lines, 5 × 8-dot matrix segments and symbols



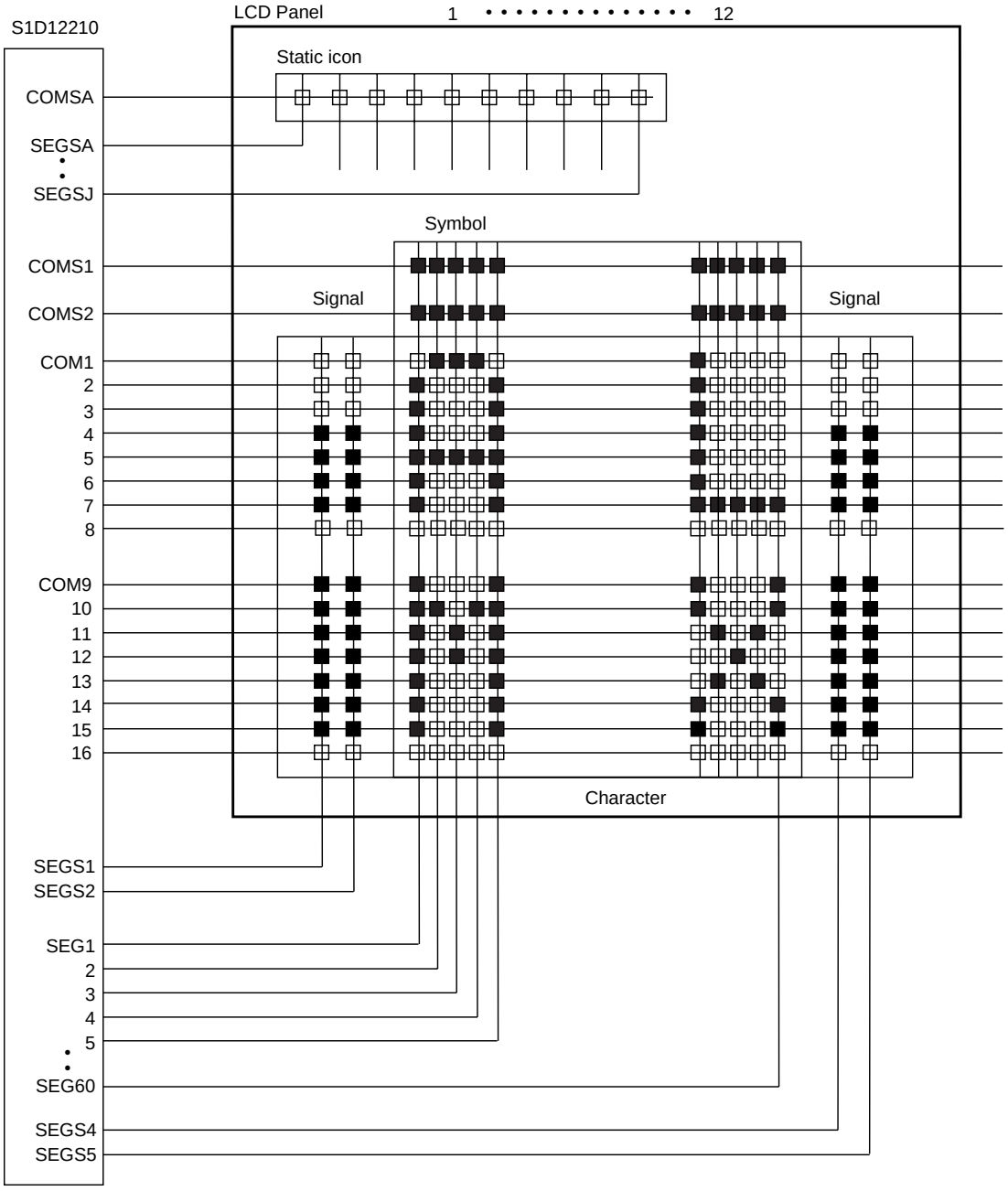
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



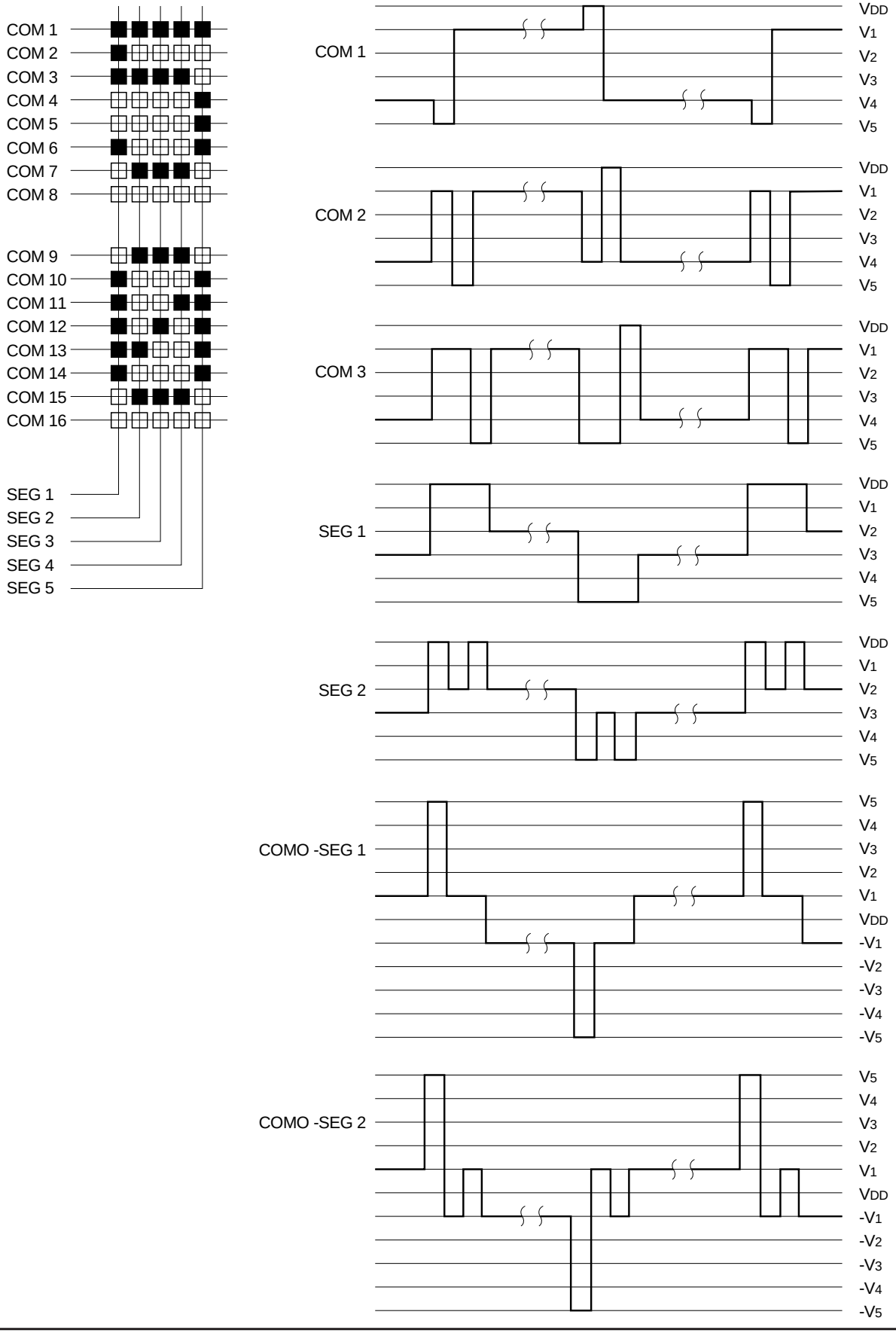
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



12 columns by 2 lines, 5 × 8-dot matrix segments and symbols

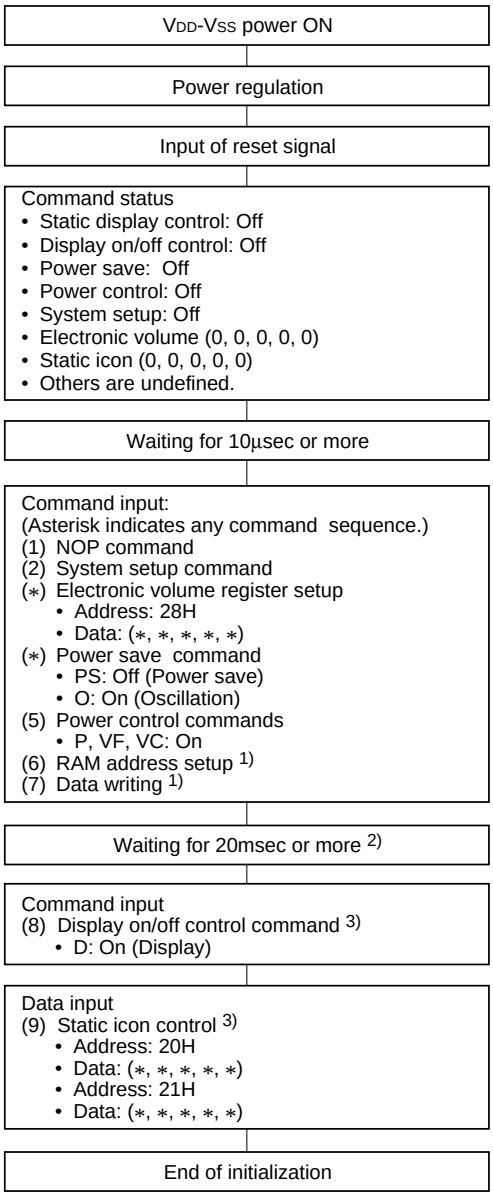


14. LCD DRIVE WAVEFORMS (B WAVEFORMS)

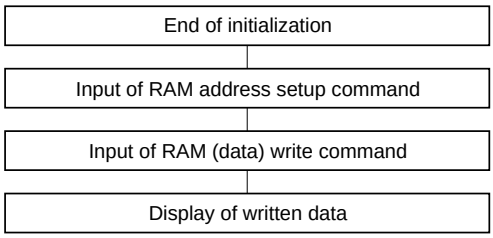


15. INSTRUCTION SETUP EXAMPLE (REFERENCE)

(1) Initial setup



(2) Display mode

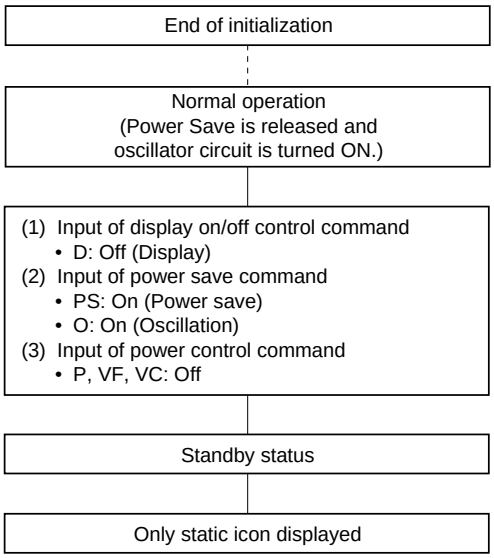


Notes 1) Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
• DDRAM: Write the 20H data (character code).
• CGRAM: Write the 00H data (data '0').
• Symbol register: Write the 00H data (data '0').
As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

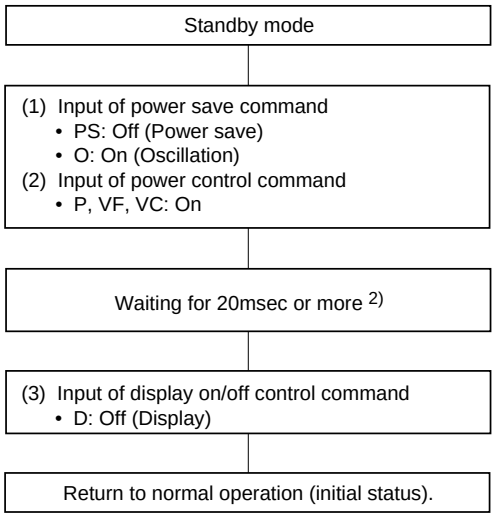
2) Since it is specified based on rise characteristics of the booster, power control and voltage follower circuits, time to be set differs depending on external capacity. Be sure to set it after the external capacity is confirmed.

3) A display of the dynamic drive series is turned on when the on command is input and the static icon is turned on using the static icon control command.
To turn both on at the same time when the display is turned on, execute display on/off command and static icon control within 1 frame period.

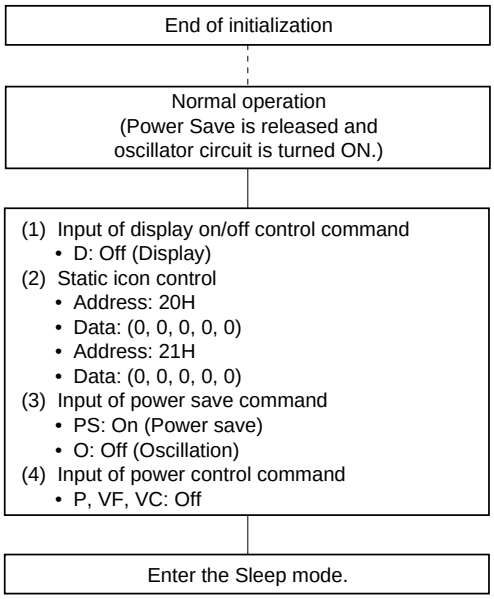
(3-1) Selecting the Standby mode



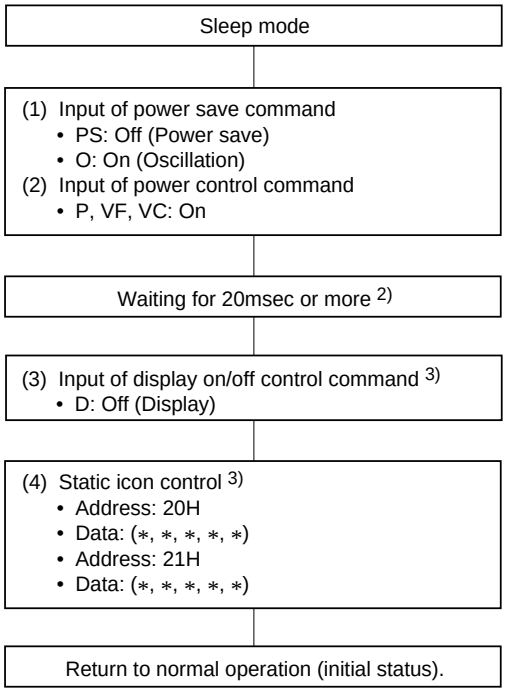
(3-2) Releasing the Standby mode



(4-1) Selecting the Sleep mode



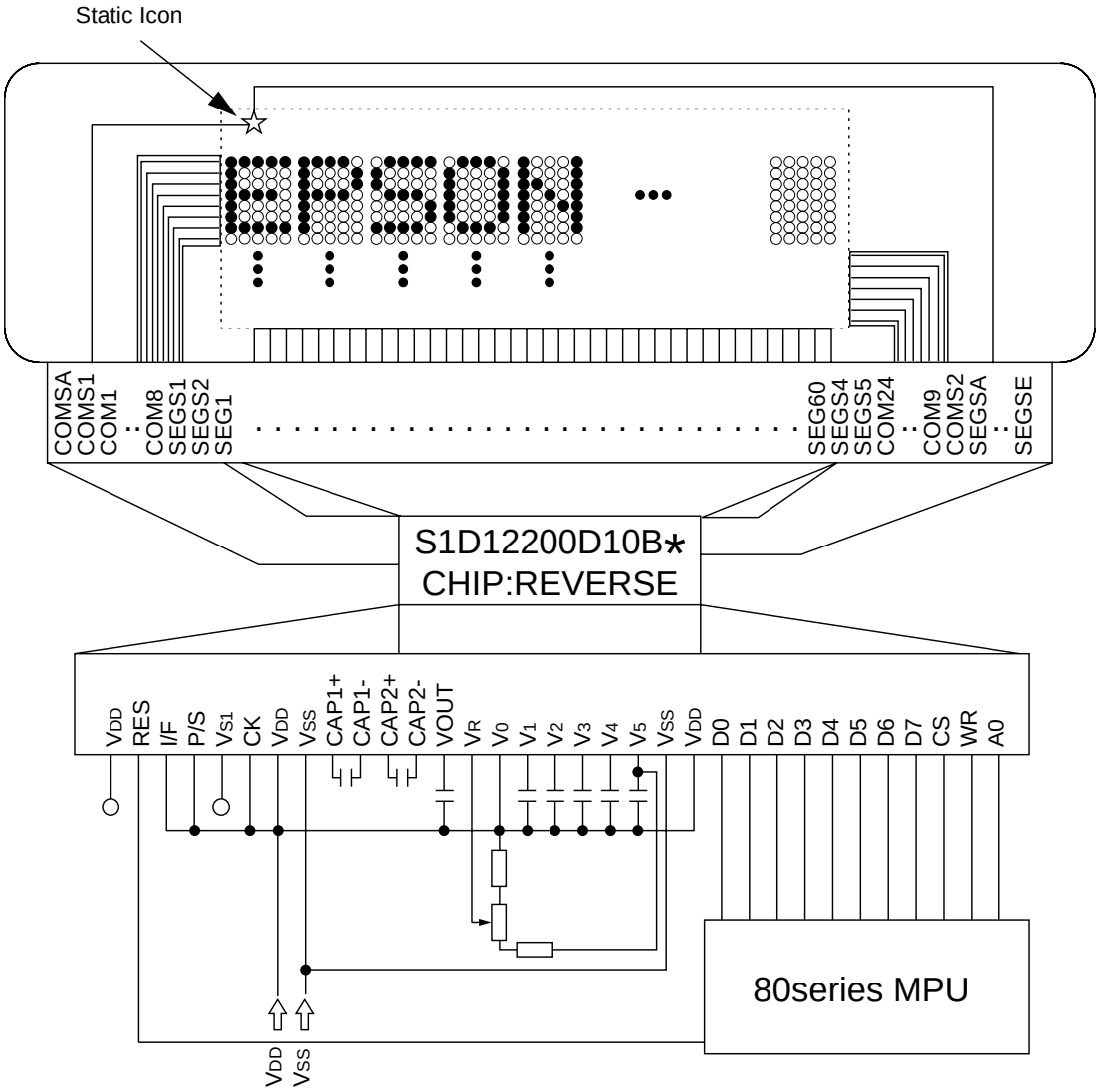
(4-2) Releasing the Sleep mode



Instruction Setup Example of S1D12200 series

(1) Initial setup
(2) display ON “EPSON”
(3) Display ON the Icon
(4) Standby Mode sequence
(5) Releasing the Standby Mode sequence

<Diagram of S1D12200T∗∗∗∗ and LCD Panel>



(1) Initial setup
(1.1) VDD–VSS Power ON

(1.2) Power regulation

(1.3) Input of RESET signal

(1.4) Command Status
- Display ON/OFF :OFF
- Power save :OFF
- Power control :OFF
- System reset :OFF
- Electronic Volume :(0, 0, 0, 0, 0)
- Static display control :OFF
- Others are undefined.

(1.5) Waiting for 10μ sec or more

(1.6) Command Input: ((*) indicates any command sequence.)
(a) System Setup command: CGRAM→Not use, 3lines, COM Left shift

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	0	0

(*) Electronic volume resister setup: Data→(0, 0, 0, 0, 0, 0)

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0

(*) Power save command: PS→0, 0→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(d) Power Control command: P, VF, VC→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(e) (f) RAM address setup, Data writing
• RAM address setup: Set address is 30H

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

• Data writing: All data→20H (for 1 Line)

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 40H

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0	0	0

• Data writing: All data→20H (for 2 line)

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 50H

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	0	0

• Data writing: All data →20H (for 3 Line)

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• End of Initialization

(2) Display ON "EPSON"

(2.1) RAM address setup command: 30H

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

(2.2) Data writing command: Writing "EPSON"

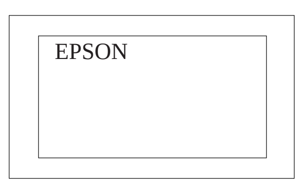
A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	1	0	0	0	1	0	1	E: 45H
1	0	0	1	0	1	0	0	0	0	P: 50H
1	0	0	1	0	1	0	0	1	1	S: 53H
1	0	0	1	0	0	1	1	1	1	O: 4FH
1	0	0	1	0	0	1	1	1	0	N: 4EH

(2.3) Waiting for 20ms or more

(2.4) Display ON/OFF control command: B, C→0, D→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

Display ON 5×7 Dots "EPSON"



(3) Display ON The Icon: Valid in Standby mode only

(3.1) Display ON/OFF command: D→OFF

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0

(3.2) Static display control command: 1 ~ 2Hz Blink

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	0

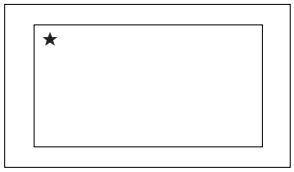
(3.3) Power save command: PS→ON, 0→ON

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	1

(3.4) Power control commands: P, VF, VC→OFF

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	0	0	0

Display ON the Icon



(4) Releasing the Standby Mode

(4.1) Power save command: PS→0, 0→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(4.2) Power control commands: P, VF, VC→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(4.3) Waiting for 20ms or more

(4.4) Display ON/OFF command: D→1

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

END of Releasing the Standby mode

16. OPTION LIST

S1D12200 Series provides the optional functions as described in the following. Being adaptable to the customer's optional demand, contact the Business Department of our company when installed.

○ Our product name corresponding to a customer's option is defined as shown below:

(Example)

S1D12200D★★B★

- Shipping form: A(Al padchip), B (Au bamp chip)
- Option corresponding digit
- Machine type: 00 (12 digits × 3 lines), 01 (12 digits × 2 lines)

1. Specification of Character Generator ROM (CGROM)
   S1D12200 Series integrates a character generator ROM which can generate a maximum of 256 type characters.
   The size of these characters is composed of 5 × 7 (8) dots.
   Being a mask ROM, the S1D12200 Series CGROM is adaptable to the character generator ROM exclusive for the customer, too.
   For our standard CGROMs, refer to the Character Fonts Table.
2. Specification of Liquid Crystal Driver Voltage Bias Value.
   S1D12200 Series integrates a liquid crystal diver voltage generator circuit. Its 5-volt potential is divided into resistance inside of IC to generate 1-V, 2-V, 3-V or 4-V potential as required for the liquid crystal driver.
   Further, the 1-V, 2-V, 3-V or 4-Vpotential is converted into impedance by a voltage follower to be supplied to the liquid crystal driver circuit.
   Either 1/5 or 1/4 bias value can be selected as demanded by the customer.
   Our standard bias value is preset to 1/5.
3. Specification of Reference Voltage of Liquid Crystal Driver Voltage Regulation Circuit.
   S1D12200 Series integrates a voltage regulation circuit using a booster voltage as its power supply to generate 5V for the liquid crystal driver via the voltage regulation circuit.
   The voltage regulation circuit integrates a reference voltage regulator V_{REG}.
   The customer can select a specification of using either the internal reference voltage or external V_{SS} reference voltage.
   Our standard specification is preset to the internal reference voltage.
4. Power Supply to Booster Circuit
   S1D12200 Series integrates a booster circuit.
   The customer can select a specification of using either the regulator output V_{S1} or V_{SS} as the supply voltage to the booster circuit.
   Our standard specification is preset to the regulator output V_{S1}.
5. External Clock Specifications
   S1D12200 Series integrates an external clock terminal and there are two clock specifications, f and 4×f oscillation.
   Either of them can be selected on your request.

	Internal oscillation	External clock f osc.	External clock 4×f osc.
Standard	○	○	×
Optional	○	×	○

   The standard external clock specification is set to f_{OSC}.

6. Reset Signal Input Polarity Specifications
   S1D12200 Series inputs reset signal from the reset terminal using edge detection and I/F specification 80/68 series can be selected according to this signal level.
   RES input polarity can also be selected on your request.

RES input polarity	Type	
	Standard	Optional
⌐↓	68 series	80 series
⌐↑	80 series	68 series

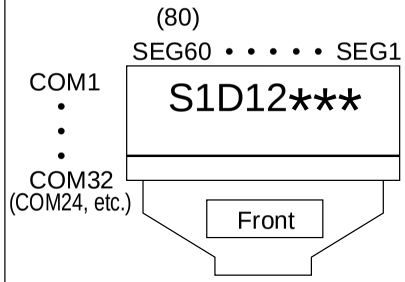
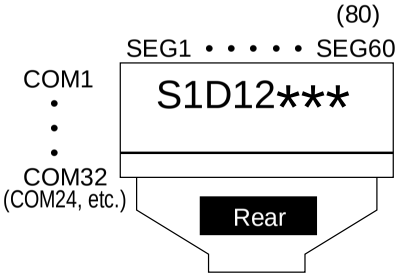
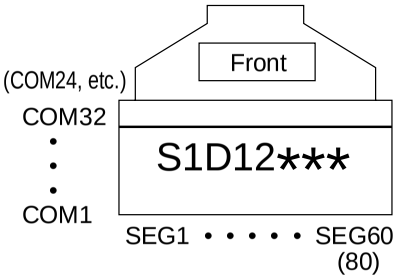
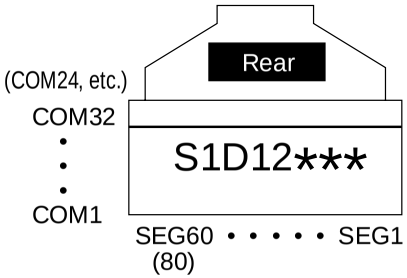
   ⌐↓ is set to the 68 series and ⌐↑ to the 80 series as the standard RES input polarities.

7. Pad Layout Specifications of COMS1 Symbol Terminal
   On S1D12200 Series, pad layout of COMS1 symbol terminal can be changed. COMS1 pad layout can be selected on your request.

	Standard	Optional
Pad No	Pad Name	Pad Name
65	COMS1	COM1
66	COM1	COM2
67	COM2	COM3
68	COM3	COM4
69	COM4	COM5
70	COM5	COM6
71	COM6	COM7
72	COM7	COM8
73	COM8	COMS1

S1D12200/12205/12400 Example of System Setup Depending on Mount Direction

Reference

	① Case1 (Chip Front)	② Case2 (Chip Rear)	③ Case3 (Chip Front)	④ Case4 (Chip Rear)
				
S1D12200	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
S1D12205	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
S1D12400	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order.

S1D12205 Series

Rev. 1.1

Contents

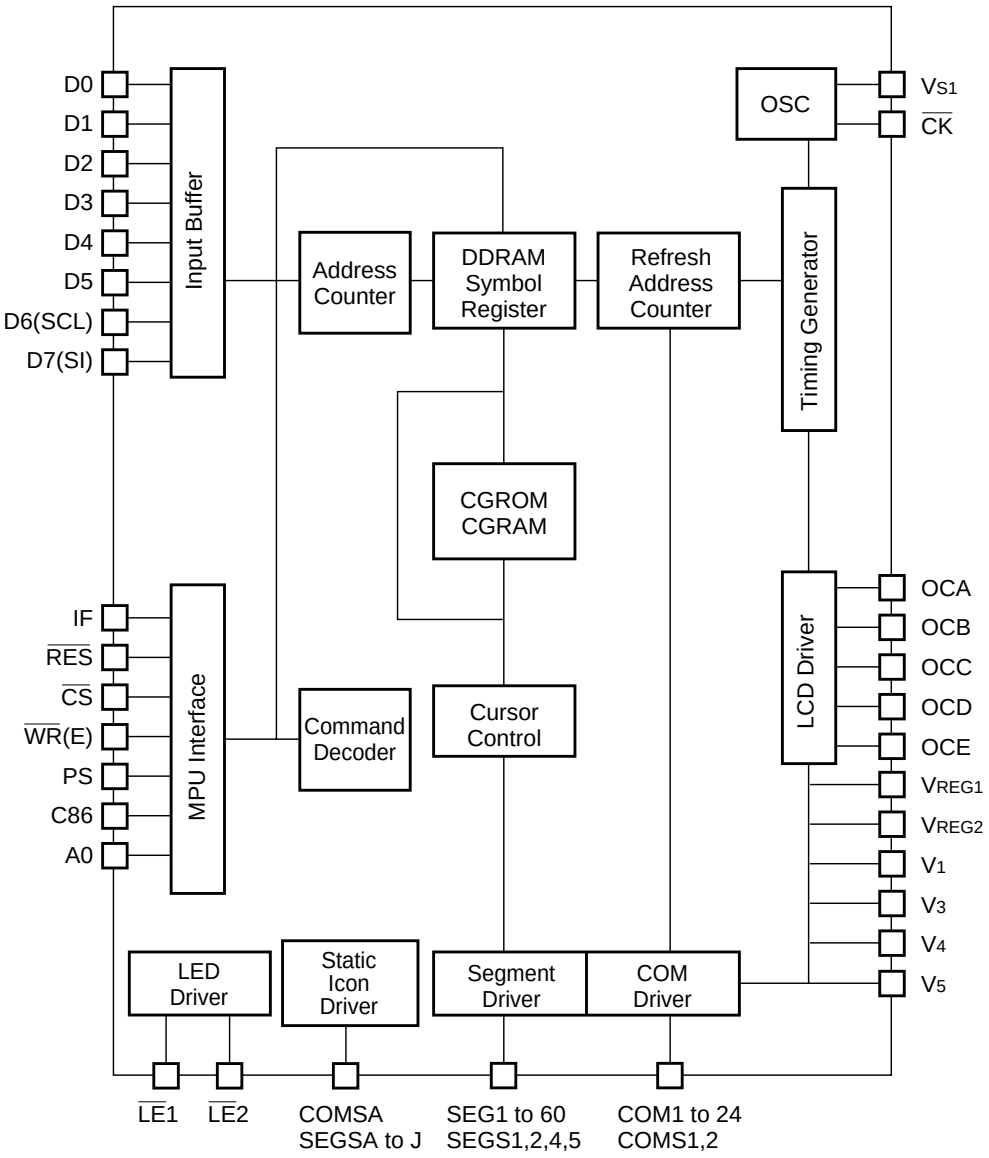
1. DESCRIPTION

The S1D12205 Series dot-matrix LCD Controller Driver receives 4-bit, 8-bit, or serial data from the microprocessor and displays up to 36 characters, four user-defined characters, and up to 120 symbols.
Up to 256 types of built-in character generator ROMs are provided. Each character font has a 5×8-dot structure. Also, the user-defined character RAM contains four 5×8-dot characters. In addition, a symbolic register can be used for flexible symbol display. The Driver featuring the very low power consumption can drive a handy terminal unit in either Sleep or Standby mode with the minimum power consumption.

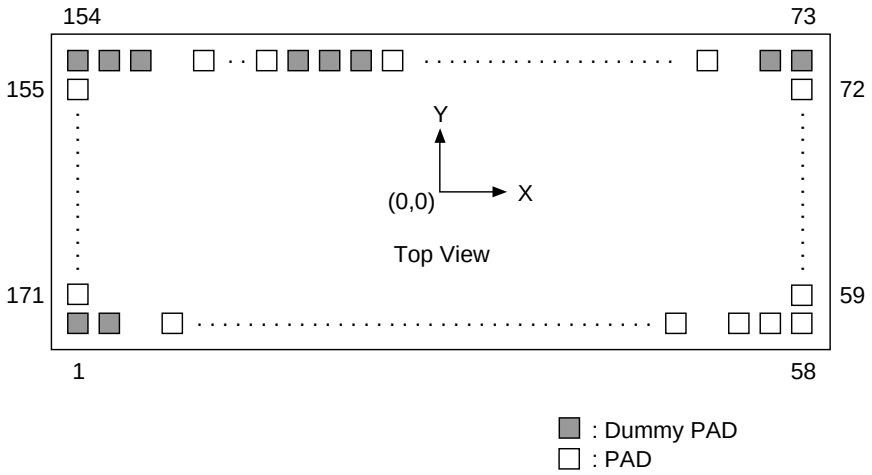
2. FEATURES

- Built-in display data RAM
  Can display up to 36 characters, 4 user-defined characters, and 120 symbols.
- Built-in CGROM (for 256-character display), CGRAM (for 4-character display), and symbol register (for 120 symbol display)
- No. of display columns by lines
  Normal mode: (12 columns plus 4 signal segments) × 3 line + 120 symbols + 10 static symbols
  Standby mode: 10 static symbols
- Built-in C&R oscillators
- Available external clock input
- HIGH-speed MPU interfaces
  Interface to both 68- and 80-series MPUs
  Support of 4/8-bit interface
- Support of serial interface
- Character font: 5x8 dots
- Duty ratio: 1/18, 1/26
- Simple command setup
- Built-in LCD drive power circuit: Power amp and regulator
- Built-in electronic controls
- Very low power consumption
  30 µA (including the operating current of the built-in power supply during normal operation)
  10 µA (Static icon display during Standby operation
  5 µA (Display off during Sleep operation)
- Power supplies
  V_{DD} – Vss: –1.7 to –3.6 V
  V_{DD} – V_5: –3.0 to –6.0 V
- Wide operating temperature range: Ta=-30 to +85°C
- CMOS process
- Package design
  Chip (Au bump): S1D12205D**B*
  TCP: S1D12205T****
- This IC package is not designed to have a radiation or strong light resistance.

3. BLOCK DIAGRAM



4. PIN LAYOUT



S1D12205D∗∗∗∗
↑
CGROM pattern version number

Chip size: 7.85 × 1.97 mm
Pad pitch: 90 µm (min)
Chip thickness (Reference): 625 µm

Au bump specifications
Bump size:
Pad Nos. 59 to 72, and 155 to 171: 78 µm × 59 µm
Pad Nos. 1 to 58, and 73 to 154: 59 µm × 78 µm
Bump height (Reference): 22.5 µm

Pad Center Coordinates

PAD		Coordinate	
No.	Name	X	Y
1	Dummy	-3768	-822
2	Dummy	-3678	
3	A0	-3349	
4	$\overline{WR}$(E)	-3200	
5	$\overline{CS}$	-3050	
6	D7(SI)	-2901	
7	D6(SCL)	-2751	
8	D5	-2602	
9	D4	-2452	
10	D3	-2303	
11	D2	-2153	
12	D1	-2004	
13	D0	-1854	
14	$\overline{LE}$1	-1705	
15	$\overline{LE}$1	-1615	
16	$\overline{LE}$2	-1466	
17	$\overline{LE}$2	-1376	
18	V_{DD}	-1286	
19	V_{DD}	-1197	
20	V_{SS}	-1107	
21	V_{SS}	-1017	
22	V_5	-868	
23	V_5	-778	
24	V_4	-629	
25	V_4	-539	
26	V_3	-389	
27	V_3	-300	
28	V_1	-150	
29	V_1	-60	
30	(V_{REG1})	89	
31	(V_{REG1})	179	
32	V_{REG2}	328	
33	V_{REG2}	418	
34	OCA	567	
35	OCA	657	
36	OCB	807	
37	OCB	896	
38	OCC	1046	
39	OCC	1136	
40	OCD	1285	
41	OCD	1375	
42	OCE	1524	
43	OCE	1614	

PAD		Coordinate	
No.	Name	X	Y
44	V_{SS}	1718	-822
45	V_{SS}	1808	
46	C86	1973	
47	PS	2122	
48	IF	2272	
49	$\overline{RES}$	2421	
50	$\overline{CK}$	2571	
51	VS1	2720	
52	(FSA)	2893	
53	(FSB)	3065	
54	(FSC)	3237	
55	(FS3)	3409	
56	(V_{DD})	3589	
57	(V_{DD})	3678	
58	(V_{DD})	3768	
59	(FS2)	3758	-628
60	(FS1)		-456
61	(FS0)		-283
62	COMSA		-179
63	COMS1		-90
64	COM1		0
65	COM2		90
66	COM3		179
67	COM4		269
68	COM5		359
69	COM6		449
70	COM7		538
71	COM8		628
72	COMS1		718
73	Dummy	3768	822
74	Dummy	3678	
75	SEGS1	3409	
76	SEGS2	3320	
77	SEG1	3230	
78	SEG2	3140	
79	SEG3	3050	
80	SEG4	2961	
81	SEG5	2871	
82	SEG6	2781	
83	SEG7	2692	
84	SEG8	2602	
85	SEG9	2512	
86	SEG10	2423	

Note 1 : Set the pins V_{DD} of Nos. 56 to 58 and the pins V_{RBG1} of Nos. 30 and 31 to the floating state.

2 : Since the pins FS* of Nos. 52 to 55 and 59 to 61 are for fuse adjustment, set them to the floating state.

PAD		Coordinate	
No.	Name	X	Y
87	SEG11	2333	822
88	SEG12	2243	
89	SEG13	2153	
90	SEG14	2064	
91	SEG15	1974	
92	SEG16	1884	
93	SEG17	1795	
94	SEG18	1705	
95	SEG19	1615	
96	SEG20	1526	
97	SEG21	1436	
98	SEG22	1346	
99	SEG23	1256	
100	SEG24	1167	
101	SEG25	1077	
102	SEG26	987	
103	SEG27	898	
104	SEG28	808	
105	SEG29	718	
106	SEG30	629	
107	SEG31	539	
108	SEG32	449	
109	SEG33	359	
110	SEG34	270	
111	SEG35	180	
112	SEG36	90	
113	SEG37	1	
114	SEG38	-89	
115	SEG39	-179	
116	SEG40	-268	
117	SEG41	-358	
118	SEG42	-448	
119	SEG43	-538	
120	SEG44	-627	
121	SEG45	-717	
122	SEG46	-807	
123	SEG47	-896	
124	SEG48	-986	
125	SEG49	-1076	
126	SEG50	-1165	
127	SEG51	-1255	
128	SEG52	-1345	
129	SEG53	-1435	

PAD		Coordinate	
No.	Name	X	Y
130	SEG54	-1524	822
131	SEG55	-1614	
132	SEG56	-1704	
133	SEG57	-1793	
134	SEG58	-1883	
135	SEG59	-1973	
136	SEG60	-2062	
137	SEGS4	-2152	
138	SEGS5	-2242	
139	Dummy	-2332	
140	Dummy	-2422	
141	Dummy	-2512	
142	COM24	-2602	
143	COM23	-2692	
144	COM22	-2781	
145	COM21	-2871	
146	COM20	-2961	
147	COM19	-3050	
148	COM18	-3140	
149	COM17	-3230	
150	COM16	-3320	
151	COM15	-3409	
152	Dummy	-3589	
153	Dummy	-3678	
154	Dummy	-3768	
155	COM14	-3758	718
156	COM13		628
157	COM12		538
158	COM11		449
159	COM10		359
160	COM9		269
161	COMS2		179
162	SEGSA		90
163	SEGSB		0
164	SEGSC		-90
165	SEGSD		-179
166	SEGSE		-269
167	SEGSF		-359
168	SEGSG		-449
169	SEGSH		-538
170	SEGSI		-628
171	SEGSJ		-718

5. PIN DESCRIPTION

Power Supply Pins

Pin Name	I/O	Description	No. of Pins
V_{DD}	Power supply	Connects to the logic power supply. This is common to the Vcc power pin of the MPU.	1
V_{SS}	Power supply	0V power pin connected to system ground (GND)	2
V_1, V_3 V_4, V_5	Power supply	Multi-level LCD drive power supplies. A capacitor is required for external stabilization.	4
V_{S1}	O	Output pin of oscillator (OSC) power voltage. Do not connect any external load to this pin.	1

Notes: Two V_{SS} pins are provided. As they are commonly connected inside the IC, an input into any V_{SS} can be used if power impedance is LOW. To have the enough noise resistance, however, the V_{SS} power input from each pin is recommended.

LCD Power Pins

Pin Name	I/O	Description	No. of Pins
V_{REG2}	O	Output pins of LCD voltage and amp source power supplies. A capacitor is required for stabilization.	1
OCA OCB OCC OCD OCE	O	A voltage capacitor pin. A capacitor is required for amplification.	5

LED Drive Terminal

Pin Name	I/O	Description	No. of Pins
$\overline{LE1}$ $\overline{LE2}$	O	An Nch open drain output terminal to drive the LED. Connects to the LED cathode.	2

System Bus Connector Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descrition</th><th>No. of Pins</th></tr>
<tr><td>D7(SI)
D6(SCL)
D5 to D0</td><td>I</td><td>An 8-bit input data bus to be connected to the standard 8- or 16-bit MPU data bus. Pins D7 and D6 function as the serial data and clock inputs respectively if PS is logical low.
<table>
<tr><th>PS</th><th>C86</th><th>IF</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3 to D0</th><th>$\overline{CS}$</th><th>A0</th><th>$\overline{WR}$</th></tr>
<tr><td>LOW</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LOW</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LOW</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
Open : May be open. However, the potential is recommended to fix to have better noise-resistance characteristics.
- : May be HIGH or LOW. However, the potential must be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, the most significant bit of MPU address bus is connected to identify data or command.
0: Indicates D0 to D7 are command.
1: Indicates D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Initializes when $\overline{RES}$ is set to LOW. The system is reset at $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>A Chip Select signal. The address bus signal is decoded and entered. This is valid when LOW.</td><td>1</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>- When an 80-series MPU is connected
Active LOW.
The $\overline{WR}$ signal of 80-series MPU is connected. The data bus signal is fetched at the rising edge of $\overline{WR}$ signal.
- When a 68-series MPU is connected
Active HIGH.
Used as an Enable Clock input of 68-series MPU. The data bus signal is fetched at the falling edge of $\overline{WR}$ signal.</td><td>1</td></tr>
<tr><td>PS</td><td>I</td><td>A switching pin between serial data input and parallel data input.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data/Command</th><th>Data</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>—</td></tr>
<tr><td>LOW</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>An interface data length select pin during parallel data input.
- 8-bit parallel input if IF=HIGH
- 4-bit parallel input if IF=LOW
This pin is connected to V_{DD} or V_{SS} if PS=LOW.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>An MPU interface switch pin.
- 68-series MPU interface if C86=HIGH
- 80-series MPU interface if C86=LOW
This pin is connected to V_{DD} or V_{SS} if PS=LOW.</td><td>1</td></tr>
<tr><td>$\overline{CK}$</td><td>I</td><td>An external clock input pin.
It must be fixed to HIGH to use the internal oscillator.
To use an external clock input, turn the internal oscillator OFF by issuing the command.</td><td>1</td></tr>
</table>

LCD Driver Signals

Dynamic drive pins

Pin Name	I/O	Description	No. of Pins
COM1 to COM24	O	Common signal output pins (for character display)	24
COMS1, COMS2	O	Common signal output pins (for non-character display) COMS1, COMS2: Common outputs for symbol display	3
SEG1 to SEG60	O	Segment signal output pins (for character display)	60
SEGS1, 2 4, 5	O	Segment signal output pins (for non-character display) SEGS1, 2, 4, 5: Segment outputs for signal output	4

Note: As the same COMS1 signal is output at two pins, one of them must be used.

Static drive pins

Pin Name	I/O	Description	No. of Pins
COMSA	O	Common signal output pin (for icon display)	1
SEGSA, B C, D, E, F G, H, I, J	O	Segment signal output pin (for icon display)	10

Notes: We recommend to separate LCD panel electrodes of static drive pins from those of dynamic drive pins. If these patterns are closely located, the LCD and its electrodes may be deteriorated.

6. FUNCTION DESCRIPTION

MPU Interfaces

Interface type selection

The S1D12205 Series can transfer data via the 4- or 8-bit data bus or via the serial data input (SI). The parallel or serial data input can be selected by setting the PS pin to HIGH or LOW (see Table 1).

Table 1

PS	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0 to D7
HIGH	Parallel input	$\overline{CS}$	A0	$\overline{WR}$	–	–	D0 to D7
LOW	Serial input	$\overline{CS}$	A0	HIGH, LOW	SI	SCL	–

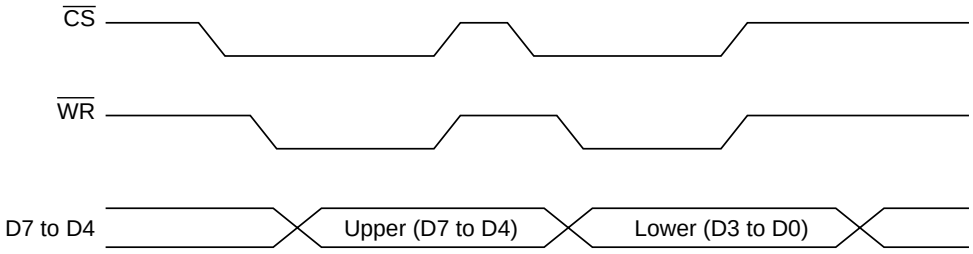
The S1D12205 Series has the C86 pin for MPU selection. If the parallel input is selected (PS=HIGH), if can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to HIGH or LOW (see Table 2). Also, the 8-bit or 4-bit data bus can be selected by the IF pin signal.

Table 2

C86 pin signal	Type	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
LOW	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
HIGH	68 series	A0	E	$\overline{CS}$	D0 to D7

Interface to 4-bit MPU

If the 4-bit interface is selected (IF=LOW), the 8-bit command and data, and its address are transferred in two times.



Note: During continuous writing, the write time greater than the system cycle time (tcyc) must be set before the subsequent write operation.

Serial interface

The serial interface consists of an 8-bit shift register and a 3-bit counter. During chip select ($\overline{CS}$=LOW), an SI input and an SCL input can be accepted. During no chip select ($\overline{CS}$=HIGH), the shift register and counter is initialized (reset).
Serial data of D7 to D0 are fetched in this order from the serial data input pin (SI) at the rising edge of serial clock. The data is converted into 8-bit parallel data at the rising edge of the eighth serial clock.
The serial data input (SI) is identified to have the display data or command by the A0 input. It is display data if A0=HIGH, and it is command if A0=LOW.
The A0 input is fetched and identified at the rising edge of "8 × n-th" serial clock (SCL). Figure 1 shows a serial interface timing chart.
The SCL signals must be well protected from the far-end reflection and ambient noise due to increased line length. The operation checkout on the actual machine is recommended.
Also, we recommend to repeat periodical command writing and status refreshing to avoid a malfunction due to noise.

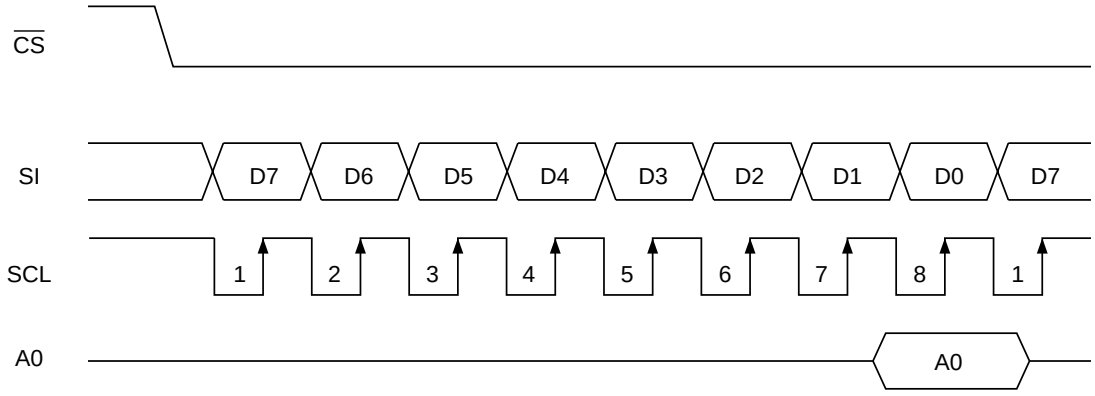


Figure 1

Data bus signal identification

The S1D12205 Series identifies the data bus based on a combination of A0, $\overline{WR}$ and E signals as defined on Table 3.

Table 3

Common	68 Series	80 Series	Function
A0	E	$\overline{WR}$	
1	1	0	Writes to the RAM and symbol register.
0	1	0	Writes to the internal (commands) register.

Chip Select

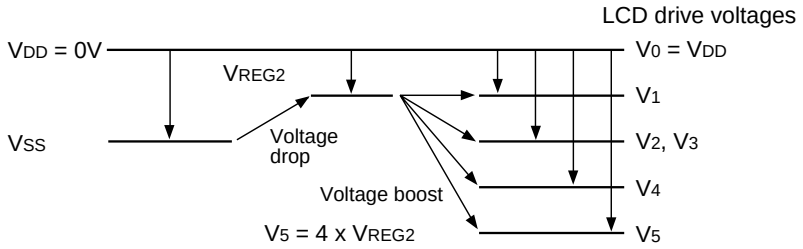
The S1D12205 Series has an Chip Select pin ($\overline{CS}$) to allow an MPU interface input only if $\overline{CS}$=LOW.
During no chip select status, all of D0 to D7, A0, $\overline{WR}$, SI and SCL inputs are made invalid. If the serial input interface is selected, the shift register and counter are reset.
However, the Reset signal is entered independent from the $\overline{CS}$ status.

Power Circuit

The built-in power circuit featuring the low power consumption generates the required LCD drive voltages. The power circuit consists of an booster and a voltage regulator.

Booster Circuit

When the capacitors are connected to the OCA, OCB, OCC, OCD, OCE, V_{REG2} pins, the LCD drive voltages are generated.
As the booster uses the signals from the oscillator, the oscillator or an external clock must be operating.
The following provides the potential relationship.



Voltage regulator

- Voltage regulator using the electronic control function
  Use the electronic control function and set the voltages appropriate to the LCD panel driving.
  When a 5-bit data is set in the electronic control register, one of 32-state voltages can be set for LCD driving. Before using the electronic control function, turn ON the power circuit by issuing the power control command.
  The following explains how to calculate the voltages using the electronic control function.

$V_5 = 4 \times V_{EV}$

Conditions:

$V_{EV} = V_{REG2} - X$

where,

$X = n\alpha$ (n=0, 1, ..., 31)

$\alpha = V_{REG2}/95$

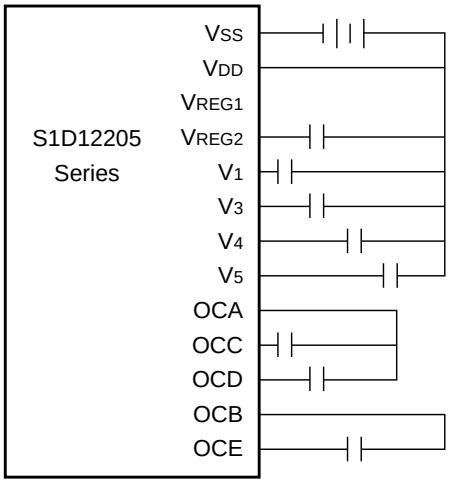
No.	Electronic control register	X	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

This is reference voltage for the liquid crystal drive power circuit. The V_{REGZ} has a temperature characteristics of about –0.05%/deg.

External unit connection examples

An external voltage regulation capacitor must be connected to the LCD power pin. The LCD drive voltages are fixed to 1/4 biasing.

1/4 bias example



Note: We recommend to display the capacitance appropriate to the LCD panel size and set up the capacitance by observing the drive signal waveforms.

Reference set value: (0.1~1.0 μF)

Power Save mode

The S1D12205 Series supports the Standby and Sleep modes to save the power consumption during system idling.

- Standby mode
  The Standby mode is selected or released by the Power Save command. During Standby mode, only the static icon is displayed.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Can light by static drive
     Use the Static Icon RAM to display the static icon with SEGSA, B, C, D, E, F, G, H, I, J and COMSA.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     The internal circuits for dynamic display are stopped.
  4. Oscillator
     The oscillator must be turned ON for static display.
- Sleep mode
  To select the Sleep mode, turn OFF the power circuit and oscillator by issuing the command, and clear all data of Static Icon register to zero. Then, issue the Power Save command. The system power consumption will be minimized to almost the stopped status.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Clear all data of Static Icon register to zero.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     All internal circuits are stopped.
  4. Oscillator
     Turn OFF the built-in power supply and oscillator by issuing the Power Save and power control commands.

Reset Circuit

When the $\overline{RES}$ input is made active, this LSI is initialized.

- Initialization status
  - (1) Display ON/OFF control
    - C=0: Cursor off
    - B=0: Blink off
    - DC=0: Normal display
    - D=0: Display off
  - (2) Power save
    - O=0: Oscillating circuit off
    - PS=0: Power save off
  - (3) Power control
    - P=0: Power circuit off
  - (4) System set
    - N=0: 3 lines
    - S2, S1=0: Direction of normal display
    - CG=0: CGRAM unused
  - (5) Electronic control
    - Address: 28H
    - Data: (0,0,0,0,0)
  - (6) Static icon
    - Address: 20H to 23H
    - Data: (0,0,0,0,0)
  - (7) LED register
    - Address: 2AH
    - Data: (0,0,0,0,0)
  - (8) CG RAM, DD RAM and symbol register
    - Address: 00H to 1FH, 30H to 7CH
    - Data: Must be initialized by MPU after reset input because of being indefinite.

Connect the $\overline{RES}$ terminal to the MPU reset terminal as described in "6-1 MPU Interface", and execute initialization simultaneously with the MPU. However, if the MPU bus and port are put into HIGH impedance for a certain time period by resetting, perform reset input to the S1D12205 Series after the input to the S1D12205 Series has been determined. When the $\overline{RES}$ terminal becomes LOW, each register is cleared and the above setup is established. If initialization by the $\overline{RES}$ terminal is not performed when power voltage is applied, resetting may be disabled.

7. COMMAND

Table 4 lists the supported commands. The S1D12205 Series identifies a data bus by a combination of A0, $\overline{WR}$ and E signals. It features HIGH-speed processing as the commands are analyzed and executed in the internal timing only.

- Command outline

Table 4

Command type	Command name	A0	$\overline{WR}$
Display control instruction	Cursor Home	0	0
	Display On/Off Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System setup	System Setup	0	0
Address control instruction	Address Setup	0	0
Data input instruction	Data Write	1	0

As the execution time of each instruction depends on the internal processing time of the S1D12205 Series, an enough time greater than the system cycle time (tcyc) must be assigned for continuous instruction execution.

- Explanation of commands

(1) Cursor Home

The Cursor Home command presets the Address counter to 30H, and shifts the cursor to column 1 of line 1 if Cursor Display is ON.

A0 $\overline{WR}$ D7 —— D0

0	0	0	0	0	1	✻	✻	✻	✻

✻ : Don't Care

(2) Display On/Off Control

The Display On/Off Control command sets the LCD character and cursor display.

A0 $\overline{WR}$ D7 —— D0

0	0	0	0	1	1	C	B	DC	D

✻ : Don't Care

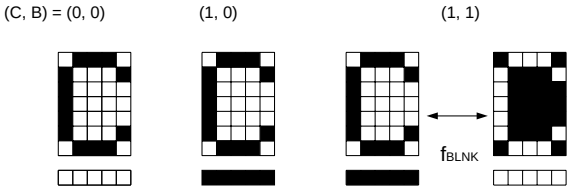
D=0: Turns the display off.
D=1: Turns the display on.
DC=0: Selects the standard size display.
DC=1: Selects the double-height vertical display.
B=0: Turns cursor blinking off.
B=1: Turns cursor blinking on.

During blinking, the cursor character is alternately displayed normally and reversely. The normal and reverse display is repeated approximately every one second.

C=0: Does not display the cursor.
C=1: Displays the cursor.

The following provides the relationship between the C and B registers and cursor display.

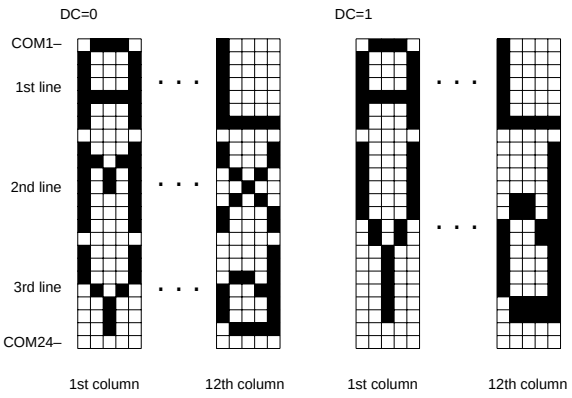
C	B	Cursor display
0	0	Not displayed
0	1	Not displayed
1	0	Underbar cursor
1	1	Alternate character display normally and reversely



The cursor display position is indicated by the address counter. Accordingly, to move the cursor, change the address counter value by automatic increment by writing the RAM address set command or RAM data.

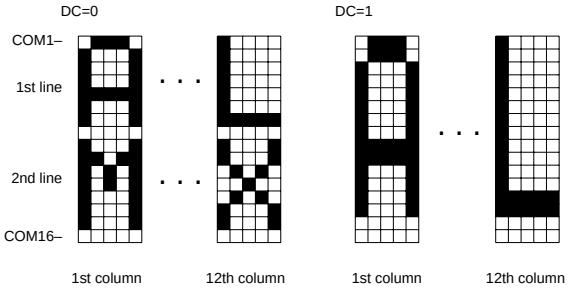
The following shows the relationship between the DC resistor and display:

(1) N=0 (1/26 duty)



The character on the 3rd line will be displayed in double size on the second and third lines by setting DC=1.

(2) N=1 (1/18 duty)



The character on the 1st line will be displayed in double size on the first and second lines by setting DC=1.

(3) Power Save

The Power Save command controls the oscillator and sets or releases the Sleep mode.

A0 $\overline{WR}$ D7 ——— D0

0	0	0	1	0	0	✻	✻	O	PS

✻ : Don't Care

PS=0: Turns the Power Save on. (Release)
PS=1: Turns the Power Save off. (Select)
O=0: Turn the oscillator off. (Stop oscillation)
O=1: Turns the oscillator on. (Oscillation)

(4) Power Control

The Power Control command controls the built-in power circuit operations.

A0 $\overline{WR}$ D7 ——— D0

0	0	0	1	0	1	0	0	0	P

✻ : Don't Care

P=0: Turns the power circuit off.
P=1: Turns the power circuit on.
Note: The oscillator must be operating to operate the voltage amp.

(5) System Reset

The System Reset command sets the display direction, the display line, and the use or no use of CGRAM. This command must first be executed after the power-on or reset.

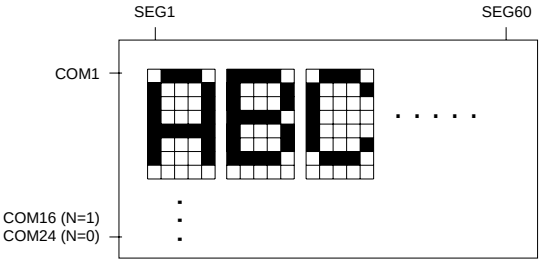
A0 $\overline{WR}$ D7 ——— D0

0	0	0	1	1	0	N	S2	S1	CG

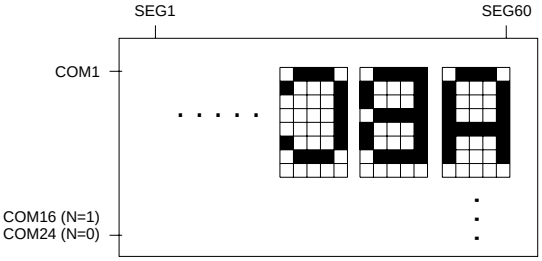
✻ : Don't Care

N=0: Displays 3 lines. (1/26 duty)
N=1: Displays 2 lines. (1/18 duty)
S2=0: Normal display
S2=1: Right and left reverse display
S1=0: Normal display
S1=1: Top and bottom reverse display
CG=0: Does not use the CGRAM.
CG=1: Uses the CGRAM.

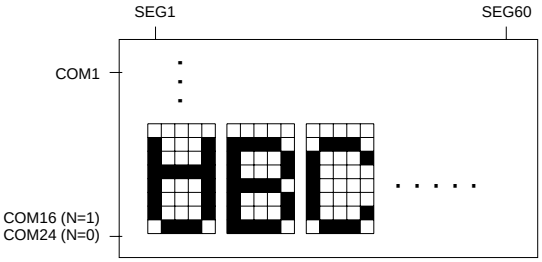
(1) Normal display



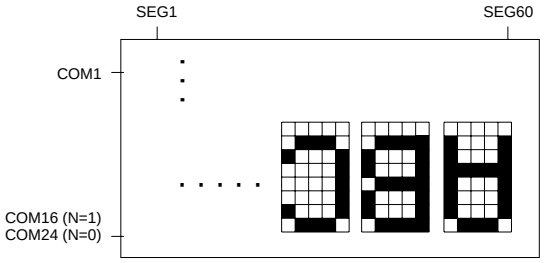
(2) Horizontal flipping



(3) Vertical flipping



(4) Horizontal vertical flipping



(6) RAM Address Setup

The RAM Address Setup command sets an address into the Address counter to write data into DDRAM, CGRAM and Symbol register.
When the cursor display is ON, the cursor is located at a position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	———	D0
0	0	1	ADDRESS	

✻ : Don't Care

① The 00H to 7FH address length can be set. To write data in the RAM, set the data write address by this command. When the subsequent data is written continuously, the address is automatically incremented.

RAM map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM (00H)								CGRAM (01H)							
10H	CGRAM (02H)								CGRAM (03H)							
20H	SI1			SI2			Unused		EV	TEST		LED	Unused			
30H	DDRAM line 1								For signals →							Unused
40H	DDRAM line 2															Unused
50H	DDRAM line 3															Unused
60H	Symbol register															Unused
70H	Symbol register															Unused

SI : Static Icon register
EV : Electronic Control register
TEST : Test register
(Do not use in normal operations.)

LED : LED register
For signals : SEGS1, 2, 4, 5
Symbol register : COMS1, COMS2

(7) Data Write

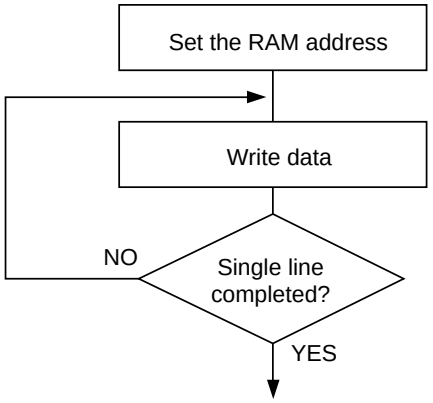
A0	$\overline{WR}$	D7	———	D0
1	0	DATA		

✻ : Don't Care

① This command writes data in the DDRAM, CGRAM or Symbol register.
② When this command is executed, the Address counter is incremented by 1 automatically. This allows continuous data writing.

Data write example:

The following gives an example to write a single line of data continuously.



Note: Assign an enough time greater than "tcyc" before executing the next instruction.

Table 4 S1D12205 Series command list

Command	Code										Function
	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Shifts the cursor to its home position.
(2) Display On/Off Control	0	0	0	0	1	1	C	B	DC	D	Turns on or off the cursor, cursor blinking, double-size display, and data display. C=1: Cursor ON; C=0: Cursor OFF B=1: Blinking ON; B=0: Blinking OFF DC=1: Double-size display; DC=0: Normal display D=1: Display ON; D=0: Display OFF
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Turns on or off the Power Save mode and oscillator. PS=1: Power Save ON; PS=0: Power Save OFF O=1: OSC ON; O=0: OSC OFF
(4) Power Control	0	0	0	1	0	1	0	0	0	P	Turns on or off the built-in power circuit and voltage follower capacity, and sets the amp frequency. P=1: Power circuit ON; P=0: Power circuit OFF
(5) System Reset	0	0	0	1	1	0	N	S2	S1	CG	Sets the use or no use of CGRAM and the display direction. N=0: 3-line display; N=1: 2-line display CG=1: Use of CGRAM; CG=0: No use of CGRAM S2=0, S1=0: Normal display S2=0, S1=1: Top and bottom reverse display S2=1, S1=0: Right and left reverse display S2=1, S1=1: 180-degree rotation display
(6) RAM Address Setup	0	0	1	ADDRESS							Sets an address of DDRAM, CGRAM or Symbol register.
(7) RAM Write	1	0	DATA								Writes data in the DDRAM, CGRAM or Symbol register.
(8) NOP	0	0	0	0	0	0	0	0	0	0	This is a non-operation command.
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	This is an IC chip test command. Do not use in normal operations.

8. BUILT-IN MEMORIES

Character Generator ROM (CGROM)

The S1D12205 Series contains up to 126 types of CGROMs. Each character has a 5×8-dot structure. Tables 5 to 8 defines the S1D12205D✱✱✱✱ character codes. Four characters (00H to 03H) of character codes are used for the CGROM or CGRAM by the System Setup command.

The S1D12205's CGROM is a mask ROM and it can be used as a custom CGROM. Consult to our sales agency for details.
The CGROM versions are identified as follows:
Example: S1D12205D00B✱

↑
CGROM pattern code

Table 5 S1D12205D10B*

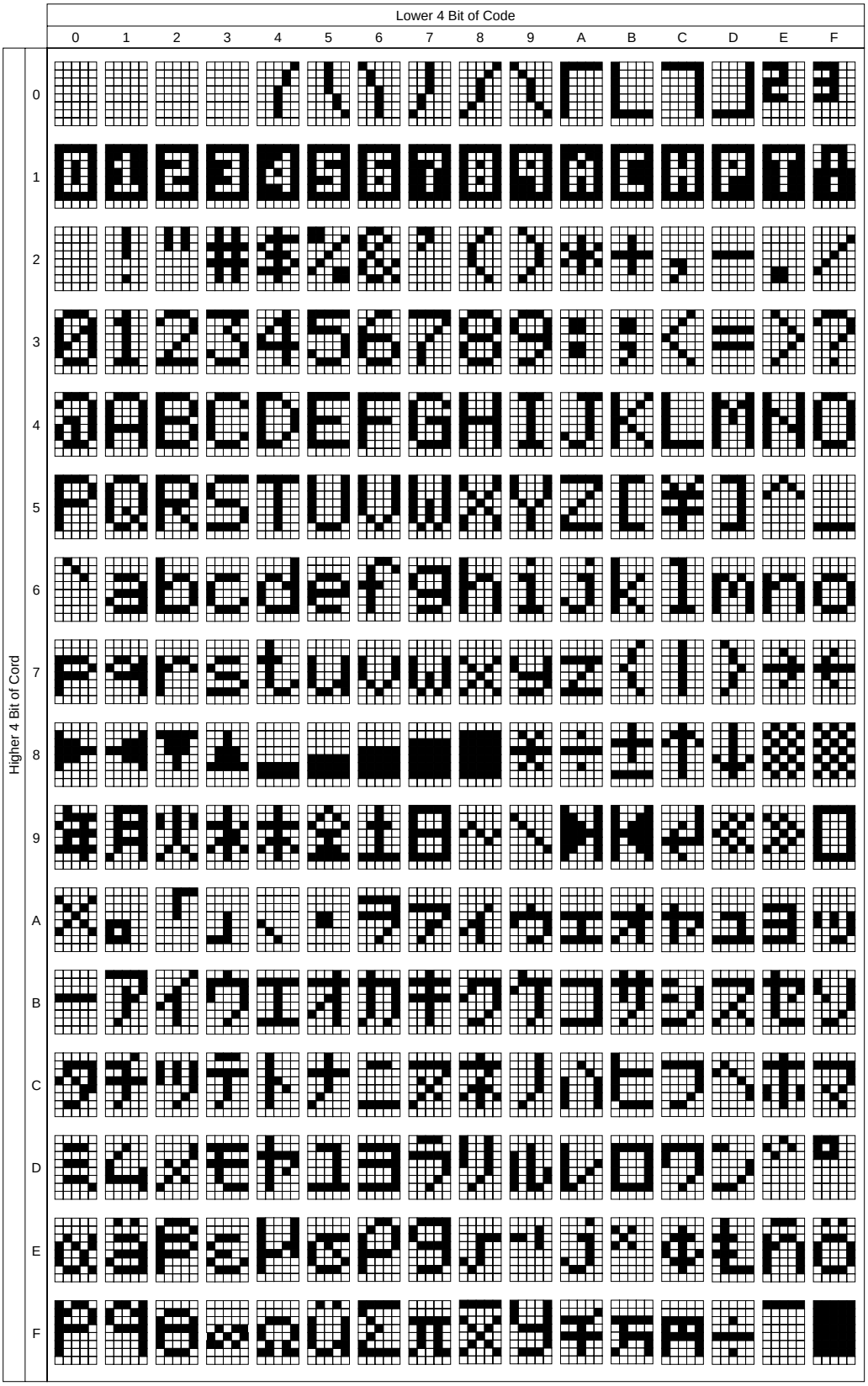
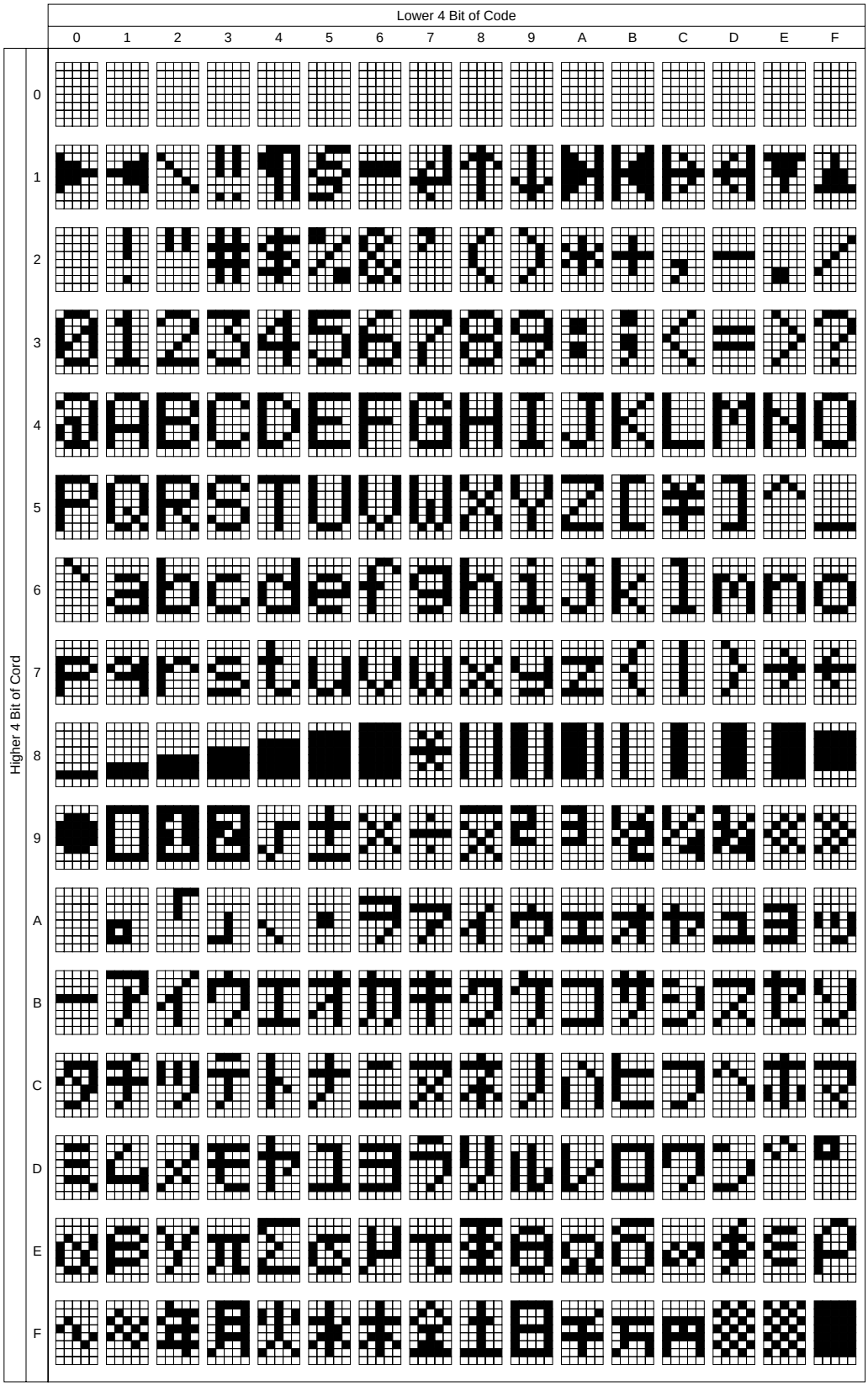


Table 6 S1D12205D11B*

Table 7 S1D12205D16B*



Character Generator RAM (CGRAM)

The S1D12205 Series has a built-in CGRAM to program user-defined character patterns for highly flexible signal and character display.
Issue the System Setup command to use the CGRAM. The CGRAM has the 160-bit storage capacity, and it can store up to four 5×8-dot character patterns.
The following provides the relationship between CGRAM character patterns and CGRAM addresses and character codes.

Character Code	RAM Address		CGRAM Data D7							D0	Character Display SEG	Signal Display SEGS 1 2	4 5
00H	00H to 07H	0	*	*	*	0	1	1	1	1	□■■■■	□■	■■
		1	*	*	*	1	0	0	0	0	■□□□□	■□	□□
		2	*	*	*	1	0	0	0	0	■□□□□	■□	□□
		3	*	*	*	0	1	1	1	1	□■■■■	□■	■■
		4	*	*	*	0	0	0	0	1	□□□□■	□□	□■
		5	*	*	*	0	0	0	0	1	□□□□■	□□	□■
		6	*	*	*	1	1	1	1	0	■■■■□	■■	■□
		7	*	*	*	0	0	0	0	0	□□□□□	□□	□□
01H	08H to 0FH	8	*	*	*	0	0	1	0	0	□□■□□	□□	□□
		9	*	*	*	0	0	1	0	0	□□■□□	□□	□□
		A	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		B	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		C	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		D	*	*	*	1	1	1	1	1	■■■■■	■■	■■
		E	*	*	*	1	1	1	1	1	■■■■■	■■	■■
		F	*	*	*	0	0	0	0	0	□□□□□	□□	□□

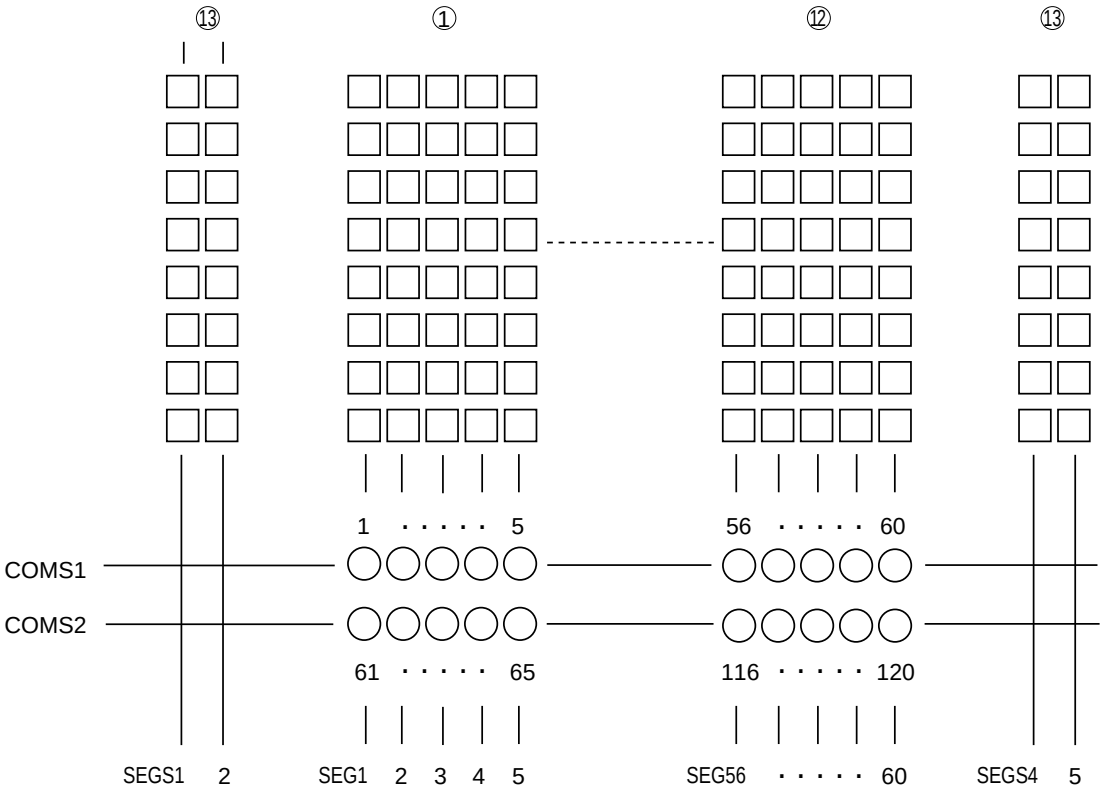
D7 to D5: Un used
D4 to D0: Character data (1 for display; 0 for no display)

The 5×8-dot character size can also be set. To do so, use the *7H and *FH RAM addresses. However, the *7H and *FH data is reversed if the underbar cursor is used.

Symbol Register

The S1D12205 Series has a built-in Symbol register to allow separate symbol setup on the display panel. The Symbol register has the 120-bit storage capacity, and it can display 120 symbols. Also, the S1D12205 Series contains a Blink register for every 5-dot blinking.

The following provides the relationship between the Symbol register display patterns, RAM addresses and write data.



RAM Address		Corresponding symbol bits							
		D7	D6	D5	D4	D3	D2	D1	D0
60H to 6BH	0	*	*	BL1	1	2	3	4	5
	1	*	*	BL2	6	7	8	9	10
	:	:							
	B	*	*	BL12	56	57	58	59	60
70H to 7BH	0	*	*	BL13	61	62	63	64	65
	1	*	*	BL14	66	67	68	69	70
	:	:							
	B	*	*	BL24	116	117	118	119	120

BL1 to BL24: Blinking setup (0 for no blinking; 1 for blinking)

Note: If the symbol size is 1.5 times greater than other dots, we recommend to divide and drive the SEG* and COMS1 and COMS2 separately.

Static Icon RAM

The S1D12205 Series has a built-in Static Icon RAM to display a static icon separately from the dynamic icon. The Static Icon RAM has the 20-bit storage capacity, and it can display 10 icons. The following provides the relationship between the static icon functions and the static icon, RAM address and write data.

(SEGSA, B, C, D, E)

Function	RAM Address	Static Icon Data D7							D0	Display SEGSA B C D E
Display ON/OFF	20H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	21H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

(SEGSF, G, H, I, J)

Function	RAM Address	Static Icon Data D7							D0	Display SEGSA B C D E
Display ON/OFF	22H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	23H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

* : Unused
1 : Display or blinking
0 : No display or no blinking
f BLINK : 1 to 2Hz

Electronic Control RAM (Register)

The S1D12205 SERIES has the electronic control functions to control LCD drive voltages and to adjust the LCD display density. One of 32-state LCD voltages can be selected when the 5-bit data is written in the Electronic Control RAM.

The following provides the relationship between the RAM address and write data by electronic control setup.

Function	RAM Address	Electronic Control Data D7 — D0								Status	VEV
Electronic Control	28H	*	*	*	0	0	0	0	0	0	VREG-0
		*	*	*	0	0	0	0	1	1	VREG-α
		*	*	*	0	0	0	1	0	2	VREG-2α
		. . . . .								. . . . .	. . . . .
		*	*	*	1	1	1	0	1	29	VREG-29α
		*	*	*	1	1	1	1	0	30	VREG-30α
		*	*	*	1	1	1	1	1	31	VREG-31α
	29H	*	*	*	*	*					For test

* : Unused
α : α=VREG/95 (1/4biased)
Note: Do not use address 29H as it can be used for IC chip test only.

LED RAM (Register)

The S1D12205 Series has the LED drive functions to drive the LCD by controlling the $\overline{LE}1$ and $\overline{LE}2$ pins.

The following provides the relationship between the RAM address and write data by LED register setup.

Function	RAM Address	LED Register Data D7				D3	D2	D1	D0
LED ON/OFF Timer	2AH	✻	✻	✻	✻	TIM2	TIM1	LED2	LED1

✻ : Unused

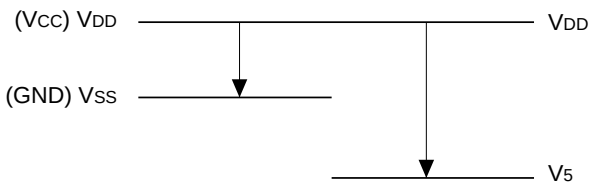
The following defines the $\overline{LE}1$ and $\overline{LE}2$ pin state depending on the TIM1, TIM2, LED1 and LED2 set values.

LED Register Set Value		Output Status ($\overline{LE}1$, $\overline{LE}2$)
TIM2 TIM1	LED2 LED1	
0	0	$\overline{LE}$ = HIGH impedance
0	1	$\overline{LE}$ = LOW
1	0	Keeps $\overline{LE}$ LOW approximately 15 sec after input of Display ON command.
1	1	$\overline{LE}$ = LOW

Note: When this function is used, minimize power supply and power cable impedance to avoid IC misoperation due to large current.

9. ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Power voltage (1)		V_{SS}	–0.6 to +0.3	V
Power voltage (2)		V_5	–7.0 to +0.3	V
Power voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		Topr	–30 to +85	°C
Storage temperature	TCP	Tstr	–55 to +100	°C
	Bare chip		–65 to +125	



Notes:
1. All voltages are referenced to V_{DD}=0 V.
2. The following voltage levels must always be satisfied:
   $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4$, and $V_{DD} \geq V_{SS} \geq V_5$
3. If the LSI is used beyond the maximum absolute rating, the LSI may be destroyed permanently. The LSI should meet the electric characteristics during normal operations. If not, the LSI may be malfunction or the LSI reliability may be lost.

10. DC CHARACTERISTICS

(V_{SS} = –3.6 to –1.7 V, Ta = –30 to +85°C unless otherwise noted.)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Pin
Power voltage (1)	Operable	V_{SS}	1/4 bias	–3.6	–3.0	–1.7	V	V_{SS}
			1/5 bias	–3.6	–3.0	–2.7		
	Data hold voltage			–3.6		–1.5		
Power voltage (2)	Operable	V_5		–6.0		–3.0	V	V_5
	Operable	V_1, V_2		0.5 × V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4		V_5		0.5 × V_5	V	V_3, V_4
HIGH input voltage		V_{IHC}		0.2 × V_{SS}		V_{DD}	V	*2
LOWinput voltage		V_{ILC}		V_{SS}		0.8 × V_{DD}	V	*2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*2
LCD driver ON resistance		R_{ON} (LCD)	Ta=25°C, ΔV=0.1V, V_5=–5.0V		10	20	kΩ	COM, SEG *3
LED driver ON resistance		R_{ON} (LED)	V_{SS}=–3.0V, I_{OL}=10mA		100		Ω	$\overline{LE1}$, $\overline{LE2}$
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5 = –5V; No loading V_{SS}=–1.8V		20	30	µA	V_{DD} *4
		During display	V_5 = –5V; No loading V_{SS}=–3.0V		30	45	µA	V_{DD} *4
		During standby	OSC On; PWR off No loading; V_{SS}=–3.0V		10	15	µA	V_{DD}
		During sleep	OSC Off; PWR off No loading; V_{SS}=–3.0V		0.1	5	µA	V_{DD}
		During access	fcyc=200KHz V_{SS}=–3.0V		150	300	µA	V_{DD} *5
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		8.0	10.0	pF	*3

Frame frequency	f_{FR}	Ta = 25°C, V_{SS} = –3.0V	70	100	130	Hz	*8
External clock frequency	f_{CK}			33.8		kHz	*8, *9

Reset time	t_R		1.0			µs	*6
Reset pulse width	t_{RW}		10			µs	*6
Reset start time	t_{RES}		50			ns	*7

Dynamic system:

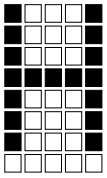
Built-in power supply	Amp output voltage	V_5	Ta = 25°C (during 1/4 bias)	4 × V_{REG2}			V	
	Reference voltage	V_{REG2}	Ta = 25°C (during 1/4 bias)	–1.55	–1.5	–1.45	V	

*1 Although the wide operating character range is guaranteed, a quick and excessive voltage variation may not be guaranteed during access by the MPU. The low-voltage data hold characteristics are valid during Sleep mode. No access by the MPU is allowed during this time.

*2 D0 to D5, D6 (SCL), D7 (SI), A0, $\overline{RES}$, $\overline{CS}$, $\overline{WR}$ (E), PS, IF, C86

*3 The resistance if a 0.1-volt voltage is supplied between the SEGn, SEGSn, COMn or COMSn output pin and each power pin (V_1, V_2, V_3 or V_4). It is defined within power voltage (2).
$R_{ON} = 0.1V/\Delta I$
where, ΔI is current that flows when the 0.1-volt voltage is supplied between the power supply and output.

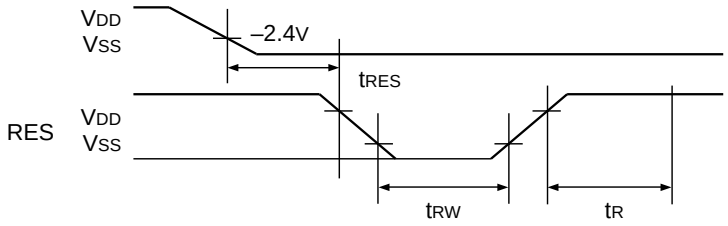
*4 Applied if not accessed by the MPU during character display and if the built-in power circuit and oscillator are operating.
Display character:



*5 Current consumption if always written in "fcyc". The current consumption during access is roughly proportional to the access frequency (fcyc).

*6 The "t_R" (reset time) indicates a time period from the rising edge of $\overline{RES}$ signal to the completion of internal circuit reset. Therefore, the S1D12205 Series enters the normal operation status after "t_R".

*7 Defines the minimum pulse width of $\overline{RES}$ signal. A pulse width greater than "t_{RW}" must be entered for reset.



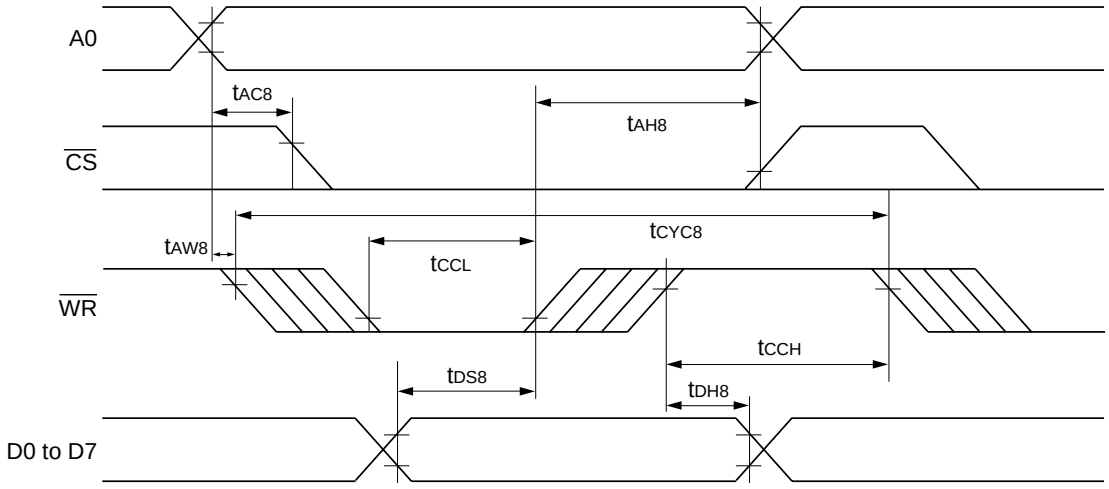
All signal timings are based on 20% and 80% of Vss.

*8 The following provides the relationship between the oscillator frequency (f_{OSC}) for built-in circuit driving and the frame frequency (f_{FR}).
$f_{OSC} = 13 \times 26 \times f_{FR}$ (3-line display)
$= 13 \times 18 \times f_{FR}$ (2-line display)
<Reference>
$f_{BLK} = (1/128) \times f_{FR}$

*9 Enter the waveforms in 40% to 60% duty to use an external clock instead of the built-in oscillator. If no external clock is entered, fix it to HIGH. (Normal HIGH)

11. TIMING CHARACTERISTICS

(1) MPU bus write timing (80 series)



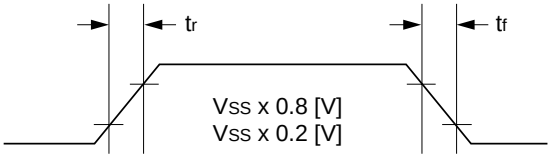
(Ta = –30 to +85°C, VSS = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time CS setup time	A0 CS	tAW8 tAH8 tAC8	All timing must be based on 20% and 80% of VSS.	60 30 0	— — —	ns
System cycle time	WR	tCYC8		1850	—	ns
Write LOW pulse width (Write)		tCCL		150	—	ns
Write HIGH pulse width (Write)		tCCH		1650	—	ns
Data setup time Data hold time	D0 to D7	tDS8 tDH8		50 50	— —	ns

(Ta = –30 to +85°C, VSS = –3.3V to –2.7V)

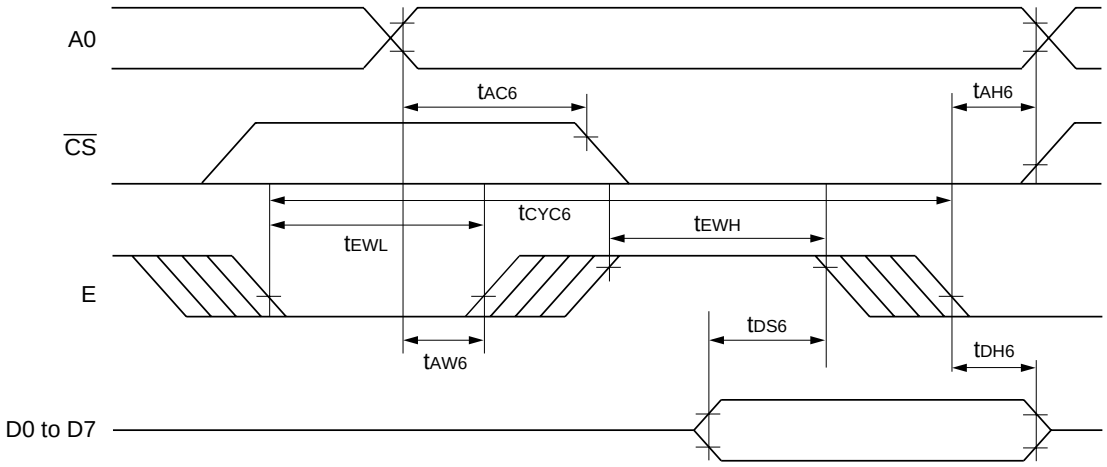
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time CS setup time	A0 CS	tAW8 tAH8 tAC8	All timing must be based on 20% and 80% of VSS.	60 30 0	— — —	ns
System cycle time	WR	tCYC8		1150	—	ns
Write LOW pulse width (Write)		tCCL		100	—	ns
Write HIGH pulse width (Write)		tCCH		1000	—	ns
Data setup time Data hold time	D0 to D7	tDS8 tDH8		20 20	— —	ns

*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for RES input).



*2 "tCCL" is defined by the overlap time of CS LOW level and WR LOW level.

(2) MPU bus write timing (68 series)



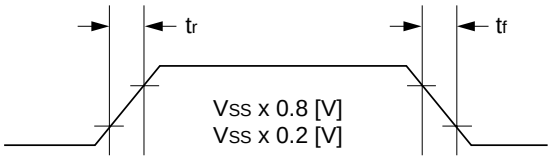
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time CS setup time	A0 CS	t_{AW6} t_{AH6} t_{AC6}	All timing must be based on 20% and 80% of V_{SS}.	60 50 0	– – –	ns
System cycle time	WR	t_{CYC6}		1850	–	ns
Enable LOW pulse width (Write)		t_{EWL}		1650	–	ns
Enable HIGH pulse width (Write)		t_{EWH}		150	–	ns
Data setup time Data hold time	D0 to D7	t_{DS6} t_{DH6}		20 80	– –	ns

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

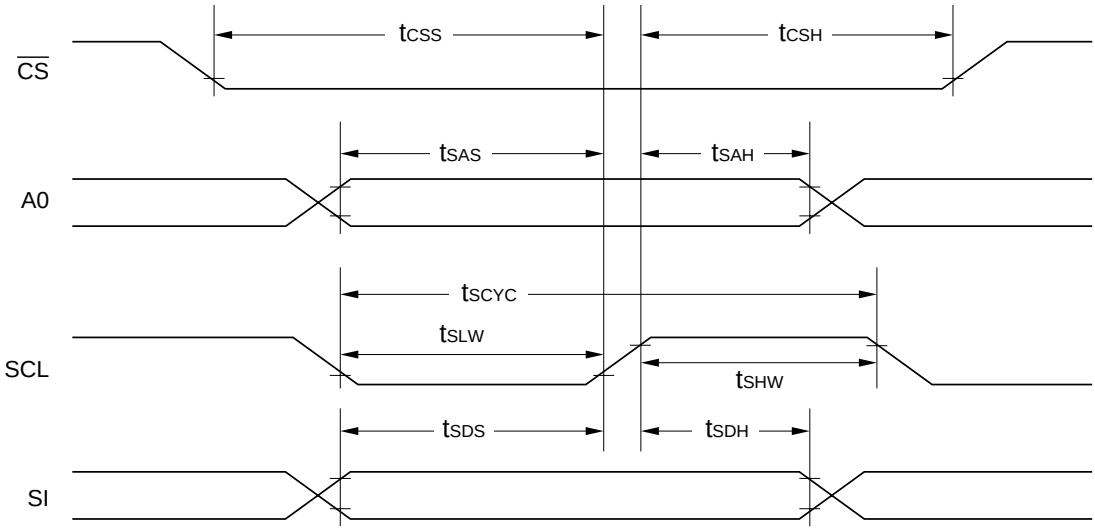
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time CS setup time	A0 CS	t_{AW6} t_{AH6} t_{AC6}	All timing must be based on 20% and 80% of V_{SS}.	60 30 0	– – –	ns
System cycle time	WR	t_{CYC6}		1150	–	ns
Enable LOW pulse width (Write)		t_{EWL}		1000	–	ns
Enable HIGH pulse width (Write)		t_{EWH}		100	–	ns
Data setup time Data hold time	D0 to D7	t_{DS6} t_{DH6}		20 50	– –	ns

*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for RES input).



*2 "t_{EWH}" is defined by the overlap time of CS LOW level and E HIGH level.

(3) Serial interface



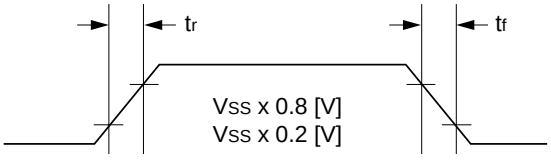
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL HIGH pulse width SCL LOW pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of V_{SS}.	3000 2850 150	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		50 800	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		50 50	— —	ns
CS-to-SCL time	$\overline{CS}$	t_{CSS} t_{CSH}		400 2500	— —	ns

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL HIGH pulse width SCL LOW pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of V_{SS}.	1400 1300 50	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SDH}		50 500	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		30 30	— —	ns
CS-to-SCL time	$\overline{CS}$	t_{CSS} t_{CSH}		200 1500	— —	ns

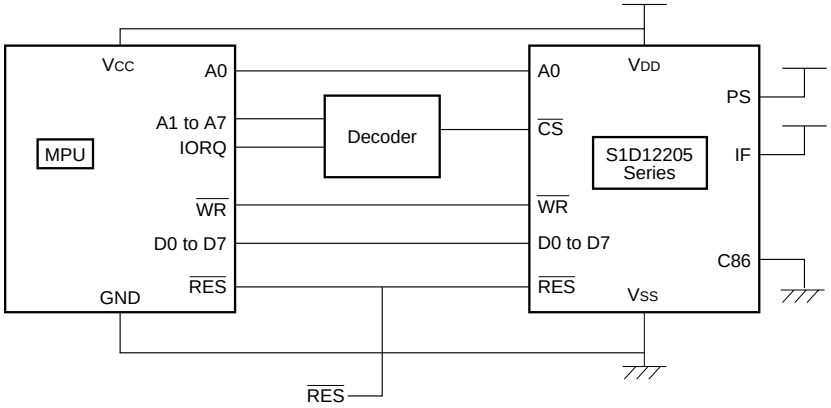
*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for $\overline{RES}$ input).



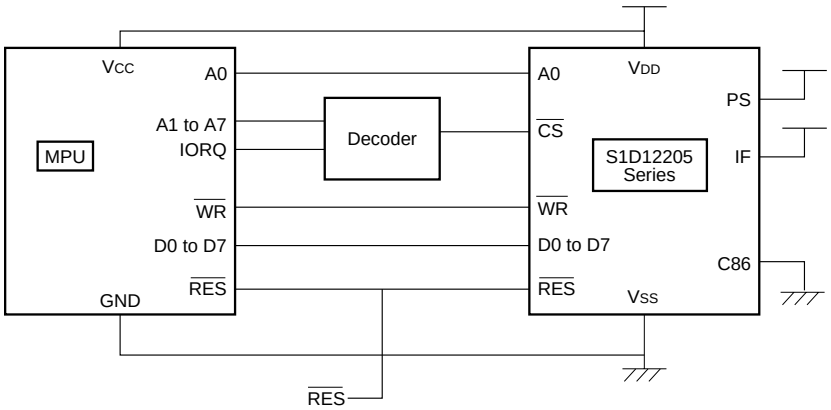
12. MPU INTERFACES (REFERENCE)

The S1D12205 Series can be connected to the 80-series or 68-series MPU. Also, it can operate with a less number of signal lines via the serial interface.
If the MPU buses and ports are set to HIGH impedance for a certain time due to RESET, the RESET signal must be entered in the S1D12205 Series after the S1D12205's inputs have been determined.

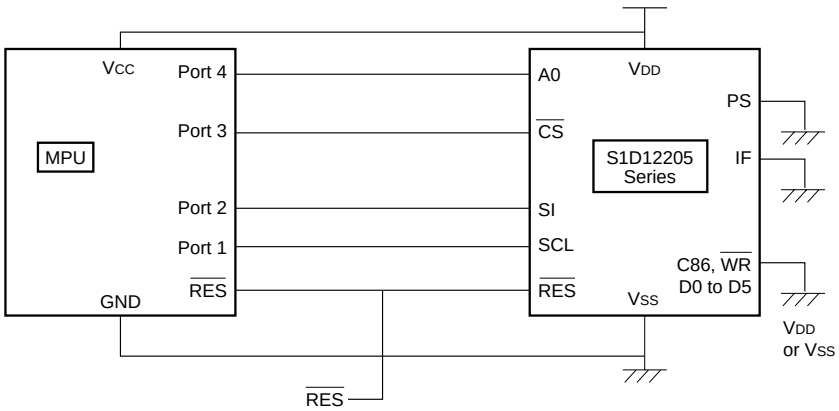
80-Series MPU



68-Series MPU

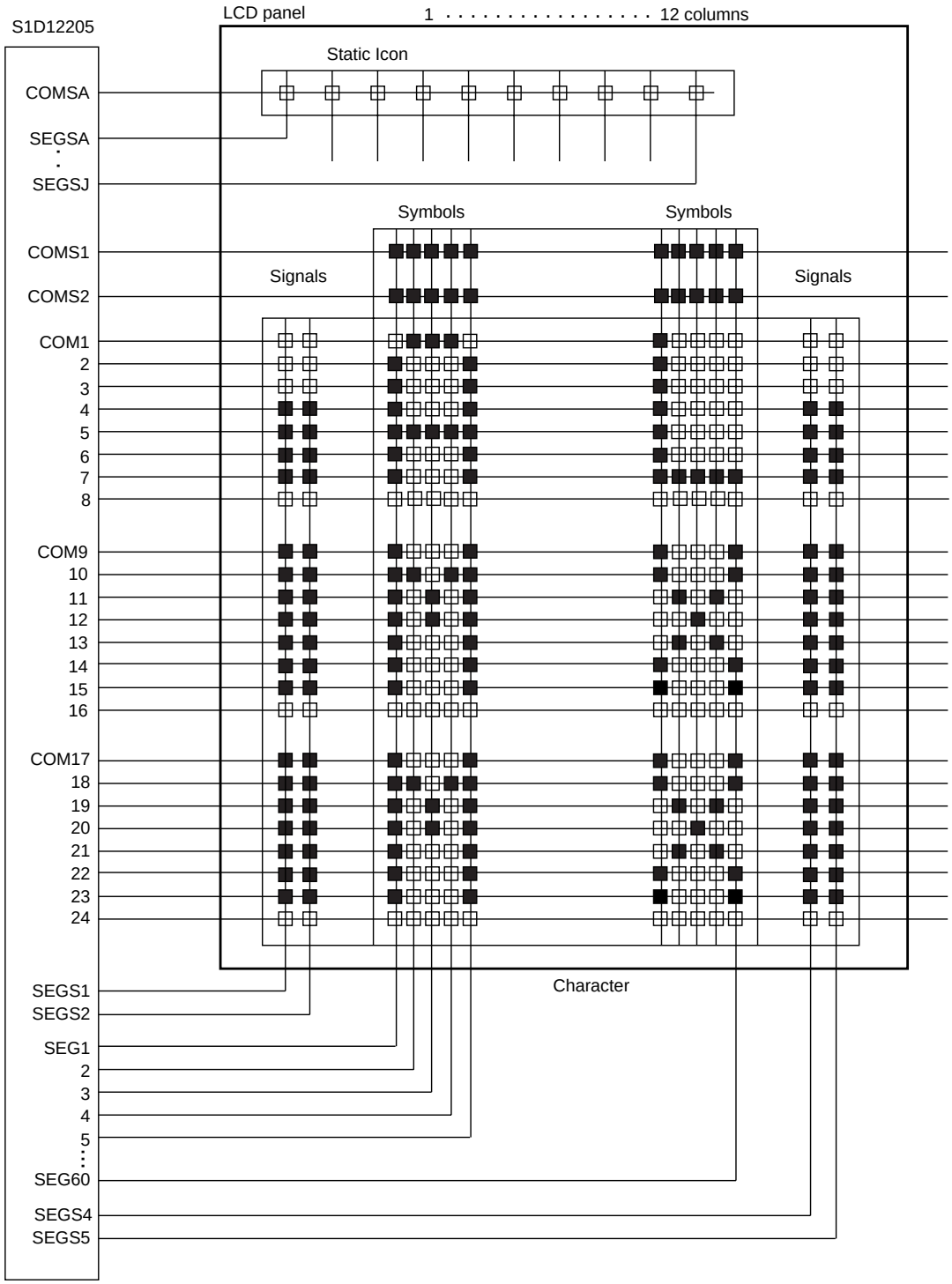


Serial Interface

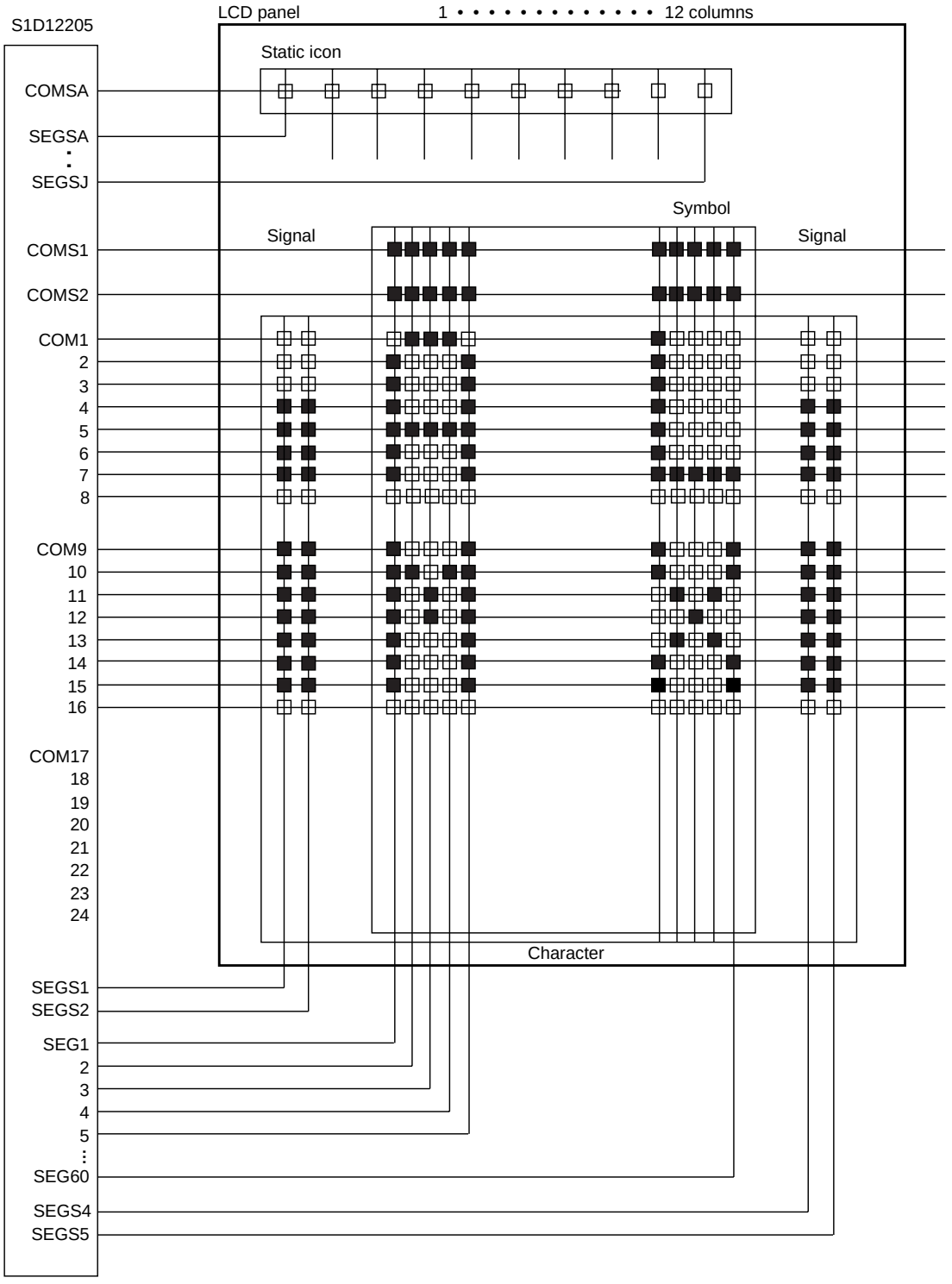


13. LCD CELL INTERFACE

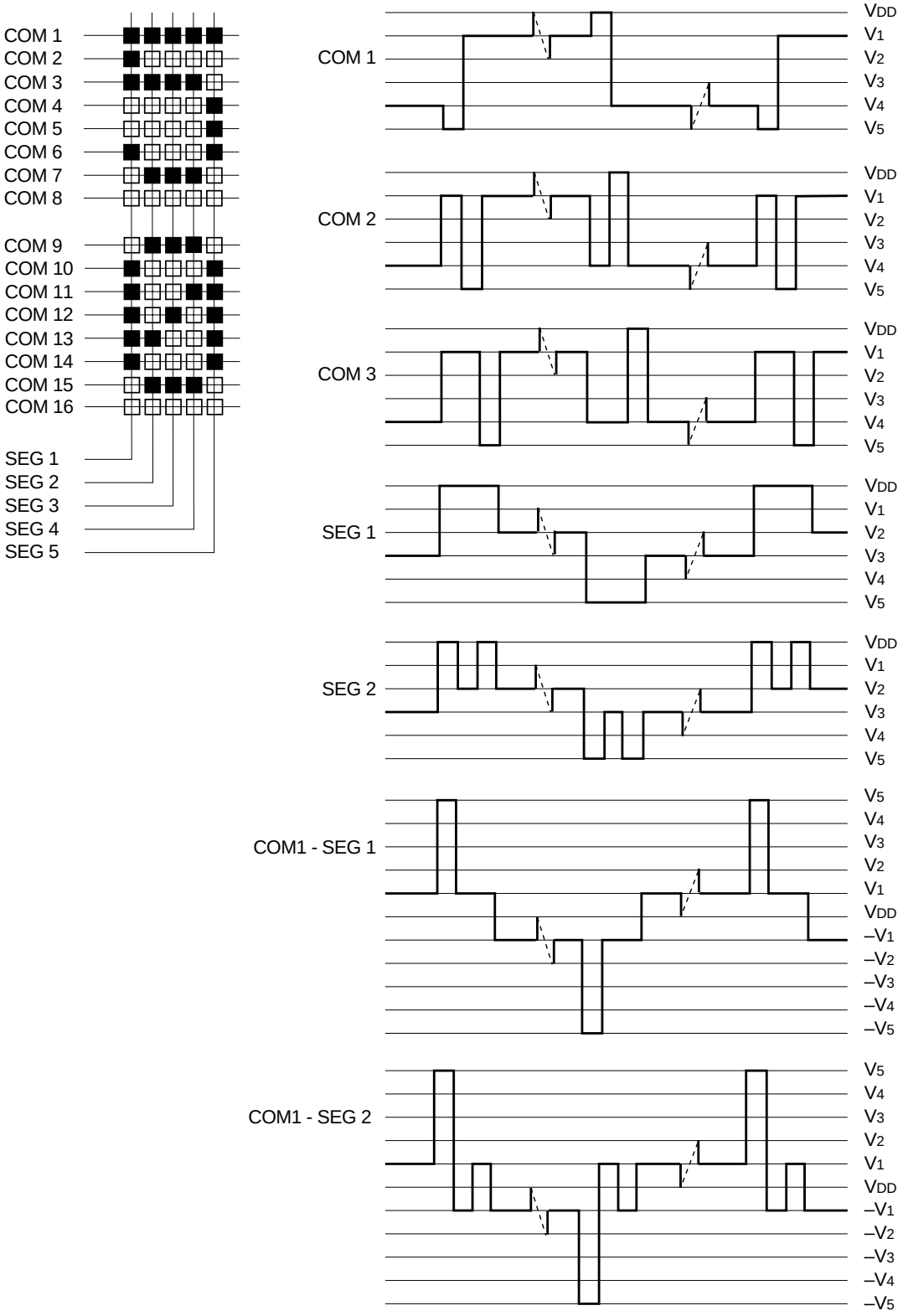
12 columns by 3 lines, 5×8 dots + Symbols



12 columns by 2 lines (N=1), 5×8 dots + Symbols

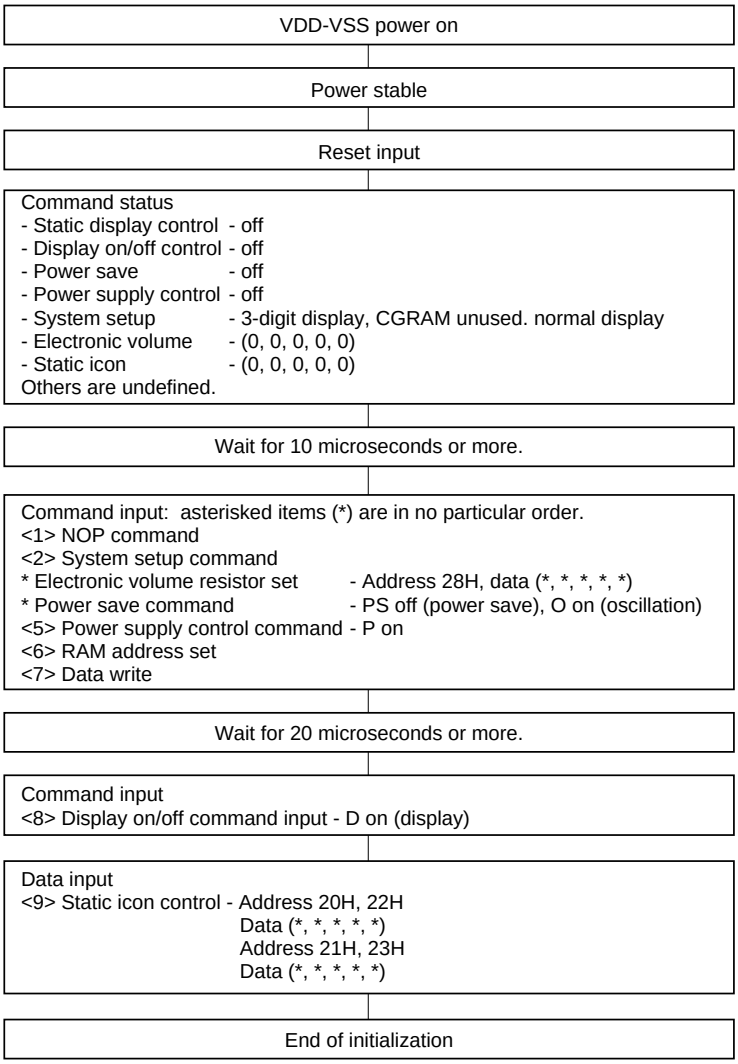


14. LCD DRIVE WAVEFORMS (B WAVEFORMS)

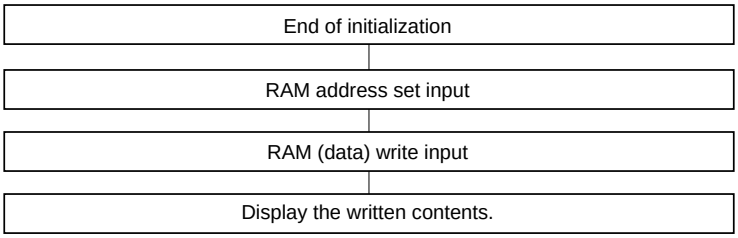


15. EXAMPLE OF INSTRUCTION SETUP (REFERENCE)

Initialization

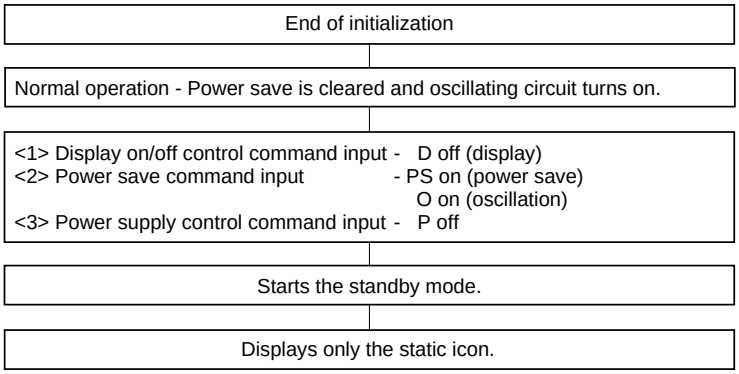


Display Mode

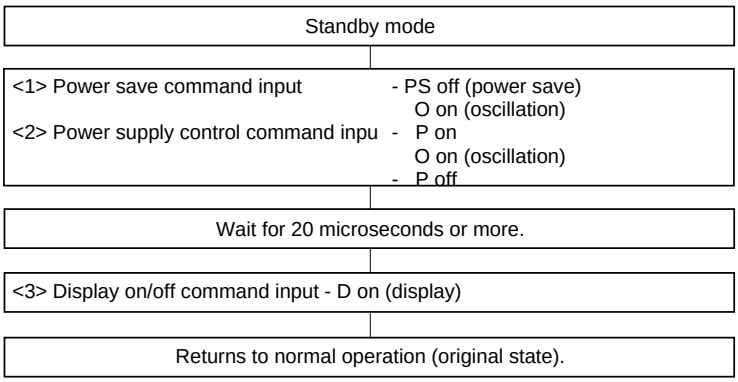


Standby Mode

(1) Setting the standby mode

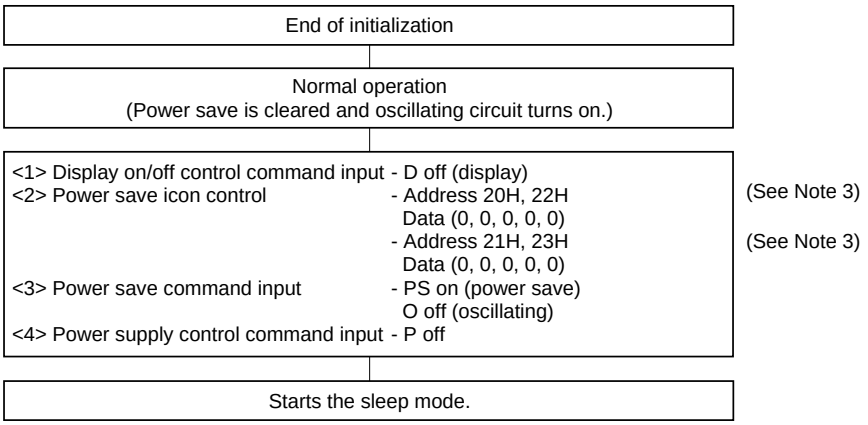


(2) Clearing the standby mode

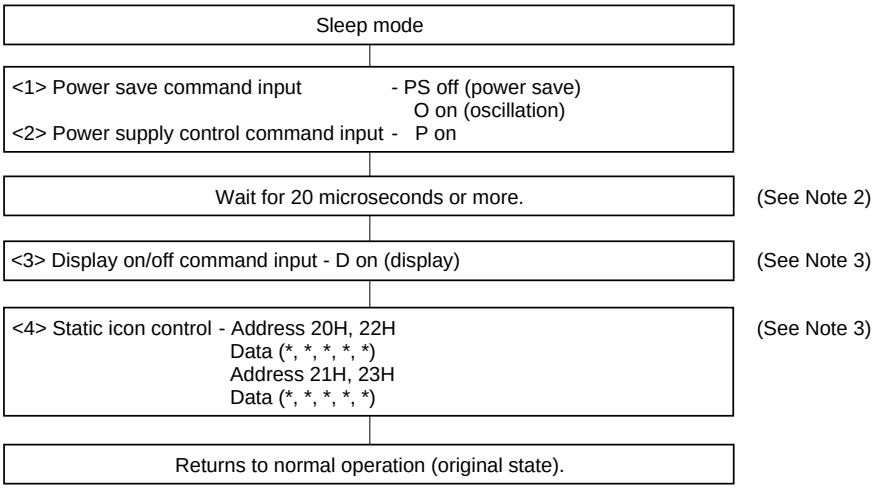


Sleep Mode

(1) Setting the Sleep mode.



(2) Clearing the sleep mode



Note 1. <6> and <7> of 15-1 indicate RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM Clear), use the following steps:
- DD RAM - write 20H (character code).
- CG RAM - write 00H (data '0').
- Symbol register - write 00H (data '0').

The RAM data is unspecified at the time of reset input (after power is turned on). If the data '0' is not written at this stage, unexpected display may occur to the unset position.

Note 2. Defined by the rising characteristics of the power circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3. The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

16. OPTION LIST

The S1D 12205 Series has the following options. Options are available exclusively for users. Please contact our Sales Department for information.

- The following shows how to define the name of the product compatible with options:

  Example: S1D12205D**B*
  ↑
  Option code

Specification of character generator ROM (CGROM)

The S1D12205 Series incorporates a characters generator ROM consisting of up to 256 types of characters, with each character size featuring 5×7 (8) dots. The S1D12205 Series CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

Specifications of external clock

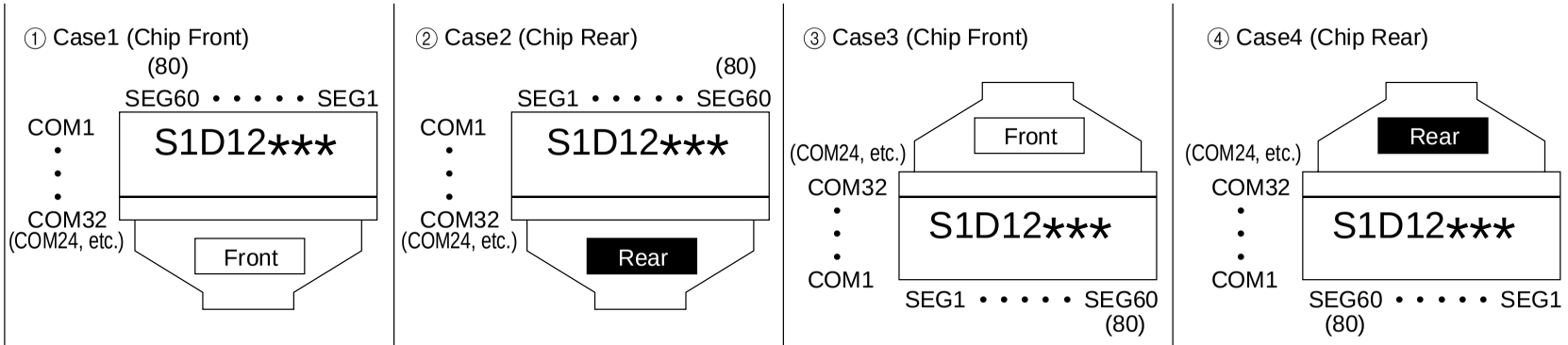
The S1D12205 Series has an external clock terminal which is provided with two types of functions; f_{OSC} and $4 \times f_{OSC}$. Either f_{OSC} or $4 \times f_{OSC}$ can be selected according to the user's requirements.

	Built-in oscillation f_{OSC}	External clock f_{OSC}	External clock $4 \times f_{OSC}$
Standard	○	○	×
Optional	○	×	○

The standard external clock specifications are set on the f_{OSC}.

S1D12200/12205/12400 Example of System Setup Depending on Mount Direction

Reference



S1D12200	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
S1D12205	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
S1D12400	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order.

17. CAUTIONS

The following points should be noted when this Development Specification is used:

1. This Development Specification is subject to modification for improvement without prior notice.
2. This Development Specification is not intended to guarantee enforcement of industrial property and other rights, or to grant license for the use of this product. Examples of applications mentioned in this Development Specification are given for effective understanding of the product. We are not responsible for any circuit problems which might occur due to use of these examples. The size of the values appearing in the characteristics table is represented by the size of the number line.
3. Part or whole of this Development Specification shall not be quoted, reproduced or used for other purposes without permission of our company.

For the use of the semi-conductor, take note of the following:

"Handling cautions for light"

According to the principle of the solar battery the semiconductor characteristics are changed when exposed to light. So misoperation may occur if this IC is exposed to light.

For the single IC unit, measures against light are not yet completely taken. The board and the product where this IC is mounted must be provided with the following measures:

(1) For designing and mounting, measures must be taken to provide the structure which ensures the light protecting properties of the IC during actual use.

(2) In the inspection process, environmental design must be made with consideration given to the light protecting properties of the IC.

(3) To ensure light protecting properties of the IC, consideration must be given to the surface, back and sides of the IC chip.

S1D12300 Series

Rev. 1.9

Contents

1. DESCRIPTION

The S1D12300 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 64 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.
A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5 × 7 dots. A user-defined character RAM for four characters of 5 × 7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and standby mode.
The S1D12300 Series are classified into S1D12300, S1D12301, S1D12302, and S1D12303 depending on the duty of use and the number of display columns.

2. FEATURES

- Built-in display RAM
  48 characters + 4 user-defined characters + 64 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (64 symbols)
- Number of display columns × number of lines
  (12 columns + 1 column for signal) × 4 lines + 52 symbols: S1D12300
  (12 columns + 1 column for signal) × 3 lines + 52 symbols: S1D12301
  (12 columns + 1 column for signal) × 2 lines + 52 symbols: S1D12302
  16 columns × 2 lines + 64 symbols: S1D12303
- CR oscillation circuit (on-chip C and R)
- HIGH-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5 × 7 dots
- Duty ratio 1/16 (S1D12302, S1D12303)
  1/23 (S1D12301)
  1/30 (S1D12300)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 µA Max. (In normal operation mode: Including the operating current of the built-in power supply)
  20 µA Max. (In standby display mode)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
  : –5.0 V to –11.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
- Shipping form: Chip S1D123∗∗D∗∗B∗,
  S1D123∗∗D∗∗E∗,
  S1D123∗∗D∗∗G∗
  (Au- bump chip)
  S1D123∗∗D∗∗A∗,
  S1D123∗∗D∗∗C∗,
  S1D123∗∗D∗∗F∗
  (Al-pad chip)
  TCP S1D123∗∗T∗∗∗∗
- This IC is not designed with a protection against radioactive rays.

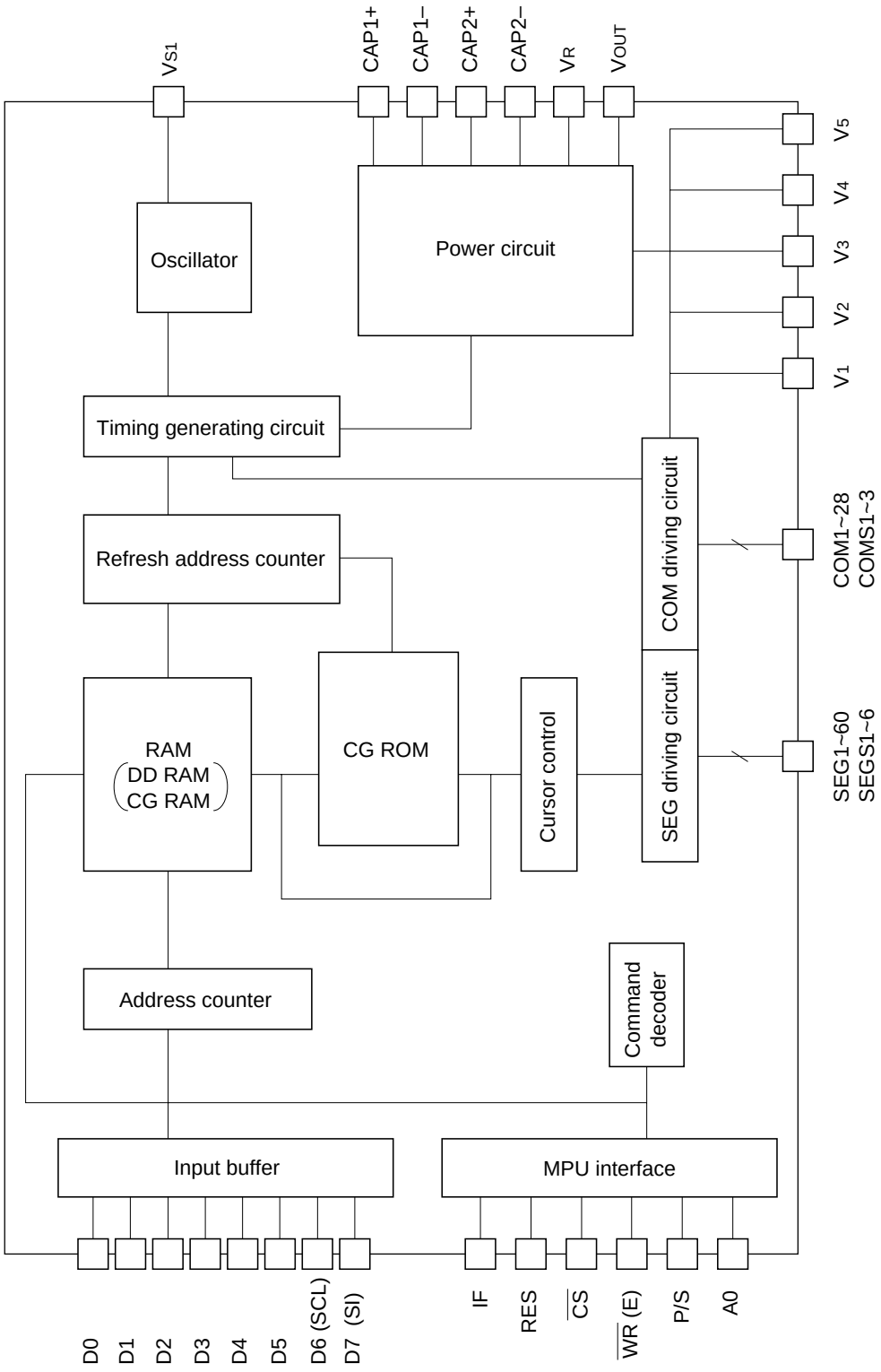
S1D12300 Series Chip Specifications

Product name	Duty	No. of digits indicated	No. of lines indicated	Font	VREG temperature slope	Chip thickness	Shipping form
S1D12300D11B*	1/30	12 columns + 1 column for signal	4 lines	Table 6 S1D123**D11**	–0.17%/°C	625µm	Gold Bump Chip
S1D12300D16B*	1/30	12 columns + 1 column for signal	4 lines	Table 7 S1D123**D16**	–0.17%/°C	625µm	Gold Bump Chip
S1D12300D16E*	1/30	12 columns + 1 column for signal	4 lines	Table 7 S1D123**D16**	–0.17%/°C	525µm	Gold Bump Chip
S1D12300D19B*	1/30	12 columns + 1 column for signal	4 lines	Table 5 S1D123**D10**	–0.04%/°C	625µm	Gold Bump Chip
S1D12300D27E*	1/30	12 columns + 1 column for signal	4 lines	Table 6 S1D123**D11**	External Input	525µm	Gold Bump Chip
S1D12301D10B*	1/23	12 columns + 1 column for signall	3 lines	Table 5 S1D123**D10**	–0.17%/°C	625µm	Gold Bump Chip
S1D12301D11E*	1/23	12 columns + 1 column for signal	3 lines	Table 6 S1D123**D11**	–0.17%/°C	525µm	Gold Bump Chip
S1D12301D19B*	1/23	12 columns + 1 column for signal	3 lines	Table 5 S1D123**D10**	–0.04%/°C	625µm	Gold Bump Chip
S1D12302D10B*	1/16	12 columns + 1 column for signal	2 lines	Table 5 S1D123**D10**	–0.17%/°C	625µm	Gold Bump Chip
S1D12302D11B*	1/16	12 columns + 1 column for signal	2 lines	Table 6 S1D123**D11**	–0.17%/°C	625µm	Gold Bump Chip
S1D12302D16B*	1/16	12 columns + 1 column for signal	2 lines	Table 7 S1D123**D16**	–0.17%/°C	625µm	Gold Bump Chip
S1D12302D22B*	1/16	12 columns + 1 column for signal	2 lines	Table 5 S1D123**D10**	External Input	625µm	Gold Bump Chip
S1D12303D10E*	1/16	16 columns	2 lines	Table 5 S1D123**D10**	–0.17%/°C	525µm	Gold Bump Chip
S1D12303D11B*	1/16	16 columns	2 lines	Table 6 S1D123**D11**	–0.17%/°C	625µm	Gold Bump Chip
S1D12303D16B*	1/16	16 columns	2 lines	Table 7 S1D123**D16**	–0.17%/°C	625µm	Gold Bump Chip
S1D12303D16E*	1/16	16 columns	2 lines	Table 7 S1D123**D16**	–0.17%/°C	525µm	Gold Bump Chip
S1D12303D22B*	1/16	16 columns	2 lines	Table 5 S1D123**D10**	External Input	625µm	Gold Bump Chip
S1D12303D27A*	1/16	16 columns	2 lines	Table 6 S1D123**D11**	External Input	625µm	AL-PAD chip
S1D12303D02E*	1/16	16 columns	2 lines	Table 7 S1D123**D16**	External Input	525µm	Gold Bump Chip
S1D12303D03E*	1/16	16 columns	2 lines	Table 7 S1D123**D16**	–0.04%/°C	525µm	Gold Bump Chip

S1D12300 Series TCP Specifications

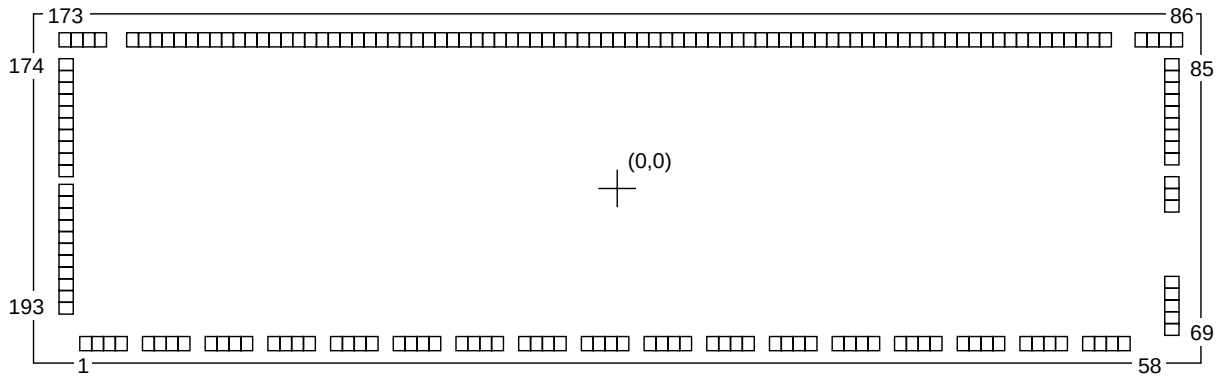
Product name	Duty	No. of digits indicated	No. of lines indicated	Font	VREG temperature slope	Shipping form
S1D12300T001*	1/30	12 columns + 1 columns for signal	4 lines	Table 6 S1D123**D11**	–0.17%/°C	TCP, 35mm 9IP
S1D12300T00A*	1/30	12 columns + 1 column for signal	4 lines	Table 6 S1D123**D11**	–0.17%/°C	TCP, 48mm 3IP
S1D12300T00B*	1/30	12 columns + 1 column for signal	4 lines	Table 5 S1D123**D10**	–0.04%/°C	TCP, 48mm 3IP
S1D12301T00B*	1/23	12 columns + 1 column for signal	3 lines	Table 5 S1D123**D10**	External Input	TCP, 48mm 3IP
S1D12303T00A*	1/16	16 columns	2 lines	Table 6 S1D123**D11**	–0.17%/°C	TCP, 48mm 3IP
S1D12303T00B*	1/16	16 columns	2 lines	Table 5 S1D123**D10**	–0.17%/°C	TCP, 48mm 3IP

3. BLOCK DIAGRAM



4. PAD

Pad layout



S1D12300D$\underline{****}$	1/30 duty	12 columns + 1 signal column
S1D12301D$\underline{****}$	1/23 duty	12 columns + 1 signal column
S1D12302D$\underline{****}$	1/16 duty	12 columns + 1 signal column
S1D12303D$\underline{****}$	1/16 duty	16 columns

↑
#1 Column for CG ROM pattern change

Chip size: 10.23 × 3.11 mm
Pad pitch: 110 µm (Min.)
Chip thickness: 625 (S1D123∗∗D∗∗A∗, S1D123∗∗D∗∗B∗)
525 (S1D123∗∗D∗∗C∗, S1D123∗∗D∗∗E∗)

1) A1 pad specification (S1D123∗∗D∗∗A∗)
Pad size: A 86 µm × 135 µm
B 135 µm × 86 µm
2) Au bump specification (S1D123∗∗D∗∗B∗)
For reference:
Bump size A 80 µm × 129 µm
B 129 µm × 80 µm
Bump height 22.5 µm

Pad center coordinate

<S1D12300D**>**

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2		–4683	
3		–4572	
4		–4462	
5	V_{DD}	–4242	
6		–4132	
7		–4021	
8		–3911	
9	V_{SSL}	–3691	
10		–3581	
11		–3470	
12		–3360	
13	V_5	–3140	
14		–3030	
15		–2919	
16		–2809	
17	V_4	–2589	
18		–2479	
19		–2368	
20		–2258	
21	V_3	–2021	
22		–1910	
23		–1800	
24		–1690	
25	V_2	–1453	
26		–1342	
27		–1232	
28		–1122	
29	V_1	–884	
30		–774	
31		–664	
32		–554	
33	V_0	–316	
34		–206	
35		–96	
36		14	
37	V_R	235	
38		345	
39		455	
40		565	
41	V_{OUT}	803	
42		913	
43		1023	
44		1133	
45	CAP2-	1354	
46		1464	
47		1574	
48		1684	
49	CAP2+	1905	
50		2015	
51		2125	
52		2235	
53	CAP1-	2473	
54		2583	

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56		2803	
57	CAP1+	3024	
58		3134	
59		3244	
60		3354	
61	V_{SSR}	3592	
62		3702	
63		3812	
64		3923	
65	V_{DD}	4143	
66		4253	
67		4363	
68		4474	
69	(NC)	4883	–1343
70	(NC)		–1233
71	(NC)		–1123
72	(NC)		–1013
73	V_{S1}	4929	–902
74	P/S		–186
75	IF		–76
76	RES		34
77	COMS1		255
78	COMS2		365
79	COM 1		475
80	COM 2		585
81	COM 3		696
82	COM 4		806
83	COM 5		916
84	COM 6		1026
85	COM 7		1136
86	(NC)	4947	1382
87		4836	
88		4726	
89		4616	
90	COM 8	4347	
91	COM 9	4237	
92	COM10	4127	
93	COM11	4017	
94	COM12	3906	
95	COM13	3796	
96	COM14	3686	
97	SEGS2	3576	
98	SEGS3	3466	
99	SEGS4	3355	
100	SEG 1	3245	
101	SEG 2	3135	
102	SEG 3	3025	
103	SEG 4	2915	
104	SEG 5	2804	
105	SEG 6	2694	
106	SEG 7	2584	
107	SEG 8	2474	
108	SEG 9	2364	

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	–1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	COM28	–3697	1382
164	COM27	–3808	
165	COM26	–3918	
166	COM25	–4028	
167	COM24	–4138	
168	COM23	–4248	
169	COM22	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 to the floating state.

<S1D12301D**>**

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2		–4683	
3		–4572	
4		–4462	
5	V_{DD}	–4242	
6		–4132	
7		–4021	
8		–3911	
9	V_{SSL}	–3691	
10		–3581	
11		–3470	
12		–3360	
13	V_5	–3140	
14		–3030	
15		–2919	
16		–2809	
17	V_4	–2589	
18		–2479	
19		–2368	
20		–2258	
21	V_3	–2021	
22		–1910	
23		–1800	
24		–1690	
25	V_2	–1453	
26		–1342	
27		–1232	
28		–1122	
29	V_1	–884	
30		–774	
31		–664	
32		–554	
33	V_0	–316	
34		–206	
35		–96	
36		14	
37	V_R	235	
38		345	
39		455	
40		565	
41	V_{OUT}	803	
42		913	
43		1023	
44		1133	
45	CAP2-	1354	
46		1464	
47		1574	
48		1684	
49	CAP2+	1905	
50		2015	
51		2125	
52		2235	
53	CAP1-	2473	
54		2583	

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56		2803	
57	CAP1+	3024	
58		3134	
59		3244	
60		3354	
61	V_{SSR}	3592	
62		3702	
63		3812	
64		3923	
65	V_{DD}	4143	
66		4253	
67		4363	
68		4474	
69	(NC)	4883	–1343
70	(NC)		–1233
71	(NC)		–1123
72	(NC)		–1013
73	V_{S1}	4929	–902
74	P/S		–186
75	IF		–76
76	RES		34
77	COMS1		255
78	COMS2		365
79	COM 1		475
80	COM 2		585
81	COM 3		696
82	COM 4		806
83	COM 5		916
84	COM 6		1026
85	COM 7		1136
86	(NC)	4947	1382
87		4836	
88		4726	
89		4616	
90	COM 8	4347	
91	COM 9	4237	
92	COM10	4127	
93	COM11	4017	
94	COM12	3906	
95	COM13	3796	
96	COM14	3686	
97	SEGS2	3576	
98	SEGS3	3466	
99	SEGS4	3355	
100	SEG 1	3245	
101	SEG 2	3135	
102	SEG 3	3025	
103	SEG 4	2915	
104	SEG 5	2804	
105	SEG 6	2694	
106	SEG 7	2584	
107	SEG 8	2474	
108	SEG 9	2364	

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164		–3808	
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 and 163 to 169 to the floating state.

<S1D12302D**>**

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2		–4683	
3		–4572	
4		–4462	
5	V_{DD}	–4242	
6		–4132	
7		–4021	
8		–3911	
9	V_{SSL}	–3691	
10		–3581	
11		–3470	
12		–3360	
13	V_5	–3140	
14		–3030	
15		–2919	
16		–2809	
17	V_4	–2589	
18		–2479	
19		–2368	
20		–2258	
21	V_3	–2021	
22		–1910	
23		–1800	
24		–1690	
25	V_2	–1453	
26		–1342	
27		–1232	
28		–1122	
29	V_1	–884	
30		–774	
31		–664	
32		–554	
33	V_0	–316	
34		–206	
35		–96	
36		14	
37	V_R	235	
38		345	
39		455	
40		565	
41	V_{OUT}	803	
42		913	
43		1023	
44		1133	
45	CAP2-	1354	
46		1464	
47		1574	
48		1684	
49	CAP2+	1905	
50		2015	
51		2125	
52		2235	
53	CAP1-	2473	
54		2583	

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56		2803	
57	CAP1+	3024	
58		3134	
59		3244	
60		3354	
61	V_{SSR}	3592	
62		3702	
63		3812	
64		3923	
65	V_{DD}	4143	
66		4253	
67		4363	
68		4474	
69	(NC)	4883	–1343
70	(NC)		–1233
71	(NC)		–1123
72	(NC)		–1013
73	V_{S1}	4929	–902
74	P/S		–186
75	IF		–76
76	RES		34
77	COMS1		255
78	COMS2		365
79	COM 1		475
80	COM 2		585
81	COM 3		696
82	COM 4		806
83	COM 5		916
84	COM 6		1026
85	COM 7		1136
86	(NC)	4947	1382
87		4836	
88		4726	
89		4616	
90	COM 8	4347	
91	COM 9	4237	
92	COM10	4127	
93	COM11	4017	
94	COM12	3906	
95	COM13	3796	
96	COM14	3686	
97	SEGS2	3576	
98	SEGS3	3466	
99	SEGS4	3355	
100	SEG 1	3245	
101	SEG 2	3135	
102	SEG 3	3025	
103	SEG 4	2915	
104	SEG 5	2804	
105	SEG 6	2694	
106	SEG 7	2584	
107	SEG 8	2474	
108	SEG 9	2364	

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164		–3808	
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM14	–4940	1136
175	COM13		1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 and 163 to 169 to the floating state.

<S1D12303D**>**

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2		–4683	
3		–4572	
4		–4462	
5	V_{DD}	–4242	
6		–4132	
7		–4021	
8		–3911	
9	V_{SSL}	–3691	
10		–3581	
11		–3470	
12		–3360	
13	V_5	–3140	
14		–3030	
15		–2919	
16		–2809	
17	V_4	–2589	
18		–2479	
19		–2368	
20		–2258	
21	V_3	–2021	
22		–1910	
23		–1800	
24		–1690	
25	V_2	–1453	
26		–1342	
27		–1232	
28		–1122	
29	V_1	–884	
30		–774	
31		–664	
32		–554	
33	V_0	–316	
34		–206	
35		–96	
36		14	
37	V_R	235	
38		345	
39		455	
40		565	
41	V_{OUT}	803	
42		913	
43		1023	
44		1133	
45	CAP2-	1354	
46		1464	
47		1574	
48		1684	
49	CAP2+	1905	
50		2015	
51		2125	
52		2235	
53	CAP1-	2473	
54		2583	

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56		2803	
57	CAP1+	3024	
58		3134	
59		3244	
60		3354	
61	V_{SSR}	3592	
62		3702	
63		3812	
64		3923	
65	V_{DD}	4143	
66		4253	
67		4363	
68		4474	
69	(NC)	4883	–1343
70	(NC)		–1233
71	(NC)		–1123
72	(NC)		–1013
73	V_{S1}	4929	–902
74	P/S		–186
75	IF		–76
76	RES		34
77	COMS1		255
78	COMS2		365
79	COM 1		475
80	COM 2		585
81	COM 3		696
82	COM 4		806
83	COM 5		916
84	COM 6		1026
85	COM 7		1136
86	(NC)	4947	1382
87		4836	
88		4726	
89		4616	
90	SEG 1	4347	
91	SEG 2	4237	
92	SEG 3	4127	
93	SEG 4	4017	
94	SEG 5	3906	
95	SEG 6	3796	
96	SEG 7	3686	
97	SEG 8	3576	
98	SEG 9	3466	
99	SEG10	3355	
100	SEG11	3245	
101	SEG12	3135	
102	SEG13	3025	
103	SEG14	2915	
104	SEG15	2804	
105	SEG16	2694	
106	SEG17	2584	
107	SEG18	2474	
108	SEG19	2364	

PAD		COORDINATES	
No.	Name	X	Y
109	SEG20	2253	1382
110	SEG21	2143	
111	SEG22	2033	
112	SEG23	1923	
113	SEG24	1813	
114	SEG25	1702	
115	SEG26	1592	
116	SEG27	1482	
117	SEG28	1372	
118	SEG29	1262	
119	SEG30	1151	
120	SEG31	1041	
121	SEG32	931	
122	SEG33	821	
123	SEG34	711	
124	SEG35	600	
125	SEG36	490	
126	SEG37	380	
127	SEG38	270	
128	SEG39	160	
129	SEG40	49	
130	SEG41	–61	
131	SEG42	–171	
132	SEG43	–281	
133	SEG44	–391	
134	SEG45	–502	
135	SEG46	–612	
136	SEG47	–722	
137	SEG48	–832	
138	SEG49	–942	
139	SEG50	–1053	
140	SEG51	–1163	
141	SEG52	–1273	
142	SEG53	–1383	
143	SEG54	–1493	
144	SEG55	–1604	
145	SEG56	–1714	
146	SEG57	–1824	
147	SEG58	–1934	
148	SEG59	–2044	
149	SEG60	–2155	
150	SEG61	–2265	
151	SEG62	–2375	
152	SEG63	–2485	
153	SEG64	–2595	
154	SEG65	–2706	
155	SEG66	–2816	
156	SEG67	–2926	
157	SEG68	–3036	
158	SEG69	–3146	
159	SEG70	–3257	
160	SEG71	–3367	
161	SEG72	–3477	
162	SEG73	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	SEG74	–3697	1382
164	SEG75	–3808	
165	SEG76	–3918	
166	SEG77	–4028	
167	SEG78	–4138	
168	SEG79	–4248	
169	SEG80	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM14	–4940	1136
175	COM13		1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 to the floating state.

5. PIN DESCRIPTION

Power Supply Pins

Pin name	I/O	Description	No. of Pins
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	No. of Pins
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{SS} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 to D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = LOW, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>D7</td><td>D6</td><td>D5 to D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>LOW</td><td>SI</td><td>SCL</td><td>—</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>HIGH</td><td>D7</td><td>D6</td><td>D5 to D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
</table>
When P/S = LOW, be sure to fix D5 to D0 to HIGH or LOW.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ⌐↓. In case of an 80 series MPU, initialization can be performed by changing ⌊↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
LOW : 68 series MPU interface
HIGH : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the LOW level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active LOW. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
When P/S = LOW, be sure to fix the $\overline{WR}$ signal to HIGH or LOW.
<When connecting a 68 series MPU>
Active HIGH. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>HIGH</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>–</td></tr>
<tr><td>LOW</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
HIGH: 8-bit parallel input
LOW: 4-bit parallel input
When P/S = LOW, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

S1D12300, S1D12301, S1D12302

Pin name	I/O	Description	No. of Pins
COM1 to COM28	O	Common signal output pin (for characters)	28
COMS1 to CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a Vss amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1 to SEG60	O	Segment signal output pin (for characters)	60
SEGS1 to SEGS6	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a Vss amplitude is output. SEGS2, SEGS6: Segment output for signal output	7

S1D12303

Pin name	I/O	Description	No. of Pins
COM1 to COM14	O	Common signal output pin (for characters)	14
COMS1 to CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a Vss amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1 to SEG80	O	Segment signal output pin (for characters)	80
SEGS1	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a Vss amplitude is output.	1

6. FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the S1D12300 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting HIGH or LOW as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0 to D7
HIGH	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0 to D7
LOW	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

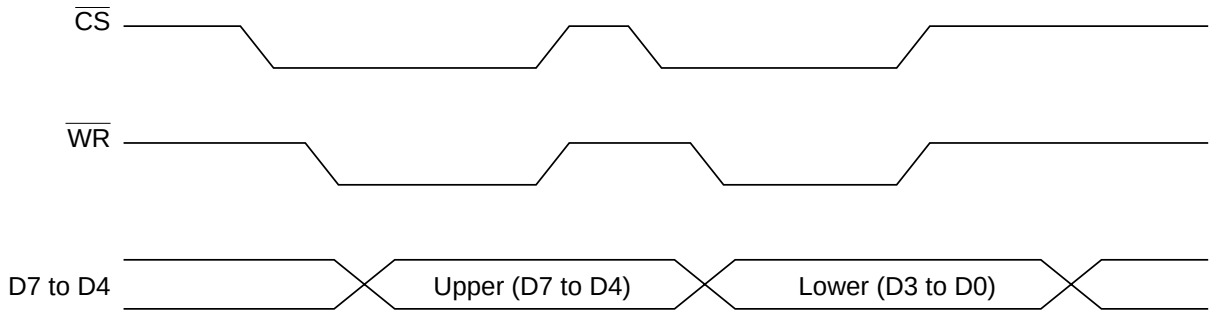
Parallel Input
In the S1D12300 Series, when parallel input is selected (P/S = HIGH), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either HIGH or LOW is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

$\overline{RES}$ input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
↓ active	68 series	A0	E	$\overline{CS}$	D0 to D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = LOW)

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = LOW).
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = HIGH, it is regarded as display data. When A0 = LOW, it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

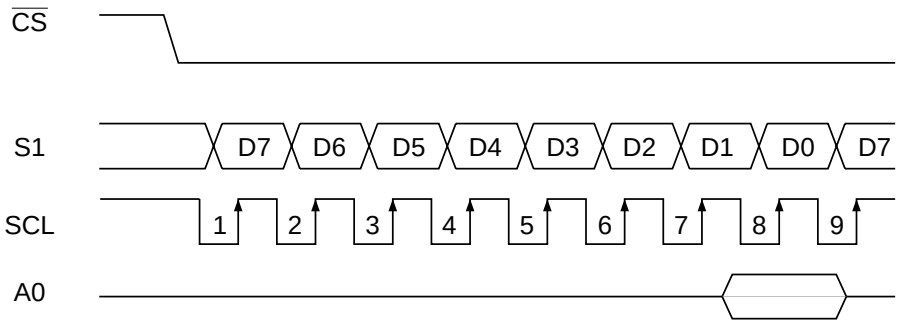


Fig. 1

Identification of data bus signals

The S1D12300 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The S1D12300 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = LOW, MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the S1D12300 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

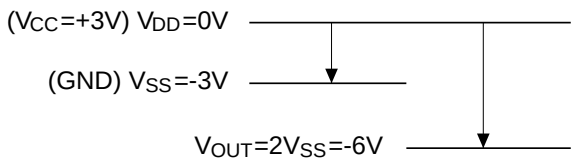
Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Triple boosting circuit

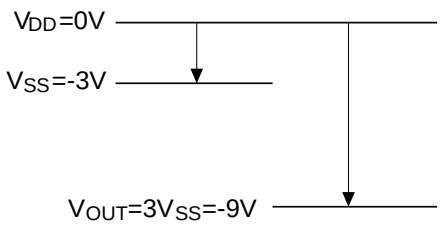
When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between VSS pin and VOUT pin respectively, the potential between the VDD pin and VSS pin is boosted triple and output to the VOUT pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and VOUT pin. Then, a double boosted output can be obtained from the VOUT pin (CAP2-).

The boosting circuit uses a signal from the oscillator output.

Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.



Potential during double boosting



Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V5 terminal.

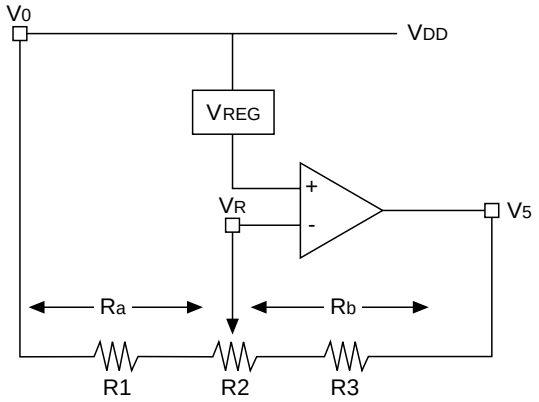
When V5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V5 can be regulated within a range of |V5|<|VOUT|. It may be calculated by the following formula:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \textcircled{1}$$

Wherein, VREG is the constant voltage source inside the S1D12300 Series and the voltage is constant at VREG ≒ 3.1V. The voltage regulation VREG ≒ 2.1V (TYP.) in option 1, and VREG = VSS in option 2. Voltage regulation of the V5 output is accomplished by connecting a variable resistor between VR, VDD and V5. For fine adjustment of the V5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/ °C under VREG outputs (standard specification), about -0.04%/°C (option). When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the VR terminal has a high input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.



Example 1:

Condition: I(R1, R2, R3) ≤ 5µA V5 = –6 to –8V

Setting:
R1+R2+R3 = 8V/5µA = 1.6MΩ
8V = (1+Rb/Ra) 3.0V Rb/Ra = 1.67
6V = (1+Rb/Ra) 3.0V Rb/Ra = 1

···· R1 = 600KΩ, R2 = 200KΩ, R3 = 800KΩ

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V_5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at (1, 1, 1, 1), the constant current value becomes: $I_{REF} \fallingdotseq 3.65uA$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = (1 + \frac{R_b}{R_c}) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots \textcircled{2}$$

$$\therefore R_c = \frac{R_a \times R_I}{R_a + R_I}$$

$$R_I = \frac{V_R}{I_{REF}}$$

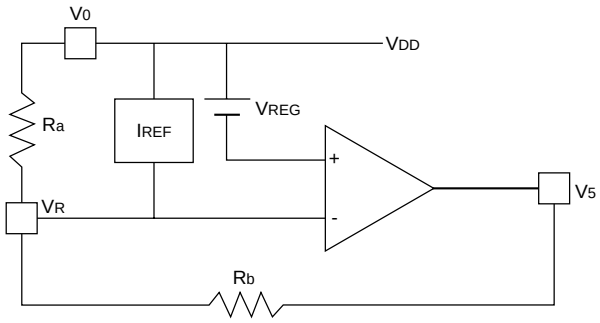


Fig. 9

(1) Determining the V_5 voltage setting range by the electronic volume control
Liquid crystal driving voltage V_5: max. -6V ~ min. -8V
V_5 variable voltage range: 2V

(2) Determining the R_b
R_b = V_5 variable voltage range/ I_{REF} ($I_{REF} \fallingdotseq 3.65\mu A$ Constant current)
= 2V/3.65μA
= 548KΩ

(3) Determining the R_a

$$R_a = \frac{V_{REG}}{(V_5 \text{ voltage setting max} - V_{REG}) / R_b}$$ (Use absolute values for V_{REG} and V_5 voltage settings.)

$$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

= 585KΩ

(4) Regulating the R_a
Set the electronic volume control register to (D3, D2, D1, D0) = (1, 0, 0, 0) or (0, 1, 1, 1) before matching the R_a value to the optimum contrast.

Since I_{REF} is a simplified constant voltage source, fluctuations upto ± 40% must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is: $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the R_a and R_b for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

When using the electronic volume control function, in order to compensate the V_5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as R_a and perform optimum contrast adjustment according to the above item (4) with each IC chip.

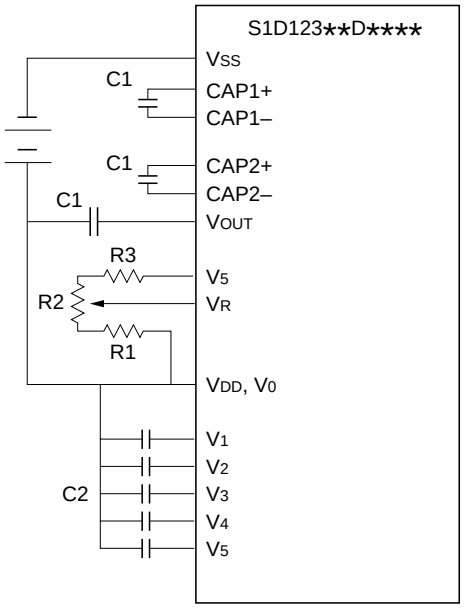
When the electronic volume control function is not being used, set the electronic volume control register to (0, 0, 0, 0) using the RES signal or the electronic volume control register setting command.

Liquid crystal voltage generating circuit

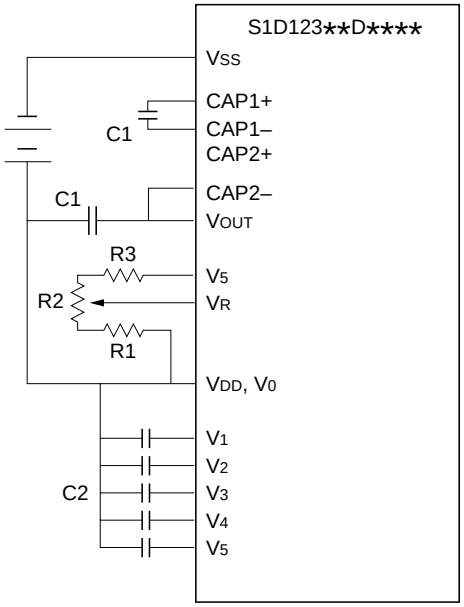
The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.
Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
The liquid crystal drive voltage is fixed to 1/5 bias.

As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V_1 to V_5 pins of liquid crystal power pins.

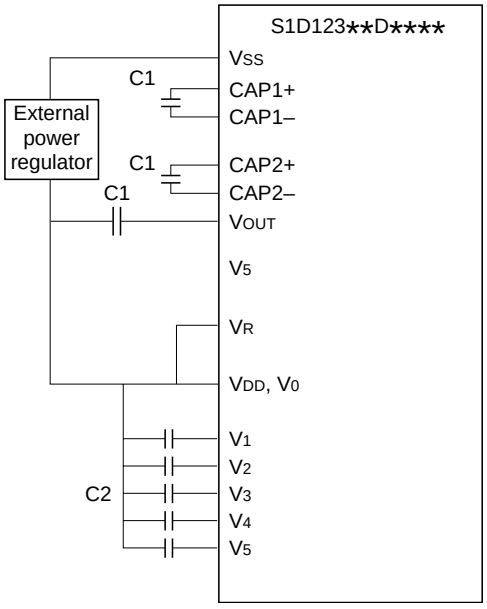
When a built-in power supply is used
Under a triple boosting

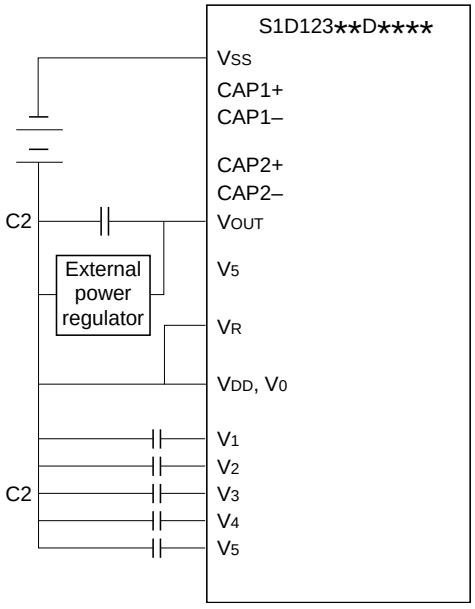


The diagram under a double boosting



When an external power regulator is used
(The built-in power regulator is not used)

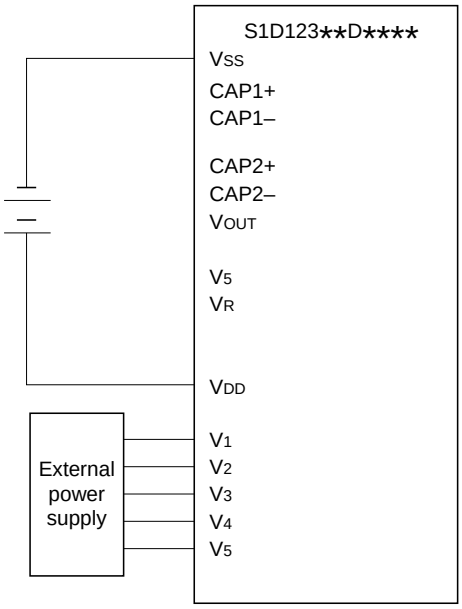




Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

When a built-in power supply is not used



Low Power Consumption Mode

The S1D12300 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

◎ Standby Mode

The standby mode is turned on and off by power save command.

In the standby mode only, static display is enabled by CMOS1 and SEGS1.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : VDD level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : VDD level
   COMS1, SEGS1 : Lighting is enabled by static drive.
   Perform display control using CMOS1 and SEGS1 by static display control command.
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the standby mode is turned on or off.
3. In the operation mode, the status precedent to execution of the standby mode is held.
   The internal circuit for dynamic display output stops.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

◎ Sleep Mode

After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : VDD level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : VDD level
   COMS1 ~ SEGS1 : VDD level
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

◎ Initialization status

1. Static display control
   SD0, SD1 = 0 : Display OFF
2. Display ON/OFF control
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   DC = 0 : Double cursor OFF
   D = 0 : Display OFF
3. Power save
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
4. Power control
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
5. System set
   CG = 0 : Not use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.

Regarding the reset signal, a pulse of at least 10 µs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 µs from the edge of the RES signal.

In the S1D12300 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.

After the RES pin goes active, each register is cleared and set to the above set status.

Unless initialization is performed by the RES pin when a power supply voltage is applied, the clear disable status may be provided.

7. COMMANDS

Table 4 shows a command list. In the S1D12300 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).
Command interpretation and execution are performed by only internal timing. This permits high-speed processing.

- **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Static Display Control	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the S1D12300 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (t_{cyc}) and execute the next instruction.

- **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Static Display Control
This command selects display or non-display of static display symbol, and blink ON or OFF. This command is effective in the standby mode only.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	*	*	SD1	SD0

* : Don't Care

SD1, SD2 = 0, 0 : Display OFF
0, 1 : Blink (1 to 2 Hz)
SD1, SD2 = 1, 0 : Blink (3 to 4 Hz)
1, 1 : All Display ON

(3) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
1 : Display ON

DC = 0 : Double cursor OFF
1 : Double cursor ON

B = 0 : Cursor blink OFF
1 : Cursor blink ON

In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display characters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

(4) Power Save

This command is used to control the oscillating circuit and set and reset the standby mode or sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save OFF (reset)
1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
1 : Oscillating circuit ON (oscillation)

(5) Power Control

This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Boosting circuit OFF
1 : Boosting circuit ON

Note: To operate the boosting circuit of the S1D12300 Series, the oscillating circuit must be in operation.

VF = 0 : Voltage follower OFF
1 : Voltage follower ON

VC = 0 : Voltage regulating circuit OFF
1 : Voltage regulating circuit ON

(6) System Set

This command set the use or non-use of display lines and CG RAM.

Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

* : Don't Care

CG = 0 : Non-use of CG RAM
1 : Use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(7) Electronic Volume Register Set

This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply, thereby adjusting the gradation of liquid crystal display.

When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code

70H ~7FH

MSB	.	.	LSB	| V_5 |	| I_{REF} |
0	0	0	0	Small	0.0 µA
		:		:	:
		. :		:	:
1	1	1	1	Large	About 3.65 µA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(8) RAM Address Set

This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.

② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map (S1D12300, S1D12301, S1D12302)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	CGRAM(00H)							–	CGRAM(01H)							–
1 0 H	CGRAM(02H)							–	CGRAM(03H)							–
2 0 H	Unused															
3 0 H	DDRAM line 1														Unused	
4 0 H	DDRAM line 2								For signals						"	
5 0 H	DDRAM line 3														"	
6 0 H	DDRAM line 4														"	
7 0 H	Symbol register														"	

– : Unused
For signals : Output from SEGS2 to SEGS6.

RAM Map (S1D12303)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	CGRAM(00H)							–	CGRAM(01H)							–
1 0 H	CGRAM(02H)							–	CGRAM(03H)							–
2 0 H	Unused															
3 0 H	DDRAM line 1															
4 0 H	DDRAM line 2															
5 0 H	DDRAM line 3															
6 0 H	DDRAM line 4															
7 0 H	Symbol register															

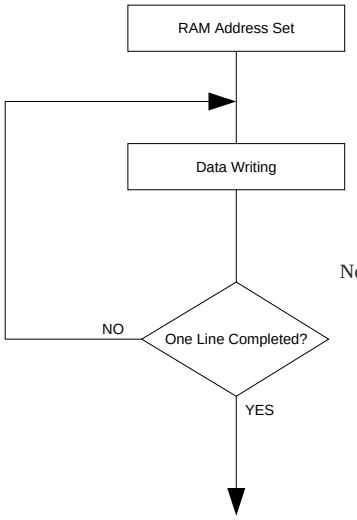
–: Unused

(9) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data into the DD RAM, CG RAM or symbol register.
② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>
The following is an example of writing one-line data into the DD RAM in succession.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 S1D12300 Series Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Static Display Control	0	0	0	0	1	0	*	*	SD1	SD0	Sets the display mode of static display symbol SD1, SD0 = 0, 0 (display OFF), 0, 1 (1 - 2 Hz blink), 1, 0 (3 4 Hz blink), 1, 1 (all display ON)
(3) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B =1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(4) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(5) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(6) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(7) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(8) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(9) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(10) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(11) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don't use this command.

8. CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The S1D12300 Series is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5 × 7 dots.

Table 5 shows a character code table of the S1D12300 Series.
The 4 characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

The CG ROM of the S1D12300 Series is a mask ROM and compatible with the user-dedicated CG ROM. Please ask us for further information of it.

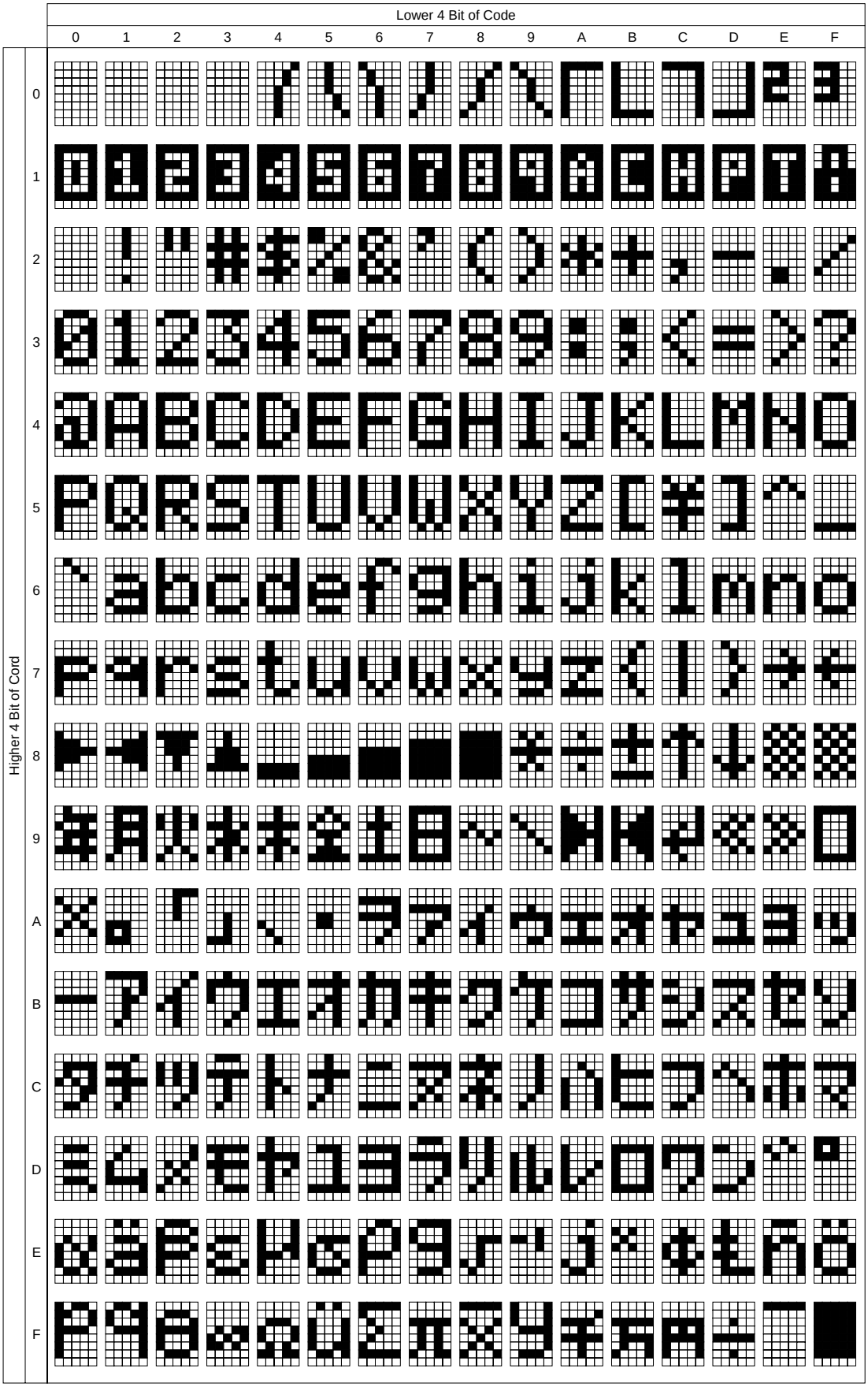
Regarding changed CG ROM, it is defined in product name as follows:

(Example) S1D12300D00B∗

Digit for CG ROM pattern change

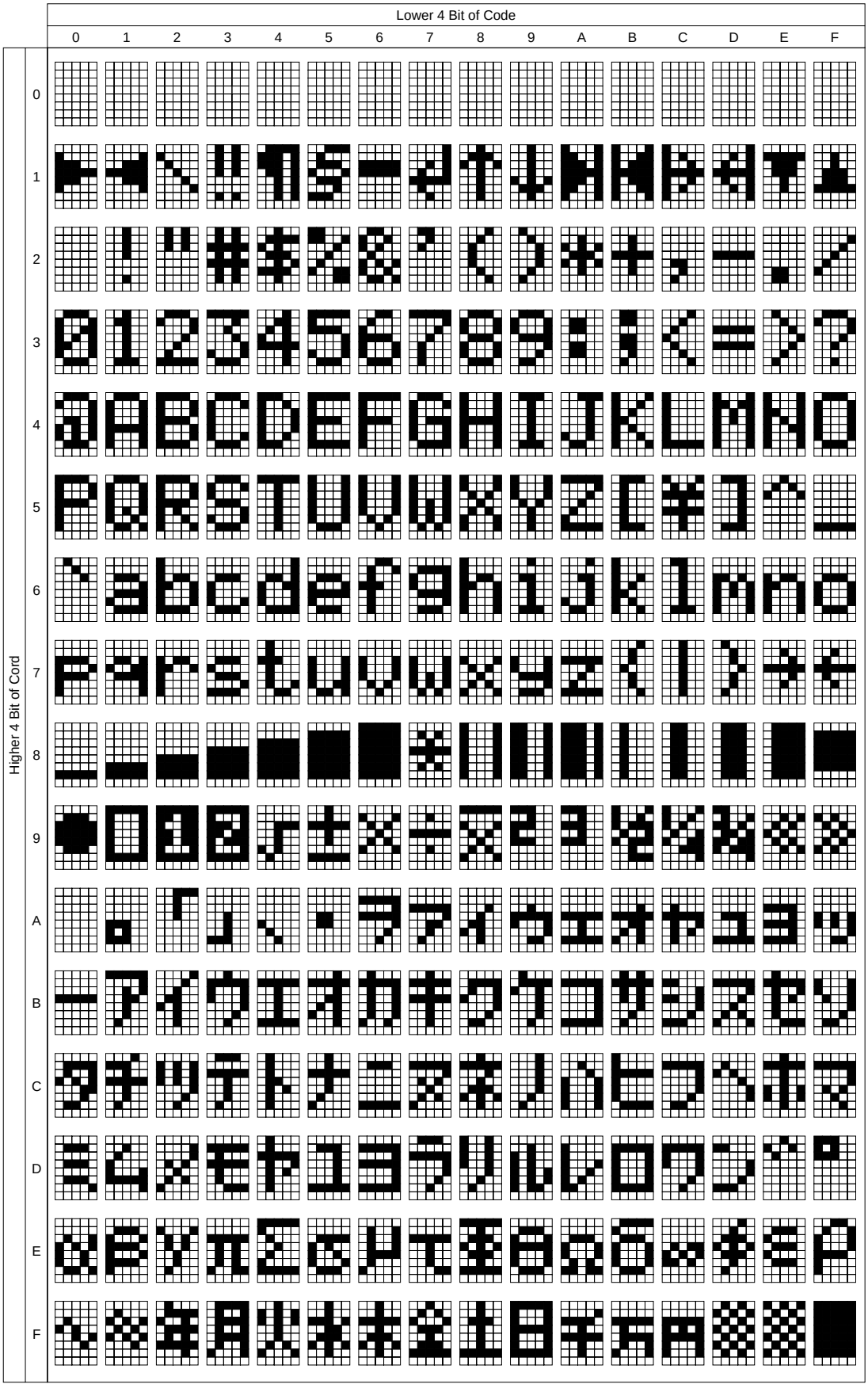
S1D123D10****

Table 5



S1D123**D11**

S1D123**D16**



Character Generator RAM (CG RAM)

The S1D12300 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5 × 7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

Character code	RAM address		CGRAM data (character pattern) D7 D6 D5 D4 D3 D2 D1 D0								Display
00H	00H to 06H	0	*	*	*	0	1	1	1	1	□■■■■
02H	10H to 16H	1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
01H	08H to 0EH	8	*	*	*	0	0	1	0	0	□□■□□
03H	18H to 1EH	9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■

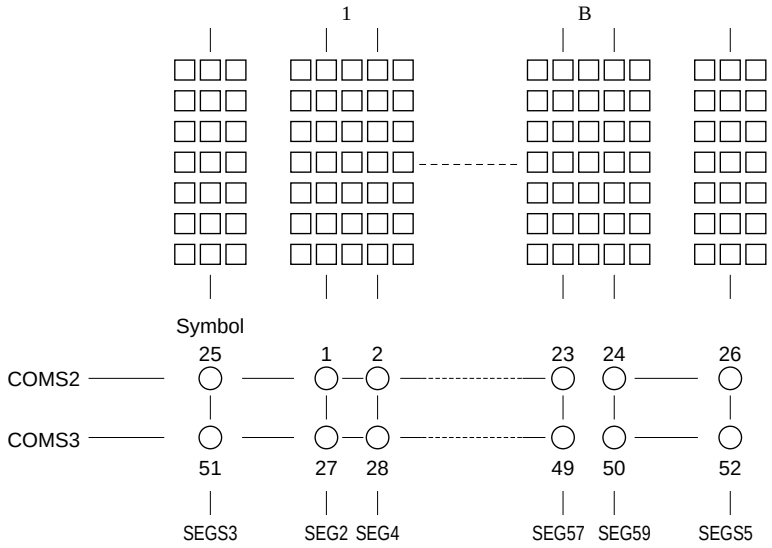
Unused

Character data
1: Display
0: Non-display

Symbol Register

The S1D12300 Series is provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 64 bits. In case of 12 digits, 48 symbols can be displayed. In case of 16 digits, 64 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.

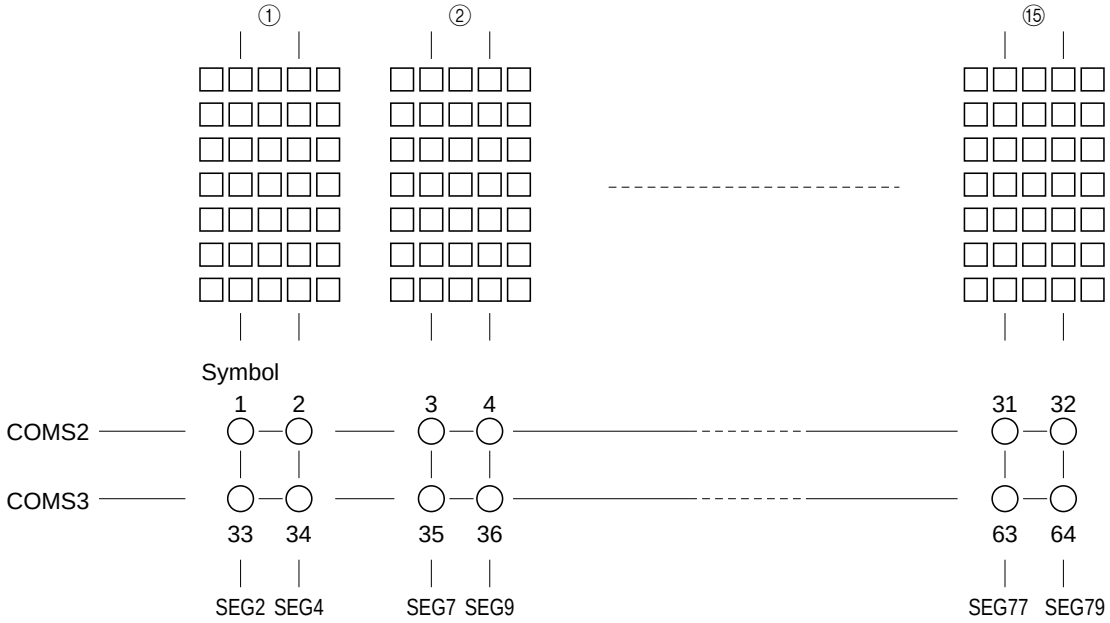
(1) S1D12300, S1D12301, S1D12302



RAM address		Symbol Bits D7							D0
70H to 7CH	0	*	*	*	27	1	28	2	*
	1	*	*	*	29	3	30	4	*
	:	:							
	B	*	*	*	49	23	50	24	*
	C	*	*	*	51	25	52	26	*

Bit
1: Display
0: Not display

(2) S1D12303



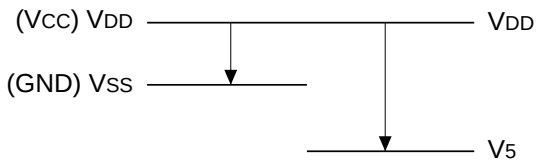
RAM address		Symbol Bits								Bit
		D7	D6	D5	D4	D3	D2	D1	D0	
70H to 7FH	0	*	*	*	33	1	34	2	*	1: Display
	1	*	*	*	35	3	36	4	*	0: Not display
	:	:								
	E	*	*	*	61	29	62	30	*	
	F	*	*	*	63	31	64	32	*	

Notes 1: If the symbol segment size is 1.5 times or more greater than the other dots, it is recommended to be divided into COMS2 and COMS3 and driven separately.

2: The segments other than symbol display must not be crossed through COMS2 or COMS3. The COMS3 symbol register must be set to all zeros if crossing.

9. ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0 to +0.3	V
Power supply voltage (2)		V_5	–12.0 to +0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes:
1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

10. DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			0.6×V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		0.4×V_5	V	V_3, V_4
HIGH-level input voltage		V_{IHC}			0.2×V_{SS}		V_{DD}	V	*3
LOW-level input voltage		V_{ILC}			V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*3	
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V			20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	µA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	µA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	µA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
			Access state	f_{cyc}=200KHz			500	µA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C V_{SS}=–3.0V		70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C f=1MHz			5.0	8.0	pF	*3

Reset time	t_R		1.0			µs	*8
Reset pulse width	t_{RW}		10			µs	*9
Reset start time	t_{RES}		50			ns	*9

Built-in power supply	Input voltage	V_{SS}		–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state	–7.2			V	V_{OUT}
			Triple boosting state	–10.8				
	Voltage follower operating voltage	V_5		–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C	–3.5	–3.1	–2.7	V	*12
	Reference voltage (option 1)	$V_{REG(VS1)}$	Ta = 25°C	–2.4	–2.1	–1.8	V	*12
	Reference voltage (option 2)	$V_{REG(VSS)}$	Ta = 25°C	V_{SS}	V_{SS}	V_{SS}	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Applied if not accessed by the MPU during character display and if the built-in power circuit and oscillator are operation.
Display character : 

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the S1D123** usually enters the operating state after t_R.

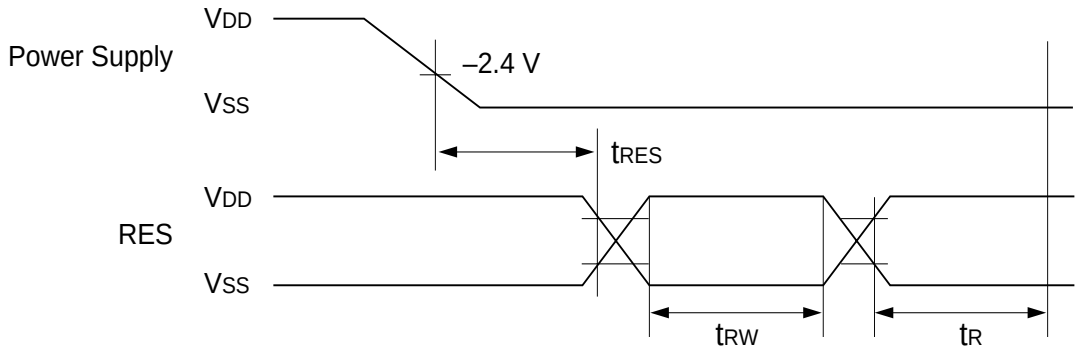
*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The S1D12300 has 13 digits of display and 1/30 duty.
f_{OSC} = 13 × 30 × 100 = 39 kHz
f_{BST} = (1/2) × (1/13) × 39 K = 1.5 kHz

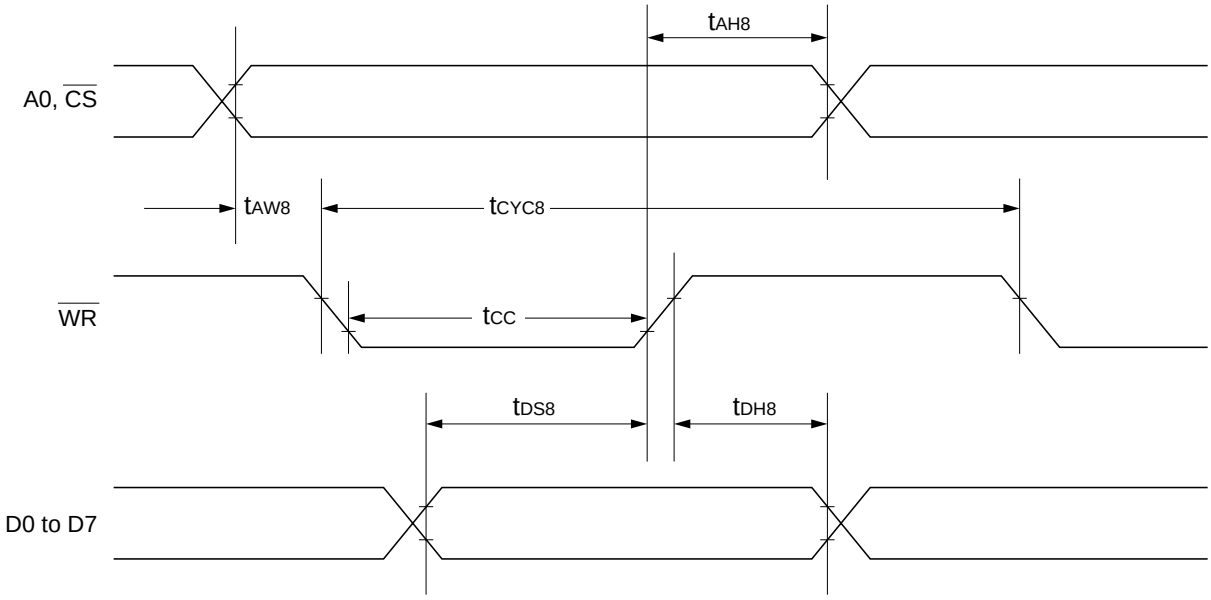
*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The voltage of power supply terminal V_{SS} can be selected as the reference power supply as an option without using the reference voltage inside the IC. In this case, however, a regulator is used for the external power supply (V_{DD} – V_{SS}). The voltage accuracy of V5 depends on that of the regulator used. The CGROM modification rules apply to the optional models.



All signal timings are based on 20% and 80% of V_{SS} signals.

11. TIMING CHARACTERISTICS

(1) System Bus Write Characteristic I (80 series MPU)

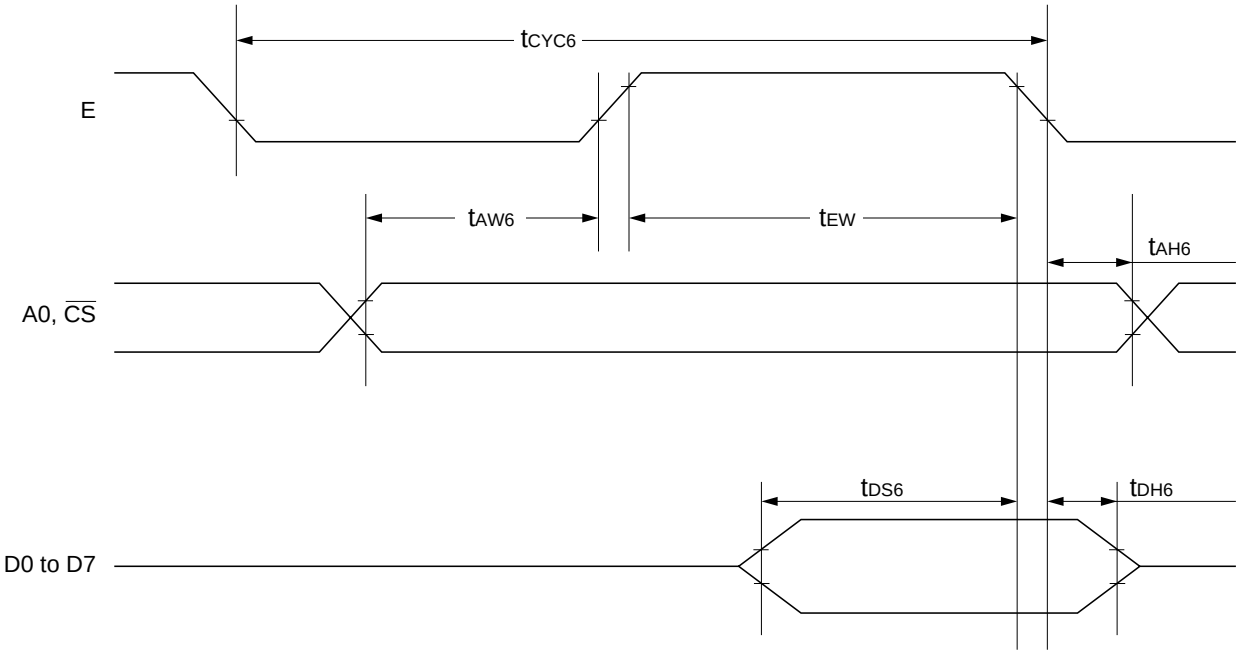


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	t AH8		30		ns
Address setup time		t AW8		60		ns
System cycle time	WR	t CYC8	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Control pulse width (Write)		t CC	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		
Data setup time	D0 to D7	t DS8		100		ns
Data hold time		t DH8		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.
*3: For A0 and CS, the same time is not required. Input signals so that A0 and CS may satisfy tAW8 and tAH8 respectively.

(2) System Bus Write Characteristic II (68 series MPU)

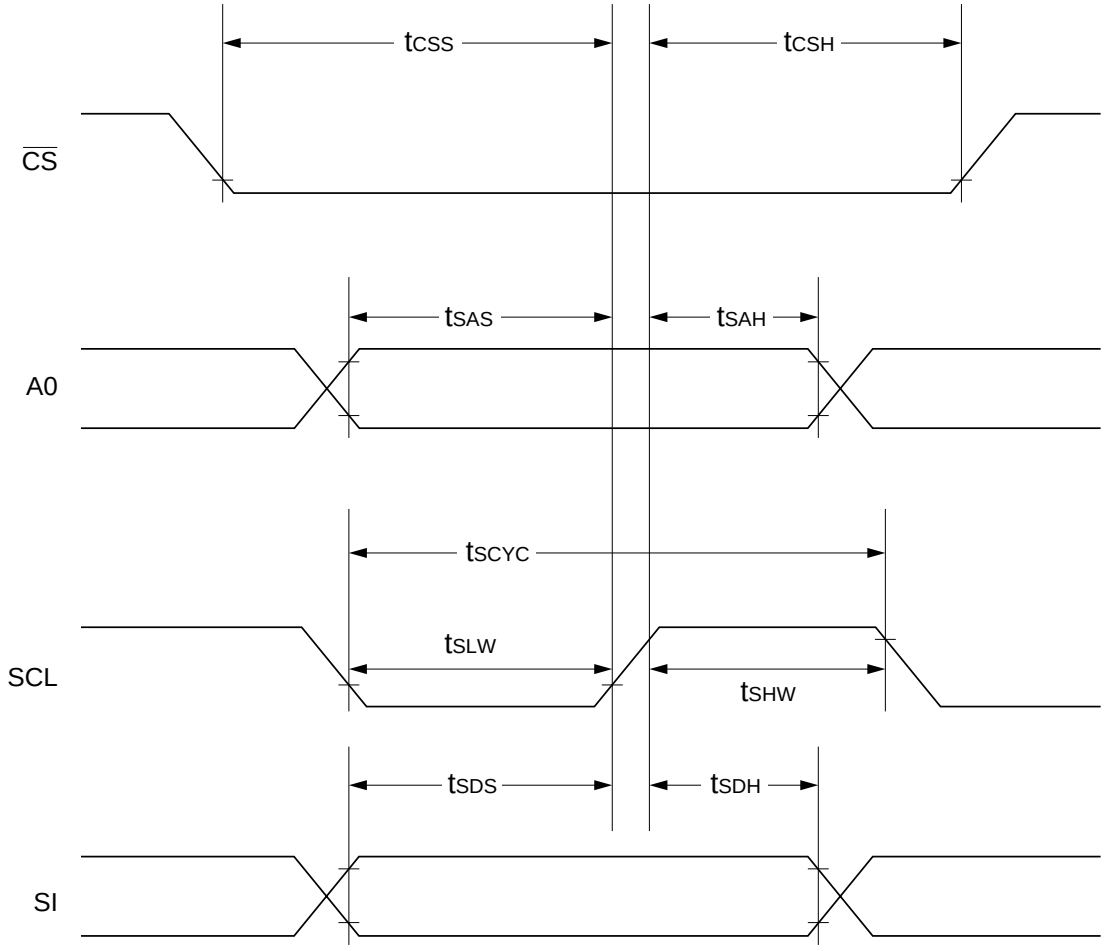


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, CS	t CYC6	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 to D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the CS active state. tCYC6 must be reserved after CS becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and CS, the same timing is not required. Input signals so that A0 and CS may satisfy tAW6 and tAH6 respectively.

(3) Serial Interface



[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C]

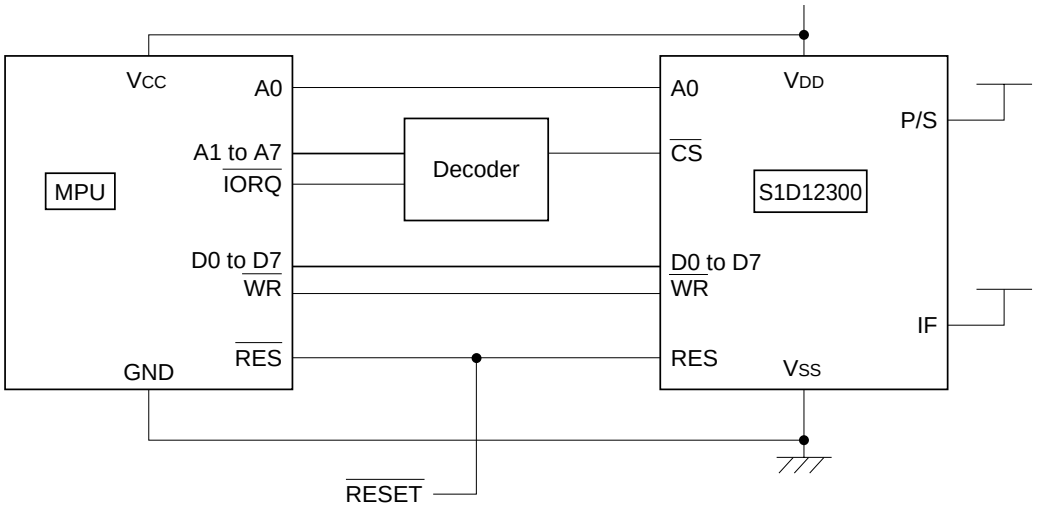
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	VSS = –3.0	700		ns
			–2.7	800		ns
			–2.4	1000		ns
SCL HIGH pulse width		tSHW		300		ns
SCL LOW pulse width		tSLW		300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH	VSS = –3.0	350		ns
			–2.7	400		ns
			–2.4	500		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS		150		ns
		tCSH	VSS = –3.0	550		ns
			–2.7	650		ns
			–2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.

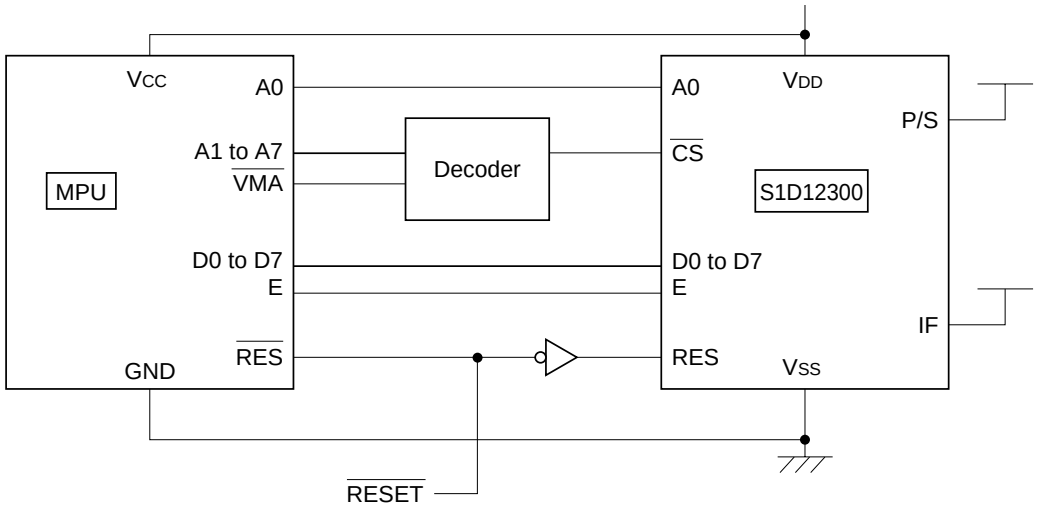
12. MPU INTERFACE (REFERENCE EXAMPLES)

The S1D12300 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the S1D12300 Series can be operated by less signal lines.

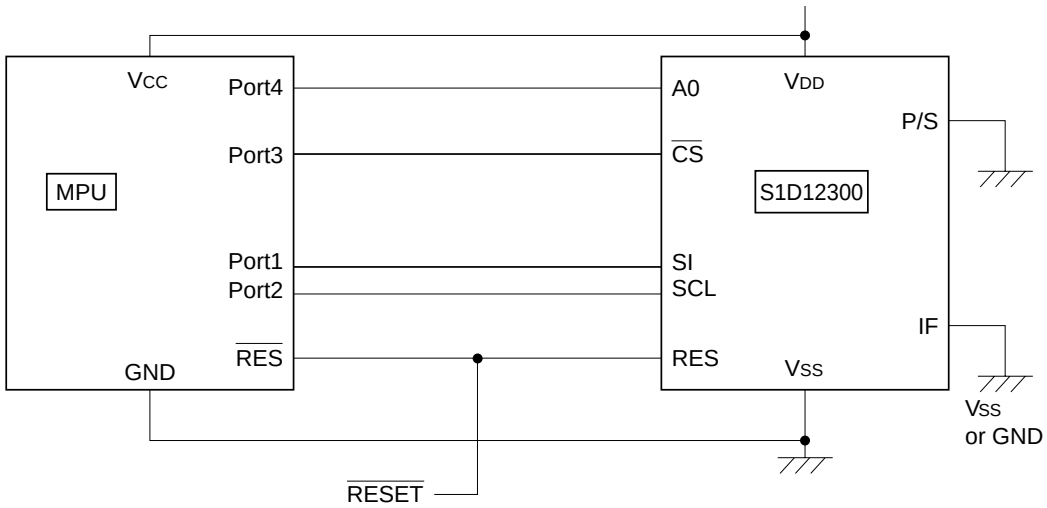
80 Series MPU



68 Series MPU

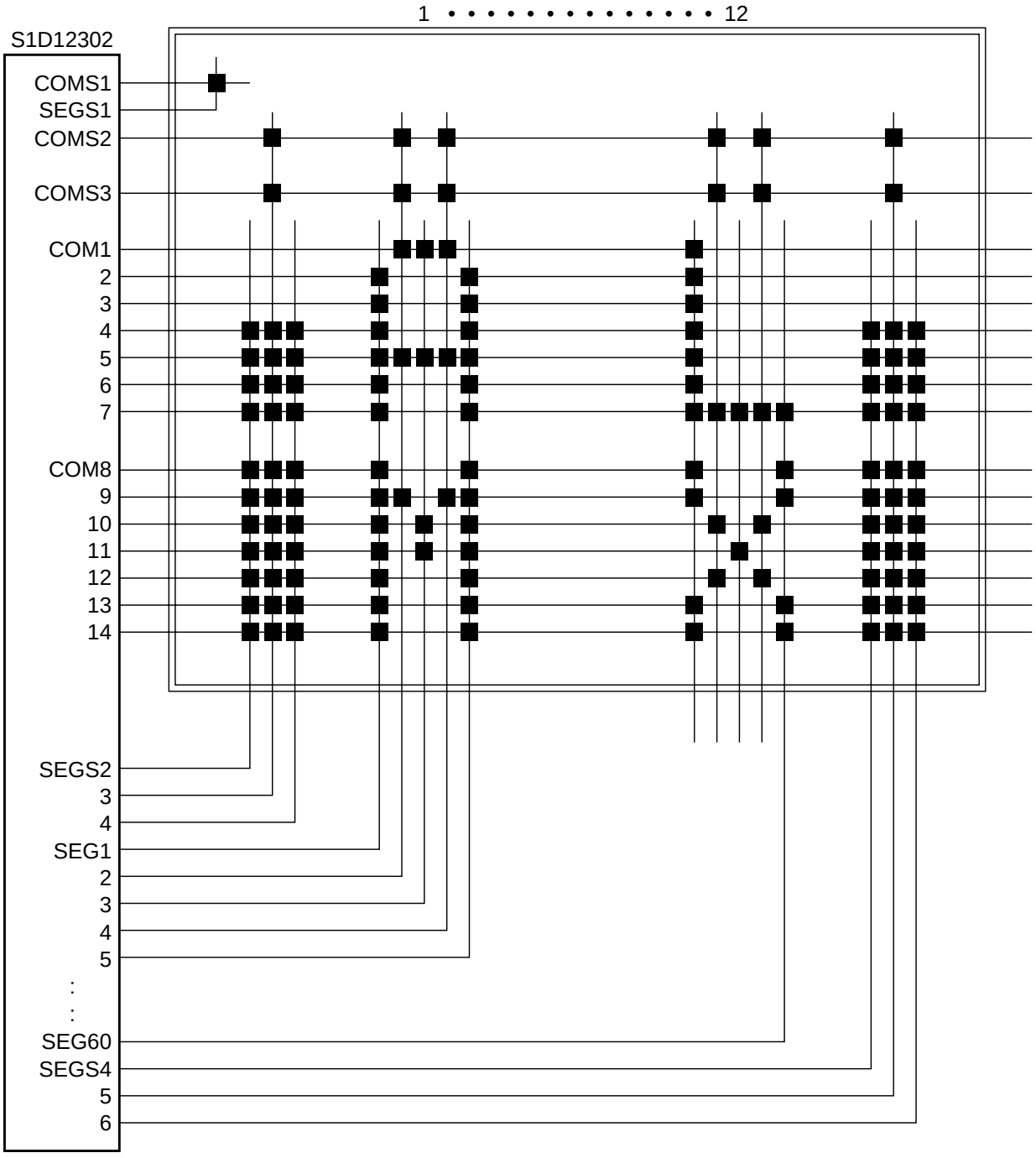


Serial Interface



13. INTERFACE TO LCD CELLS (REFERENCE)

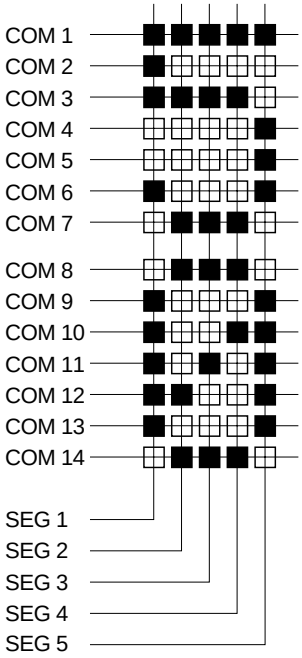
12 columns by 2 lines, 5 × 7-dot matrix segments and symbols

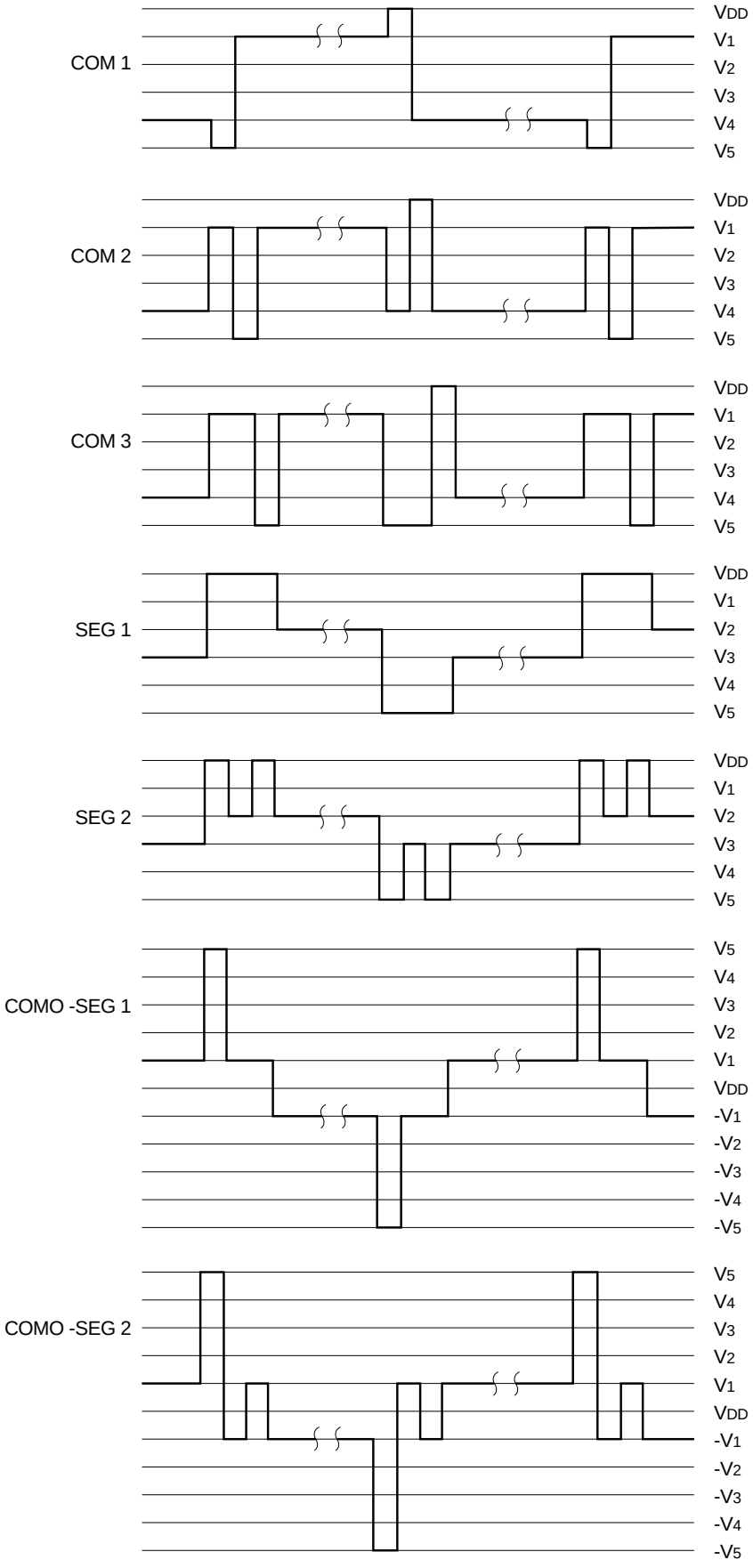


■ System Setup

N2	N1
0	0

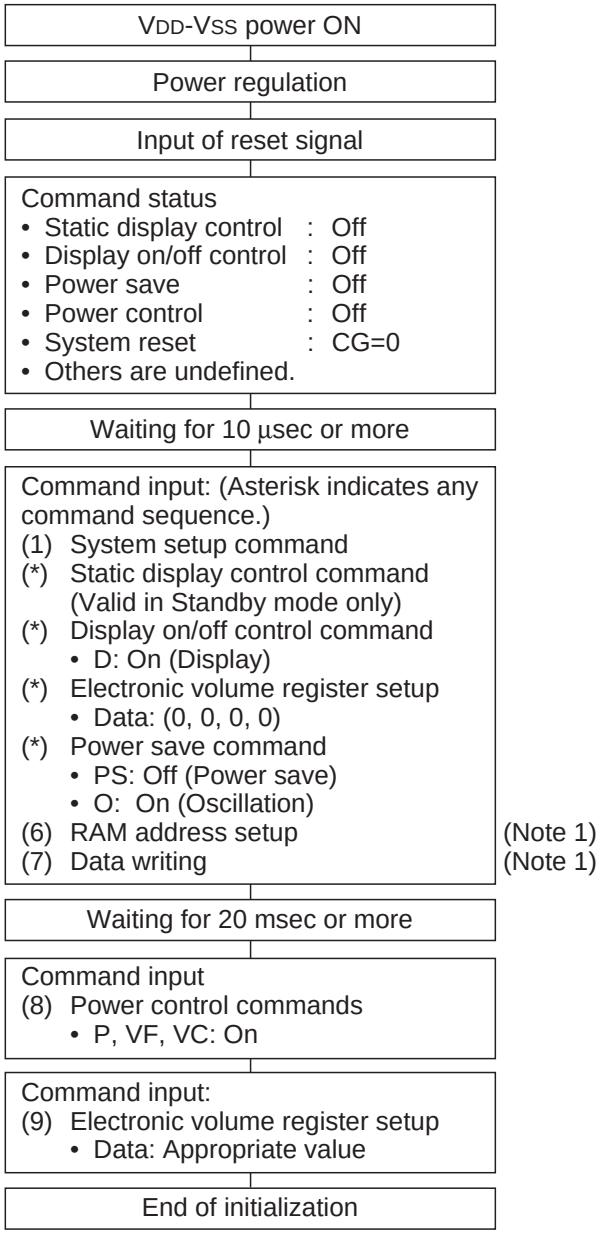
14. LCD DRIVE WAVEFORMS (B WAVEFORMS)



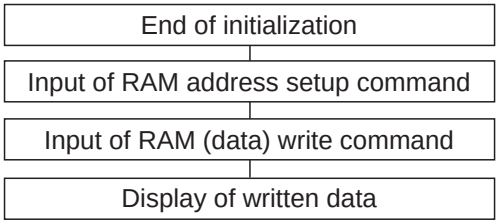


15. INSTRUCTION SETUP EXAMPLE (REFERENCE)

(1) Initial setup



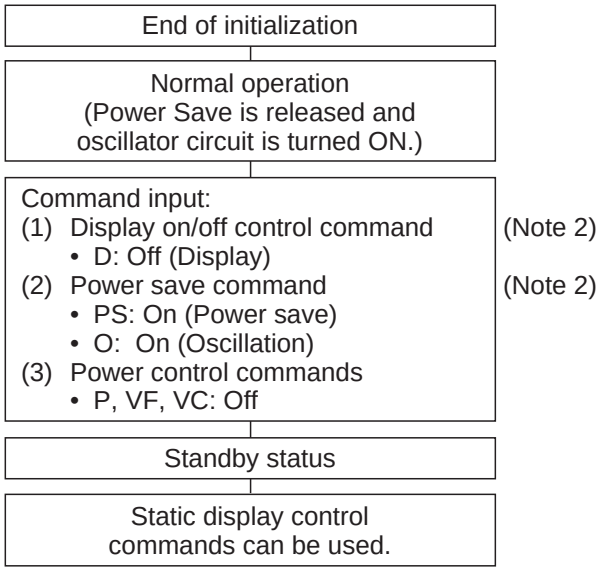
(2) Display mode



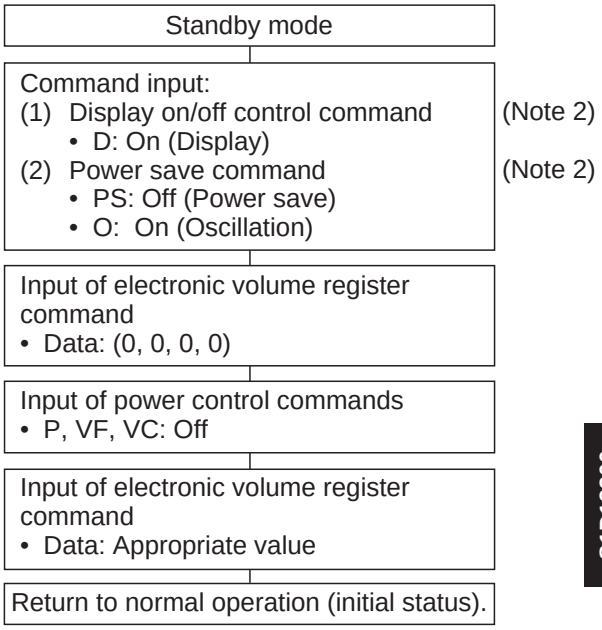
Note 1: Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

(3-1) Selecting the Standby mode

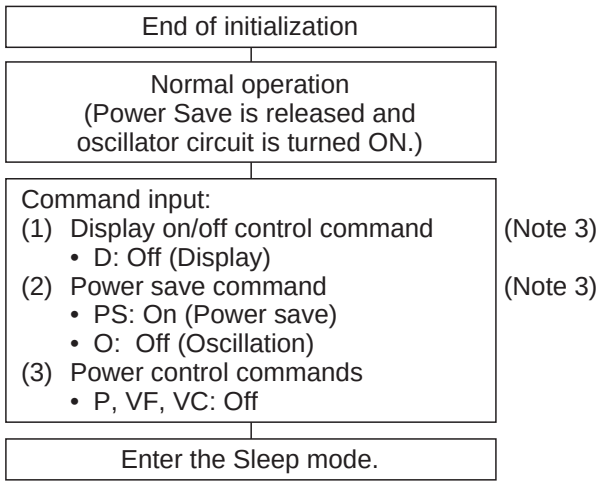


(3-2) Releasing the Standby mode

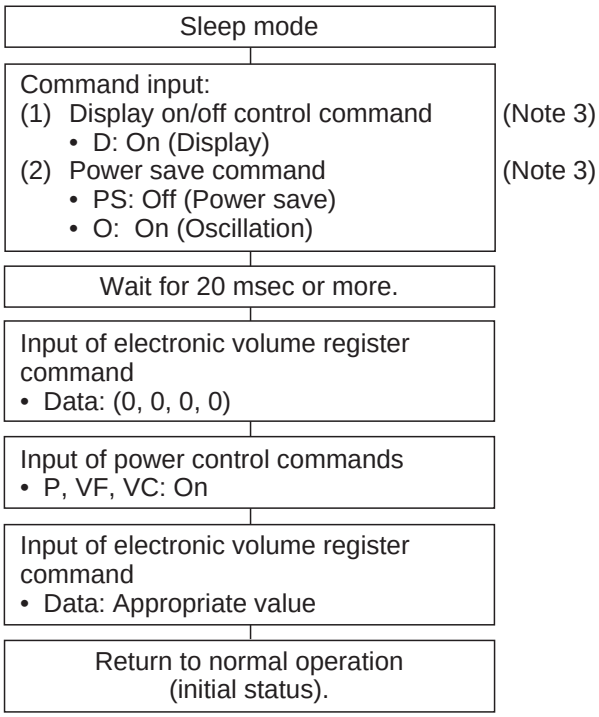


Note 2: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode



(4-2) Releasing the Sleep mode



Note 3: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

S1D12304/12305 Series

Rev. 2.4

Contents

1. DESCRIPTION

The S1D12304/12305 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maxi-mum of 48 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.
A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5 × 7 dots. A user-defined character RAM for four characters of 5 × 7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and sleep mode.
S1D12304, and 12305 depending on the duty of use and the number of display columns.

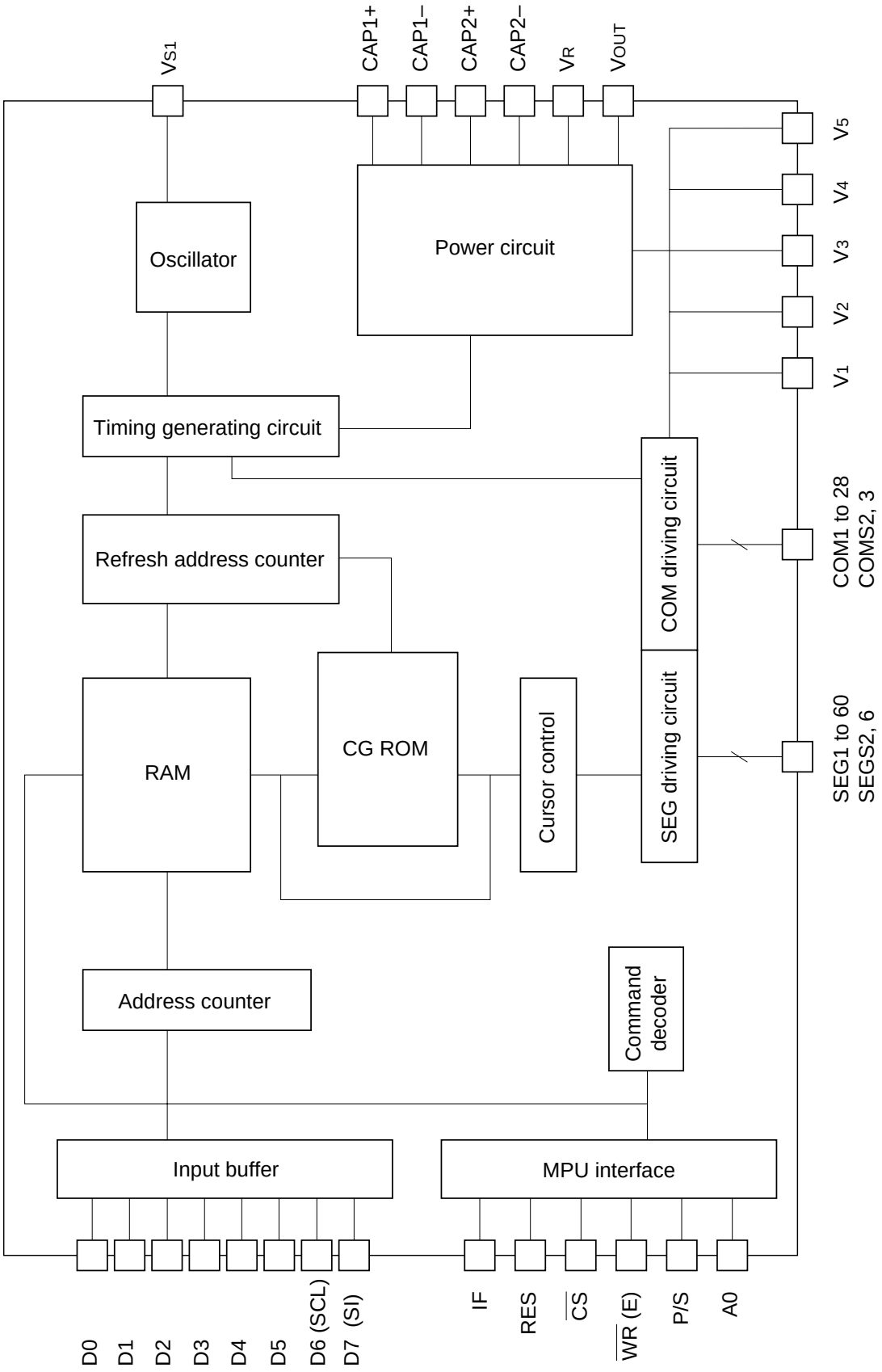
2. FEATURES

- Built-in diplay RAM
  48 characters + 4 user-defined characters + 48 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (48 symbols)
- Number of display columns × number of lines
  (12 columns + 2 segment for signal) × 4 lines + 48 symbols: S1D12304
  (12 columns + 2 segment for signal) × 2 lines + 48 symbols: S1D12305
- CR oscillation circuit (on-chip C and R)
- High-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5 × 7 dots
- Duty ratio 1/16 (S1D12305)
  1/30 (S1D12304)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 µA Max. (In normal operation mode: Including the operating current of the built-in power supply)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
  : –5.0 V to –8.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
  (Pad Pitch)
- COB assemble 126 µm min.
- Delivery form: Chip S1D123∗∗D∗∗A∗,
  S1D123∗∗D∗∗C∗,
  S1D123∗∗D∗∗F∗
- This IC is not designed with a protection against radioactive rays.

S1D12300 Series (S1D12304/12305) Chip Specifications

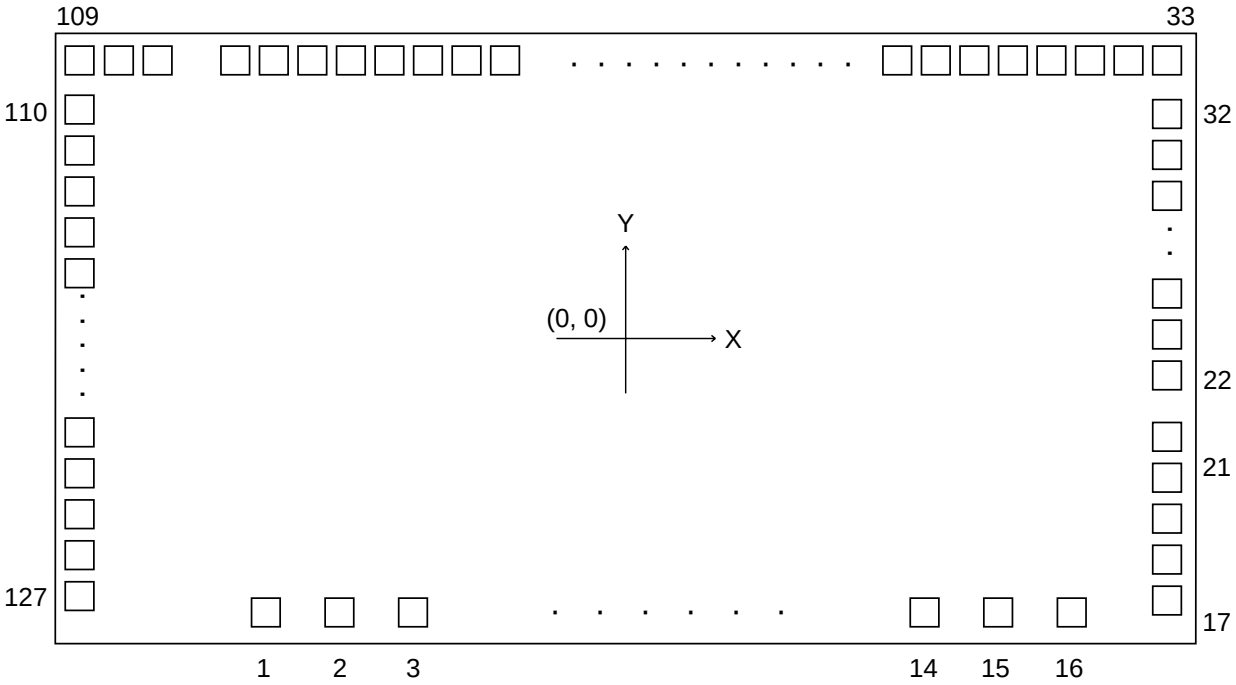
Product name	Duty	No. of digits indicated	No. of lines indicated	Font	V_{REG} temperature slope	Chip thickness	Form at delivery
S1D12305D10A∗	1/16	12 columns + 2 segment for signal	2 lines	Table 5 S1D123∗∗D10∗∗	–0.17%/°C	625µm	AL-PAD chip
S1D12305D10B∗	1/16	12 columns + 2 segment for signal	2 lines	Table 6 S1D123∗∗D11∗∗	–0.17%/°C	625µm	AL-PAD chip
S1D12305D16A∗	1/16	12 columns + 2 segment for signal	2 lines	Table 7 S1D123∗∗D16∗∗	–0.17%/°C	625µm	AL-PAD chip
S1D12305D02C∗	1/16	12 columns + 2 segment for signal	2 lines	Table 7 S1D123∗∗D16∗∗	External Input	525µm	AL-PAD chip

3. BLOCK DIAGRAM



4. PAD

Pad Layout



□ : NC (Make it floating.)

S1D12304D∗∗∗∗ 1/30 duty
S1D12305D∗∗∗∗ 1/16 duty

#1 Column for CG ROM pattern change

Chip size: 10.23 × 3.11 mm
Pad pitch: 126 µm (Min.)
Chip thickness: 625 ± 25 µm (S1D123∗∗D∗∗A∗)
525 ± 25 µm (S1D123∗∗D∗∗C∗)

1) A1 pad specification
Pad size: A 91 µm × 90 µm
B 114 µm × 114 µm

Pad Center Coordinate

<S1D12304D****>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	V_{DD}	–4077	–1371
2	V_{SSL}	–3526	
3	V_5	–2975	
4	V_4	–2424	
5	V_3	–1855	
6	V_2	–1287	
7	V_1	–719	
8	V_0	–151	
9	V_R	400	
10	V_{OUT}	968	
11	CAP2–	1519	
12	CAP2+	2070	
13	CAP1–	2638	
14	CAP1+	3189	
15	V_{SSR}	3757	
16	V_{DD}	4308	
17	(NC)	4883	
18	(NC)	4883	
19	(NC)	4883	
20	(NC)	4883	
21	V_{S1}	4929	
22	P/S	4924	
23	IF	4924	
24	RES	4924	
25	COMS2	4950	
26	COM1	4950	
27	COM2	4950	
28	COM3	4950	
29	COM4	4950	
30	COM5	4950	
31	COM6	4950	
32	COM7	4950	
33	COM8	4896	
34	COM9	4769	
35	COM10	4642	
36	COM11	4515	
37	COM12	4388	
38	COM13	4262	
39	COM14	4135	
40	SEGS2	4008	
41	SEG1	3881	
42	SEG2	3754	
43	SEG3	3627	
44	SEG4	3501	
45	SEG5	3374	
46	SEG6	3247	
47	SEG7	3120	
48	SEG8	2993	
49	SEG9	2866	
50	SEG10	2740	
51	SEG11	2613	
52	SEG12	2486	
53	SEG13	2359	
54	SEG14	2232	

PAD		COORDINATES	
No.	Name	X	Y
55	SEG15	2106	1406
56	SEG16	1979	
57	SEG17	1852	
58	SEG18	1725	
59	SEG19	1598	
60	SEG20	1471	
61	SEG21	1345	
62	SEG22	1218	
63	SEG23	1091	
64	SEG24	964	
65	SEG25	837	
66	SEG26	710	
67	SEG27	584	
68	SEG28	457	
69	SEG29	330	
70	SEG30	203	
71	SEG31	76	
72	SEG32	–51	
73	SEG33	–177	
74	SEG34	–304	
75	SEG35	–431	
76	SEG36	–558	
77	SEG37	–685	
78	SEG38	–812	
79	SEG39	–938	
80	SEG40	–1065	
81	SEG41	–1192	
82	SEG42	–1319	
83	SEG43	–1446	
84	SEG44	–1572	
85	SEG45	–1699	
86	SEG46	–1826	
87	SEG47	–1953	
88	SEG48	–2080	
89	SEG49	–2207	
90	SEG50	–2333	
91	SEG51	–2460	
92	SEG52	–2587	
93	SEG53	–2714	
94	SEG54	–2841	
95	SEG55	–2968	
96	SEG56	–3094	
97	SEG57	–3221	
98	SEG58	–3348	
99	SEG59	–3475	
100	SEG60	–3602	
101	SEGS6	–3729	
102	COM28	–3855	
103	COM27	–3982	
104	COM26	–4109	
105	COM25	–4236	
106	COM24	–4363	
107	COM23	–4679	1405
108	COM22	–4806	1405

PAD		COORDINATES	
No.	Name	X	Y
109	COM21	–4933	1405
110	COM20	–4964	1094
111	COM19	↓	966
112	COM18	↓	839
113	COM17	↓	712
114	COM16	↓	584
115	COM15	↓	457
116	COMS3	↓	330
117	$\overline{A0}$	↓	202
118	$\overline{WR}$	↓	75
119	$\overline{CS}$	↓	–52
120	D7	↓	–180
121	D6	↓	–307
122	D5	↓	–434
123	D4	↓	–562
124	D3	↓	–689
125	D2	↓	–816
126	D1	↓	–943
127	D0	↓	–1071

Note 1 : Set the pin (NC) to the floating state.
2 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

<S1D12305D****>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	V_{DD}	–4077	–1371
2	V_{SSL}	–3526	
3	V_5	–2975	
4	V_4	–2424	
5	V_3	–1855	
6	V_2	–1287	
7	V_1	–719	
8	V_0	–151	
9	V_R	400	
10	V_{OUT}	968	
11	CAP2–	1519	
12	CAP2+	2070	
13	CAP1–	2638	
14	CAP1+	3189	
15	V_{SSR}	3757	
16	V_{DD}	4308	
17	(NC)	4883	–1343
18	(NC)	4883	–1233
19	(NC)	4883	–1123
20	(NC)	4883	–1013
21	V_{S1}	4929	–903
22	P/S	4924	–184
23	IF	4924	–57
24	RES	4924	70
25	COMS2	4950	255
26	COM1	4950	382
27	COM2	4950	510
28	COM3	4950	637
29	COM4	4950	764
30	COM5	4950	891
31	COM6	4950	1019
32	COM7	4950	1146
33	COM8	4896	1406
34	COM9	4769	
35	COM10	4642	
36	COM11	4515	
37	COM12	4388	
38	COM13	4262	
39	COM14	4135	
40	SEGS2	4008	
41	SEG1	3881	
42	SEG2	3754	
43	SEG3	3627	
44	SEG4	3501	
45	SEG5	3374	
46	SEG6	3247	
47	SEG7	3120	
48	SEG8	2993	
49	SEG9	2866	
50	SEG10	2740	
51	SEG11	2613	
52	SEG12	2486	
53	SEG13	2359	
54	SEG14	2232	

PAD		COORDINATES	
No.	Name	X	Y
55	SEG15	2106	–1406
56	SEG16	1979	
57	SEG17	1852	
58	SEG18	1725	
59	SEG19	1598	
60	SEG20	1471	
61	SEG21	1345	
62	SEG22	1218	
63	SEG23	1091	
64	SEG24	964	
65	SEG25	837	
66	SEG26	710	
67	SEG27	584	
68	SEG28	457	
69	SEG29	330	
70	SEG30	203	
71	SEG31	76	
72	SEG32	–51	
73	SEG33	–177	
74	SEG34	–304	
75	SEG35	–431	
76	SEG36	–558	
77	SEG37	–685	
78	SEG38	–812	
79	SEG39	–938	
80	SEG40	–1065	
81	SEG41	–1192	
82	SEG42	–1319	
83	SEG43	–1446	
84	SEG44	–1572	
85	SEG45	–1699	
86	SEG46	–1826	
87	SEG47	–1953	
88	SEG48	–2080	
89	SEG49	–2207	
90	SEG50	–2333	
91	SEG51	–2460	
92	SEG52	–2587	
93	SEG53	–2714	
94	SEG54	–2841	
95	SEG55	–2968	
96	SEG56	–3094	
97	SEG57	–3221	
98	SEG58	–3348	
99	SEG59	–3475	
100	SEG60	–3602	
101	SEGS6	–3729	
102	(NC)	–3855	
103	(NC)	–3982	
104	(NC)	–4109	
105	(NC)	–4236	
106	(NC)	–4363	
107	(NC)	–4679	1405
108	(NC)	–4806	1405

PAD		COORDINATES	
No.	Name	X	Y
109	COM14	–4933	1405
110	COM13	–4964	1094
111	COM12	↓	966
112	COM11	↓	839
113	COM10	↓	712
114	COM9	↓	584
115	COM8	↓	457
116	COMS3	↓	330
117	$\overline{A0}$	↓	202
118	$\overline{WR}$	↓	75
119	$\overline{CS}$	↓	–52
120	D7	↓	–180
121	D6	↓	–307
122	D5	↓	–434
123	D4	↓	–562
124	D3	↓	–689
125	D2	↓	–816
126	D1	↓	–943
127	D0	↓	–1071

Note 1 : Set the pin (NC) to the floating state.
2 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

5. PIN DESCRIPTION

Power Supply Pins

Pin name	I/O	Description	No. of Pins
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$, $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	No. of Pins
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{SS} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 to D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = LOW, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>D7</td><td>D6</td><td>D5 to D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>LOW</td><td>SI</td><td>SCL</td><td>—</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>HIGH</td><td>D7</td><td>D6</td><td>D5 to D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
</table>
When P/S = LOW, be sure to fix D5 to D0 to HIGH or LOW.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ↓. In case of an 80 series MPU, initialization can be performed by changing ↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
LOW : 80 series MPU interface
HIGH : 68 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the LOW level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (E)</td><td>I</td><td><When connecting an 80 series MPU>
Active LOW. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
When P/S = LOW, be sure to fix the $\overline{WR}$ signal to HIGH or LOW.
<When connecting a 68 series MPU>
Active HIGH. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>HIGH</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>–</td></tr>
<tr><td>LOW</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
HIGH: 8-bit parallel input
LOW: 4-bit parallel input
When P/S = LOW, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

S1D12304

Pin name	I/O	Description	No. of Pins
COM1 to COM28	O	Common signal output pin (for characters)	28
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG1 to SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

S1D12305

Pin name	I/O	Description	No. of Pins
COM1 to COM14	O	Common signal output pin (for characters) COM8 to COM14:W output	14 (21)
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG2 to SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

6. FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the S1D12304/12305, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting HIGH or LOW as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0 to D7
HIGH	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0 to D7
LOW	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

Parallel Input

In the S1D12304/12305, when parallel input is selected (P/S = HIGH), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either HIGH or LOW is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.

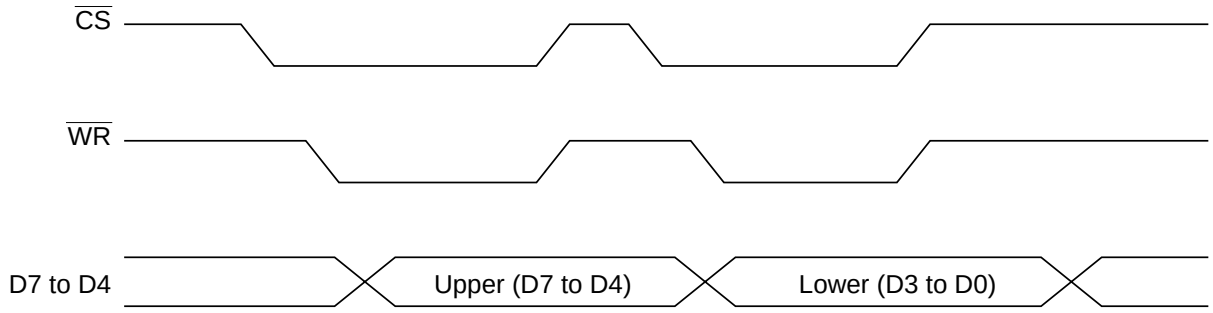
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
HIGH-to-LOW active	68 series	A0	E	$\overline{CS}$	D0 to D7
LOW-to-HIGH active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0 to D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = LOW)

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = LOW).

When no chip is selected, the shift register and counter are reset to the initial status.

Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL). At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.

The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = HIGH, it is regarded as display data. When A0 = LOW, it is regarded as a command.

The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.

Fig. 1 shows a timing chart of the serial interface.

Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.

We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

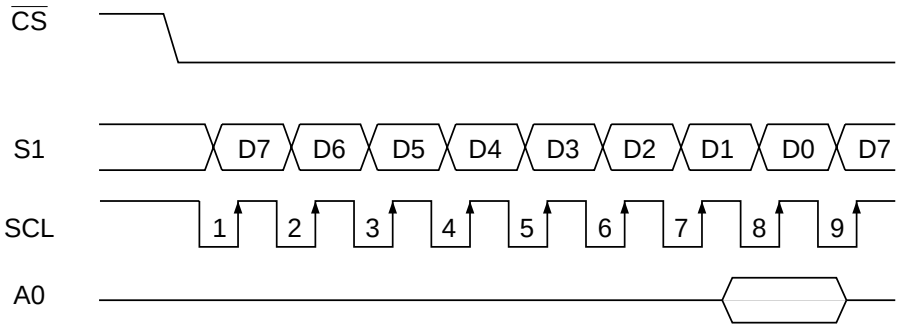


Fig. 1

Identification of data bus signals

The S1D12304/12305 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The S1D12304/12305 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = LOW, MPU interfacing is enabled. In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a LOW-power-consumption power circuit that generates a voltage required for liquid crystal drive. The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the S1D12304/12305 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity. In this case, an external power supply must be used.

A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

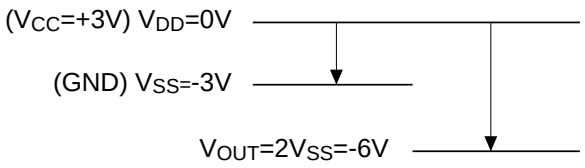
Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Triple boosting circuit

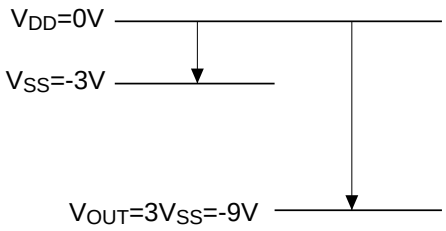
When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between VSS pin and VOUT pin respectively, the potential between the VDD pin and VSS pin is boosted triple and output to the VOUT pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and VOUT pin. Then, a double boosted output can be obtained from the VOUT pin (CAP2-).

The boosting circuit uses a signal from the oscillator ourput.

Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.



Potential during double boosting



Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V5 terminal.

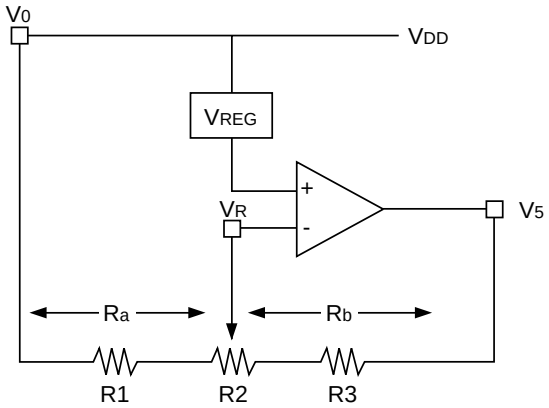
When V5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V5 can be regulated within a range of |V5|<|VOUT|. It may be calculated by the following formula:

$$V_5 = (1+\frac{R_b}{R_a}) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots ①$$

Wherein, VREG is the constant voltage source inside the S1D12300 Series and the voltage is constant at VREG ≒ 3.1V. Voltage regulation of the V5 output is accomplished by connecting a variable resistor between VR, VDD and V5. For fine adjustment of the V5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/°C under VREG outputs. When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the VR terminal has a HIGH input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.



Example 1:

Condition: I(R1, R2, R3) ≤ 5µA V5 = –6 to –8V

Setting:
R1+R2+R3 = 8V/5µA = 1.6MΩ
8V = (1+Rb/Ra) 3.0V Rb/Ra = 1.67
6V = (1+Rb/Ra) 3.0V Rb/Ra = 1

···· R1 = 600KΩ, R2 = 200KΩ, R3 = 800KΩ

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V_5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at (1, 1, 1, 1), the constant current value becomes: $I_{REF} \fallingdotseq 3.65\mu A$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = (1 + \frac{R_b}{R_c}) \cdot V_{REG} \cdots\cdots\cdots\cdots\cdots\cdots ②$$

$$\therefore \quad R_c = \frac{R_a \times R_I}{R_a + R_I}$$

$$R_I = \frac{V_R}{I_{REF}}$$

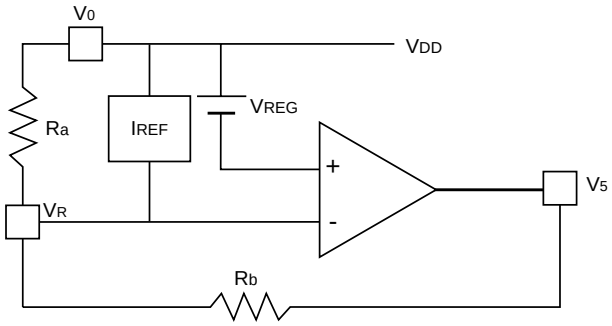


Fig. 9

(1) Determining the V_5 voltage setting range by the electronic volume control
Liquid crystal driving voltage V_5: max. -6v ~ min. -8V
V_5 variable voltage range: 2V

(2) Determinig the R_b
R_b = V_5 variable voltage range/ I_{REF}
= 2V/3.65µA
= 548KΩ

(3) Determining the R_a

$$R_a = \frac{V_{REG}}{(V_5 \text{ voltage setting max} - V_{REG}) / R_b}$$ (Use absolute values for V_{REG} and V_5 voltage settings.)

$$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

= 585KΩ

(4) Regulating the R_a
Set the electronic volume control register to (D3, D2, D1, D0) = (1, 0, 0, 0) or (0, 1, 1, 1) before matching the R_a value to the optimum contrast.

Since I_{REF} is a simplified constant voltage source, fluctuations upto ± 40% must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is : $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the R_a and R_b for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

When using the electronic volume control function, in order to compensate the V_5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as Ra and perform optimum contrast adjustment according to the above item (4) with each IC chip.

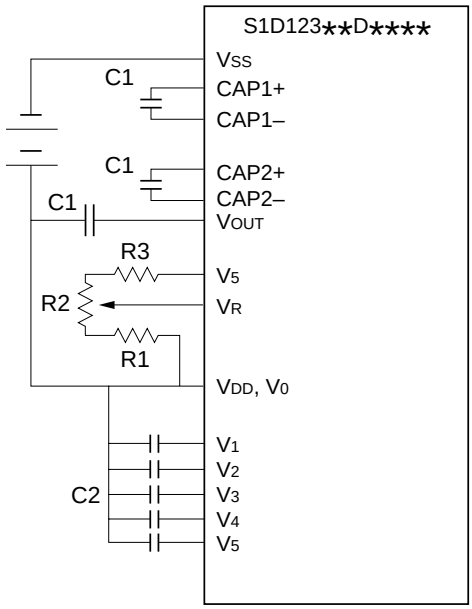
When the electronic volume control function is not being used, set the electronic volume control register to (0, 0, 0, 0) using the RES signal or the electronic volume control register setting command.

Liquid crystal voltage generating circuit

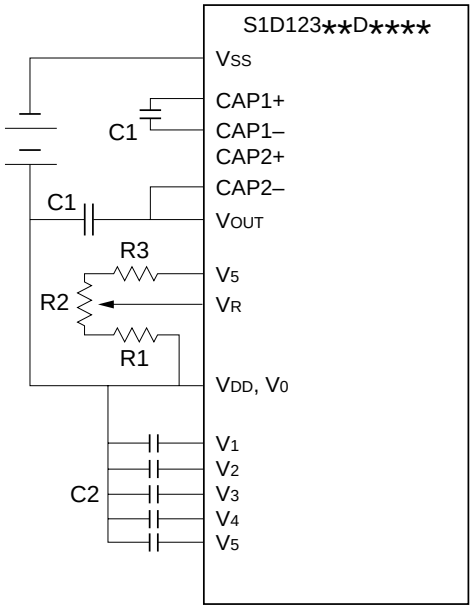
The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.
Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
The liquid crystal drive voltage is fixed to 1/5 bias.

As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V_1 to V_5 pins of liquid crystal power pins.

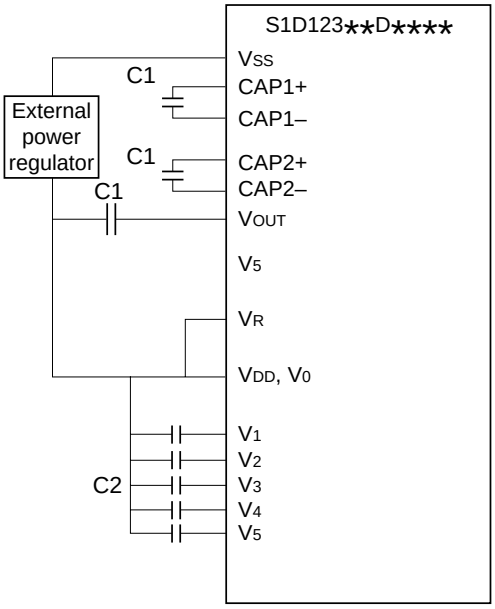
When a built-in power supply is used
Under a triple boosting



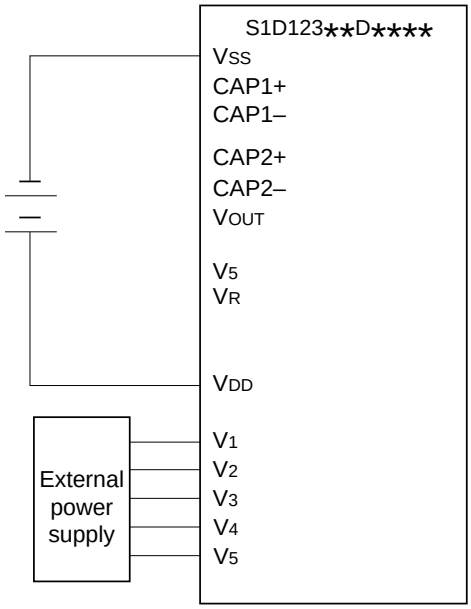
The diagram under a double boosting



When an external power regulator is used
(The built-in power regulator is not used)



When a built-in power supply is not used



Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Low Power Consumption Mode

The S1D12304/12305 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

● Sleep Mode

After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
   COM1 to COM28, COMS2, COMS3 : V_{DD} level
   SEG1 to SEG60, SEGS2, SEGS6 : V_{DD} level
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

1. Display ON/OFF control
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   DC = 0 : Double cursor OFF
   D = 0 : Display OFF
2. Power save
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
3. Power control
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
4. System set
   CG = 0 : No use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.
Regarding the reset signal, a pulse of at least 10 µs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 µs from the edge of the RES signal.
In the S1D12304/12305 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.

7. COMMANDS

Table 4 shows a command list. In the S1D12304/12305 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).
Command interpretation and execution are performed by only internal timing. This permits HIGH-speed processing.

- **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the S1D12304/12305 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (t_{cyc}) and execute the next instruction.

- **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
1 : Display ON

DC = 0 : Double cursor OFF
1 : Double cursor ON

B = 0 : Cursor blink OFF
1 : Cursor blink ON

In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display characters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

(3) Power Save
This command is used to control the oscillating circuit and set and reset sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save OFF (reset)
1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
1 : Oscillating circuit ON (oscillation)

(4) Power Control
This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Boosting circuit OFF
1 : Boosting circuit ON

Note: To operate the boosting circuit the oscillating circuit must be in operation.

VF = 0 : Voltage follower OFF
1 : Voltage follower ON

VC = 0 : Voltage regulating circuit OFF
1 : Voltage regulating circuit ON

(5) System Set
This command set the use or non-use of display lines and CG RAM.
Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

* : Don't Care

CG = 0 : Use of CG RAM
1 : Non-use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(6) Electronic Volume Register Set
This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply, thereby adjusting the gradation of liquid crystal display.
When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code
70H to 7FH

MSB	.	.	LSB	$\lvert V_5 \rvert$	$\lvert I_{REF} \rvert$
0	0	0	0	Small	0.0µA
		:		:	:
		.	:	:	:
1	1	1	1	Large	3.65µA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(7) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM(00H)							–	CGRAM(01H)							–
10H	CGRAM(02H)							–	CGRAM(03H)							–
20H	Unused															
30H	DDRAM line 1														Unused	
40H	DDRAM line 2							For signals							"	
50H	DDRAM line 3														"	
60H	DDRAM line 4														"	
70H	Symbol register														"	

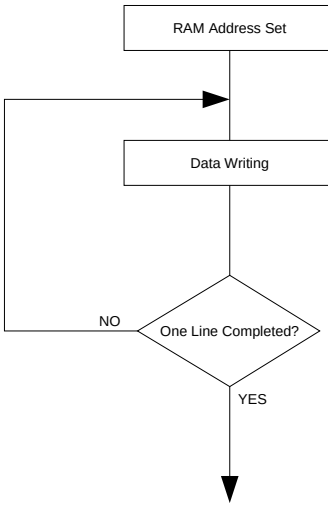
– : Unused
For signals : Output from SEGS2 to SEGS6.

(8) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data into the DD RAM, CG RAM or symbol register.
② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>
The following is an example of writing one-line data into the DD RAM in succession.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 S1D12304/S1D12305 Command List

Command	Code										Function
	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(6) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(7) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(8) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(9) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(10) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don't use this command.

8. CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The S1D12304/12305 is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5 × 7 dots.

Table 5 shows a character code table of the S1D123∗∗D∗∗∗∗ Series.
The 4characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

The CG ROM of the S1D12304/12305 is a mask ROM and compatible with the use-dedicated CG ROM. Please ask us for further information of it.

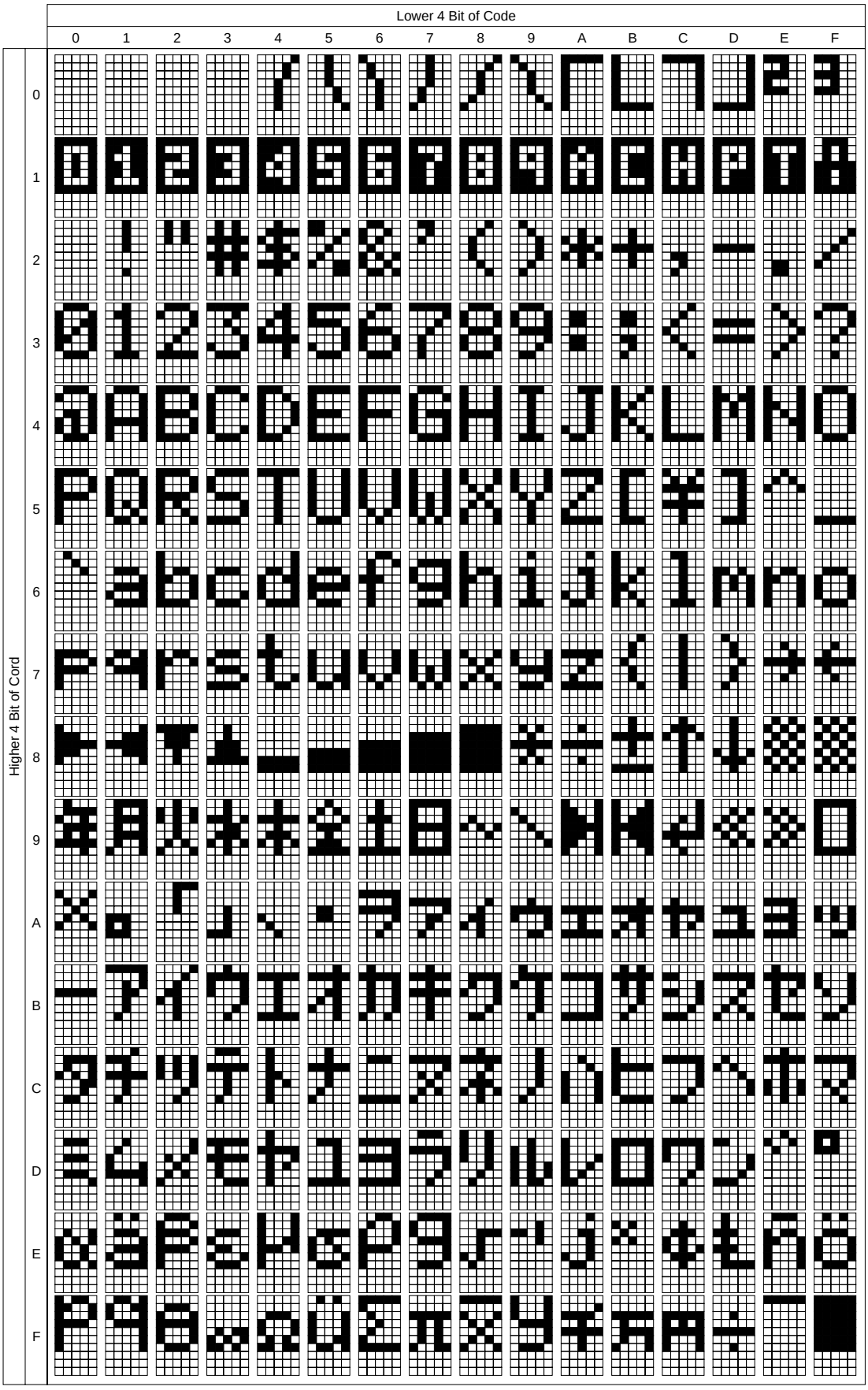
Regarding changed CG ROM, it is defined in product name as follows:

(Example) S1D12305D∗∗A∗

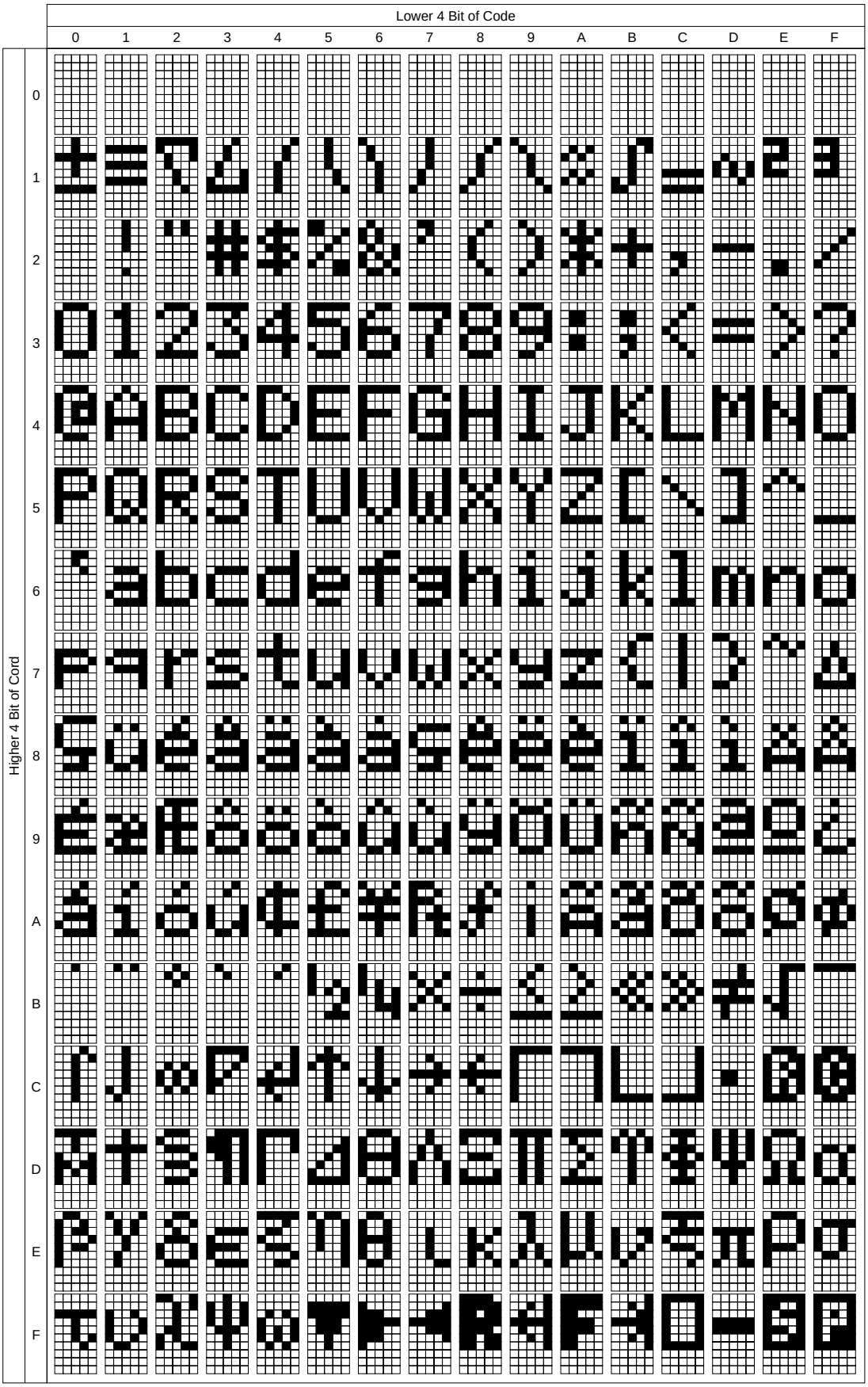
Digit for CG ROM pattern change

S1D123**D10**

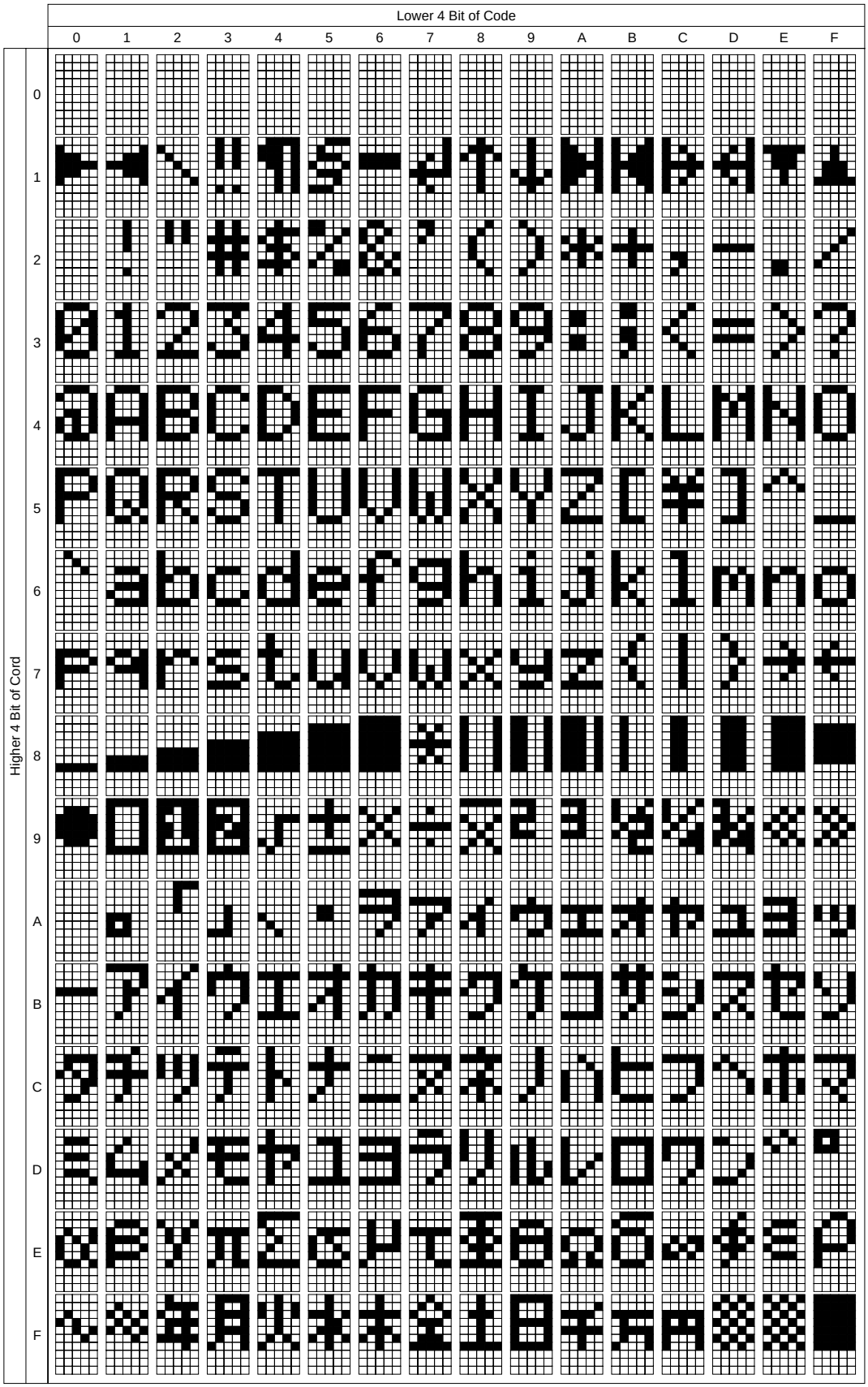
Table 5



S1D123**D11**



S1D123**D16**



Character Generator RAM (CG RAM)

The S1D12304/12035 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5 × 7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

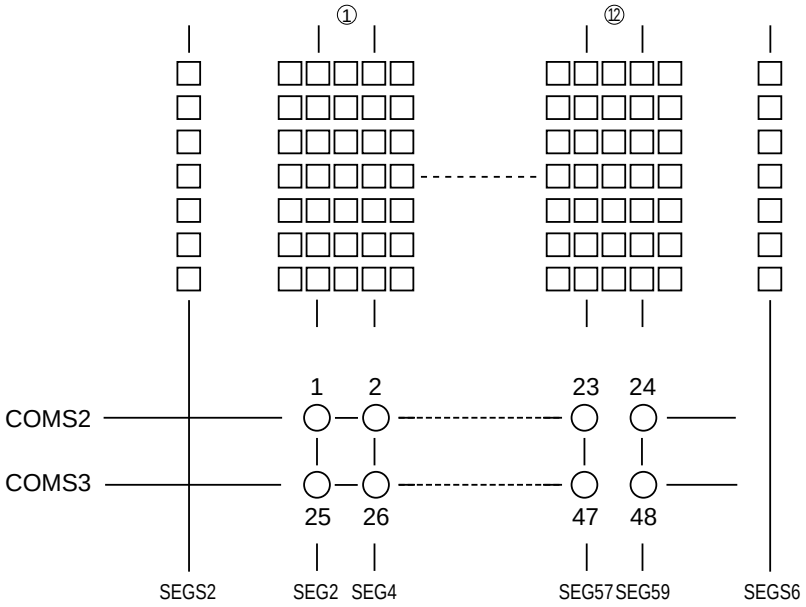
Character code	RAM address		CGRAM data (character pattern) D7 — D0								Display
00H	00H to 06H	0	*	*	*	0	1	1	1	1	□■■■■
02H	10H to 16H	1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
01H	08H to 0EH	8	*	*	*	0	0	1	0	0	□□■□□
03H	18H to 1EH	9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■

Unused

Character data
1: Display
0: Non-display

Symbol Register

The S1D12304/12305 provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 48 bits. In case of 48 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.



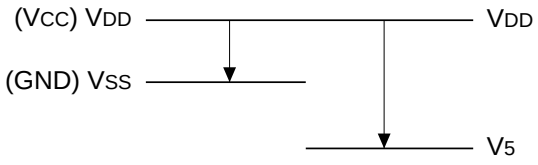
RAM address		Symbol Bits D7							D0
70H to 7BH	0	*	*	*	25	1	26	2	*
	1	*	*	*	27	3	28	4	*
	:	:							
	B	*	*	*	47	23	48	24	*

Bit
1: Display
0: Not display

Notes: 1. We recommend to drive a symbol by dividing it into COMS2 and COMS3 separately if it is larger than other dots for 1.5 times or more.
2. Do not cross a segment (other than those used for symbol display) with COMS2 or COMS3. If segment crossing is required, set the symbol registers of COMS3 to all zeros (0s).

9. ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0 to +0.3	V
Power supply voltage (2)		V_5	–16.0 to +0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes:
1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

10. DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			0.6×V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		0.4×V_5	V	V_3, V_4
HIGH-level input voltage		V_{IHC}			0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}			V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS} –1.0			1.0	µA	*3	
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V			20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	µA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	µA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	µA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
			Access state	f_{cyc}=200KHz			500	µA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C V_{SS}=–3.0V		70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C f=1MHz			5.0	8.0	pF	*3
Reset time		t_R			1.0			µs	*8
Reset pulse width		t_{RW}			10			µs	*9
Reset start time		t_{RES}			50			ns	*9
Built-in power supply	Input voltage	V_{SS}			–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state		–7.2			V	V_{OUT}
			Triple boosting state		–10.8				
	Voltage follower operating voltage	V_5			–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C		–3.5	–3.1	–2.7	V	*12
	Reference voltage (option)	$V_{REG(VS1)}$	Ta = 25°C		–2.4	–2.1	–1.8	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 to D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Applied if not accessed by the MPU during character display and if the built-in power circuit and oscillator are operating.
Display character. 

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the S1D123** usually enters the operating state after t_R.

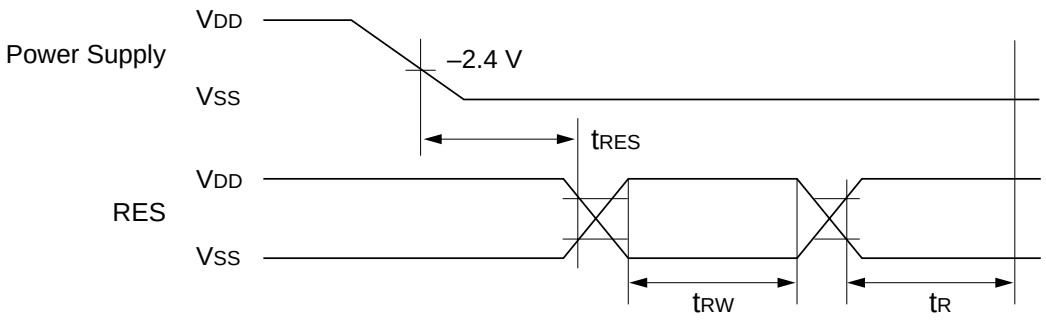
*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The SED1230 has 13 digits of display and 1/30 duty.
f_{OSC} = 13 × 30 × 100 = 39 kHz
f_{BST} = (1/2) × (1/13) × 39 K = 1.5 kHz

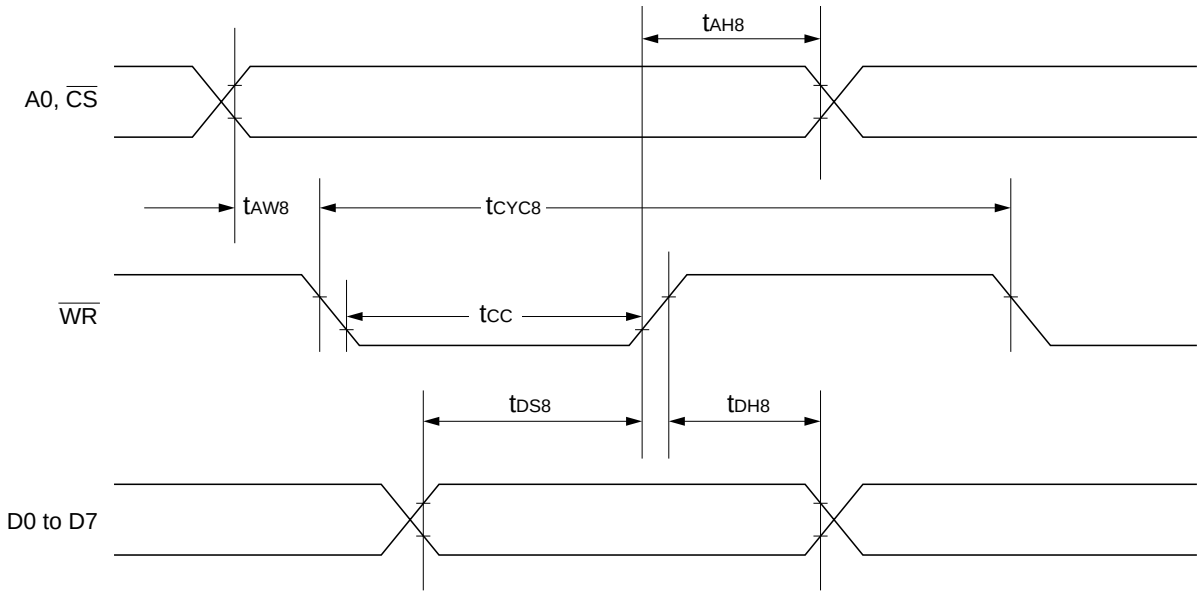
*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The CGROM modification rules apply to the optional models.



All signal timings are based on 20% and 80% of V_{SS} signals.

11. TIMING CHARACTERISTICS

(1) System Bus Write Characteristic I (80 series MPU)

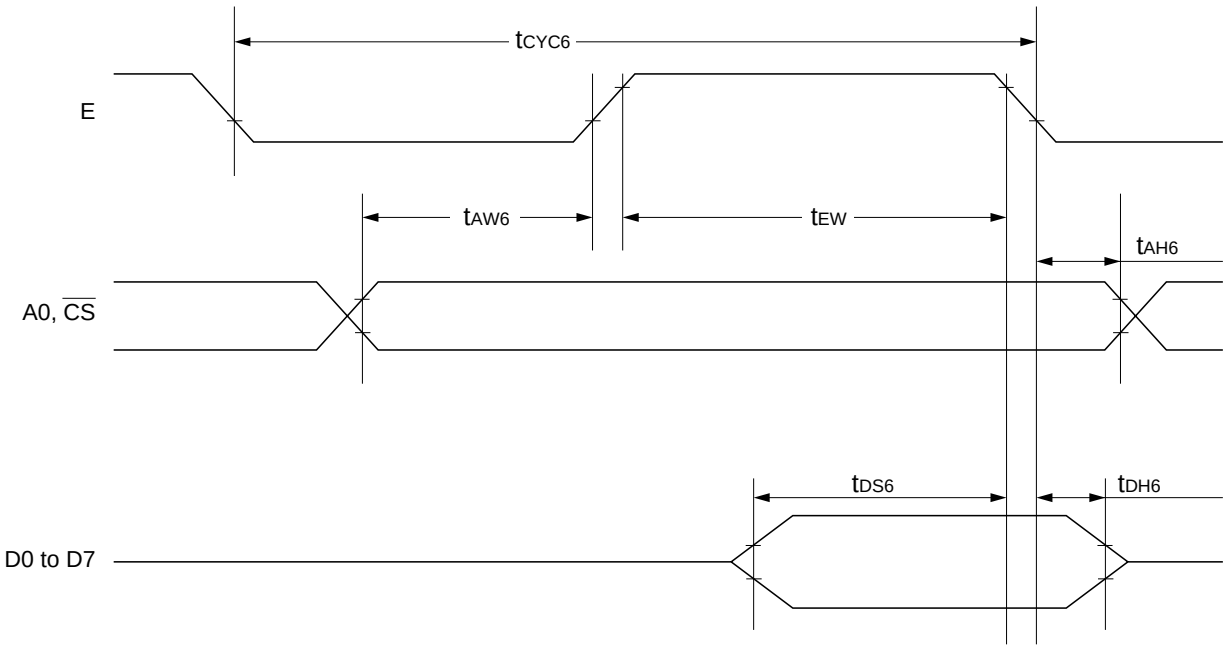


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	t AH8		30		ns
Address setup time		t AW8		60		ns
System cycle time	WR	t CYC8	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Control pulse width (Write)		t CC	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		
Data setup time	D0 to D7	t DS8		100		ns
Data hold time		t DH8		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.
*3: For A0 and CS, the same time is not required. Input signals so that A0 and CS may satisfy tAW8 and tAH8 respectively.

(2) System Bus Write Characteristic II (68 series MPU)

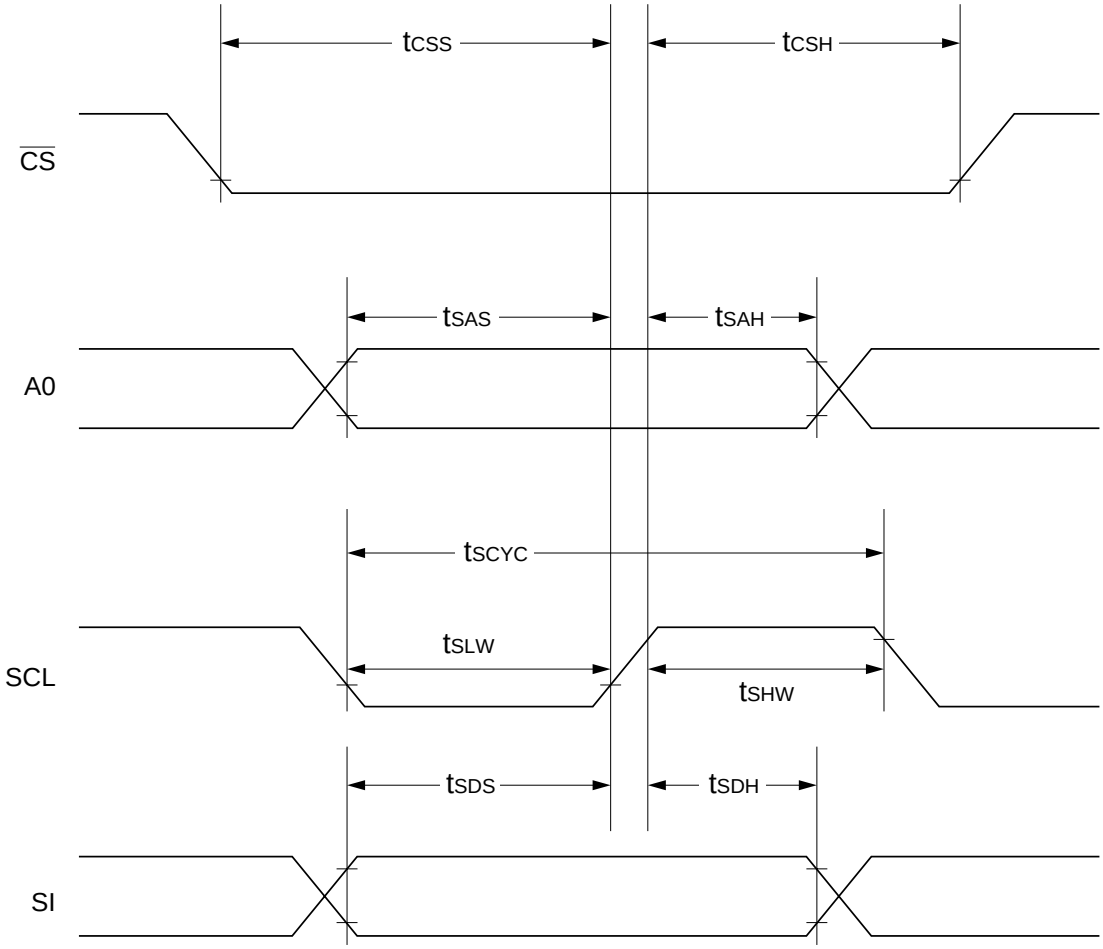


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, CS	t CYC6	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 to D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the CS active state. tCYC6 must be reserved after CS becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and CS, the same timing is not required. Input signals so that A0 and CS may satisfy tAW6 and tAH6 respectively.

(3) Serial Interface



[V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C]

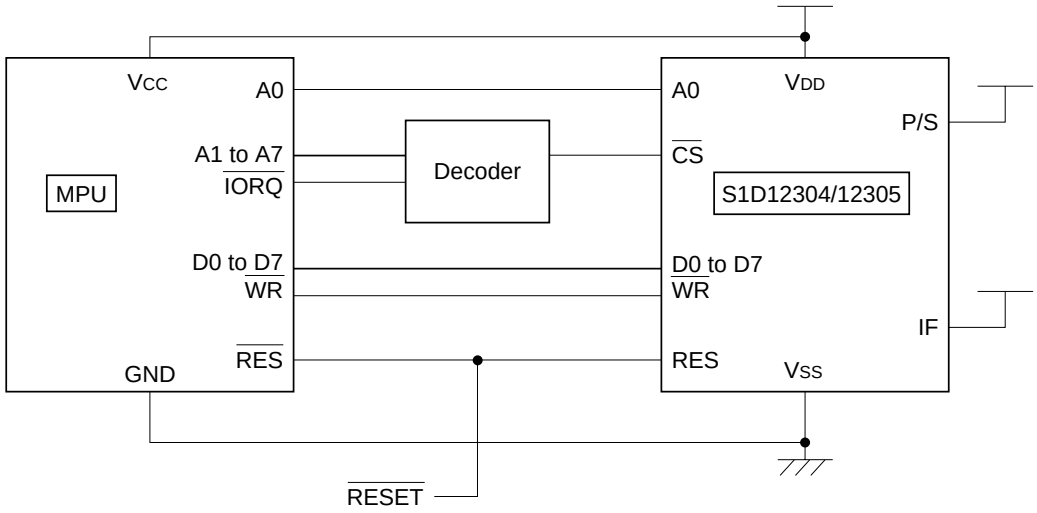
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}	V_{SS} = –3.0	700		ns
			–2.7	800		ns
			–2.4	1000		ns
SCL HIGH pulse width		t_{SHW}		300		ns
SCL LOW pulse width		t_{SLW}		300		ns
Address setup time	A0	t_{SAS}		50		ns
Address hold time		t_{SAH}	V_{SS} = –3.0	350		ns
			–2.7	400		ns
			–2.4	500		ns
Data setup time	SI	t_{SDS}		50		ns
Data hold time		t_{SDH}		50		ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		150		ns
		t_{CSH}	V_{SS} = –3.0	550		ns
			–2.7	650		ns
			–2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of V_{SS}.

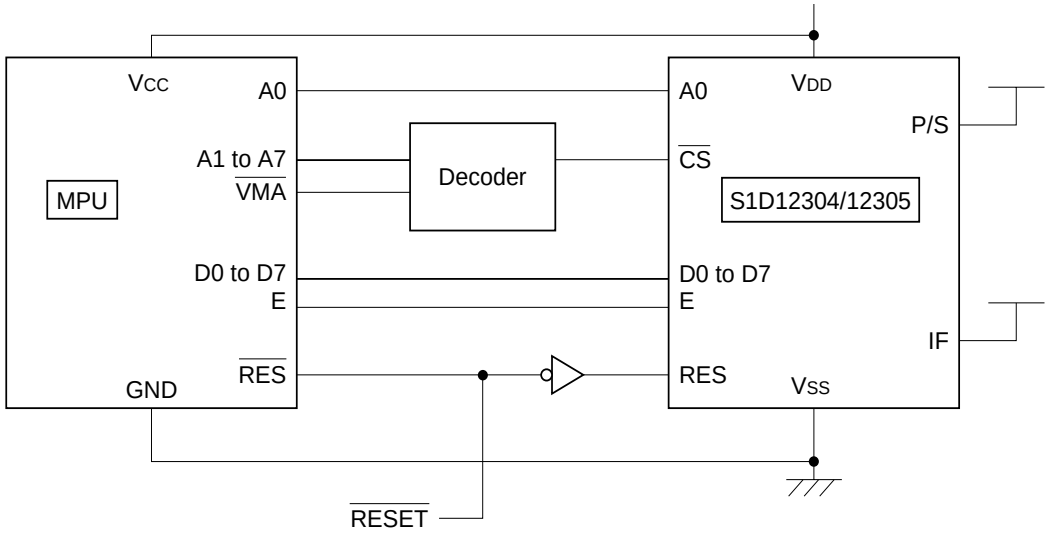
12. MPU INTERFACE (REFERENCE EXAMPLES)

The S1D12304/12305 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the S1D12304/12305 Series can be operated by less signal lines.

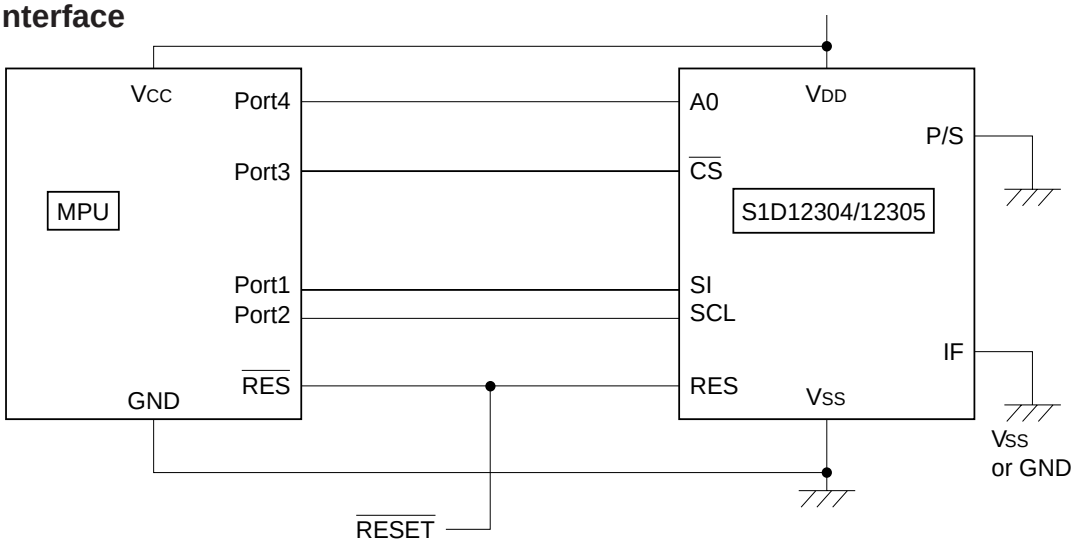
80 Series MPU



68 Series MPU

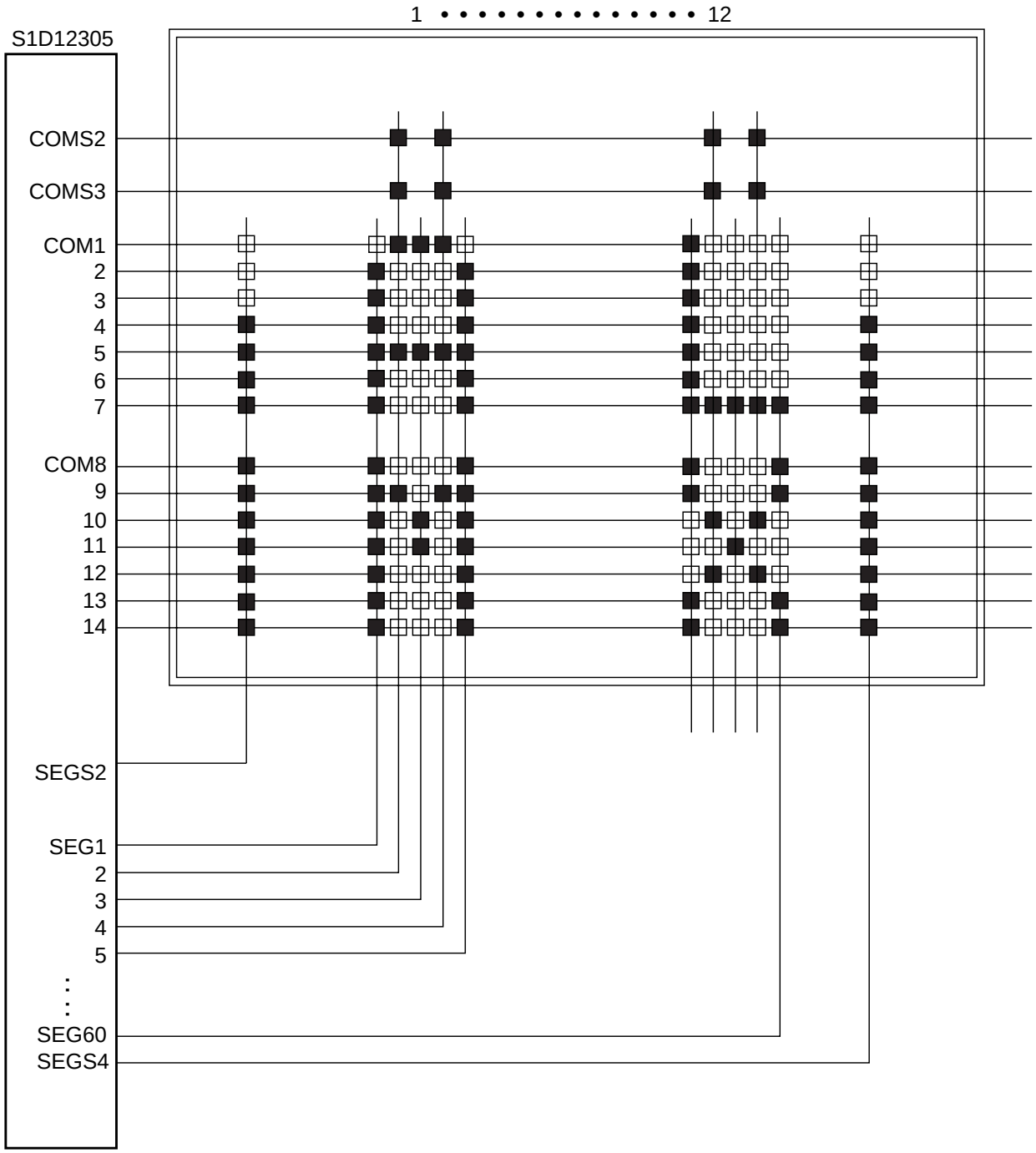


Serial Interface



13. INTERFACE TO LCD CELLS (REFERENCE)

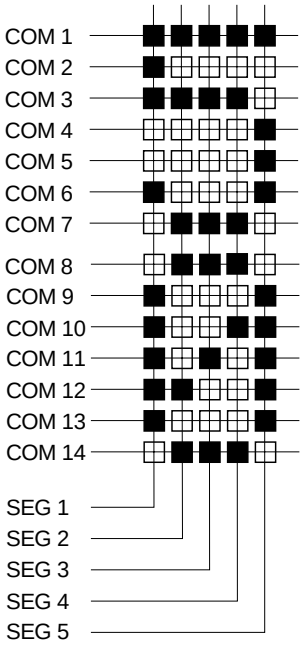
12 columns by 2 lines, 5×7-dot matrix segments and symbols

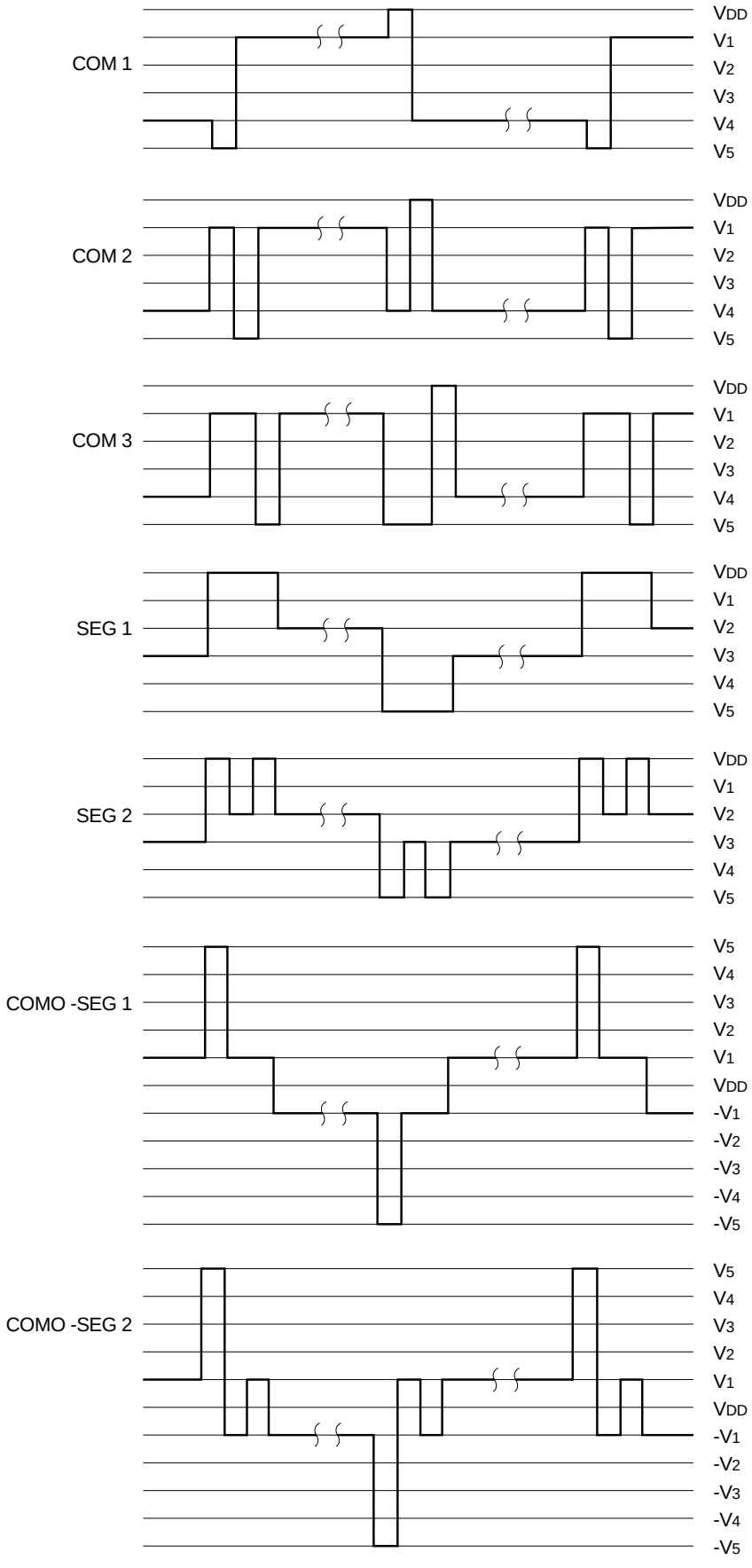


■ System Setup

N2	N1
0	0

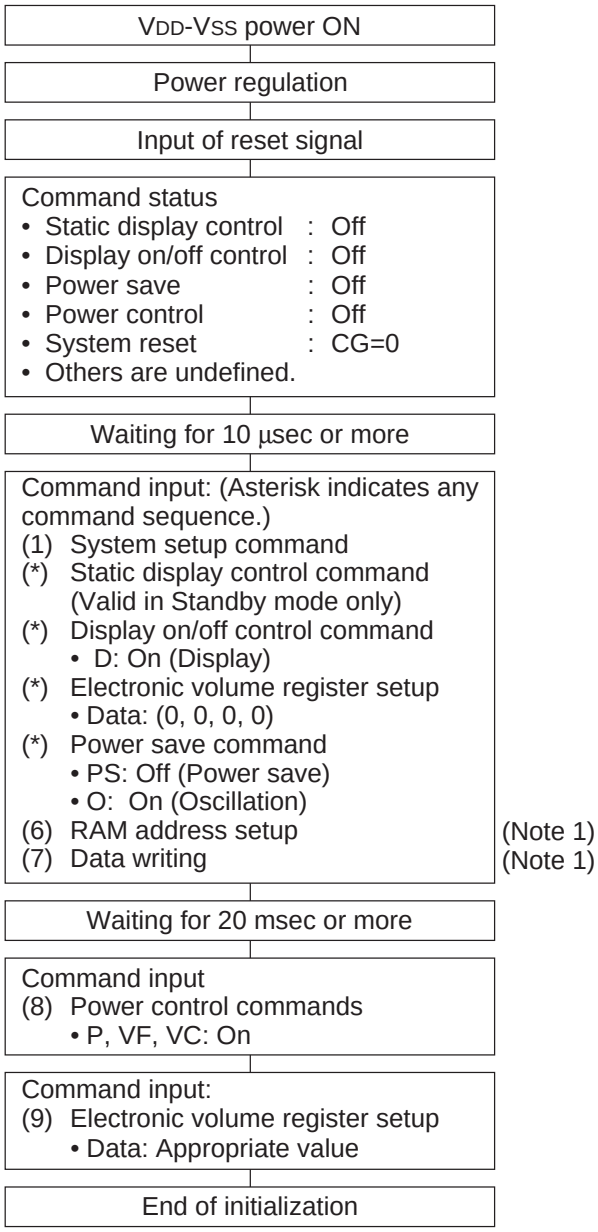
14. LCD DRIVE WAVEFORMS (B WAVEFORMS)



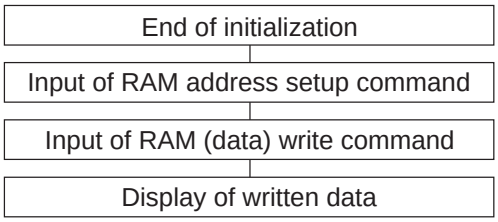


15. INSTRUCTION SETUP EXAMPLE (REFERENCE)

(1) Initial setup



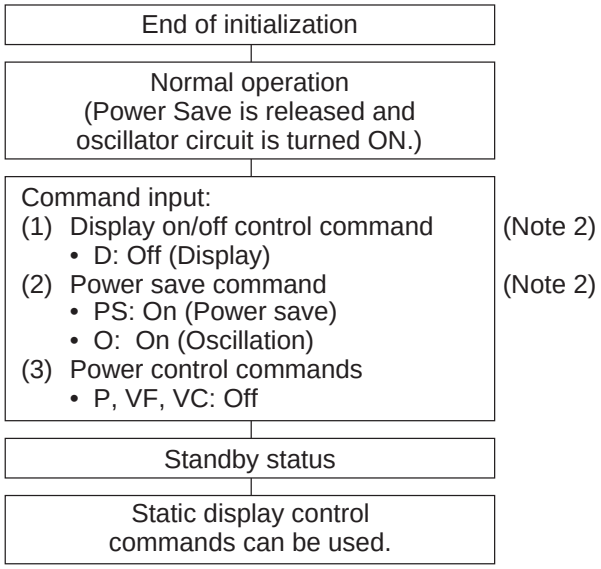
(2) Display mode



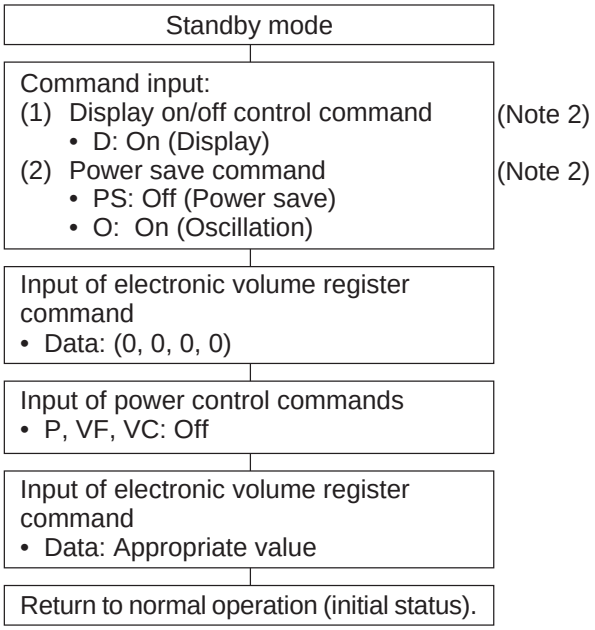
Note 1: Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

(3-1) Selecting the Standby mode

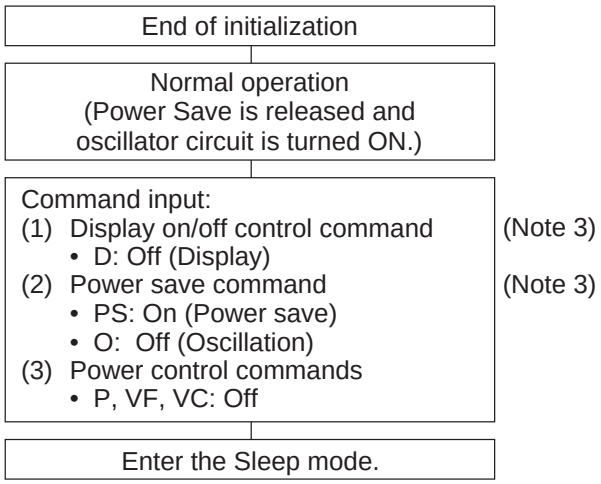


(3-2) Releasing the Standby mode

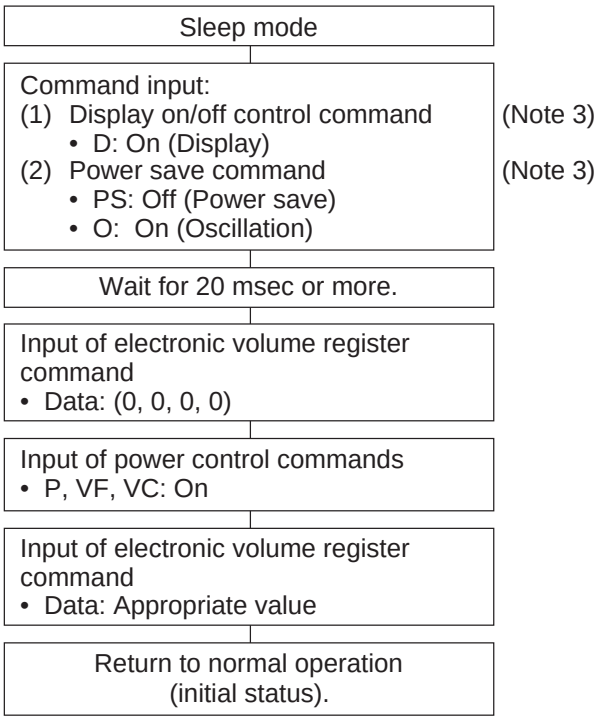


Note 2: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode



(4-2) Releasing the Sleep mode



Note 3: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

S1D12400 Series

Rev. 2.1

Contents

1. DESCRIPTION

The S1D12400 Series is a character display dot matrix LCD controller driver. This driver can display up to 64 characters and 6 user-defined characters, and up to 160 symbols according to the 4-bit, 8-bit or serial data which is sent from a microcomputer.
The built-in character generator ROM is provided with up to 544 types of character fonts having a structure of 5 × 8 dots. Up to 256 types can be continuously called by register option selection. This can cope with many different character fonts by uses and countries and permits a wider range of use. This driver incorporates a user-defined character RAM for 6 characters of 5 × 8 dots and can be used for the display of higher degree of freedom by means of a symbol register.
The driver can operate handy units at the minimum power consumption by using its merit of lower power consumption, standby mode, and sleep mode.

2. FEATURES

- Built-in display data RAM 80-character + 6-character user-defined characters + 160 symbols
- CGROM (for up to 544 characters), CGRAM (6 characters), symbol register (160 symbols)
- Display digits × Number of lines
  <Ordinary mode>
  ① (16 digits) × 4 lines + 160 symbols + 10 static irons (S1D12400)
  ② (16 digits) × 3 lines + 160 symbols + 10 static icons (S1D12401)
  ③ (16 digits) × 2 lines + 160 symbols + 10 static icons (S1D12402)
  <Standby mode>
  ① 10 static icons (S1D12400)
  ② 10 static icons (S1D12401)
  ③ 10 static icons (S1D12402)
- Vertical double-size display function
- Line vertical scroll function
- Line blink function
- Symbol blink function
- Built-in CR oscillating circuit (Built-in C, R)
- External clock input
- High-speed MPU interface
  Interface with both MPUs of 68 series/80 series
  Interface by 4 bits/8 bits
- Serial interface
- Character font 5 × 8 dots
- Duty ratio ① 1/34 (S1D12400)
  ② 1/26 (S1D12401)
  ③ 1/18 (S1D12402)
- Simple command setup
- Built-in liquid crystal drive power circuit
  The boosting circuit, voltage regulating circuit, voltage follower × 4, and resistor for power regulating circuit for bias select commands are incorporated.
- Built-in electronic volume function
- Lower power consumption

80 µA max	(at ordinary operation (during display): Including the internal power supply operating current)
500 µA max	(at ordinary operation (during access): fcyc = 200 KHz, including the internal power supply operating current)
20 µA max	(in standby mode: Oscillation ON, power OFF, static icon display)
5 µA max	(in sleep mode: oscillation OFF, power OFF, display OFF)

- Power supply:

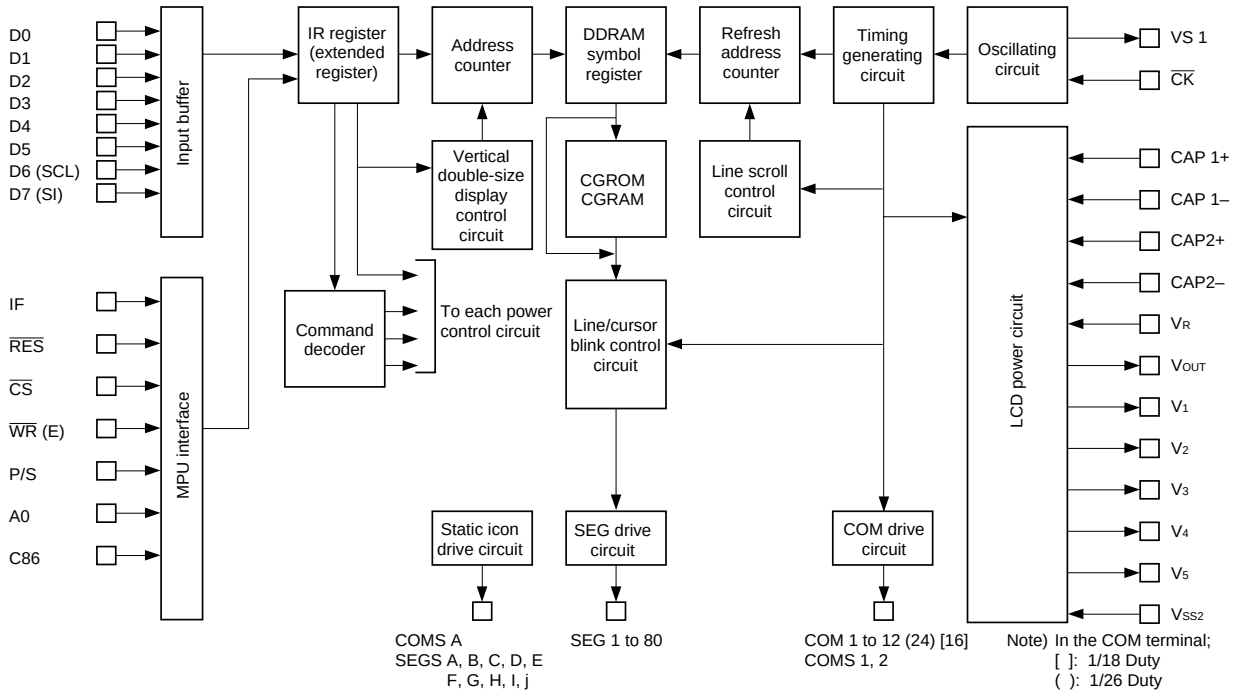
V_{DD} - V_{SS}	1.8 V to 5.5 V
V_{DD} - V_{SS2}	1.8 V to 5.5 V
V_{DD} - V_5	5.5 V to 16.0 V

- Wide operating temperature range
  Ta = –30 to +85°C
- CMOS process
- Pad pitch 90 µm Min
- Delivery form

Chip (gold bump product)	S1D124**D****
TCP	S1D124**T****

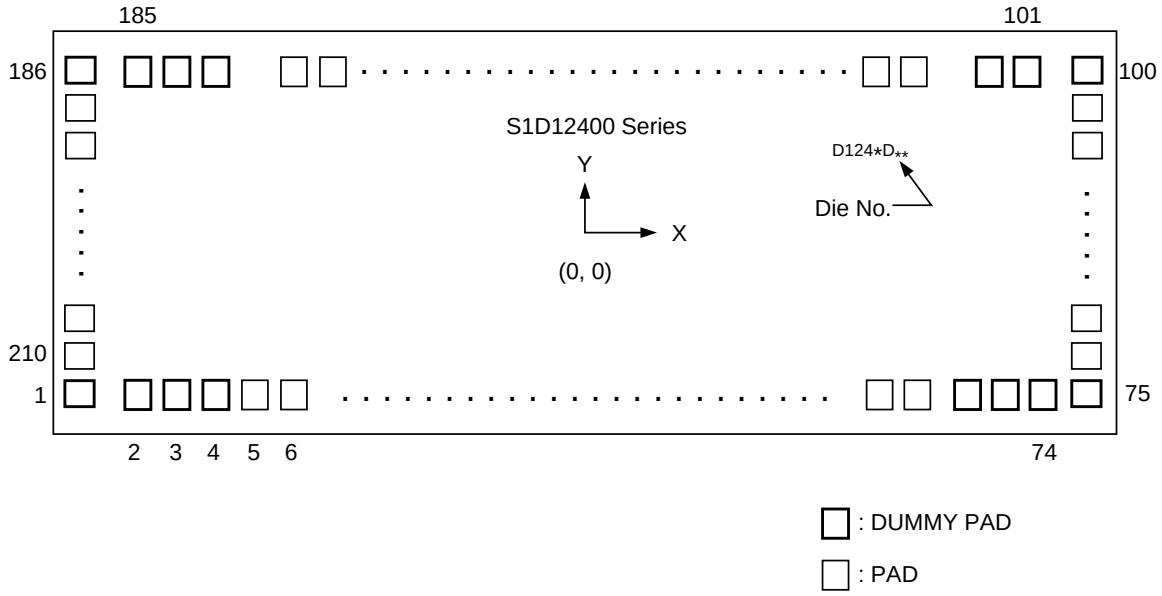
- This IC is not designed against radiation and strong light and noise.

3. BLOCK DIAGRAM



4. PAD

Pad Layout



S1D124✱✱✱✱✱✱✱

Digits for CGROM pattern change
Number of display line
00: 4-line display
01: 3-line display
02: 2-line display

Chip size: 8.70 × 2.80 mm
Pad pitch: 90 µm (Min.)
Chip thickness (reference value): 625 ± 50 µm (S1D124✱✱D✱✱✱✱)

Au bump specifications

Bump size	A TYPE	60.0 µm × 81.5 µm
	B TYPE	81.5 µm × 60.0 µm
	C TYPE	85.0 µm × 85.0 µm
	D TYPE	60.0 µm × 85.0 µm
Bump height (reference value)		22.5 µm ± 5.5 µm

(For bump types, refer to the pad coordinate diagram.)

Note: The board of this IC has V_{DD} potential. It is recommended to stabilize power supply by connecting the board to the V_{DD} potential at the time of mounting.

Pad Center Coordinate

<S1D12400****>

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	↓
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	↓

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	↓
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	↓
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]	↓	–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]	↓	1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	↓
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	↓

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	COM32 [B TYPE]		1041
189	COM31 [B TYPE]		951
190	COM30 [B TYPE]		861
191	COM29 [B TYPE]		772
192	COM28 [B TYPE]		682
193	COM27 [B TYPE]		592
194	COM26 [B TYPE]		503
195	COM25 [B TYPE]		413
196	COM24 [B TYPE]		323
197	COM23 [B TYPE]		234
198	COM22 [B TYPE]		144
199	COM21 [B TYPE]		54
200	COM20 [B TYPE]		–36
201	COM19 [B TYPE]		–125
202	COM18 [B TYPE]		–215
203	COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it is the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.

<S1D12401****>

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]		–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]		1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	*COM32 [B TYPE]		1041
189	*COM31 [B TYPE]		951
190	*COM30 [B TYPE]		861
191	*COM29 [B TYPE]		772
192	*COM28 [B TYPE]		682
193	*COM27 [B TYPE]		592
194	*COM26 [B TYPE]		503
195	*COM25 [B TYPE]		413
196	COM24 [B TYPE]		323
197	COM23 [B TYPE]		234
198	COM22 [B TYPE]		144
199	COM21 [B TYPE]		54
200	COM20 [B TYPE]		–36
201	COM19 [B TYPE]		–125
202	COM18 [B TYPE]		–215
203	COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.
*: Don't connect COM25 to COM32.

<S1D12402★★★★>

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]		–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]		1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	*COM32 [B TYPE]		1041
189	*COM31 [B TYPE]		951
190	*COM30 [B TYPE]		861
191	*COM29 [B TYPE]		772
192	*COM28 [B TYPE]		682
193	*COM27 [B TYPE]		592
194	*COM26 [B TYPE]		503
195	*COM25 [B TYPE]		413
196	*COM24 [B TYPE]		323
197	*COM23 [B TYPE]		234
198	*COM22 [B TYPE]		144
199	*COM21 [B TYPE]		54
200	*COM20 [B TYPE]		–36
201	*COM19 [B TYPE]		–125
202	*COM18 [B TYPE]		–215
203	*COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.
*: Don't connect COM17 to COM32.

5. PIN DESCRIPTION

Power Supply Pins

Pin name	I/O	Description	No. of Pins
Substrate potential		IC board is based on V_{DD} potential. To lock the board potential with V_{DD}.	
V_{DD}	Power supply	Connected to the logic power supply. This is used in common with the MPU power pin V_{CC}.	6
V_{SS}	Power supply	0 V power pin that is connected to system GND.	4
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined for the liquid crystal cell is applied by resistance-division or impedance conversion by operational amplifier. The potential is determined on V_{DD} and the following relations must be observed. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_5 \geq V_{OUT}$ $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to V1 to V4 by command selection. $V_1 = 1/5\ V_5$ (1/4 V_5) $V_2 = 2/5\ V_5$ (2/4 V_5) $V_3 = 3/5\ V_5$ (2/4 V_5) $V_4 = 4/5\ V_5$ (3/4 V_5)	6
V_{S1}	O	Supply voltage output pin for oscillating circuit. Don't connect a load to the outside.	1

LCD Power Circuit Pins

Pin name	I/O	Description	No. of Pins
CAP1+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP1– pin.	1
CAP1–	O	Boosting condenser negative side connecting pin. Condenser is connected with the CAP1+ pin.	1
CAP2+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP2– pin.	1
CAP2–	O	A boosting condenser negative side connecting pin. Condenser is connected with the CAP2+ pin.	1
V_{OUT}	O	Output pin for boosting. Smoothing condenser is connected with V_{DD}.	1
V_R	I	Voltage adjusting pin. Voltage between V_{DD} and V_5 is given by resistance-division.	1
V_{SS2}	I	Boosting power pin. The voltage between V_{DD} and V_{SS2} is boosted by a specified multiple.	1

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 to D0</td><td>I</td><td>8-bit input data bus which is connected to the 16-bit standard MPU data bus.
Pin D7 and pin D6 function as a serial data input and a serial clock input at P/S = LOW, respectively.
<table>
<tr><th>Pin / Mode</th><th>P/S</th><th>C86</th><th>IF</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3-D0</th><th>$\overline{CS}$</th><th>A0</th><th>$\overline{WR}$</th></tr>
<tr><td>Serial I/F</td><td>LOW</td><td>HIGH or LOW</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>68I/F 8bit</td><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>68I/F 4bit</td><td>HIGH</td><td>HIGH</td><td>LOW</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>80I/F 8bit</td><td>HIGH</td><td>LOW</td><td>HIGH</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>80I/F 4bit</td><td>HIGH</td><td>LOW</td><td>LOW</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
C86: An MPU selecting pin
OPEN: OPEN is allowable, but it is recommend to fix it to one of potentials as a matter of noise-resistance characteristic.
—:Either HIGH or LOW is allowable, but the potential should be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually used to distinguish data from a command to which the LSB of the MPU address bus is connected.
LOW : Indicates that D0 to D7 are of a command.
HIGH : Indicates that D0 to D7 are of data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset pin for initializing the whole IC. Be sure to input it once when the power supply is turned on. A reset operation is performed at the LOW level of the $\overline{RES}$ signal.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU selecting pin. Fix it to HIGH or LOW depending on the MPU to be used.
LOW : 80 series MPU interface
HIGH : 68 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip selecting pin. Usually, it inputs a signal that is obtained by decoding an address signal. Chip selection is enabled at the LOW level.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(E)</td><td>I</td><td><When the 80 series MPU is selected> Active LOW
A pin for connecting the WR signal of the 80 series MPU.
The signal on the data bus is latched at the rise of the $\overline{WR}$ signal.
<When the 68 series MPU is connected> Active HIGH
Becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>A pin for selecting either serial interface or parallel interface.
LOW : Serial interface
HIGH : Parallel interface</td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>A data bit length selecting pin at parallel interface.
HIGH : 8-bit parallel interface
LOW : 4-bit parallel interface
At P/S = LOW, set pins D3 to D0 to V_{DD} or V_{SS}, or OPEN.</td><td>1</td></tr>
<tr><td>$\overline{CK}$</td><td>I</td><td>An external clock input pin.
When using the internal oscillating circuit, fix it to HIGH.
When using an external clock input, the internal oscillating circuit must be turned off by command.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic Drive Pins [S1D12400]

Pin name	I/O	Description	No. of Pins
COM1 to COM32	O	Common signal output pins (for characters)	32
COMS1, COMS2	O	Common signal output pins (for others than characters) COMS1, COMS2: Symbol output command output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [S1D12401]

Pin name	I/O	Description	No. of Pins
COM1 to COM24	O	Common signal output pins (for characters)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [S1D12402]

Pin name	I/O	Description	No. of Pins
COM1 to COM16	O	Common signal output pins (for characters) (Keep COM17 to COM32 unconnected.)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Static Drive Pins

Pin name	I/O	Description	No. of Pins
COMSA	O	Common signal output pin (for static icons)	2
SEGS A to J	O	Segment signal output pins (for static icons)	10

Note: For the electrode of the liquid crystal display panel connected to the static drive terminal, it is recommended use the pattern separated from the electrode connected to the dynamic drive terminal. If this pattern is too close, the liquid crystal and electrode may be deteriorated.

6. FUNCTION DESCRIPTION

MPU Interfaces

In the S1D12400 series, an MPU type, interface bit length and interface method can be selected depending on pins IF, P/S and C86.

Selection of MPU

In the S1D12400 series, when parallel input is selected (P/S = HIGH), pin C86 has an MPU selecting function.
When either HIGH or LOW is selected as the polarity of pin C86, the 80 series MPU or 68 series MPU can be selected as shown in Table 1.
Selection of an interface bit length (8 bits, 4 bits) is performed by pin IF.

Table 1

MPU type	Pin C86 state	Polarity of $\overline{RES}$ function input	MPU connection			
			A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
68 series	HIGH level	LOW level active	A0	E	$\overline{CS}$	D0 to D7
80 series	LOW level		A0	$\overline{WR}$	$\overline{CS}$	D0 to D7

Selection of interface type

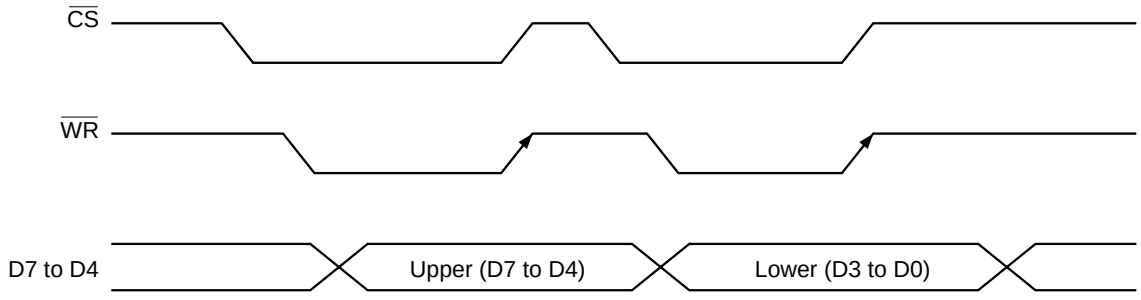
In the S1D12400 series, it is possible to select an 8-bit or 4-bit parallel interface or a serial interface that permits a data transfer through a serial input (SI). As the selecting method, set the polarity of pins of P/S and IF to HIGH or LOW.

Table 2

Interface type	Interface bit length	Selecting pin state		Pin state										
		P/S	IF	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	8 bits	HIGH	HIGH	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	4 bits	HIGH	LOW	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	OPEN or HIGH or LOW			
Serial	1 bit	LOW	HIGH or LOW	$\overline{CS}$	A0	HIGH or LOW	SI	SCL	OPEN or HIGH or LOW					

Interface with 4-bit MPU

When data is transferred by a 4-bit interface (IF = 0), 8-bit commands, data and addresses are divided into 2 parts for transfer. A timing example of the 80 series MPU is shown below.



Note: For continuous writing, perform it after securing a time exceeding the system cycle time (t_{cyc}).

Serial interface (P/S = LOW)

The serial interface consists of an 8-bit shift register and a 3-bit counter, and becomes ready to accept an SI input or SCL input in the chip selected state ($\overline{CS}$ = LOW).
Unless any chip is selected, the shift register and the counter are reset to the initial state. (Refresh state)
Data is input in the order of D7, D6, ... D0 from the serial data input pin (SI) at the rise of the serial clock (SCL). At the rising edge of the 8th serial clock, the data is converted into parallel data.
Whether the serial data input (SI) is display data or a command is identified and judged by A0 input. When A0 = HIGH, the data becomes display data. When A0 = LOW, the data becomes a command. The A0 input is read and identified at the rise of the 8 × nth serial clock (SCL) after chip selection.

Fig. 1 shows a timing chart of the serial interface. In case of the SCL signal, extreme care should be taken about terminal reflection and external noise due to a wiring length. Accordingly, it is recommended to make an operation check.
It is also recommended to periodically refresh the each command write state to prevent a malfunction from being caused by noise.

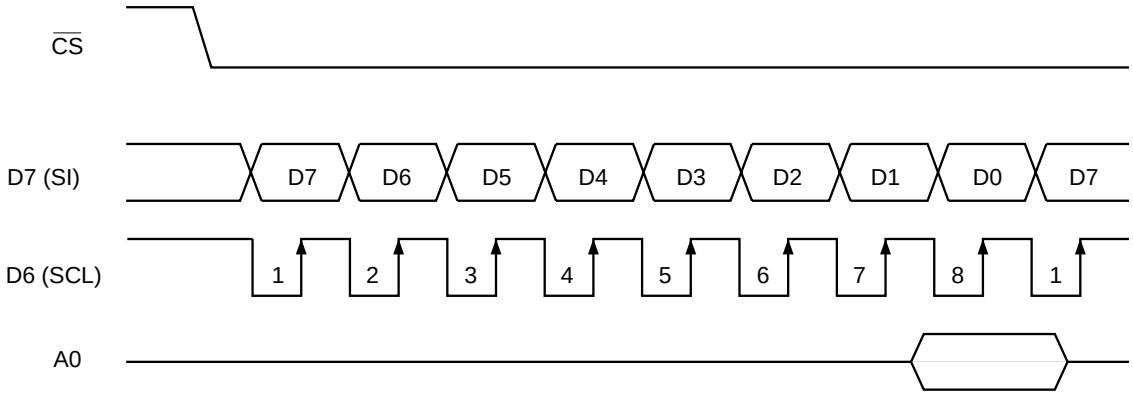


Fig. 1 Serial Interface Input Timing

Identification of data bus signals

The S1D12400 series identifies each data bus signal by a combination of A0 and $\overline{WR}$ (E) as shown in Table 3.

Table 3

Common	68 series	80 series	Function
A0	(E)	$\overline{WR}$	
1	1	0	Writes into the RAM and symbol register.
0	1	0	Writes into the internal register (commands)

Chip select

The S1D12400 series has chip select pin $\overline{CS}$. Only when $\overline{CS}$ = LOW, the MPU interface is enabled. In the other states than the chip select state, D0 to D7 and A0, $\overline{WR}$, SI, and SCL inputs are invalidated. When an serial input interface is selected, the shift register and the counter are reset. However, the $\overline{RES}$ input can be performed regardless of the $\overline{CS}$ state.

Power Circuit

The power circuit built in the S1D12400 series is a low power consumption power circuit that generates a voltage required for liquid crystal drive, and consists of a boosting circuit, voltage regulating circuit, and voltage follower.
The power circuit capacity is set for a small-scale liquid crystal panel.
In the case of a liquid crystal panel with a large display capacity, the display quality may be remarkably degraded. In this case, an external power supply is required.
Functional selection is performed by power control commands.
Some parts of the external power supply and the internal power supply can be used together.

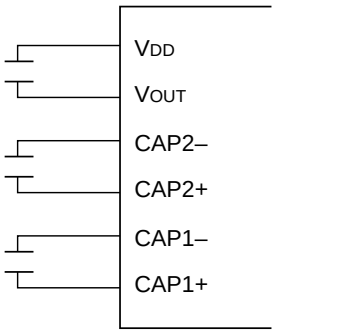
Table 4

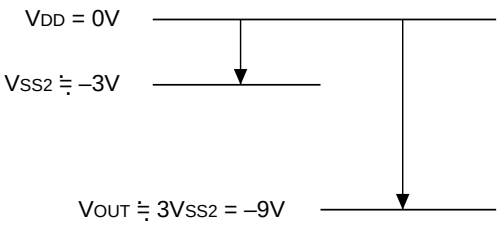
	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	V_{SS2}	USE
Note 1	×	○	○	V_{OUT}, V_{SS2}	OPEN
Note 2	×	×	○	V_5, V_{SS2}	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, set the boosting system pins (CAP1+, CAP1–, CAP2+, CAP2–) to OPEN so that liquid crystal drive voltages may be applied to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, set the V_{OUT} pin and the boosting system pins to OPEN and connect the V_5 pin to give liquid crystal drive voltages from the outside.
Note 3: When all the built-in power supplies are turned off, liquid crystal drive voltages V_1, V_2, V_3, V_4, and V_5 are supplied from the outside and set the CAP1+, CAP1–, V_{SS2} and V_{OUT} pins to OPEN.

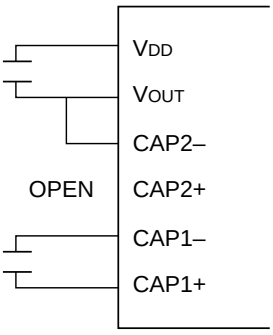
Boosting circuit

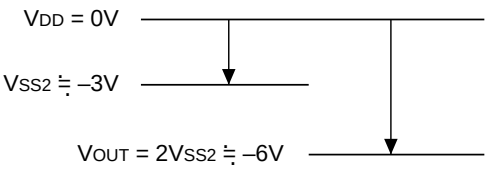
The S1D12400 series is provided with a boosting circuit for triple boosting and double boosting for the potential between V_{DD} and V_{SS2}.
For triple boosting, connect a capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, and between V_{DD} and V_{OUT}, and the V_{DD} - V_{SS2} potential is triple-boosted to the negative side and output to the V_{OUT} pin.
For double boosting, connect a capacitor between CAP1+ and CAP1– and between V_{DD} and V_{OUT}, set CAP2+ to OPEN, and connect CAP2– to V_{OUT}, and the V_{DD} - V_{SS2} potential is double-boosted to the negative side and output to the V_{OUT} pin.
Because the boosting circuit uses signals from the oscillator output, the internal oscillating circuit or the external clock must be in operation.
The relation of boosting voltages is shown below.
Set the potential between the V_{DD} and V_{SS2} to ensure that the V_{OUT} does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} (V_5) when double or triple boosted.





Potential relation of triple boosting voltages





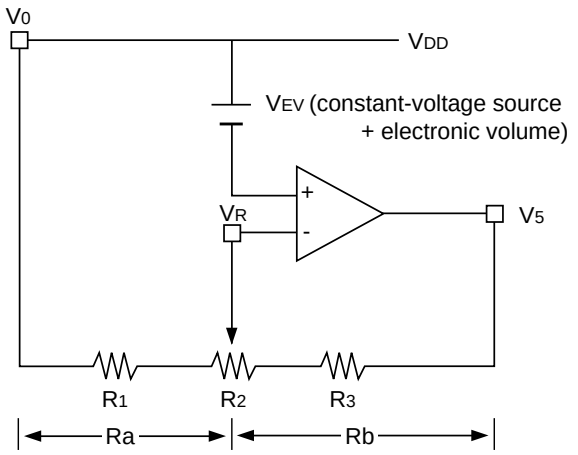
Potential relation of double boosting voltages

* Set the V_{SS2} voltage range to ensure that V_{OUT} terminal voltage does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} and absolute maximum rating.

Voltage regulating circuit

The boosting voltage generated at V_{OUT} is output as a liquid crystal drive voltage of V_5 through the voltage regulating circuit.
The S1D12400 series is provided with a high-precision constant-voltage source, a 32-step electronic volume function, and a V_5 voltage regulating resistor. This permits constructing a high-precision voltage regulating circuit with a small quantity of parts. The voltage regulating circuit outputs V_{EV} and has a temperature gradient of about –0.05%.
As the V_5 voltage regulating resistor, a built-in resistor or an external resistor can be selected by command as a matter of configuration.

[When using an external resistor (No use of V_5 voltage regulating built-in resistor is set by command.)]
The V_5 voltage can be obtained from the following expression ① by adjusting resistors Ra and Rb within the range of $|V_5| < |V_{OUT}|$.



$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

In this case, V_{EV} is determined by the constant-voltage source in the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq$ 2.0 V, being constant.
For voltage adjustment of V_5 output, connect a variable resistor among V_R, V_{DD}, and V_5. For fine voltage adjustment of V_5 output, it is recommended to combine fixed resistors R1 and R3 with variable resistor R2.

[R1, R2 and R3 setup example]

- R1 + R2 + R3 = 1.2 MΩ (Determined by the current value I_{05} flowing between V_{DD} and V_5. Supposing $I_{05} \leq 5$ μA)
- Minimum voltage of V_5: –6 V (Determined by liquid crystal characteristic)
- Variable voltage range by R2: –4 to –6 V (Determined by the liquid crystal characteristic)
- When the electronic volume register is set to (0, 0, 0, 0, 0), V_{EV} = 2.0 V (TYP). Accordingly, each resistor value can be calculated by the above conditions and expression ① as follows.

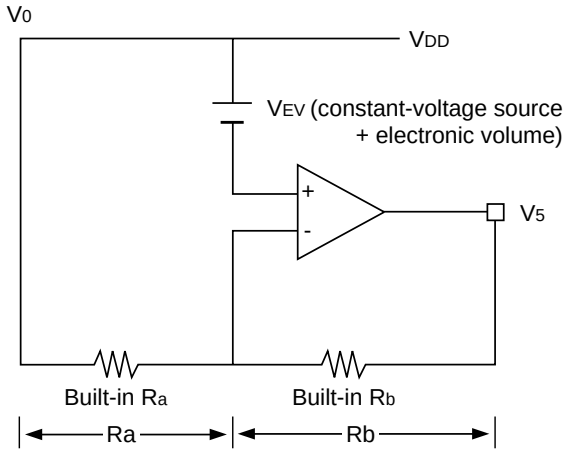
R1 = 400 KΩ
R2 = 200 KΩ
R3 = 600 KΩ

Note 1: The input impedance of the V_R pin is high, so it is necessary to take a proper measure against noise for short wiring and shielding wiring.

[When using the V_5 voltage regulating built-in resistor (Use of V_5 voltage regulating built-in resistor is set by command.)]
When the V_5 voltage regulating built-in resistor and the electronic volume function are used, the liquid crystal supply voltage V_5 can be controlled and the density of liquid crystal display can be controlled by commands only without adding any external resistor.
The V_5 voltage can be obtained by the following expression ② by adjusting resistors Ra and Rb within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots ②$$

In this case, V_{EV} is determined by the constant-voltage source within the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq 2.0$ V, being constant.



The voltage range of the V_5 output can be adjusted by changing the built-in resistor ratio (1 + Rb/Ra) by command. Reference values are shown in Table 5 and Fig. 2.

Table 5 V_5 voltage regulating built-in resistor ratio set values (reference values)

Command		(1 + Rb/Ra)
IR1	IR0	
0	0	2.81
0	1	3.27
1	0	3.72
1	1	4.21

S1D12400 Series

V5 voltage by V5 voltage regulating built-in resistor ratio set value and electronic volume resistor value (reference value)
[Fig. 2]

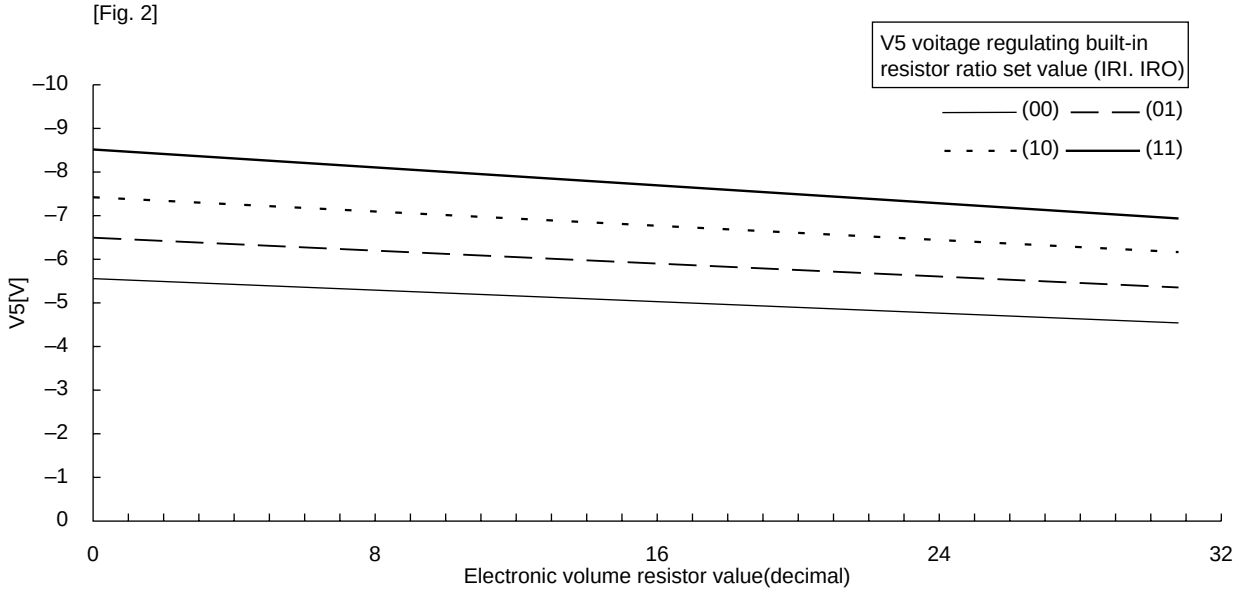
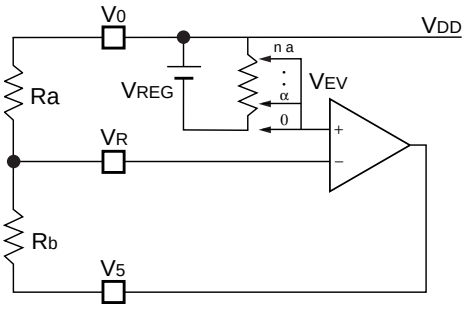


Fig. 2

- Voltage regulating circuit using the electronic volume function
  When the electronic volume function is used, the liquid crystal drive voltage V_5 can be controlled by the command to adjust the density of liquid crystal display. Regarding this method, set 5-bit data in the electronic volume register, and the liquid crystal drive voltage V_5 can take one of 32 states of voltage value.
  When the electronic volume function is used, the voltage regulating circuit must be turned on by the power control command.

[Constant setup example when using the electronic volume function]



$$V_5 = (1 + \frac{R_b}{R_a}) \times V_{EV}$$

However: $V_{EV} = V_{REG} - \alpha$

$\alpha = V_{REG} / 150$

Table 6

No.	Electronic volume register	α	V5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

When the electronic volume function is not used, set the electronic volume register to (0,0,0,0,0).

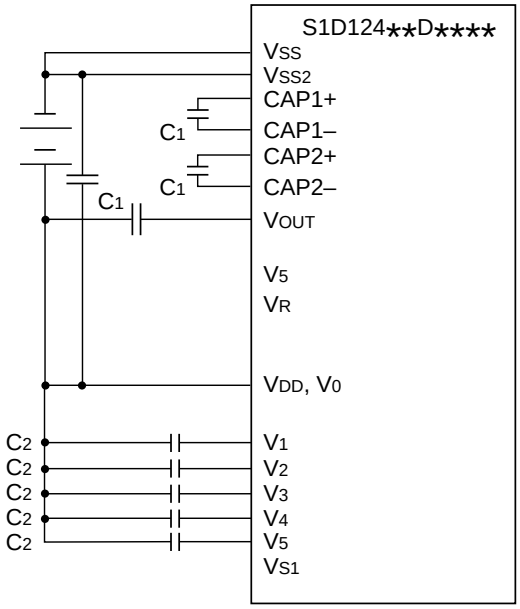
Liquid crystal voltage generating circuit

The V_5 potential is resistance-divided by the built-in resistor of the IC or external resistors Ra and Rb, generating potentials V_1, V_2, V_3, and V_4 required for liquid crystal drive. Furthermore, potentials V_1, V_2, V_3, and V_4 are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

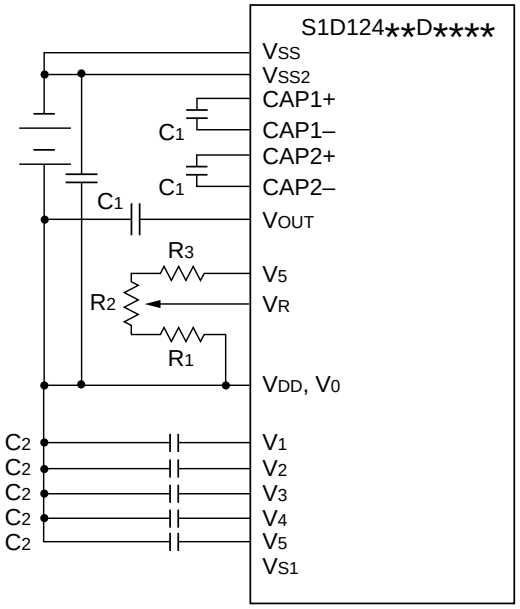
Regarding the liquid crystal drive voltage, the 1/5 bias or 1/4 bias can be selected by command. For liquid crystal power pins, capacitors C2 for voltage stabilization must be connected to pins V_1 to V_5 externally.
A reference circuit example of each case is shown below.

① Using all of the boosting circuit, power regulating circuit, and voltage follower

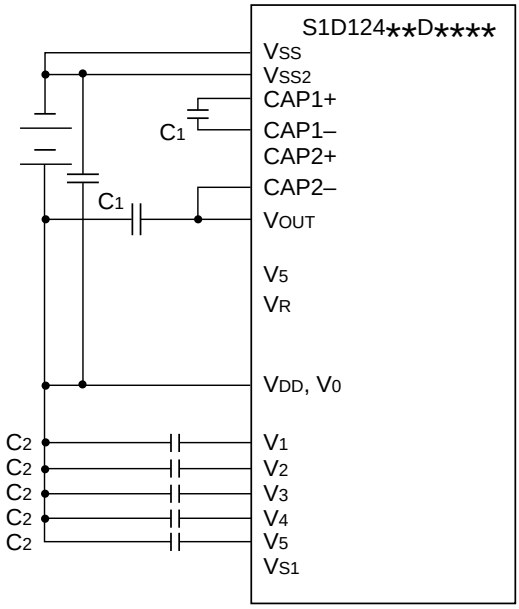
[When using a V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



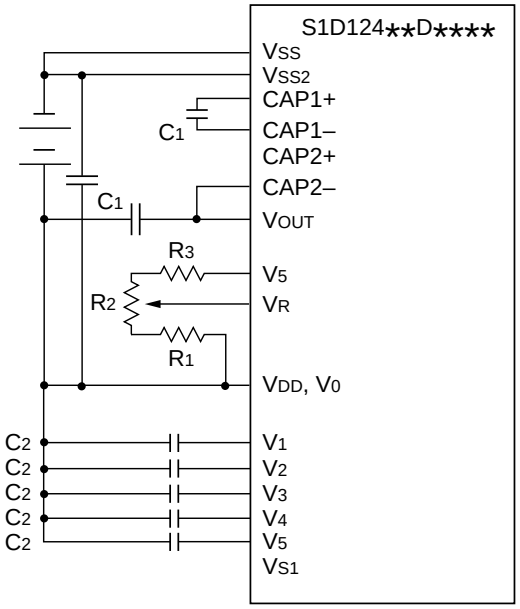
[When using no V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



(Example of V_{SS2} = V_{SS}, double boosting)



(Example of V_{SS2} = V_{SS}, double boosting)

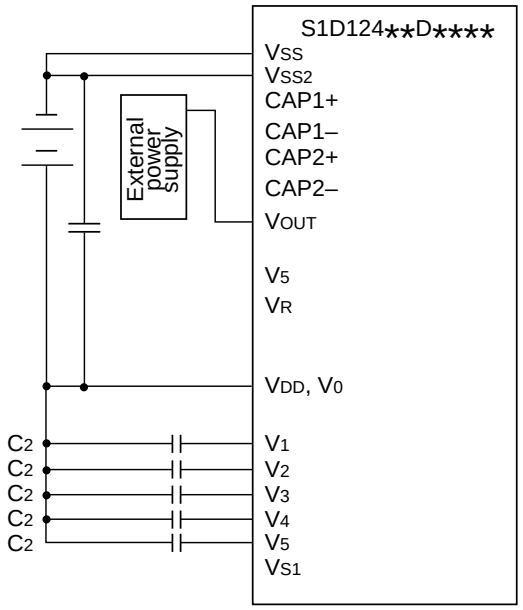


Reference set values: C_1: 0.47 to 4.7 µF
C_2: 0.1 to 4.7 µF

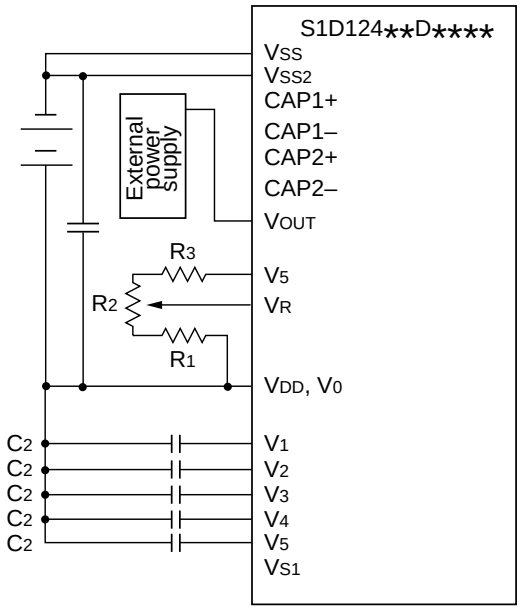
It is recommended to set optimum values suitable for the panel size in capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

② Using only the voltage regulating circuit and the voltage follower.

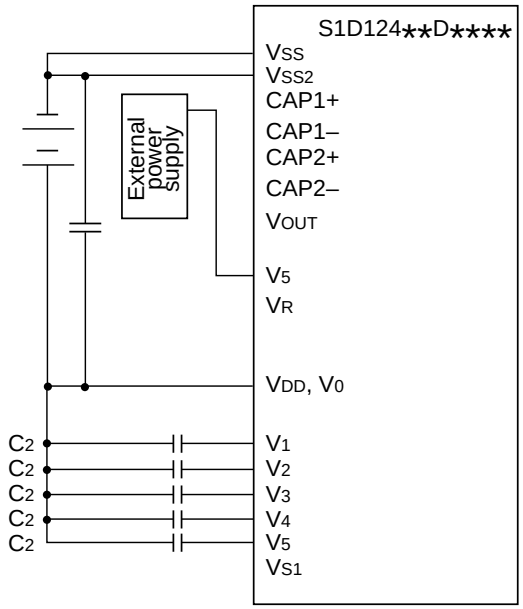
[When using a V_5 voltage regulating built-in resistor]
(Example of $V_{SS2} = V_{SS}$)



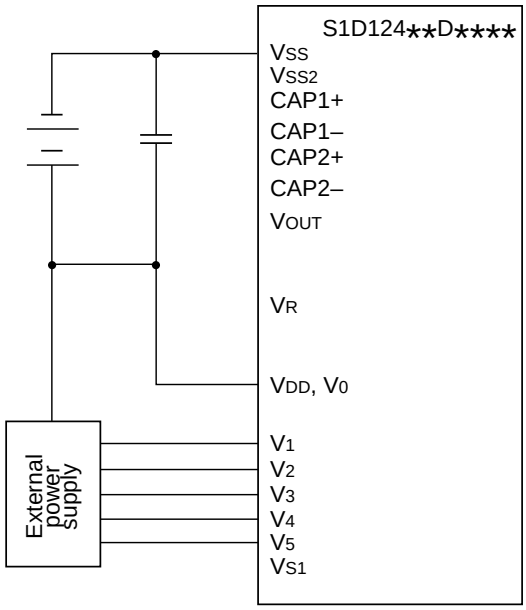
[When using no V_5 voltage regulating built-in resistor]
(Example of $V_{SS2} = V_{SS}$)



(Example of $V_{SS2} = V_{SS}$)



(Example of $V_{SS2} = V_{SS}$)



Reference set values: C_1: 0.47 to 4.7 µF It is recommended to set optimum values suitable for the panel size in
C_2: 0.1 to 4.7 µF capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

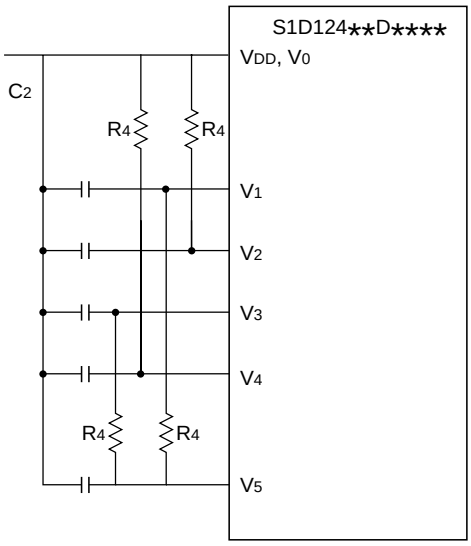
*1 Because the input impedance of the V_R pin is high, use a short wire and a shielding wire.

*2 Determine C_1 and C_2 values depending on the size of the LCD panel to be driven. Set proper values that permit stabilizing the liquid crystal drive voltages.

[Setting example]
- Turn on the voltage regulating circuit and the voltage follower and give a voltage to V_{OUT} from the outside.
- Display a LCD heavy load pattern like horizontal stripes and determine a C_2 value so that the liquid crystal drive voltages (V_1 to V_5) may be stabilized. However, it is necessary to set the same capacity value in C_2 in every case.
- Next, turn on the built-in power supply and determine a C_1 value.

*3 Connect a capacity between V_{DD} and V_{SS} for voltage stabilization.

When driving a liquid crystal panel with heavy alternating or direct current load using an internal power supply circuit, we recommend that you connect an external resistance in order to stabilize the level of the internal voltage follower outputs V_1, V_2, V_3 and V_4.



Reference setting value: R_4: 100 k ohm to 1 M ohm

For resistance value R_4, we recommend that you set it to an optimum value according to the liquid crystal panel indication and the drive waveform.

High power mode

The power circuit built-in the S1D12400 series is a LOW power consumption type. (when the high power mode is OFF)
Accordingly, in the case of a large load liquid crystal or panel, the display quality may be degraded. In this case, the display quality can be improved by entering HPM = '1' by command. Before determining whether or not to use this mode, it is recommended to make a display check with a real machine.
In case the display quality cannot be improved satisfactorily though the high power mode is set, a liquid crystal drive power must be supplied from the outside.

Low Power Consumption Mode

The S1D12400 series is provided with the standby mode/ sleep mode to attain LOW power consumption in the standby status of the unit.

● Standby mode
The standby mode is turned on and off by the power save command and display off/booster circuit off command. Only static icons can be displayed.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be caused to come on by static drive.
   Control the static icon display by SEGSA, B, C, D, E, F, G, H, I, J, COMSA by the static icon RAM.
2. Contents of DDRAM, CGRAM, and symbol register
   The written contents are kept in memory regardless of the ON/OFF status of the standby mode.
3. The operation mode remains in the status provided before execution of the standby mode. The internal circuit for dynamic display output is stopped.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

● Sleep mode
Turn off the power circuit and the oscillating circuit, set '0' in all the data of the static icon register, and execute the power save command.
Then, the sleep mode is set and the current consumption can be reduced to a value close to the static current.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80, SEGS1, 2, 4, 5: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Set '0' in all the data of the static icon register and blink ON/ OFF (for static icons).
2. Contents of SSRAM, CGRAM and symbol register
   The written contents can be kept in memory regardless of the ON/OFF status of the sleep mode.
3. The operation mode remains in the status provided before execution of the sleep mode. All the internal circuits are stopped.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by the power save command and the power control command.

* Caution: If the oscillating circuit is stopped with the static icon register data and blinking kept off, previous display will remain on the icon. To avoid this, be sure to turn off the data and blinking before stopping the oscillating circuit.

Reset Circuit

When the $\overline{RES}$ input becomes active, this LSI will be put into the initial setup status. Resetting is performed at the LOW level of the $\overline{RES}$ input signal.

● Initial setup status

1. Line scroll register
   LS1, 0 = 0 : Scroll amount 0 line
2. Line blink control

LB4 = 0 : DDRAM line 4 blink OFF
LB3 = 0 : DDRAM line 3 blink OFF
LB2 = 0 : DDRAM line 2 blink OFF
LB1 = 0 : DDRAM line 1 blink OFF

3. Vertical double-size display register
   DD4 = 0 : Line 4 is displayed in standard form.
   DD3 = 0 : Line 3 is displayed in standard form.
   DD2 = 0 : Line 2 is displayed in standard form.
   DD1 = 0 : Line 1 is displayed in standard form.
4. Display ON/OFF register
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   D = 0 : Display OFF
   RE = 0 : Extended register OFF
5. Power save register
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
6. Power control register
   HPM = 0 : High power mode OFF
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
   IRS = 1 : For built-in resistor
   BAS = 0 : 1/5 bias
   IR1,0 = 00 : Rb/Ra = small
7. System set register
   CG = 0 : CGRAM not used
   CS = 0 : Left shift
   SS = 0 : Normal display
   R1, 0 = 0 : Standard ROM + OPTION ROM1
8. Electronic volume
   (0,0,0,0,0)
9. Static icon ON/OFF control
   (SEGSA, B, C, D, E, F, G, H, I, J) =
   (0,0,0,0,0,0,0,0,0,0): Display OFF
10. Static icon blink control
    (SEGSA, B, C, D, E, F, G, H, I, J) =
    (0,0,0,0,0,0,0,0,0,0): Blink OFF

As seen in MPU Interface, the $\overline{RES}$ pin inputs data at the same timing as MPU resetting and performs initialization concurrently with the MPU. However, if this pin is put into the high impedance for a certain period after the MPU bus and ports are reset, perform a reset input after the input to the S1D12400 series is definitively set.

For the reset signal, it is necessary to input '0' level pulses at least for 10 µs as described in DC Characteristics. The ordinary operation will be started in 1 µs or more after the rising edge of the $\overline{RES}$ signal. When the $\overline{RES}$ pin becomes active, each register will be cleared and set to the above setup status.

If initialization is not executed by the $\overline{RES}$ pin when the supply voltage is applied, a clear disable status may appear.

In case the built-in liquid crystal power circuit is not used, the $\overline{RES}$ input must be active when the external liquid crystal power supply is turned on.

7. COMMANDS

Table 7 shows a command table. The S1D12400 series identifies each data/command by a combination of A0 and $\overline{WR}$ (E).
An extended command can be selected by the RE bit in the command.
Interpreting and executing commands are performed only at the internal timing. This permits high-speed processing.

Overview of Commands

Table 7

Command type	Command name	RE	A0	$\overline{WR}$
Display control instructions	Cursor Home	0	0	0
	Display ON/OFF Control	0/1	0	0
	Line Blink Control	0	0	0
	Line Scroll Control	1	0	0
	Static Icon Display Control	0	1	0
	Static Icon Display Blink Control	0	1	0
	Vertical Double-size Display Control	1	0	0
Power control	Power Save	0/1	0	0
	Power Control (1)	0	0	0
	Power Control (2)	1	0	0
	Electronic Volume Control	0	1	0
System set	System Set (1)	0	0	0
	System Set (2)	1	0	0
Address control instructions	DDRAM, Symbol Register	0	0	0
	CGRAM	1	0	0
Data input instruction	Data Write	0/1	1	0

The execution time of each instruction is determined by the internal processing time of the S1D12400 series. Accordingly, for executing an instruction, secure a time exceeding the cycle time (tcyc) and then execute the instruction.

Table 8 S1D12400 Series Command Table

Command	Code											Function
	RE	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home/ Line Scroll Control	0	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position. (Set the address to 30H.)
	1	0	0	0	0	0	1	*	*	LS1	LS0	Specifies the number of display scrolls in units of line.
(2) Line Blink/ Vertical Double-size Display Control	0	0	0	0	0	1	0	LB4	LB3	LB2	LB1	Exerts blink control for each specified line. LB4 = 1 (Blinks the display for line 4 of DDRAM in black-and-white reverse form.) LB4 = 0 (Does not blink the display for line 4 of DDRAM.) LB3 = 1 (Blinks the display for line 3 of DDRAM in black-and-white reverse form.) LB3 = 0 (Does not blink the display for line 3 of DDRAM.) LB2 = 1 (Blinks the display for line 2 of DDRAM in black-and-white-reverse form.) LB2 = 0 (Does not blink the display for line 2 of DDRAM.) LB1 = 1 (Blinks the display for line 1 of DDRAM in black-and-white reverse form.) LB1 = 0 (Does not blink the display for line 1 of DDRAM.)
	1	0	0	0	0	1	0	DD4	DD3	DD2	DD1	Displays the specified DDRAM line in vertical double-size form. DD4 = 1 (Displays the data for line 4 of DDRAM in vertical double-size form.) DD4 = 0 (Displays the data for line 4 of DDRAM in standard form.) DD3 = 1 (Displays the data for line 3 of DDRAM in vertical double-size form.) DD3 = 0 (Displays the data for line 3 of DDRAM in standard form.) DD2 = 1 (Displays the data for line 2 of DDRAM in vertical double-size form.) DD2 = 0 (Displays the data for line 2 of DDRAM in standard form.) DD1 = 1 (Displays the data for line 1 of DDRAM in vertical double-size form.) DD1 = 0 (Displays the data for line 1 of DDRAM in standard form.)

LS1	LS0	Function
0	0	Scroll amount 0 line
0	1	One-line upward scroll
1	0	Two-line upward scroll
1	1	Three-line upward scroll

Command	Code											Function
	RE	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(3) Display ON/OFF/ Extended Register ON/OFF Control	0/1	0	0	0	0	1	1	C	B	RE	D	Sets cursor ON/OFF, cursor blink ON/OFF (B), display ON/OFF (D), use/no-use of extended register (RE), and electronic volume LBS (RE). C= 1 (cursor ON) C = 0 (cursor OFF) B = 1 (blink ON) B = 0 (blink OFF) D = 1 (display ON) D = 0 (display OFF) RE = 1 (extended register ON) RE = 0 (extended register OFF)
(4) Power Save Control	0/1	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (O). PS = 1 (power save ON) PS = 0 (power save OFF) O = 1 (oscillation ON) O = 0 (oscillation OFF)
(5) Power Control	0	0	0	0	1	0	1	HPM	VC	VF	P	Sets high power mode ON/OFF (HPM), voltage regulating circuit ON/OFF (VC), voltage follower ON/OFF (VF), and boosting circuit ON/OFF (P). HPM = 1 (high power mode ON) HPM = 0 (high power mode OFF) VC = 1 (voltage regulating circuit ON) VC = 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) VF = 0 (voltage follower OFF) P = 1 (boosting circuit ON) P = 0 (boosting circuit OFF)
	1	0	0	0	1	0	1	IRS	BAS	IR1	IR0	Sets V_5 voltage regulating resistor selection (IRS), LCD bias set (BAS), and V_5 voltage regulating built-in resistor ratio set (IR1, IR0). IRS = 1 (use of built-in resistor) IRS = 0 (no use of built-in resistor) BAS = 1 (1/4 bias) BAS = 0 (1/5 bias) (IR1, IR0) = (11, 10, 01, 00) ... (Rb/Ra ratio large to small)
(6) System Set	0	0	0	0	1	1	0	R1	R0	CS	CG	Sets ROM option (R1, R0), use/no use of CGRAM (CG), and COM shift direction (CS) CG = 1 (use of CGRAM) CG = 0 (no use of CGRAM) CS = 1 (right shift) CS = 0 (left shift) R1 / R0 / Function 0 / 0 / Standard ROM + OPTION ROM1 0 / 1 / Standard ROM + OPTION ROM2 1 / 0 / Standard ROM + OPTION ROM3 1 / 1 / Standard ROM + OPTION ROM4
	1	0	0	0	1	1	0	*	*	SS	*	Sets the normal/reverse display (SS) of each segment character. SS = 1 (reverse) SS = 0 (normal)
(7) RAM Address Set	0	0	0	1	ADDRESS							Sets the address of DDRAM, static icon RAM or electronic volume RAM.
	1	0	0	1	ADDRESS							Sets the address of CGRAM or symbol register RAM.

Command	Code											Function
	RE	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(8) RAM Data Write	0/1	1	0	DATA								Writes data into the DDRAM, CGRAM, symbol register RAM, static icon RAM or electronic volume RAM. This is determined by the address set instruction executed immediately before writing data.
(9) NOP	0/1	0	0	0	0	0	0	0	0	0	0	A command for NON-OPERATION. This also serves as a test mode clear command, so it is recommended to input it periodically.
(10) Test Mode	0/1	0	0	0	0	0	0	*	*	*	*	A command for IC chip test. Don't use this command.

Description of Command Functions

Cursor home

Function: Presets the address counter to 30H. Only when the previous RAM access is made to the area of RE = 0 of the RAM map, the cursor is moved to digit 1 on line 1 if the cursor is displayed.
If line scroll is set, it is cleared to the scroll amount = 0 line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	*	*	*	*

*: Don't Care

Line scroll control

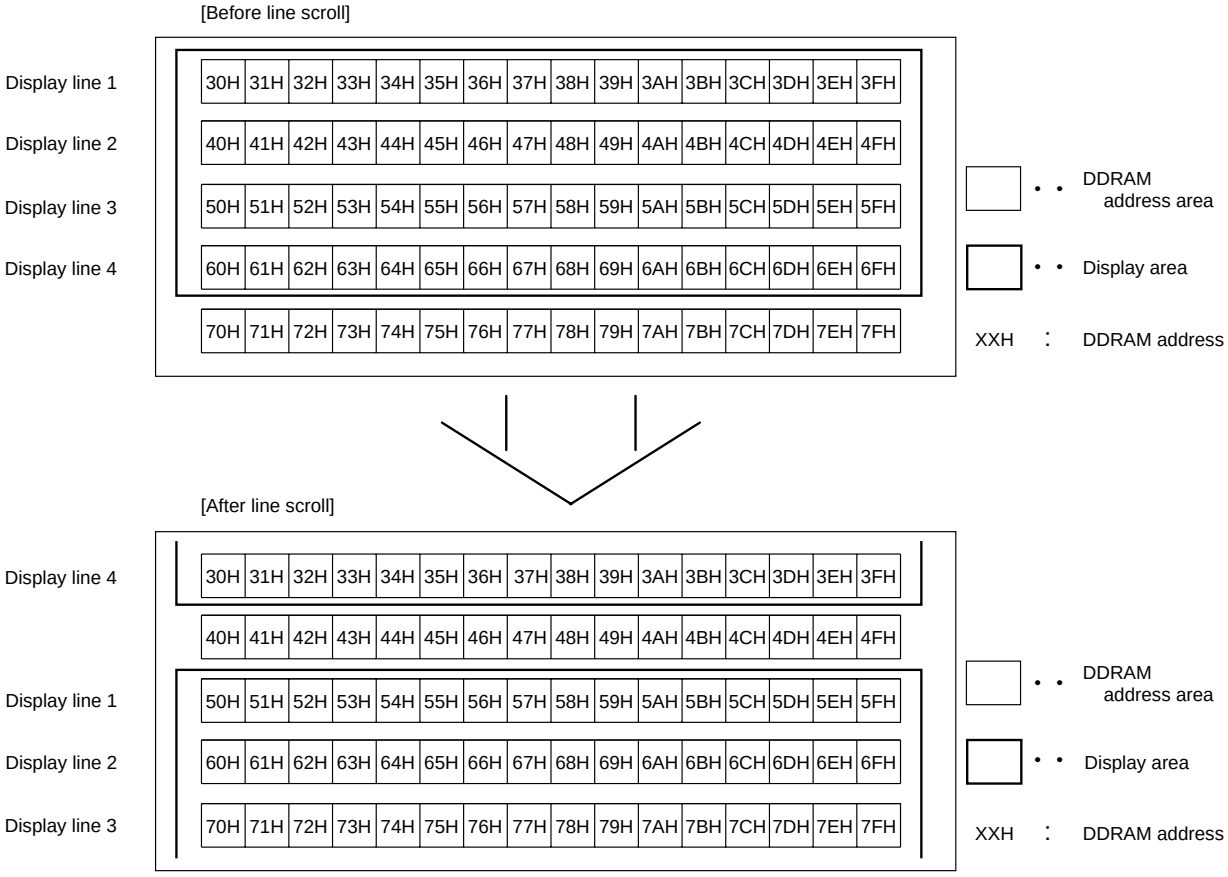
Function: Controls the display scroll amount for each line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	*	*	LS1	LS0

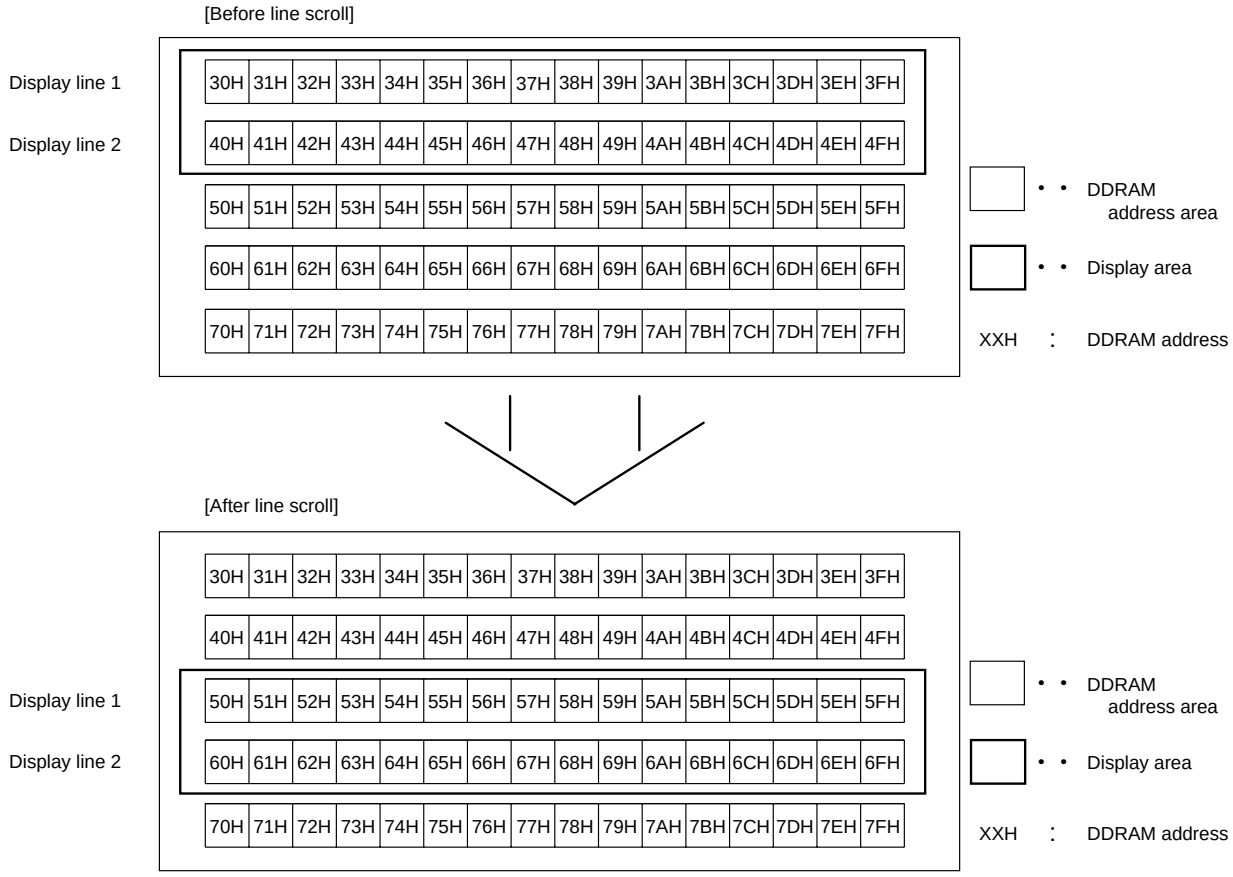
*: Don't Care

LS1	LS0	Function
0	0	Scroll amount 0 line
0	1	Scrolls 1 line upward. (display line 1 from DDRAM line 2)
1	0	Scrolls 2 lines upward. (display line 1 from DDRAM line 3)
1	1	Scrolls 3 lines upward. (display line 1 from DDRAM line 4)

- When 2-line scroll has been performed upward at the 4-line display



- When 2-line scroll has been performed upward at the 2-line display [(LS1, LS2) = (1, 0)]



Line blink display control

Function: Displays the specified line in back-and-while reverse form.
The specified line corresponds to the address line of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	LB4	LB3	LB2	LB1

- Displays the specified line of the DDRAM in black-and-white form by setting LB4 to LB1.
  - LB4 = 0 : Displays the data for line 4 of the DDRAM in standard form. (no blink) [DDRAM 60H to 6FH]
  - LB4 = 1 : Displays the data for line 4 of DDRAM in black-and-white reverse blink form. [DDRAM 60H to 6FH]
  - LB3 = 0 : Displays the data for line 3 of the DDRAM in standard form. (no blink) [DDRAM 50H to 5FH]
  - LB3 = 1 : Displays the data for line 3 of the DDRAM in black-and-white reverse blink form. [DDRAM 50H to 5FH]
  - LB2 = 0 : Displays the data for line 2 of the DDRAM in standard form. (no blink) [DDRAM 40H to 4FH]
  - LB2 = 1 : Displays the data for line 2 of the DDRAM in black-and-white reverse blink form. [DDRAM 40H to 4FH]
  - LB1 = 0 : Displays the data for line 1 of the DDRAM in standard form. (no blink) [DDRAM 30H to 3FH]
  - LB1 = 1 : Displays the data for line 1 of the DDRAM in black-and-white reverse blink form. [DDRAM 30H to 3FH]
- f_{BLINK} = 1 to 2Hz.
- Blinking is performed at the same frequency as cursor blink.
  If blinking is caused to occur at the same time, the cursor position will be hard to know.

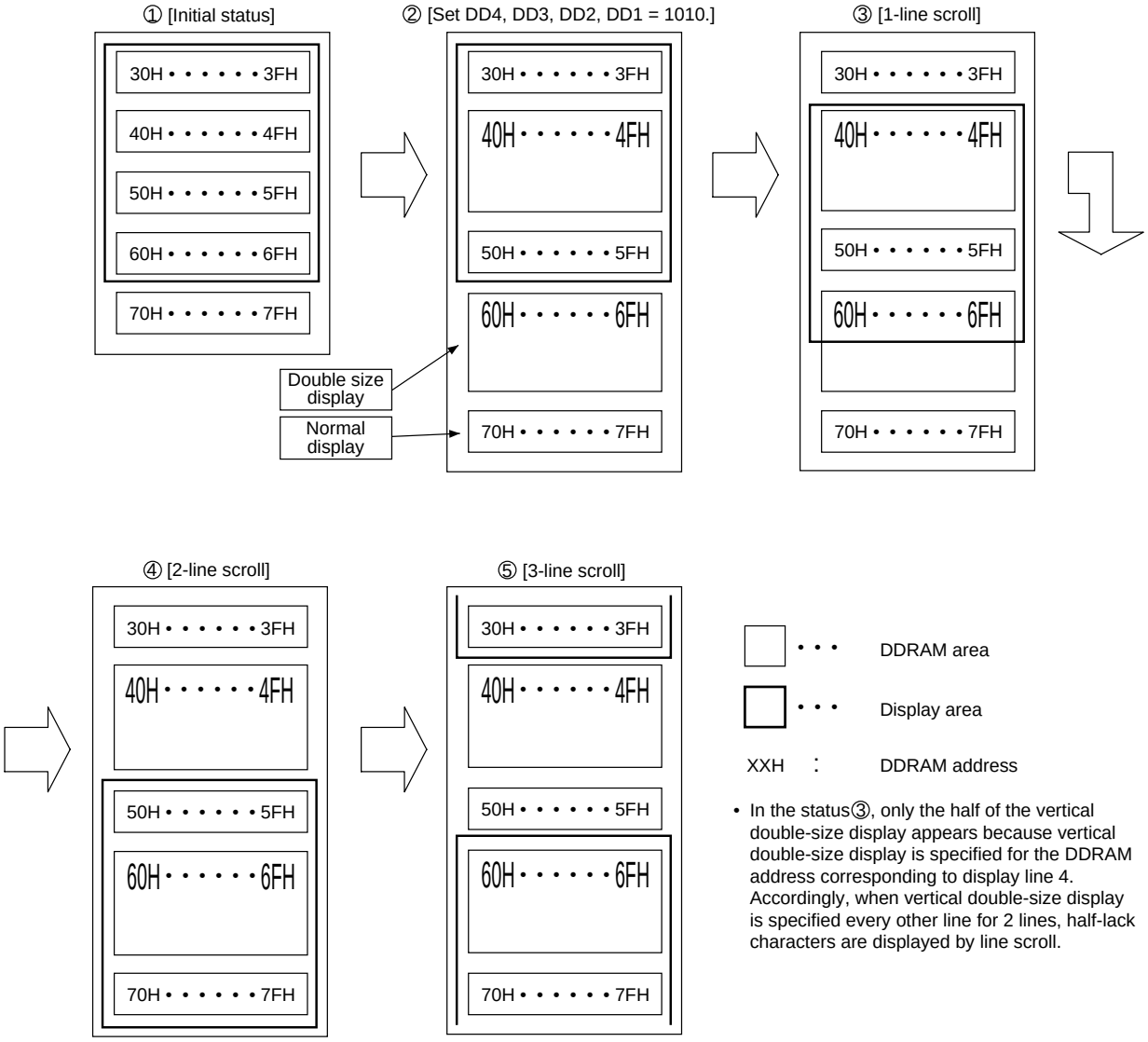
Vertical double-size display control

Function: Displays the specified line in vertical double-size form.
The specified line corresponds to the address of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	DD4	DD3	DD2	DD1

- Displays the specified line of the DDRAM in vertical double-size form by setting DD4 to DD1.
  - DD4 = 0 : Displays the data for line 4 of the DDRAM in standard form. [DDRAM 60H to 6FH]
  - DD4 = 1 : Displays the data for line 4 of the DDRAM in vertical double-size form. [DDRAM 60H to 6FH]
  - DD3 = 0 : Displays the data for line 3 of the DDRAM in standard form. [DDRAM 50H to 5FH]
  - DD3 = 1 : Displays the data for line 3 of the DDRAM in vertical double-size form. [DDRAM 50H to 5FH]
  - DD2 = 0 : Displays the data for line 2 of the DDRAM in standard form. [DDRAM 40H to 4FH]
  - DD2 = 1 : Displays the data for line 2 of the DDRAM in vertical double-size form. [DDRAM 40H to 3FH]
  - DD1 = 0 : Displays the data for line 1 of the DDRAM in standard form. [DDRAM 30H to 3FH]
  - DD1 = 1 : Displays the data for line 1 of the DDRAM in vertical double-size form. [DDRAM 30H to 3FH]

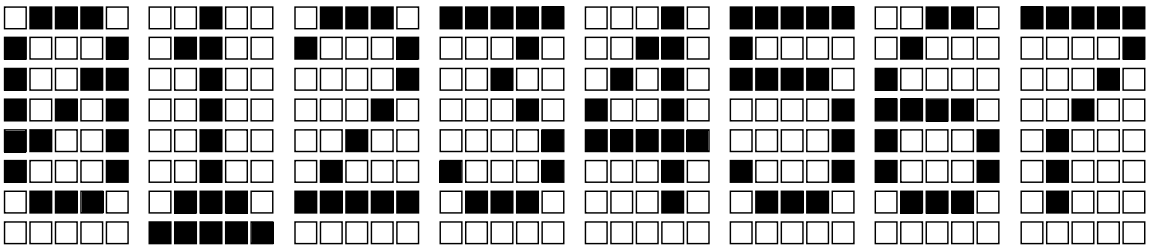
- Example of vertical double-size display
  An example of 4-line display will be cited for explanation.

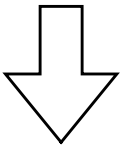


- In the status③, only the half of the vertical double-size display appears because vertical double-size display is specified for the DDRAM address corresponding to display line 4. Accordingly, when vertical double-size display is specified every other line for 2 lines, half-lack characters are displayed by line scroll.

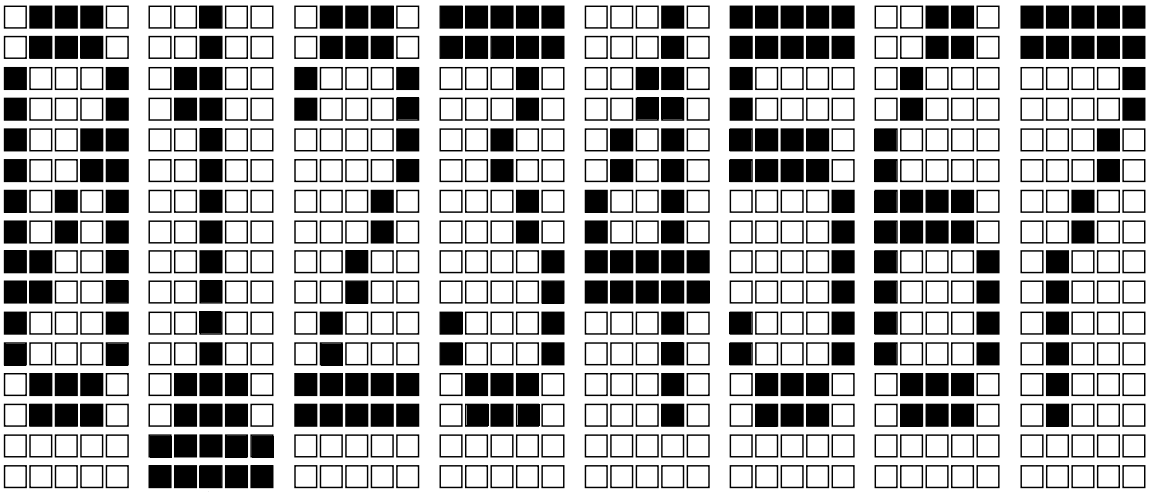
- Example of vertical double-size display (characters)

[Standard display]





[Vertical double-size display]



When the under-bar cursor is displayed, this will also be of double-size.

Display ON/OFF control

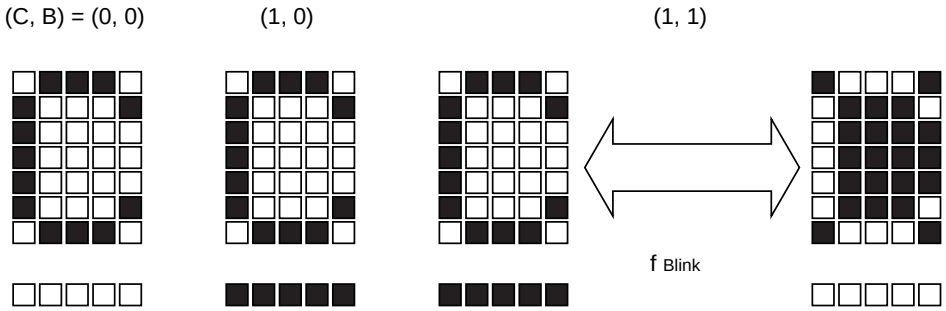
Function: Sets both display and cursor ON/OFF, and extended register access.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	1	1	C	B	RE	D

- Display ON/OFF is specified by setting D.
  D = 0 : Display ON
  D = 1 : Display ON
- Character blink ON/OFF at the cursor position is specified by setting B. However, when the cursor is OFF, this bit is invalidated.
  B = 0 : Cursor blink OFF
  B = 1 : Cursor blink ON
- Cursor ON/OFF is specified by setting C.
  C = 0 : No display of cursor
  C = 1 : Display of cursor
- Extended register access is specified by setting RE.
  RE = 0 : Extended register OFF
  RE = 1 : Extended register ON
- The relation between C/B register and cursor display is shown in the following table.

C	B	Cursor display
0	0	No display (fixed)
0	1	No display (fixed)
1	0	Display of under-bar cursor
1	1	Alternate display of display characters and black-and-white reversed display characters

- Example of cursor display



The cursor display position is indicated by the address counter. Accordingly, when moving the cursor, change the address counter value by the RAM address set command or the auto increment by the RAM data write command.
To display the under-bar cursor when character data (CGRAM) at the cursor position, the position corresponding to the cursor position will be displayed in black-and-white reverse form.
If the address counter is set to the symbol register position at (C, B) = (1, 1), symbols can be caused to blink selectively (every 5 dots because symbols correspond to characters).

Power save

Function: Controls the oscillating circuit and sets and resets the power save mode and the sleep mode.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	1	0	0	*	*	O	PS

*: Don't Care

- Power save mode ON/OFF is specified by setting PS.
  PS = 0 : Power save OFF (reset)
  PS = 1 : Power save ON (set)
- Oscillating circuit ON/OFF is specified by setting O.
  O = 0 : Oscillating circuit OFF (stop of oscillation)
  O = 1 : Oscillating circuit ON (start of oscillation)

Power control (1)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	HPM	VC	VF	P

∗: Don't Care

- Boosting circuit ON/OFF is specified by setting P. For operating the boosting circuit, the oscillating circuit must be in operation.
  P = 0 : Boosting circuit OFF
  P = 1 : Boosting circuit ON
- Voltage follower ON/OFF is specified by setting VF.
  VF = 0 : Voltage follower OFF
  VF = 1 : Voltage follower ON
- Voltage regulating circuit ON/OFF is specified by setting VC.
  VC = 0 : Voltage regulating circuit OFF
  VC = 1 : Voltage regulating circuit ON.
- High power mode ON/OFF is specified by setting HPM.
  HPM = 0 : High power mode OFF
  HPM = 1 : High power mode ON

Power control (2)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	IRS	BAS	IR1	IR0

∗: Don't Care

- The relation of IR0 and option combinations is shown in the following table.

IR1	IR0	(1 + Rb/Ra)
0	0	Small
0	1	↓
1	0	
1	1	Large

- Bias selection is performed by setting BAS.
  BAS = 0 : 1/5 bias
  BAS = 1 : 1/4 bias
- Either built-in V5 voltage regulating resistor or external resistor (no use of built-in resistor) is selected by setting IRS.
  IRS = 0 : No use of built-in resistor
  IRS = 1 : Use of built-in resistor

System set (1)

Function: Selects an option ROM and sets the common shift direction and the use/no use of CGRAM.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	R1	R0	CS	CG

- The relation of R1 and R0 combinations is shown in the following figure.

R1	R0	ROM combination
0	0	Standard ROM (160 characters or 154 characters) + option ROM1 (96 characters)
0	1	Standard ROM (160 characters or 154 characters) + option ROM2 (96 characters)
1	0	Standard ROM (160 characters or 154 characters) + option ROM3 (96 characters)
1	1	Standard ROM (160 characters or 154 characters) + option ROM4 (96 characters)

- The COM shift direction is specified by setting CS.
  CS = 0 : COM left shift (COM1 → COM32 → COMS1 → COMS2)
  CS = 1 : COM right shift (COM32 → COM1 → COMS1 → COMS2)
- The use/no use of CGRAM is specified by setting CG.
  CG = 0 : No use of CGRAM
  CG = 1 : Use of CGRAM

System set (1)

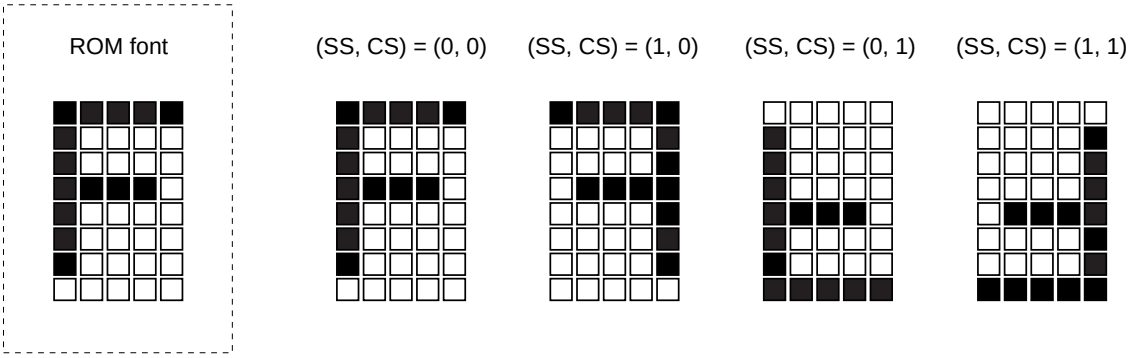
Function: sets the normal/reverse display of SEG characters.
This function operates for each character.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	*	*	SS	*

∗: Don't Care

- The normal/reverse display of SEG is specified by setting SS.
  SS = 0 : Normal display of SEG
  SS = 1 : Reverse display of SEG
- For the symbol register RAM output, only the normal display is available.

- Example of display (compared by the same mounting method)



RAM address set (1) [DDRAM, static icon RAM, electronic volume RAM]

Function: Sets the address for writing data into the DDRAM, static icon RAM (including blink control), and electronic volume RAM in the address counter. When the cursor appears, it is displayed at the display position corresponding to the DDRAM address set by this command. (When the static icon RAM or electronic volume RAM is specified, the cursor disappears on the display.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ADDRESS						

① The settable address is the address 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, when data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 0, 09H is for testing. Be sure not to use it!

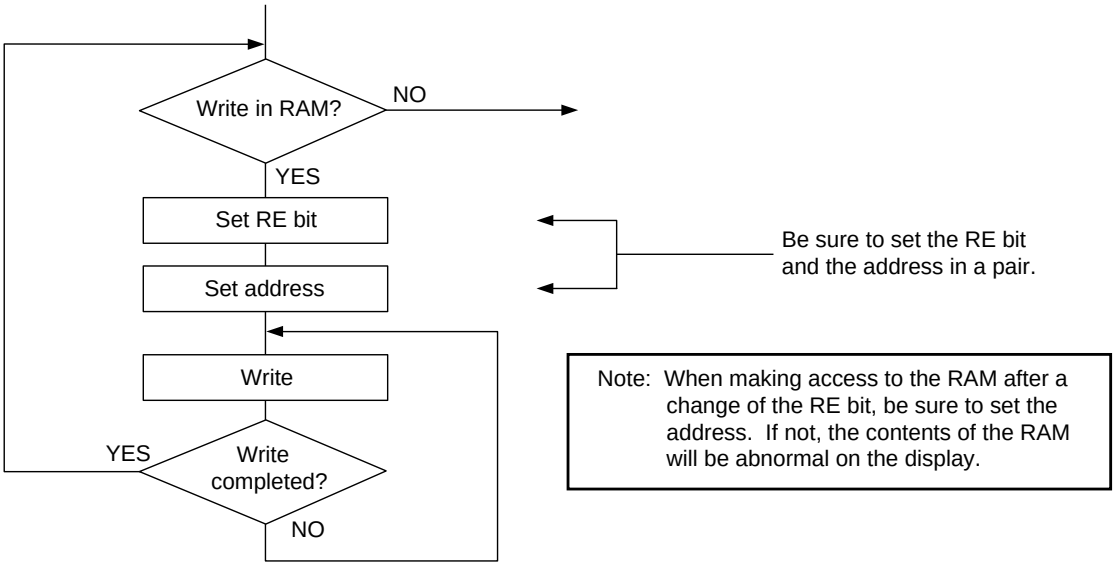
RAM address set (2) [CGRAM, symbol register RAM]

Function: Sets the address for writing data into the CGRAM or symbol register RAM in the address counter.
When the CGRAM address is set, the cursor will disappear on the display. When the symbol register RAM is set, the cursor moves to the corresponding symbol position, causing this symbol to blink selectively.
When the cursor home command is executed immediately after execution of this instruction (before execution of RAM Address Set (1)), the cursor will not be displayed. (Because the address is set at address 30H of RE-1 of the RAM map.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	ADDRESS						

① The settable address of the address of 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, if data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 1, 30H - 5FH i8s set to No Use. It is not available.

<Example of Address Set>



[S1D12400 RAM map] (4-line 16-digit display)

RE	High \ Low order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST	Unused					
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI :Static icon RAM
SIB :Static icon blink control RAM
EV :Electronic volume RAM
TEST :Testing register. Don't use it.

[S1D12400 Series RAM map] (2-line 16-digit display)

RE	High \ Low order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST	Unused					
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI :Static icon RAM
SIB :Static icon blink control RAM
EV :Electronic volume RAM
TEST :Testing register. Don't use it.

[Display range of each master]

The following shows the display range for the DDRAM area when the vertical double size is unspecified and scroll amount is 0 line:

S1D12400 (4 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
	4th line on display	RE = 0	60H to 6FH
S1D12401 (3 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
S1D12402 (2 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH

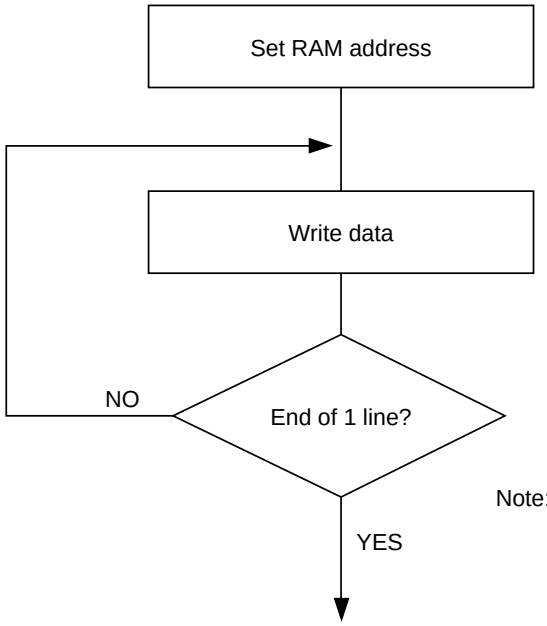
RAM data write

Function: Writes data in the RAM areas of the DDRAM, CGRAM, symbol register RAM, static icon RAM, and electronic volume RAM.
Before this command, be sure to execute the address set command.
After that, each time data is written, the address will be automatically incremented. (Regarding the RE bit, the contents set by the command will be kept in memory.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	0	DATA							

① Data is written into the DDRAM, CGRAM, symbol register RAM, static icon RAM, or electronic volume RAM.
② The address counter is automatically incremented by 1, so data can be written in succession. However, the address counter advances from 00H to 7FH to 00H. Accordingly, when writing data into the CGRAM, take care not to write it at the addresses subsequent to 30H.

<Data write example>
An example of writing one line of data into the DDRAM continuously is shown below.



Note: Before executing instructions in succession, secure a time exceeding tCYC and then execute them.

NOP

Function: A no-operation command. No operation is performed functionally. However, because a test mode reset function exists inside, the test mode can be reset if the IC is put into this mode by an effect of noise.
It is recommended to add this command at each breakpoint of the program.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	0	0	0	0

Test mode

Function: An IC test mode set command. Don't use it in any case.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	*	*	*	*

8. CHARACTER GENERATOR

Character Generator ROM (CGROM)

The S1D12400 series is provided with a character generator ROM consisting of up to 544 types of characters. Each character size is of a structure of 5 × 8 dots.
A character code table of the S1D12400 series is shown in CGROM Table X to X. In this case, which of CGROM and CGRAM should be used for the 6 characters of 00H to 05H of the character code is specified by the system set command.

The CGROM of the S1D12400 series is a mask ROM and is compatible with the user's own CGROM. Please ask our sales department for further information.
Regarding a changed product of CGROM, the product name is defined as follows:

Example: S1D12400D10B∗
↑
Digits corresponding to CGROM pattern change

The following shows the standard font specified for S1D12400 series:

S1D12400D10B∗, S1D12400T00A∗ : JISS1 (Font A)
S1D12400D11B∗, S1D12400T00B∗ : ASCII (Font B)
S1D12400D16B∗, S1D12400T00G∗ : JISS2 (Font G)

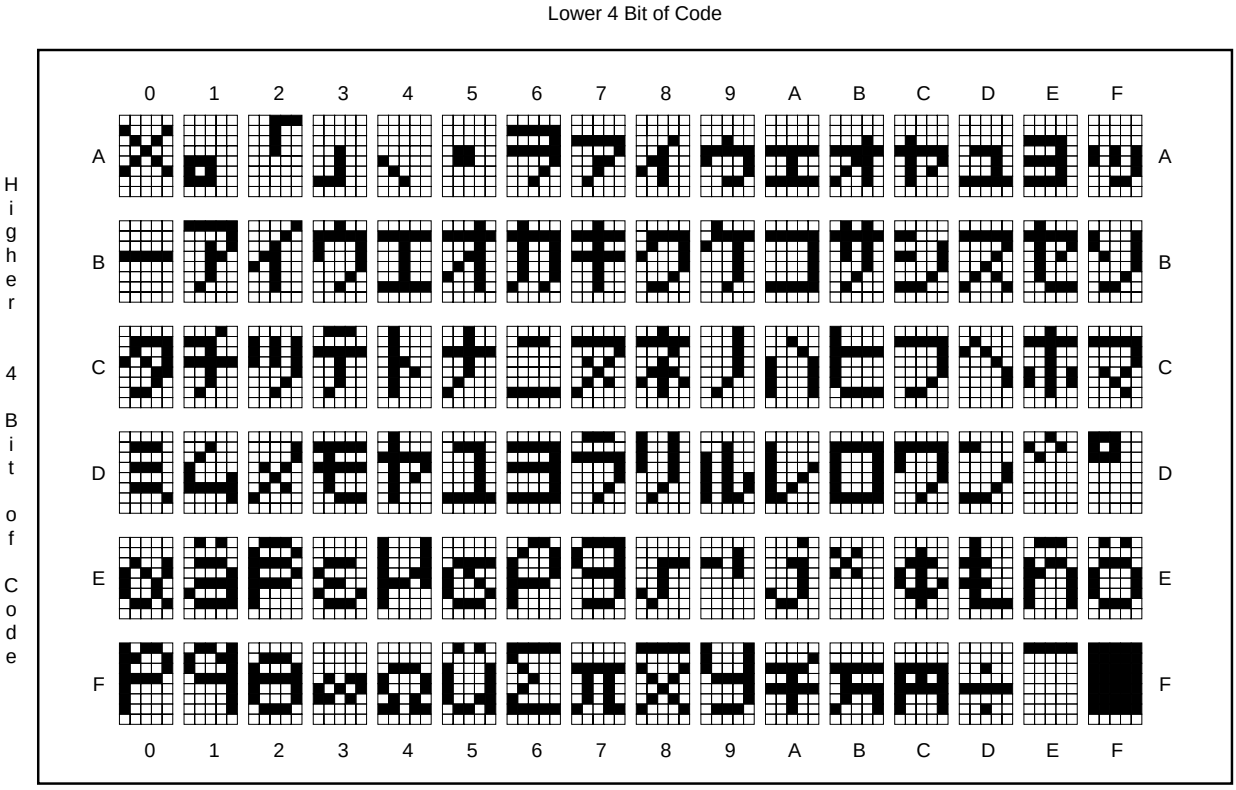
S1D12401D10B∗, S1D12401T00A∗ : JISS1 (Font A)
S1D12401D11B∗, S1D12401T00B∗ : ASCII (Font B)
S1D12401D16B∗, S1D12401T00G∗ : JISS2 (Font G)

S1D12402D10B∗, S1D12402T00A∗ : JISS1 (Font A)
S1D12402D11B∗, S1D12402T00B∗ : ASCII (Font B)
S1D12402D16B∗, S1D12402T00G∗ : JISS2 (Font G)

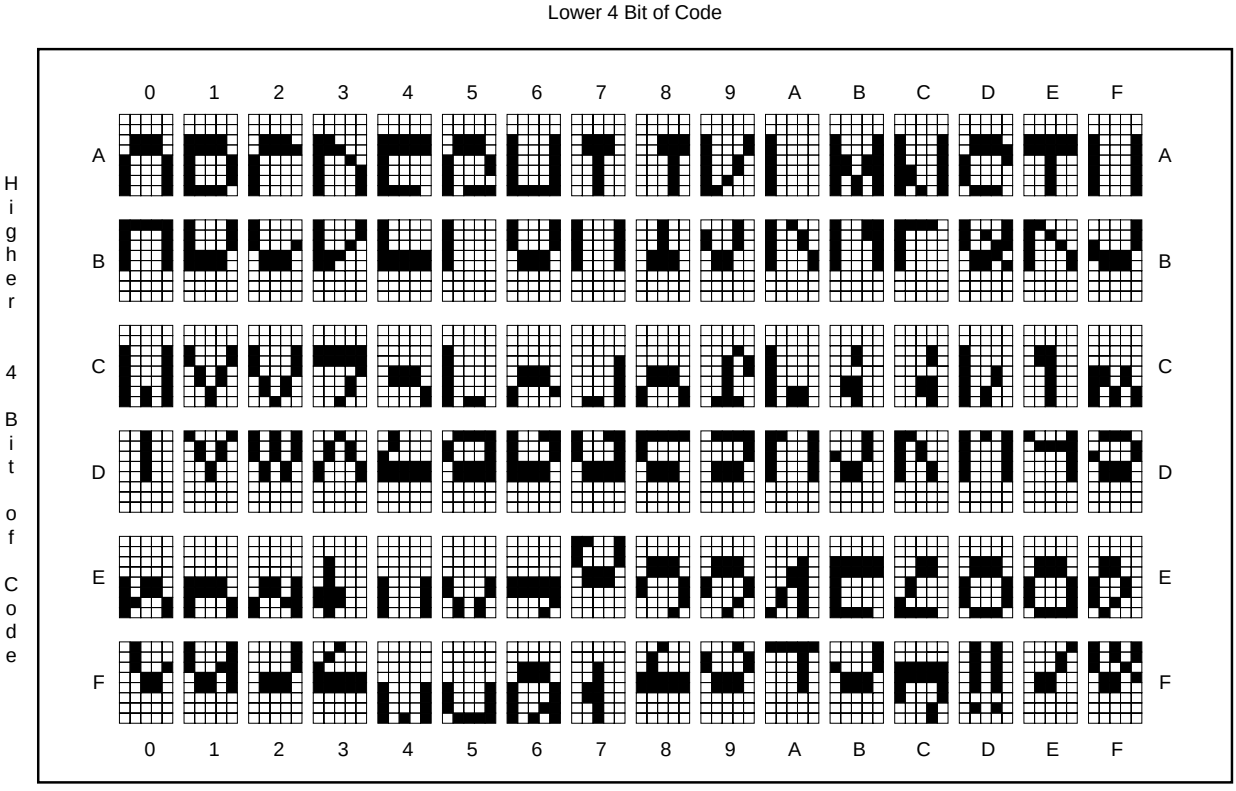
[JIS1: A Font]

Standard ROM Font

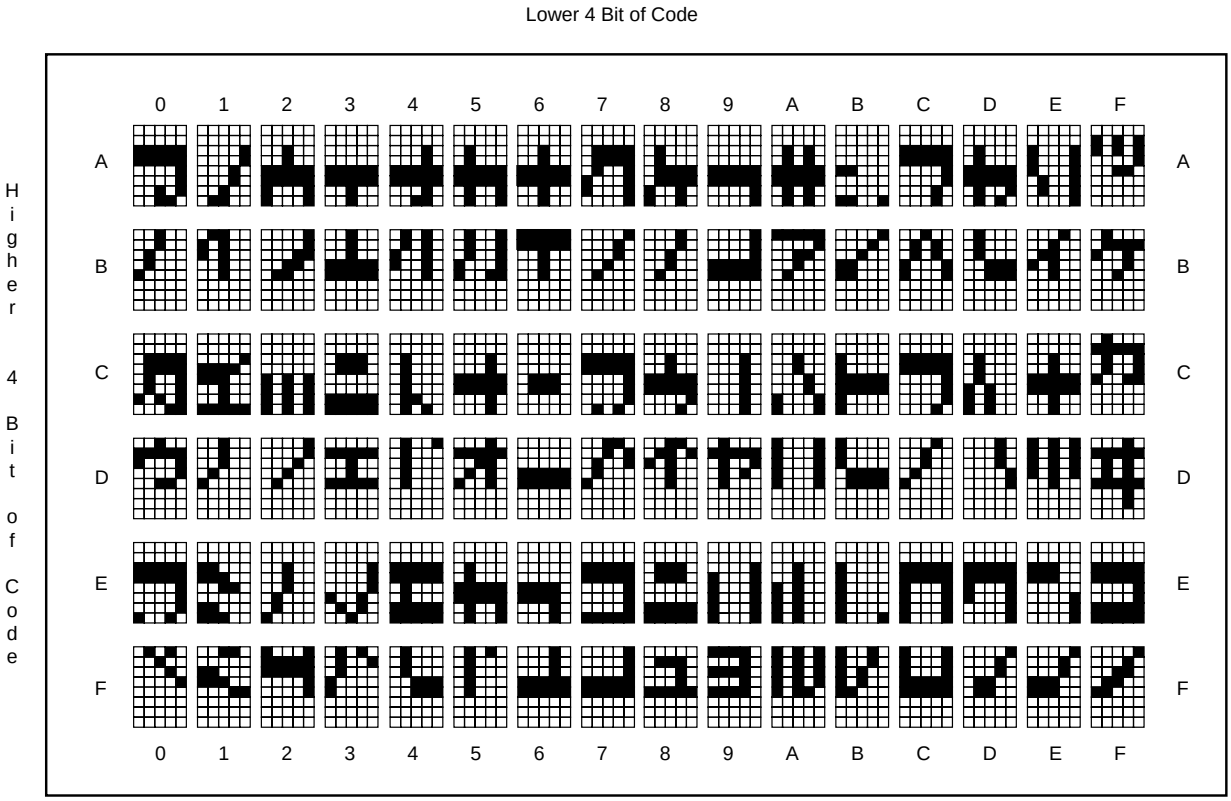
OPTION ROM1 (when R1, R0 = 0, 0 is selected)



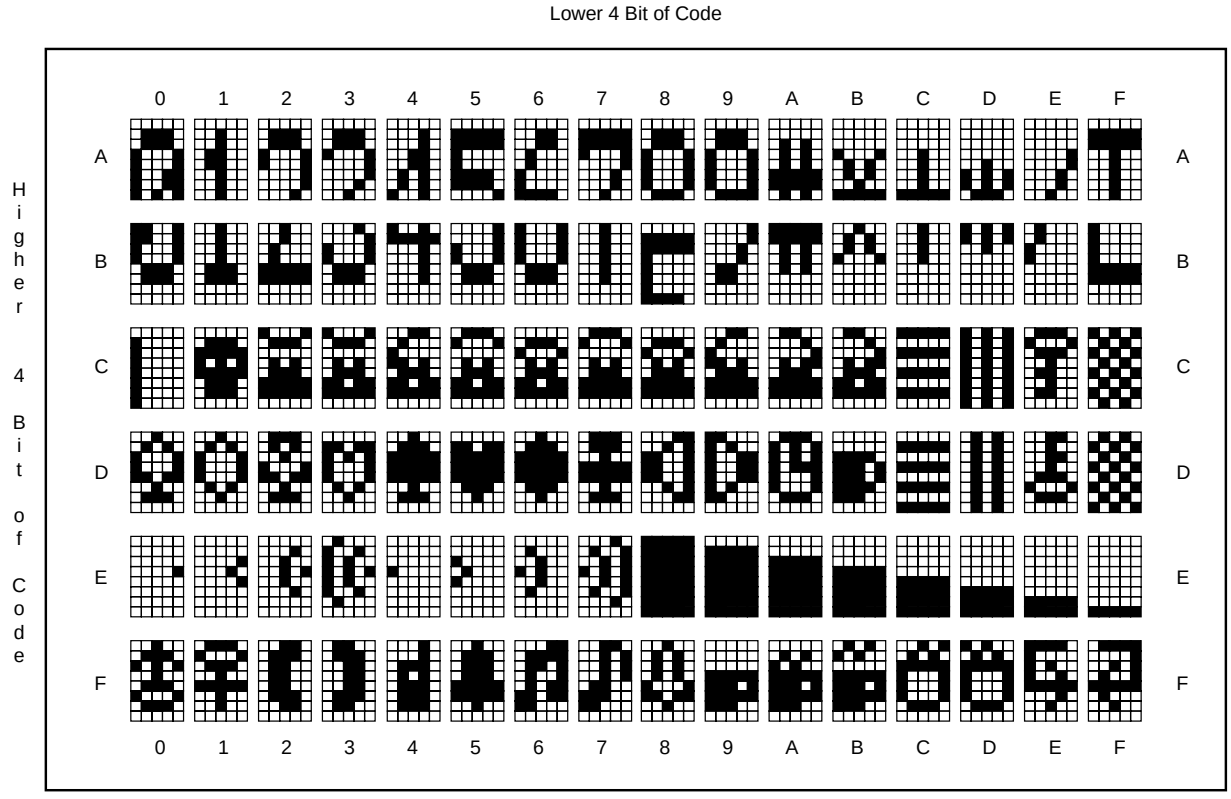
OPTION ROM2 (when R1, R0 = 0, 1 is selected)



OPTION ROM3 (when R1, R0 = 1, 0 is selected)

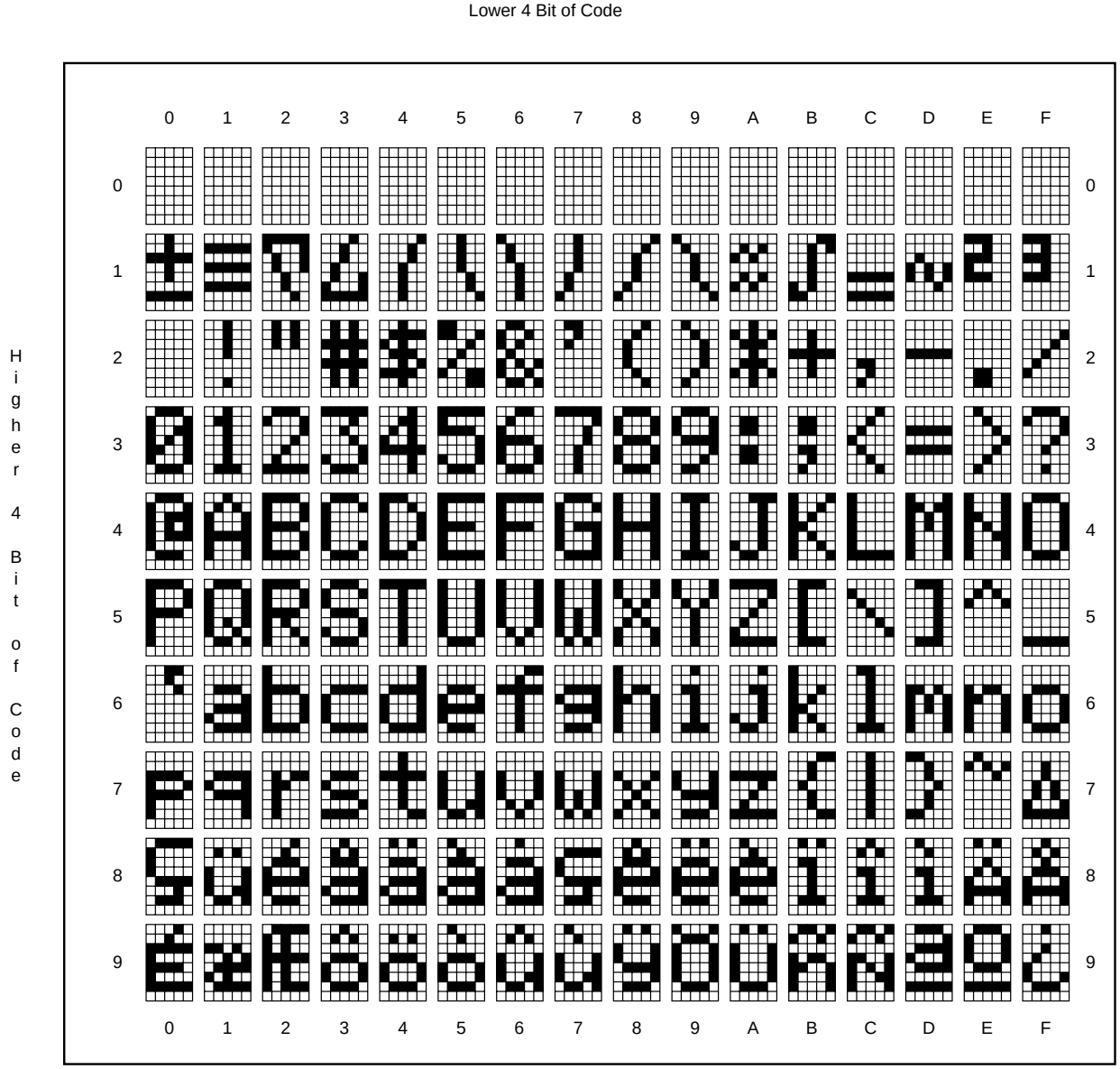


OPTION ROM4 (R1, R0 = 1,1 is selected)



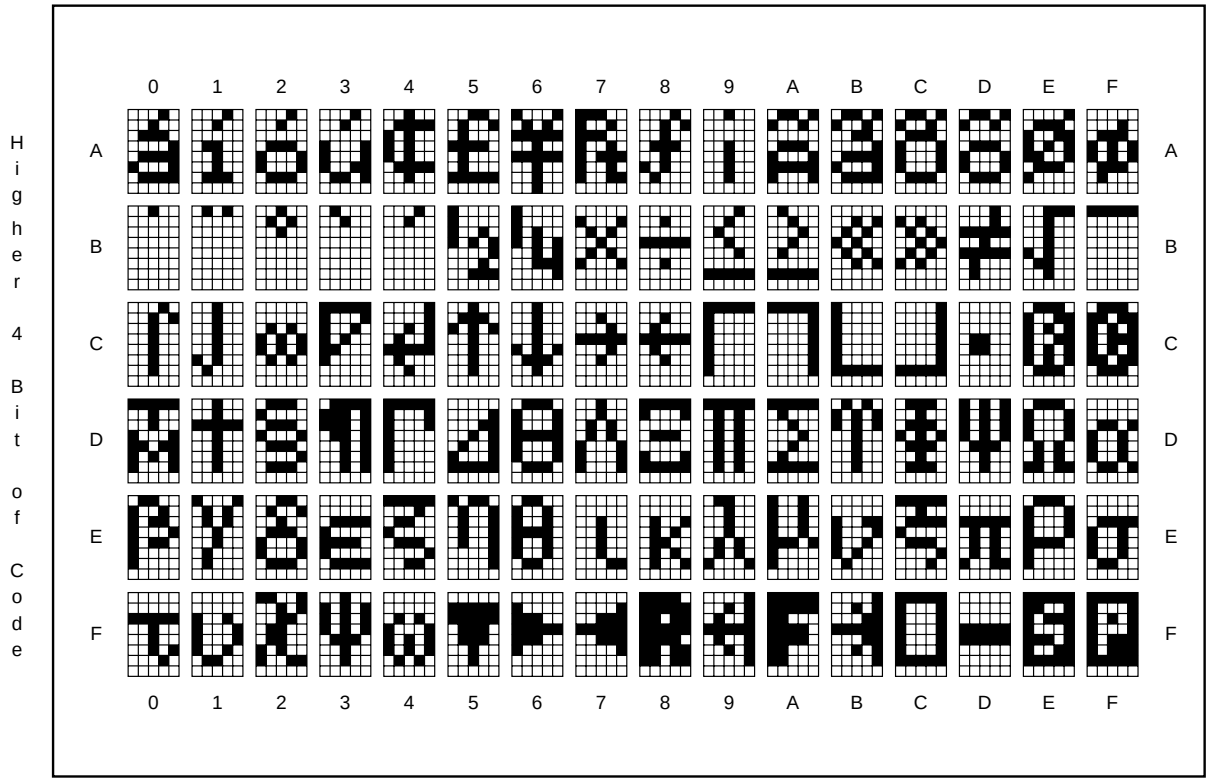
[CGROM Font (ASCII: Font B)]

Standard ROM Font



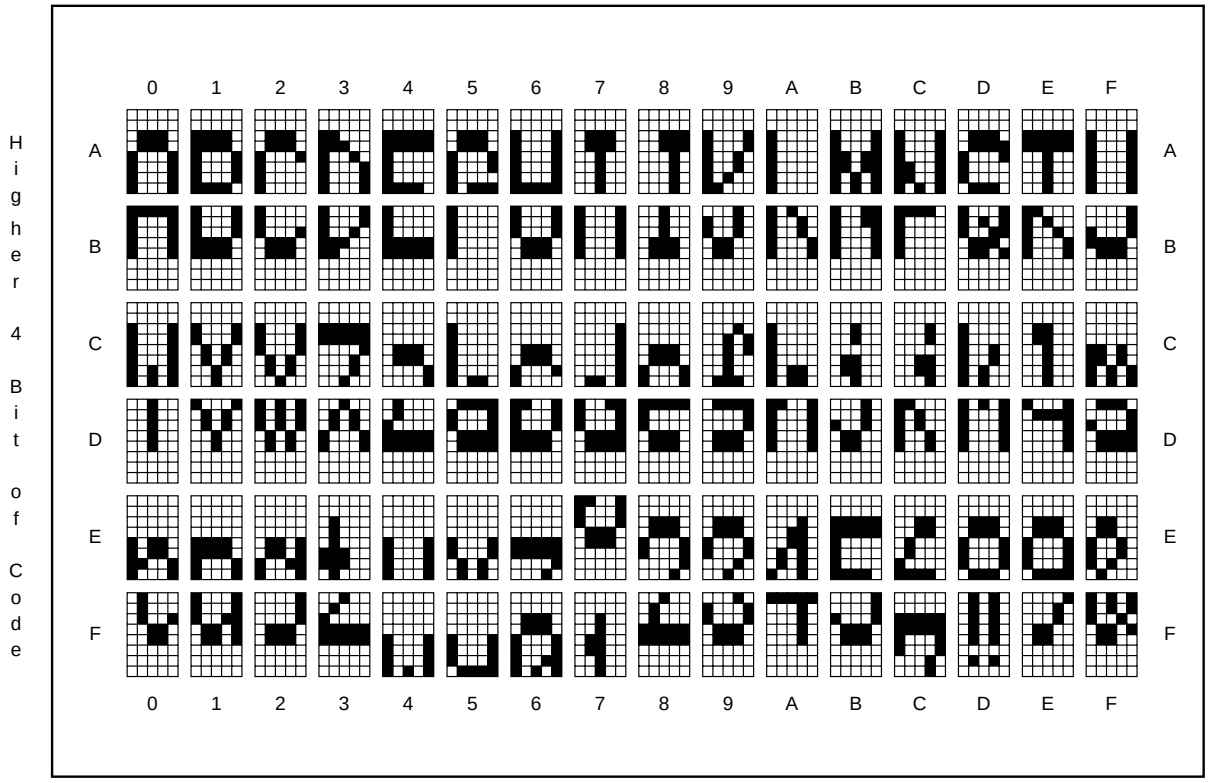
OPTION ROM1 (when R1, R0 = 0, 0 is selected)

Lower 4 Bit of Code

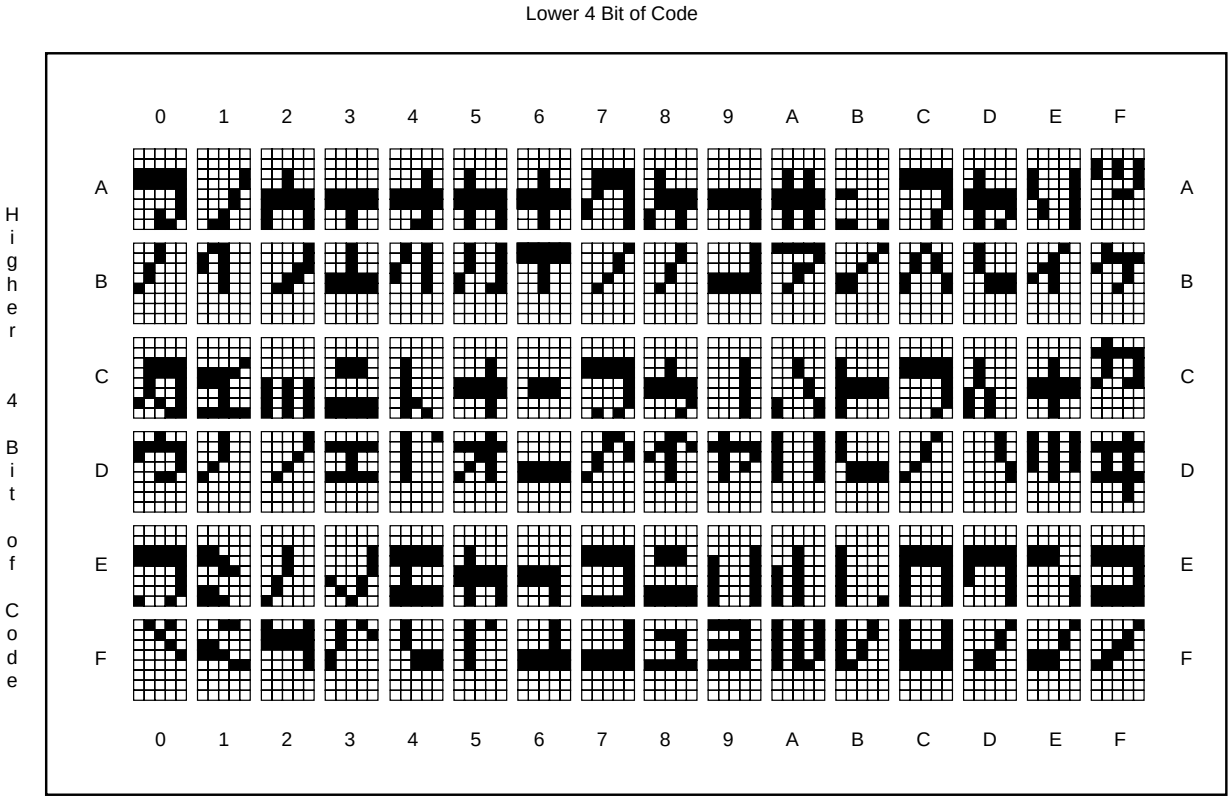


OPTION ROM2 (when R1, R0 = 0, 1 is selected)

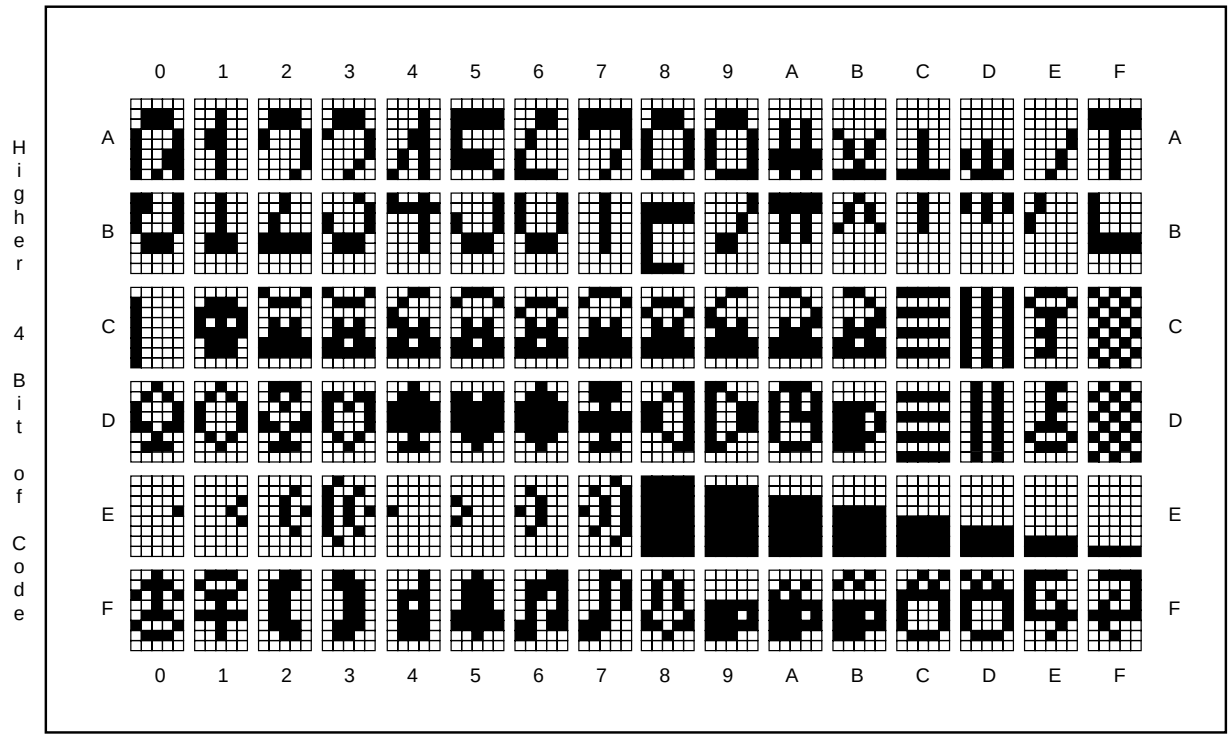
Lower 4 Bit of Code



OPTION ROM3 (when R1, R0 = 1, 0 is selected)

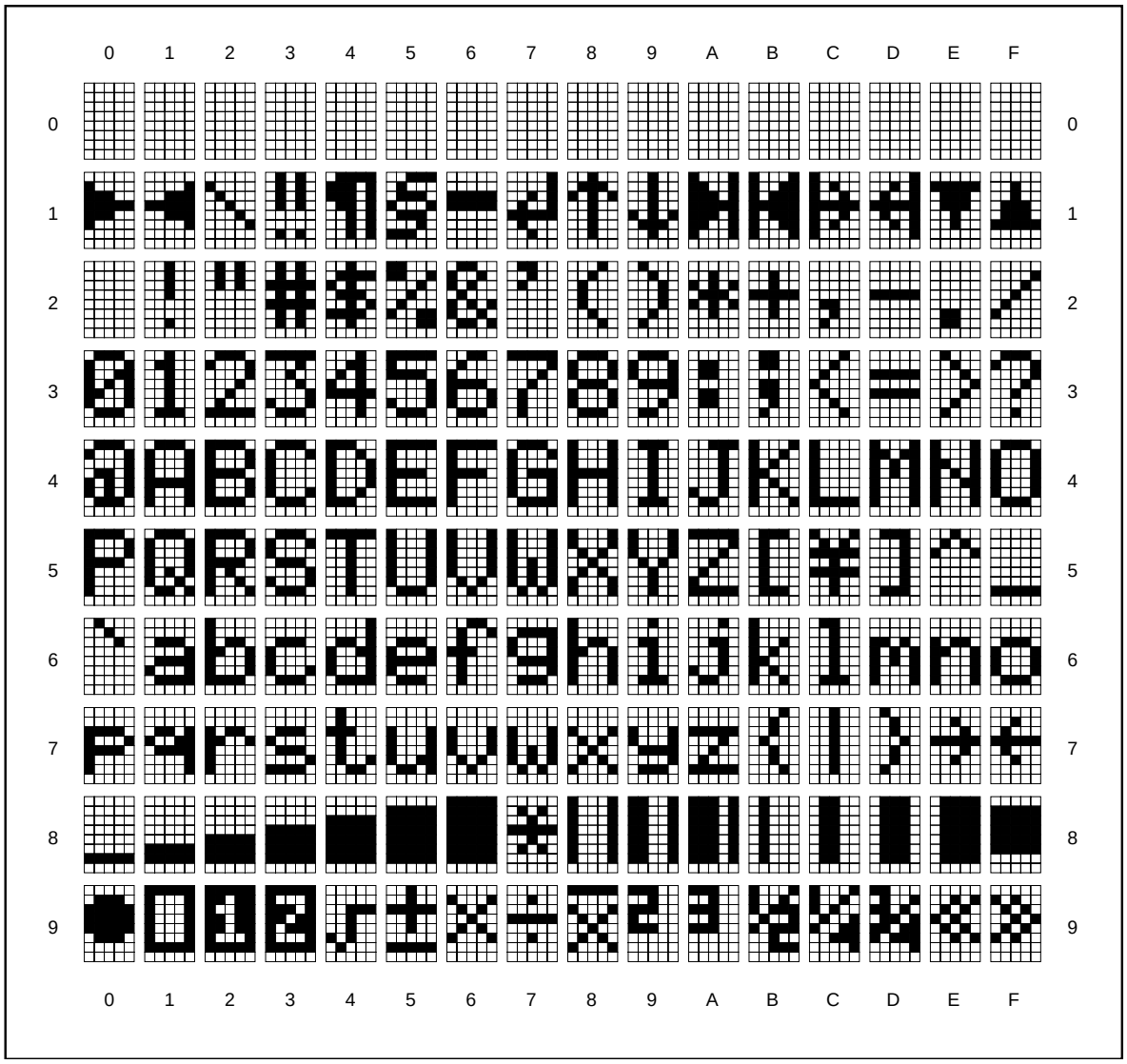


OPTION ROM4 (R1, R0 = 1,1 is selected)

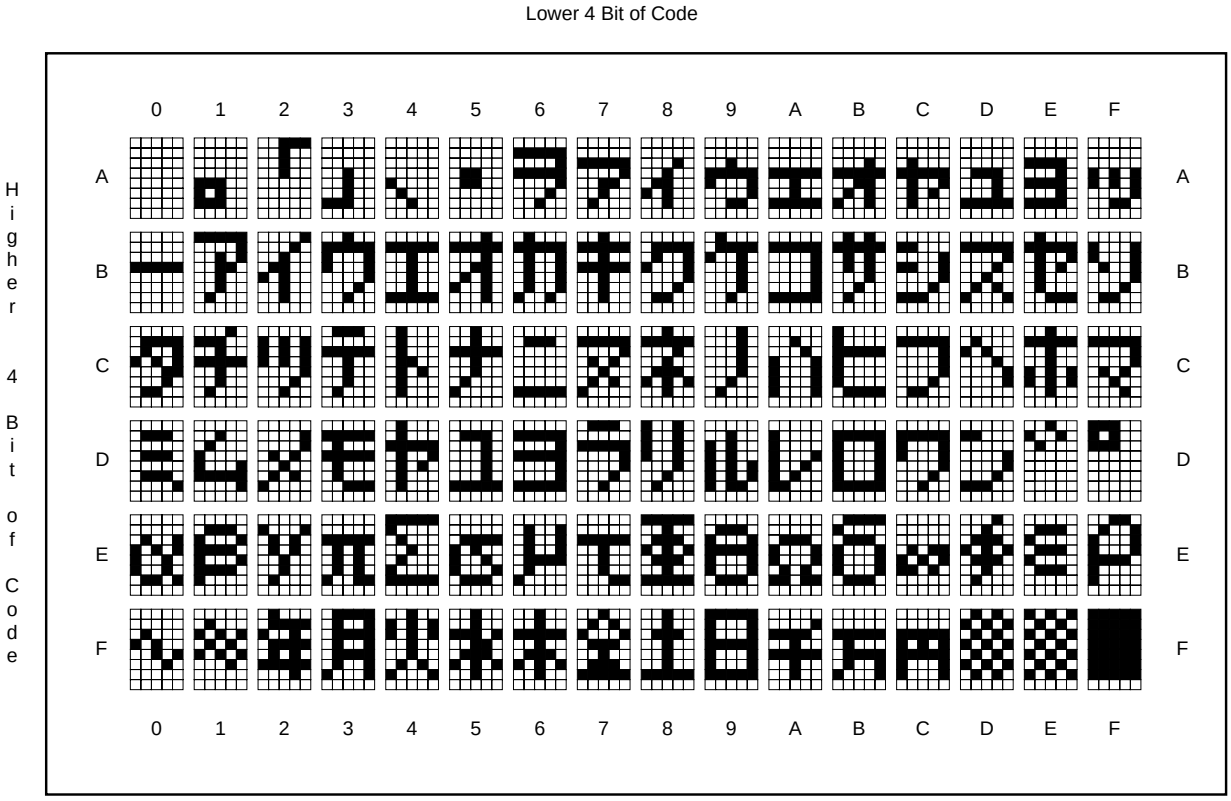


[CGROM Font (JISS2: Font G)]

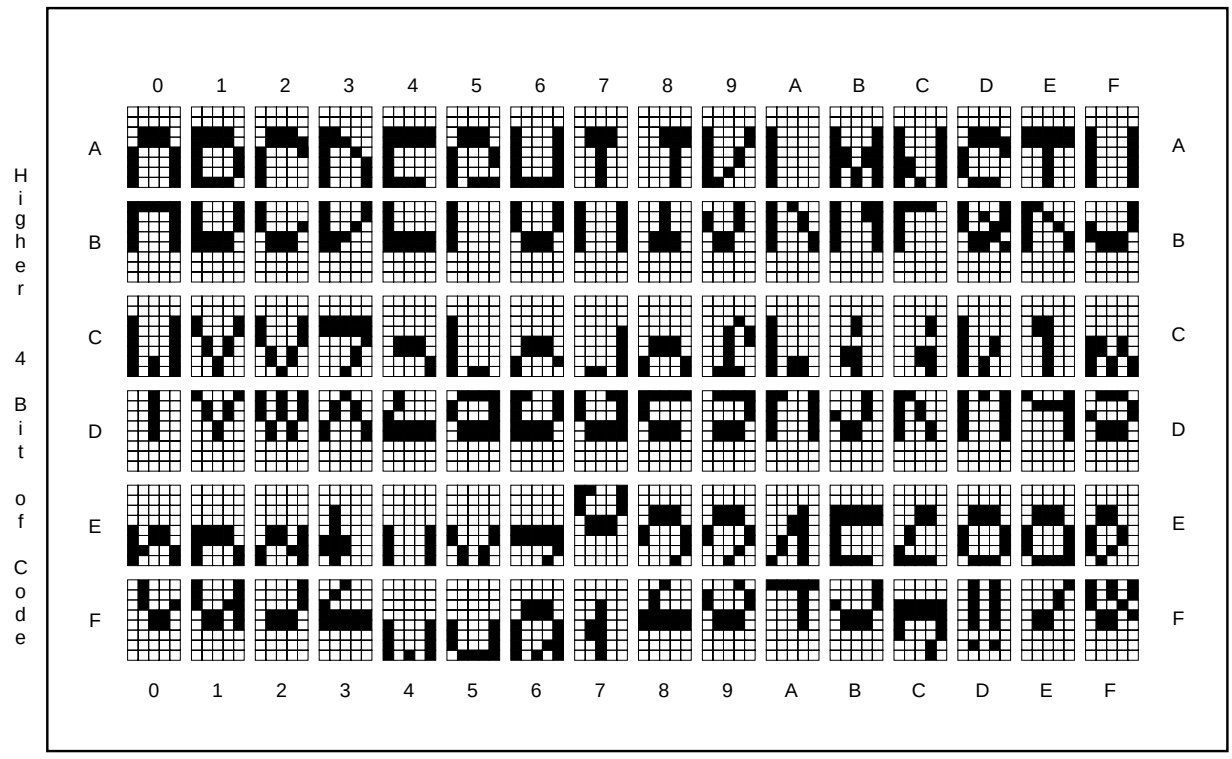
Standard ROM Font



OPTION ROM1 (when R1, R0 = 0, 0 is selected)

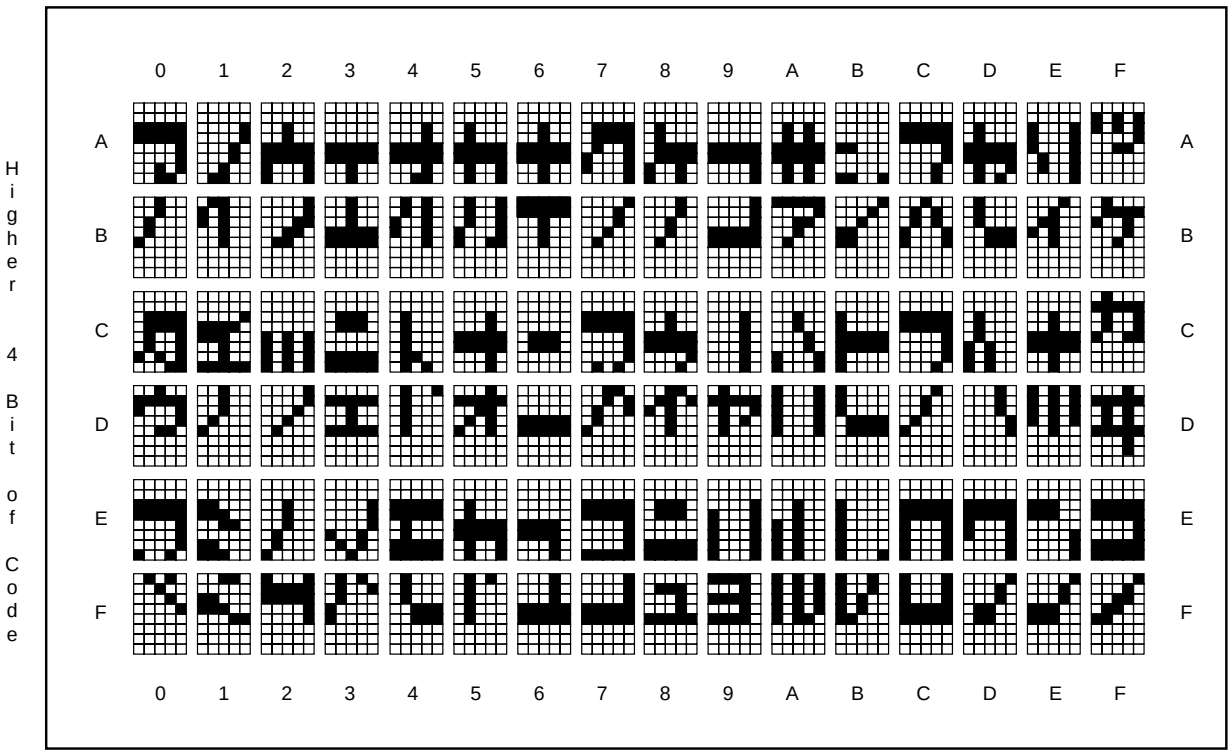


OPTION ROM2 (when R1, R0 = 0, 1 is selected)



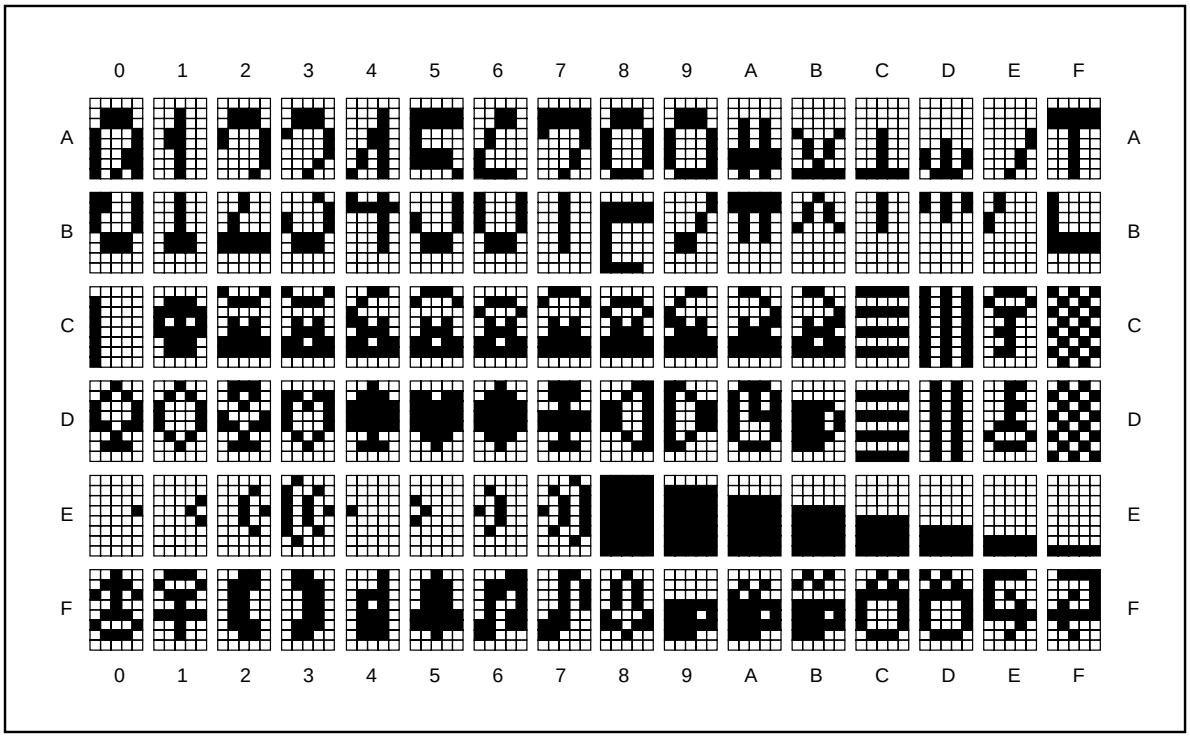
OPTION ROM3 (when R1, R0 = 1, 0 is selected)

Lower 4 Bit of Code



OPTION ROM4 (R1, R0 = 1,1 is selected)

Lower 4 Bit of Code



Character Generator RAM (CGRAM)

The S1D12400 series is provided with a CGROM that permits the user to program character patterns so as to attain a character display with a high degree of freedom. When using the CGRAM, select Use of CGRAM by the system set command. The CGRAM capacity is 240 bits having a structure of 5 × 8 dots and optional 6 types of patterns can be registered.
The relation among CGRAM character patterns, CGRAM addresses, and character codes is shown below.

Character code	RAM Address (CGRAM selection: RE = 1)		CGRAM data (character pattern) D7							D0	Character display SEG
00H	(00H to 07H)	0	*	*	*	0	1	1	1	1	
02H	(10H to 17H)	1	*	*	*	1	0	0	0	0	
04H	(20H to 27H)	2	*	*	*	1	0	0	0	0	
		3	*	*	*	0	1	1	1	1	
		4	*	*	*	0	0	0	0	1	
		5	*	*	*	0	0	0	0	1	
		6	*	*	*	1	1	1	1	0	
		7	*	*	*	0	0	0	0	0	
01H	(08H to 0FH)	8	*	*	*	0	0	1	0	0	
03H	(18H to 1FH)	9	*	*	*	0	0	1	0	0	
05H	(28H to 2FH)	A	*	*	*	0	1	1	1	0	
		B	*	*	*	0	1	1	1	0	
		C	*	*	*	0	1	1	1	0	
		D	*	*	*	1	1	1	1	1	
		E	*	*	*	1	1	1	1	1	
		F	*	*	*	0	0	0	0	0	

Unused — Character data

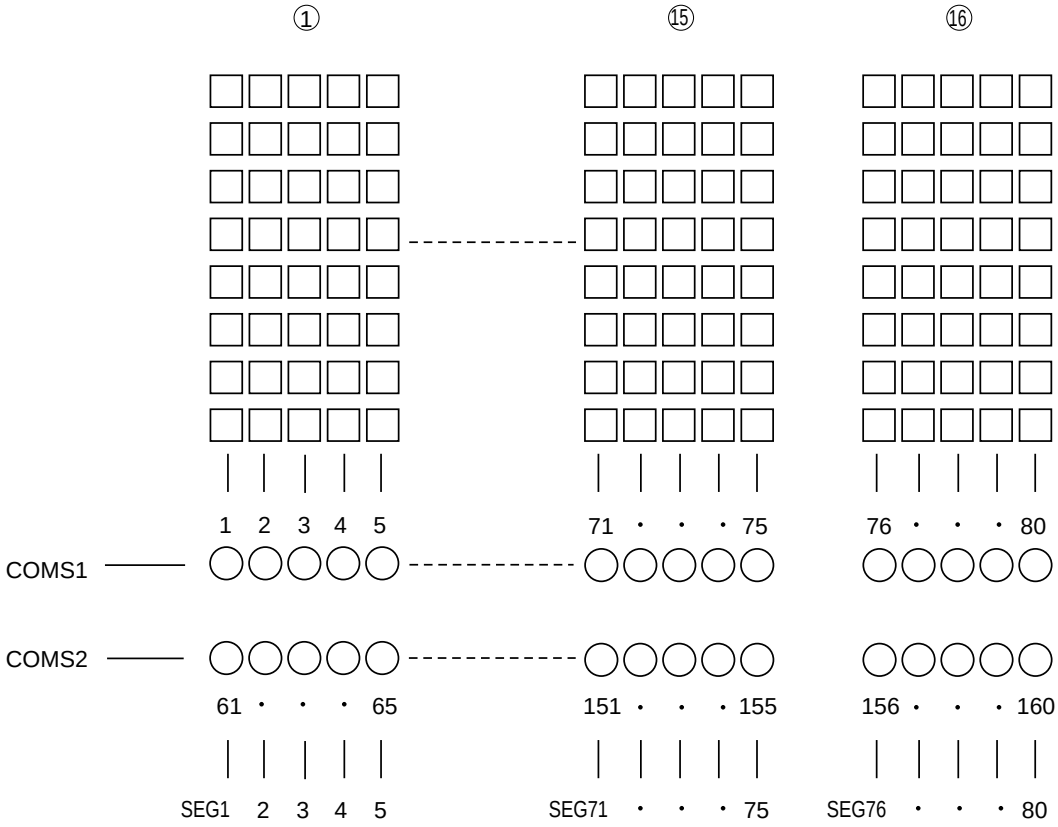
1: Display
0: No display

The character size of 5 × 8 can also be set. In this case, use the RAM of *7H, *FH of the CGRAM address. However, when the under-bar cursor is used, the data of *7H, *FH is displayed in reverse form.

Symbol Register RAM

The S1D12400 series is provided with a symbol register RAM that permits setting each symbol so that symbols may be displayed individually on the screen.
The symbol register capacity is 160 bits in both S1D12400, S1D12401 and S1D12402 series and up to 160 symbols can be displayed.
Each symbol can be blink-controlled in units of bit by using D7 and D6.
The relation among symbol register display patterns, RAM address and write data is shown by citing an example.

[S1D12400 (4-line 16-digit display), S1D12401 (2-line 16-digit display)]



RAM address [RE = 1]		Bits for symbol							
		D7							D0
60H to 6FH	0	BONF	IORH	*	1	2	3	4	5
	1	BONF	IORH	*	6	7	8	9	10
	:				:				
	F	BONF	IORH	*	76	77	78	79	80
70H to 7FH	0	BONF	IORH	*	81	82	83	84	85
	1	BONF	IORH	*	86	87	88	89	90
	:				:				
	F	BONF	IORH	*	156	157	158	159	160

Note 1: When a symbol is 1.5 times as large as other bits, it is recommended to divide it into COMS1 and COMS2 for driving.

D7 (BONF)	D6 (IORH)	Function
0	*	No blink
1	0	D4 to D0 blink in black-and-white reverse form.
1	1	The bits of “1” out of D4 to D0 blink.

f_{BLINK} : 1 to 2Hz

Static Icon RAM

The S1D12400 series can display static icons in the standby mode.
Each of 10 icons can be set in respect of ON/OFF and blink by using the pins of COMSA to SEGSA to J. The relation between static icon functions and static icon RAM write data is shown below.

RAM address [RE = 0]	SI data								Display
	D7	D6	D5	D4	D3	D2	D1	D0	[□ · · · OFF ■ · · · ON]
00H									SEGSA B C D E
	✳	✳	✳	0	0	0	0	0	□ □ □ □ □
	✳	✳	✳	0	0	0	0	1	□ □ □ □ ■
	✳	✳	✳	0	0	0	1	0	□ □ □ ■ □
	✳	✳	✳	1	1	1	1	1	■ ■ ■ ■ ■
01H									SEGSF G H I J
	✳	✳	✳	0	0	0	0	0	□ □ □ □ □
	✳	✳	✳	0	0	0	0	1	□ □ □ □ ■
	✳	✳	✳	0	0	0	1	0	□ □ □ ■ □
	✳	✳	✳	1	1	1	1	1	■ ■ ■ ■ ■

For static icons, blink ON/OFF control can be exerted independently for each pin.

RAM address [RE = 0]	ISB data VS pin								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
02H	✳	✳	✳	SEGSA	SEGSB	SEGSC	SEGSD	SEGSE	Blink 1 = ON 0 = OFF
03H	✳	✳	✳	SEGSF	SEGSG	SEGSH	SEGSI	SEGSJ	

The following table shows a static icon ON/OFF function and static icon blink control.

RAM address [RE = 0]	SI data								Display
	D7	D6	D5	D4	D3	D2	D1	D0	[□ · · · OFF ■ · · · ON]
00H	✳	✳	✳	1	0	1	1	0	SEGSA B C D E
02H	✳	✳	✳	0	1	0	1	0	■ □ ■ ■ □ ⇕ f_{BLINK} ■ ■ ■ □ □

f_{BLINK}: 1 to 2Hz

<Cautions for static icon operation>
- Be sure to write static icon data when the oscillating circuit is on. If the data is written when the oscillating circuit is off (Sleep Mode), previous display may remain and instantaneous lighting may occur.
- To perform resetting on the $\overline{RES}$ terminal except at the time of turning on power, turn off the static icon and blinking in advance, then turn off the oscillating circuit. If resetting is performed when the static icon or blinking is on, instantaneous lighting may be caused by stopping of the oscillating circuit.

Electronic Volume RAM

The S1D12400 series is provided with an electronic volume function that permits controlling the liquid crystal drive voltage V_5 and adjusting the density of liquid crystal display. The electronic volume function can select one of 32 states of the liquid crystal drive voltage by writing 5-bit data into the electronic volume RAM.

When a V_5 voltage regulating built-in resistor is used, this function can attain a wider adjustment if the resistor ratio set command is used together.

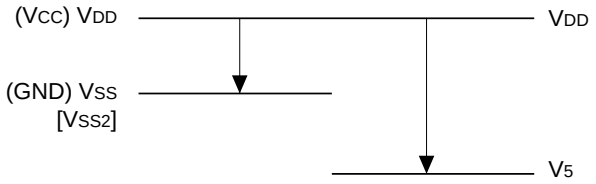
The relation between electronic volume set RAM addresses and write data is shown below.

Function	RAM address [RE=0]	Electronic volume data								State	V_{EV}
		D7	D6	D5	D4	D3	D2	D1	D0		
Electronic volume	08H	*	*	*	0	0	0	0	0	0	V_{REG-0}
		*	*	*	0	0	0	0	1	1	$V_{REG-\alpha}$
		*	*	*	0	0	0	1	0	2	$V_{REG-2\alpha}$
		.	.	.	.	.	.	.	.	.	.
		*	*	*	1	1	1	0	1	29	$V_{REG-29\alpha}$
		*	*	*	1	1	1	1	0	30	$V_{REG-30\alpha}$
		*	*	*	1	1	1	1	1	31	$V_{REG-31\alpha}$
	09H	*	*	*	*	T4	T2	T1	T0	–	For test

* :Unused
α :$\alpha = V_{REG}/150$
Note :Address"09H"(RE=0)isusedfortest.Don'tuseit.

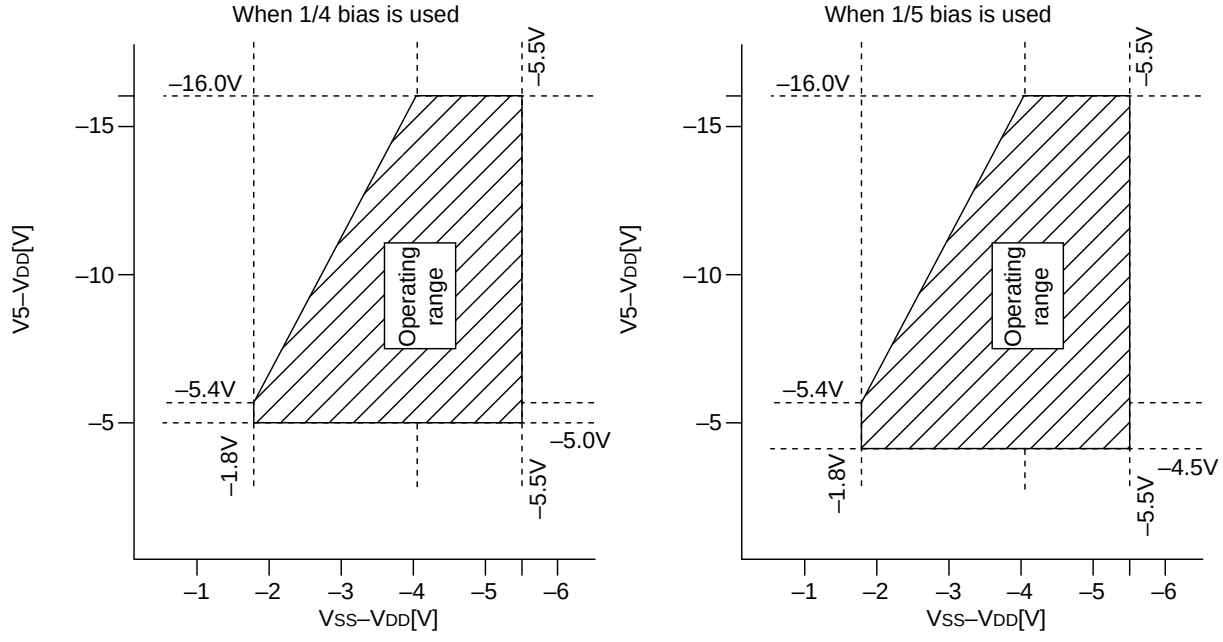
9. ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Supply voltage (1)		V_{SS}	–7.0 to +0.3	V
Supply voltage (2)		V_{SS2}	–7.0 to +0.3	V
	Double boosting		–7.0 to +0.3	
	Triple boosting		–6.0 to +0.3	
Supply voltage (2)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes:
1. All the voltage values are based on V_{DD} = 0 V.
2. The voltages of V_1, V_2, V_3, and V_4 must always meet the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and the condition of $V_{DD} \geq V_5 \geq V_{OUT}$, $V_{DD} \geq (V_{SS}, V_{SS2}) \geq V_{OUT}$.
3. If the LSI is used exceeding the absolute maximum ratings, it may result in permanent destruction. It is desirable to use the LSI in the condition of electric characteristics at ordinary operation. If this condition is exceeded, a malfunction may be caused to the LSI, having a bad effect on its reliability.

● Operating voltage range for V_{SS} system (V_{SS} and V_{SS2}) and V_5 system (V_5)
Set the V_{SS2} to ensure that the V_{OUT} does not exceed the following operating voltage range:
It applies when an external power supply is used. When using an internal power supply, make sure to set V_{SS} in such that V_{OUT} may not exceed the operating voltage range of V_5 system given below.



S1D12400 Series

10. DC CHARACTERISTICS

[V_{SS} = –5.5 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	Recommended operation	V_{SS}	—	–3.6 –5.5	—	–2.4 –1.8	V	V_{SS} *1
Supply voltage (2)	Recommended operation	V_{SS2}	—	–3.6 –5.5	—	–2.4 –1.8	V	V_{SS2} *2 *9
Supply voltage (3)	Recommended operation	V_5	When 1/4 bias used	–16.0	—	–5.0	V	V_5 *2
			When 1/5 bias used	–16.0	—	–4.5	V	
		V_1, V_2	—	0.6×V_5	—	V_{DD}	V	V_1, V_2
		V_3, V_4	—	V_5	—	0.4×V_5	V	V_3, V_4
HIGH-level input voltage (1)		V_{IHC}	V_{SS} = –2.4V to –1.8V	0.1×V_{SS}	—	V_{DD}	V	*3
LOW-level input voltage (1)		V_{ILC}		V_{SS}	—	0.9×V_{SS}	V	
HIGH-level input voltage (2)		V_{IHC}	V_{SS} = –5.5V to –2.4V	0.2×V_{SS}	—	V_{DD}	V	
LOW-level input voltage (2)		V_{ILC}		V_{SS}	—	0.8×V_{SS}	V	
Input leak current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	µA	*3
Liquid crystal driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V	—	20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}	—	—	0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5=–6V no load	—	—	80	µA	V_{DD} *5
		At standby	Oscillation ON, power OFF	—	—	20	µA	V_{DD} *6
		At sleep	Oscillation OFF, power OFF	—	—	5	µA	V_{DD}
		During access	fcyc=200KHZ	—	—	500	µA	V_{DD} *7
Input pin capacity		C_{IN}	Ta=25°C f=1MHZ	—	5.0	8.0	pF	*3

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{CK}	2-line display (S1D12402)	—	28.8	—	KHz	*10 *11
	f_{CK}	3-line display (S1D12401)	—	41.6	—	KHz	*10 *11
	f_{CK}	4-line display (S1D12400)	—	54.4	—	KHz	*10 *11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Minimum reset pulse width	t_{RW}	—	10	—	—	µs	*8
Reset start time	t_{RES}	—	—	—	50	ns	*8

Dynamic system

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Built-in power supply	Input voltage	V_{SS2}	Double boosting	–5.5	—	–1.8	V	V_{SS2}
			Triple boosting	–5.5	—	–1.8		
	Boosting output voltage	V_{OUT}	Double boosting	–11.0	—	—	V	V_{OUT}
			Triple boosting	–16.5	—	—		
	Voltage regulating circuit operating voltage	V_{OUT}	—	–16.5	—	–5.4	V	V_{OUT}
	Voltage follower operating voltage	V_5	—	–16.0	—	–4.5	V	V_5 *12
	Reference voltage	V_{REG}	Ta = 25°C –0.05%/°C	–2.06	–2.0	–1.94	V	—

*1: The wide operating voltage range is guaranteed except the case where a sudden voltage change occurs during MPU access.
In the low-supply voltage data holding characteristic, it is applied in the sleep mode and MPU access cannot be guaranteed

*2: At triple boosting, take care about supply voltage V_{SS2} so that it may not exceed the V_5 operating voltage range.

*3: D0 to D5, D6 (SCL), D7 (SI), A0, $\overline{RES}$, $\overline{CS}$, $\overline{WR}$ (E), P/S, IF. C86. $\overline{CK}$

*4: This is a resistance value when a voltage of 0.1 V is applied between output pins SEGn, SEGSn, COMn, and COMSn, and each power pin (V_1, V_2, V_3, V_4). This is specified within the range of operating voltage (2).

$R_{ON} = 0.1\ V / \Delta I$

(ΔI: A current flowing when 0.1 V is applied between the power supply and the output)

*5: Applies under the following conditions:
- No access from MPU during all characters 'HIGH' display
- The built-in circuit and oscillating circuit are operating.
- CGRAM unused, HPM = 0 specified, V_{SS} = -3.0

*6: Applies under the following conditions:
- Standby mode
- ALl the built-in power circuit off
- Display off
- Oscillating circuit on

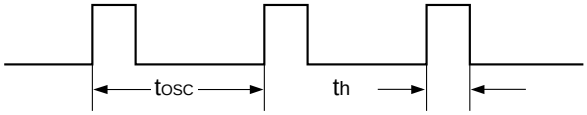
*7: Indicates that fcyc is used for writing at all times. The current consumption during access is approximately proportional to the access frequency (fcyc).

*8: Specifies the $\overline{RES}$ signal minimum pulse width. To perform resetting, it is necessary to input the pulse having a width of t_{RW} or more. Original, the method for reset case 1 is used, but the method for reset case 2 can also be used if the reset start time condition of t_{RES} or less is satisfied.

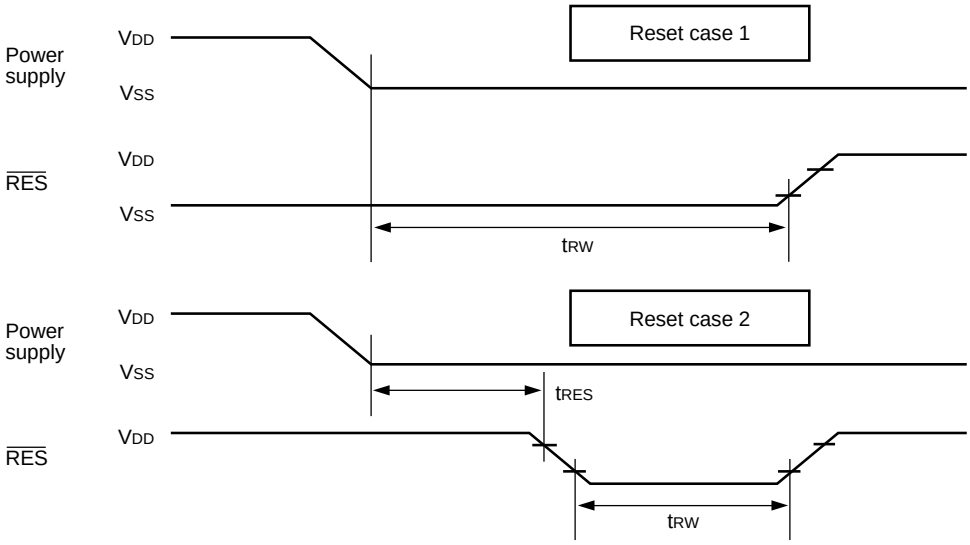
*9: The boosting circuit performs boosting, using voltage between the V_{DD} and V_{SS2} as source voltage. Check the V_{SS2} input voltage to ensure that it does not exceed V_{OUT} absolute maximum rating, or the operating voltage range of the V_{SS} system (V_{SS}) and V_5 system (V_5).

*10: Frequency f_{OSC} of the internal circuit drive oscillating circuit and boosting clock fBST vary according to the type. The following shows the relationship between the oscillating circuit f_{OSC} and boosting clock f BST:
- f_{OSC} = (number of digits) × (1/duty) × f_{FR}
- f_{BST} = (1/2) × (1/number of digits) × f_{OSC}

*11: Enter the following input when performing operations by the external clock, without using the built-in oscillating circuit:
- Duty = (t_h/t_{OSC}) × 100 = 20 to 30%
- $f_{OSC} = 1/t_{OSC}$



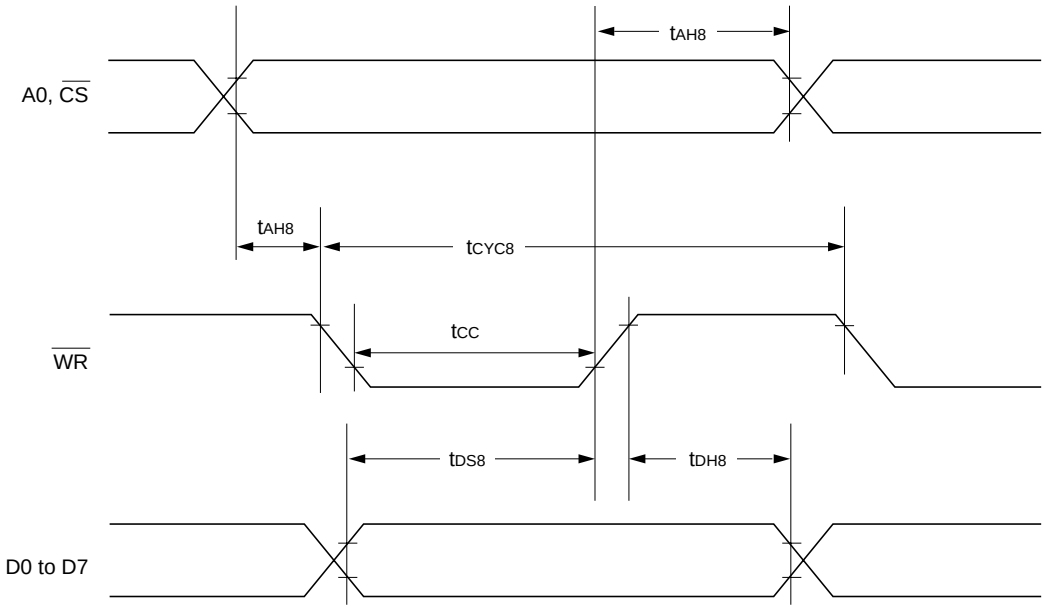
*12: Adjust the V_5 voltage regulating circuit within the voltage follower operating voltage range.



* All timing are specified on the basis of 20% and 80% of V_{SS}.

11. AC CHARACTERISTICS

System Bus Write Characteristics I (80 series MPU)



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	300	–	ns
Control pulse width (Write)		tCC	–	60	–	ns
Data setup time	D0 to D7	tDS8	–	60	–	ns
Data hold time		tDH8	–	50	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

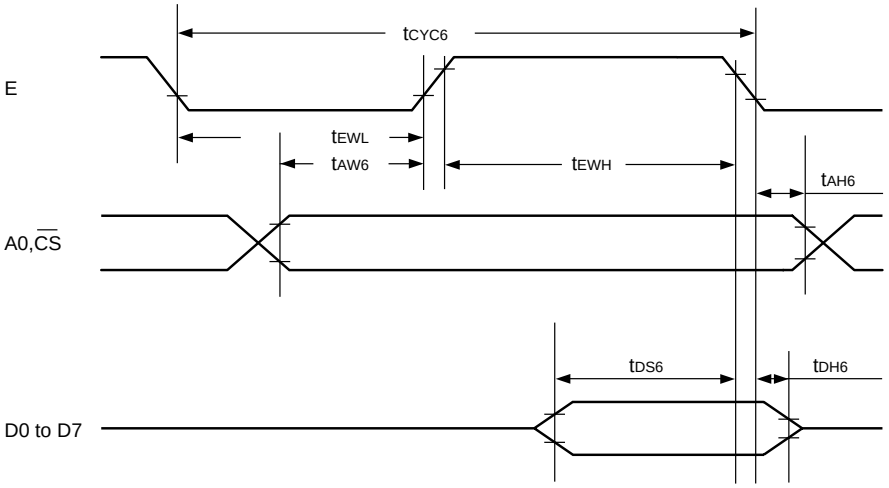
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	500	–	ns
Control pulse width (Write)		tCC	–	100	–	ns
Data setup time	D0 to D7	tDS8	–	100	–	ns
Data hold time		tDH8	–	50	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	1000	–	ns
Control pulse width (Write)		tCC	–	200	–	ns
Data setup time	D0 to D7	tDS8	–	200	–	ns
Data hold time		tDH8	–	50	–	ns

*1: At the fall and rise time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of VSS.
*3: The same timing is not required for A0 and CS. Input signals so that A0 and CS may satisfy tAW8 and tAH8 respectively.

System Bus Write Characteristics II (68 series MPU)



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	300	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	60	–	ns
Data hold time		tDH6	–	50	–	ns
Enable HIGH pulse width	E	tEWH	–	60	–	ns
Enable LOW pulse width	E	tEWL	–	60	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

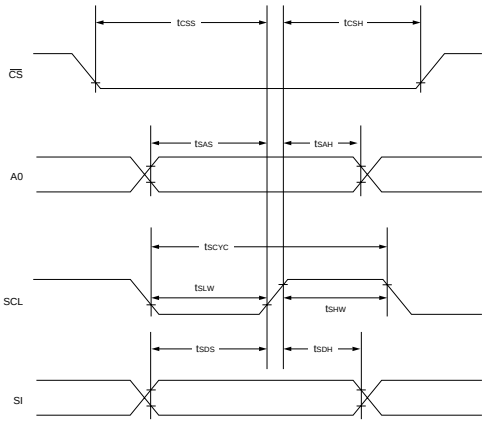
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	500	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	100	–	ns
Data hold time		tDH6	–	50	–	ns
Enable HIGH pulse width	E	tEWH	–	100	–	ns
Enable LOW pulse width	E	tEWL	–	100	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	1000	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	200	–	ns
Data hold time		tDH6	–	50	–	ns
Enable HIGH pulse width	E	tEWH	–	200	–	ns
Enable LOW pulse width	E	tEWL	–	200	–	ns

*1: tCYC6 indicates the cycle of the E signal in the $\overline{CS}$ active state.
It is necessary to secure tCYC6 after $\overline{CS}$ becomes active.
*2: For the rise and fall time of input signals, set 15 ns or less.
*3: Every timing is specified on 20% and 80% of VSS.
*4: The same timing is not required for A0 and $\overline{CS}$. Input signals so that A0 and $\overline{CS}$ may satisfy tAW6 and tAH6 respectively.

Serial Interface



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	700	–	ns
SCL HIGH pulse width		tSHW	–	250	–	ns
SCL LOW pulse width		tSLW	–	250	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	250	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	500	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	1000	–	ns
SCL HIGH pulse width		tSHW	–	300	–	ns
SCL LOW pulse width		tSLW	–	300	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	300	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	700	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C]

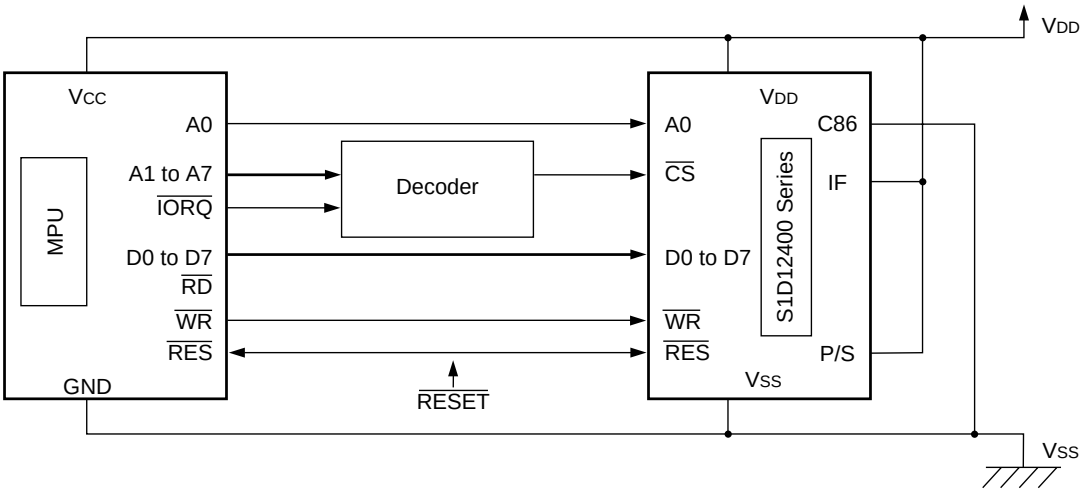
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	2000	–	ns
SCL HIGH pulse width		tSHW	–	300	–	ns
SCL LOW pulse width		tSLW	–	300	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	500	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	900	–	ns

*1: For the rise and fall time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of VSS.
*3: To validate a command or data immediately before the rise of $\overline{CS}$, tCSH must be satisfied at the latch timing of D0 data. If $\overline{CS}$ is started at another data latch timing, the previous command or data will not be input.

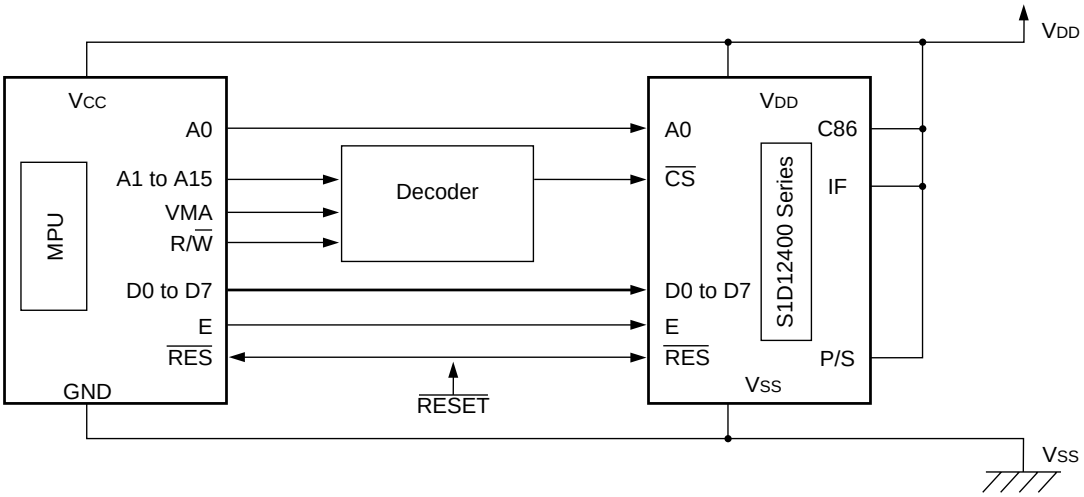
12. MPU INTERFACE CONNECTION EXAMPLES (FOR REFERENCE)

The S1D12400 series can be connected to the 80 series MPU or 68 series MPU. Furthermore, it can be operated with less signal lines if the serial interface is used.
When an MPU bus, port, etc. are put into high-impedance for a certain period by RESET, input RESET into this machine after the input to the S1D12400 series becomes definitive.

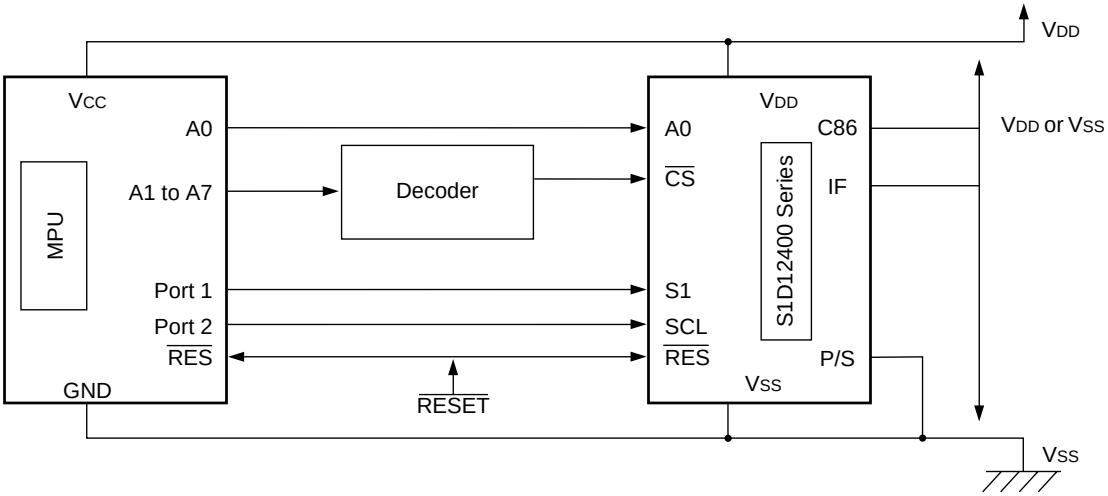
80 Series MPU



68 Series MPU

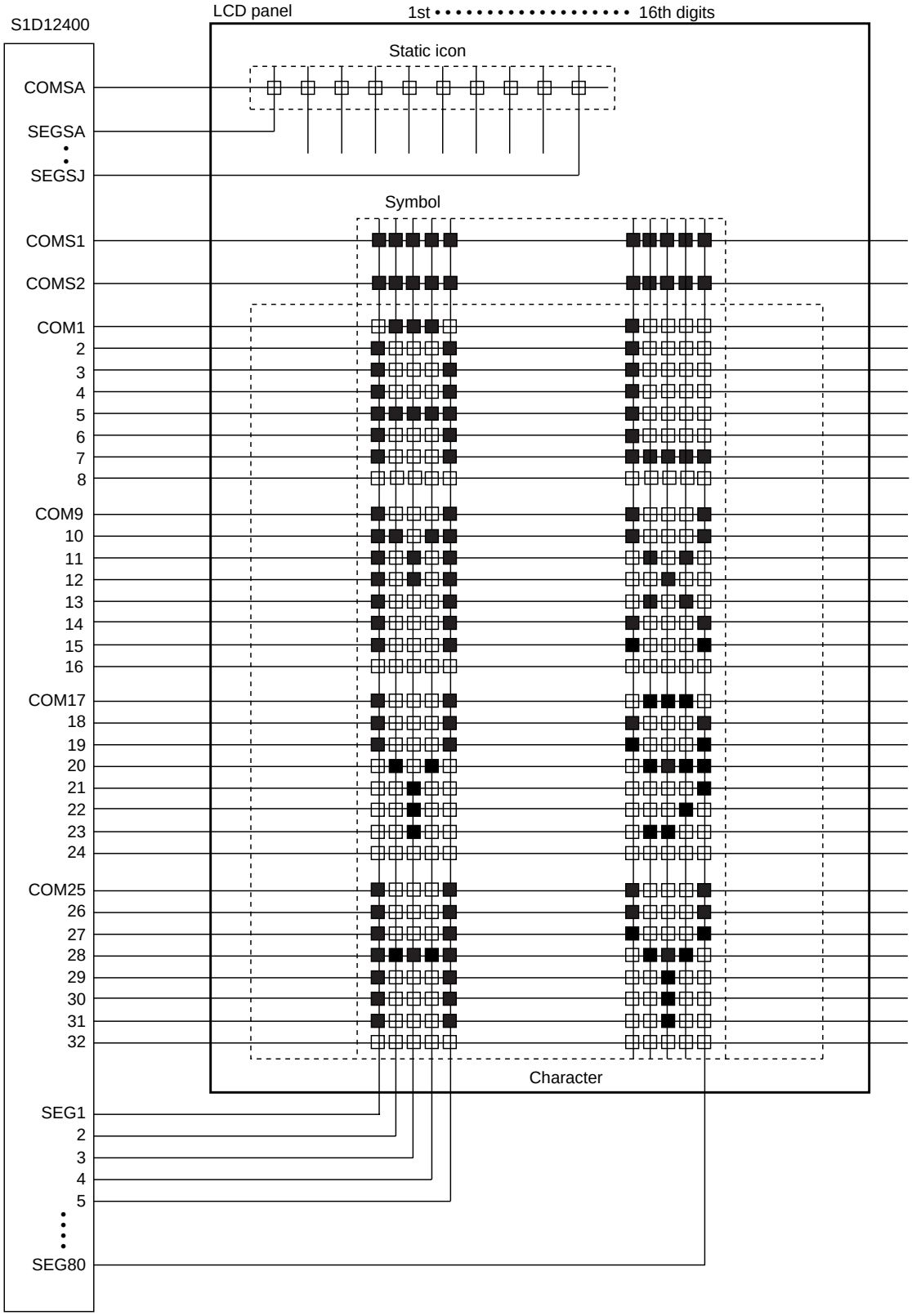


Serial Interface

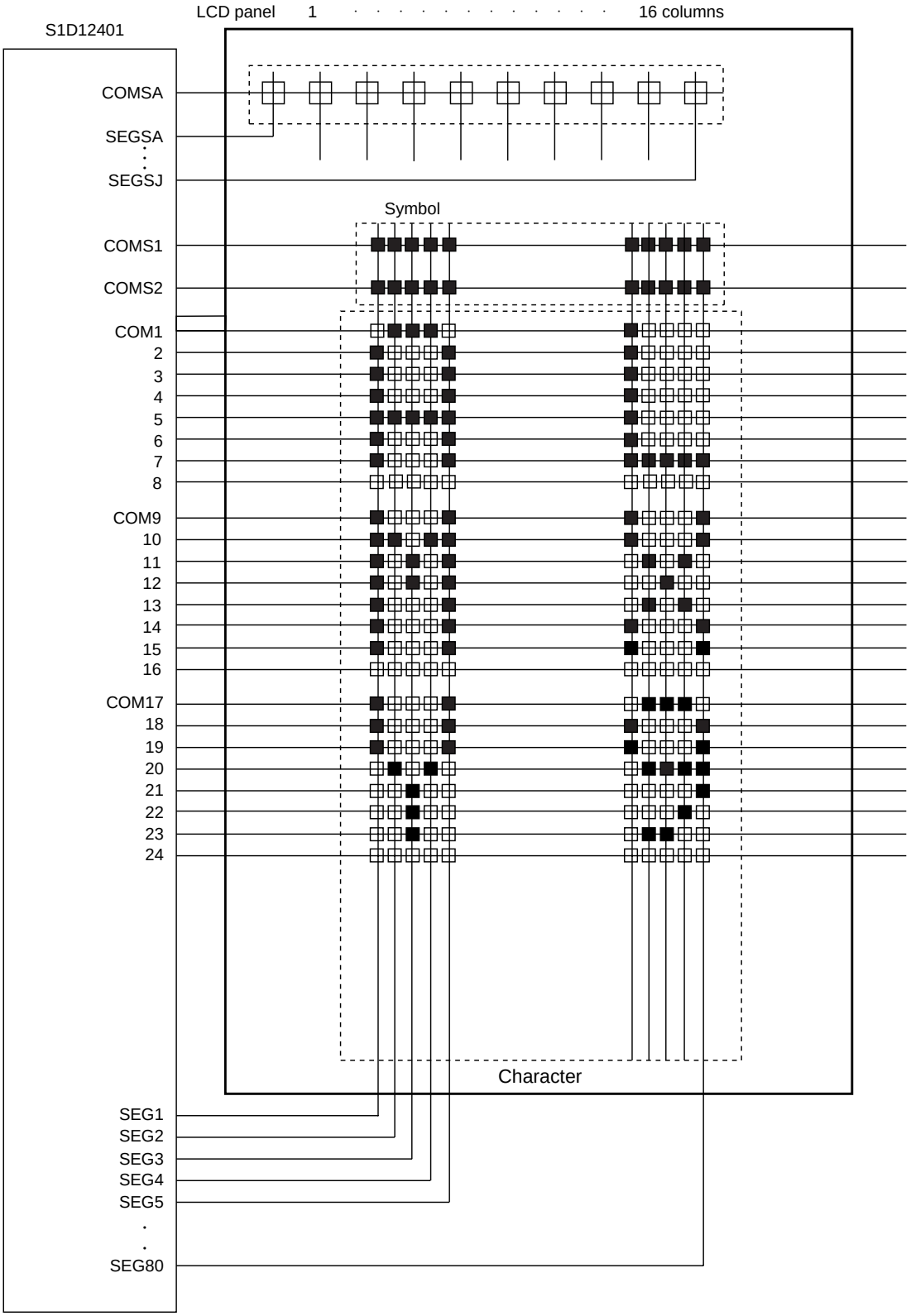


13. INTERFACE WITH LCD CELL (FOR REFERENCE)

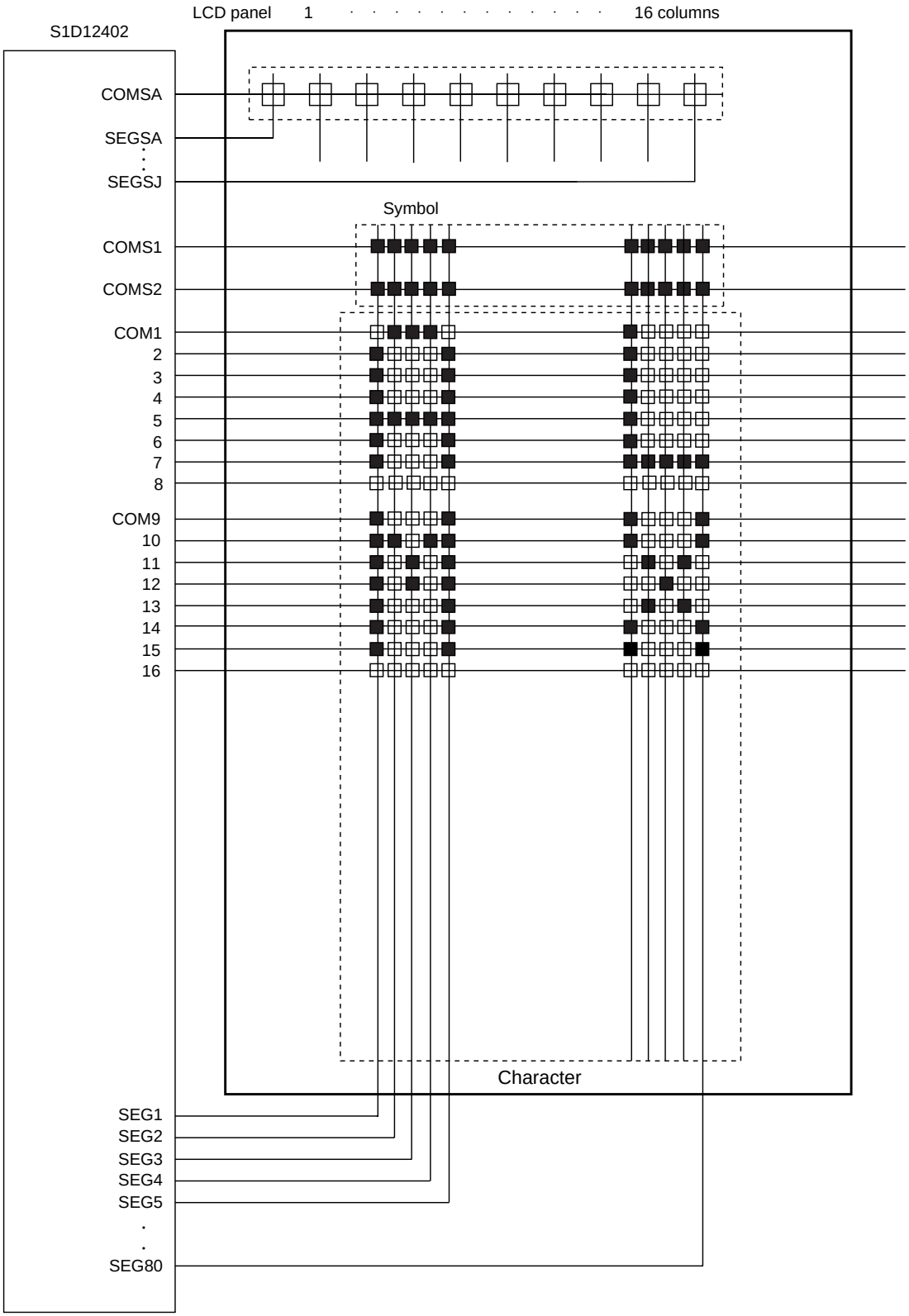
[16 digits × 4 line 5 × 8 dots + symbol]



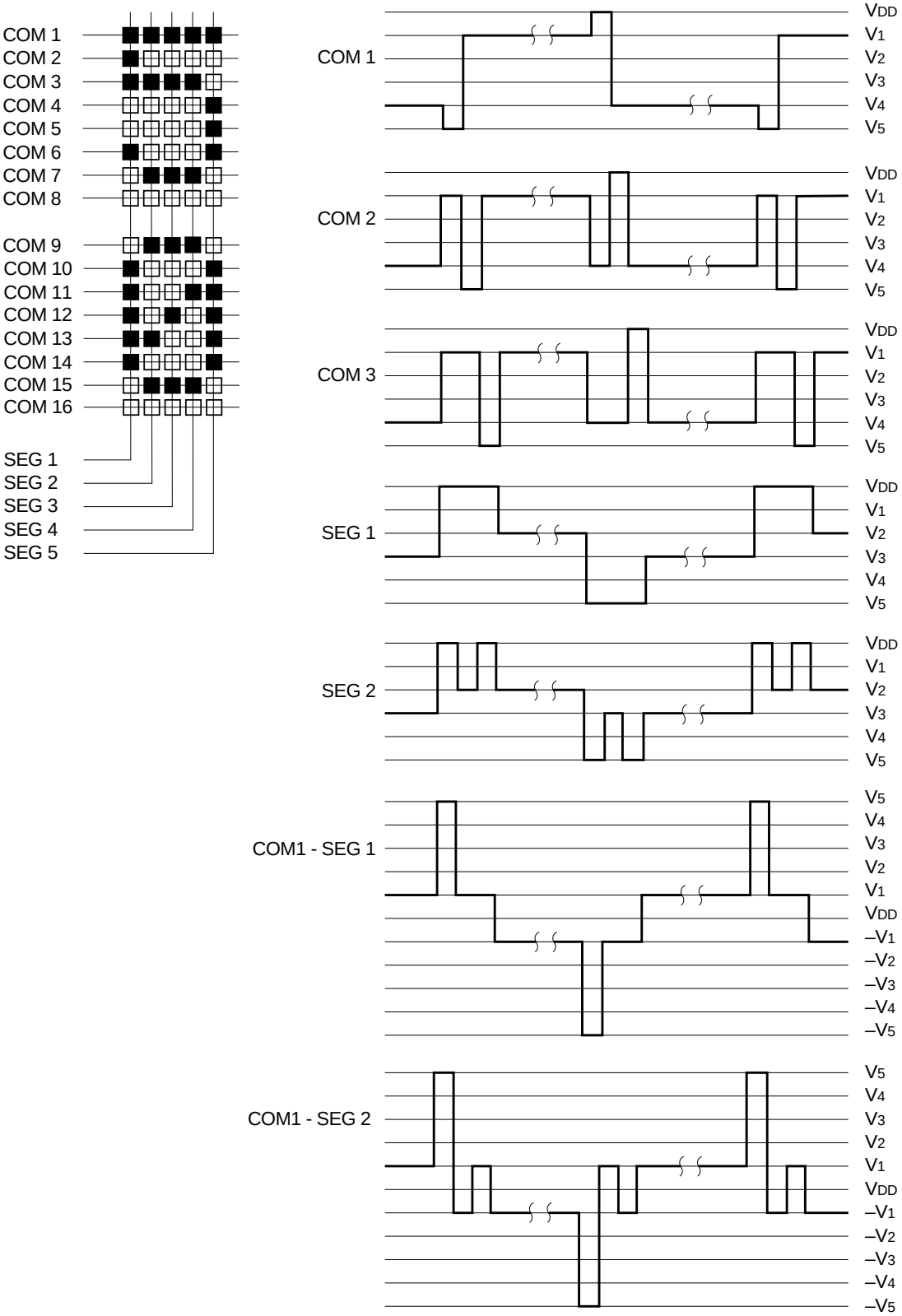
[16 digits × 3 line 5 × 8 dots]



[16 digits × 2 line 5 × 8 dots]



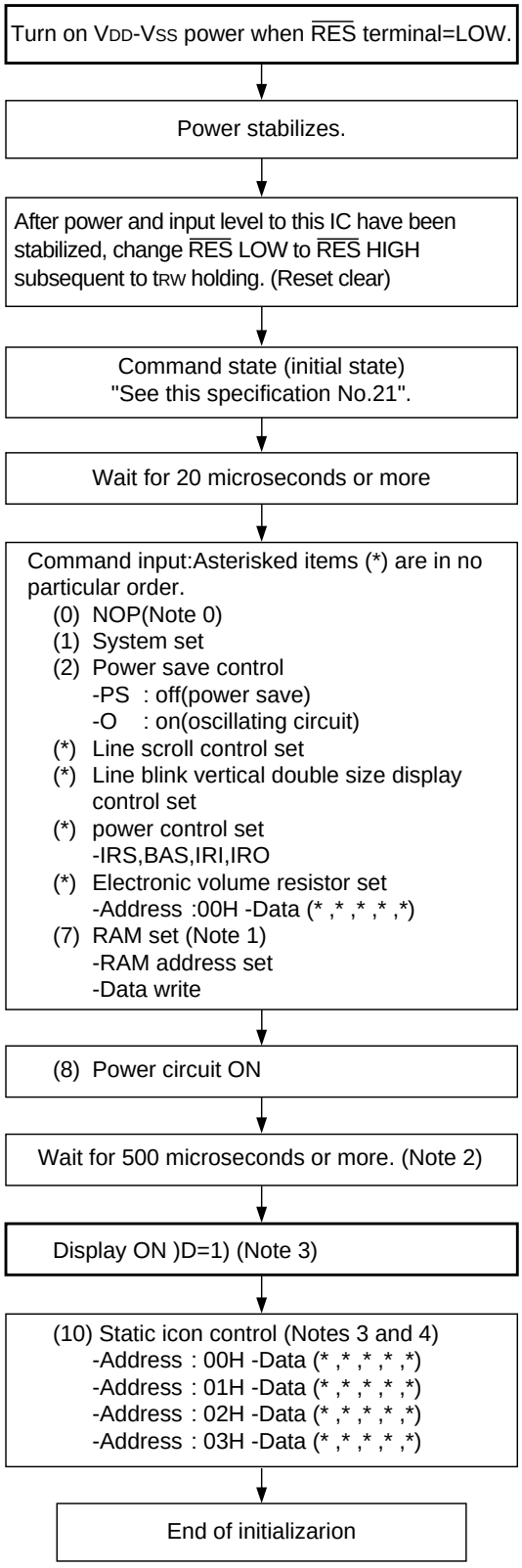
14. LCD DRIVE WAVEFORM (B WAVEFORM)



15. INSTRUCTION SETUP EXAMPLE (REFERENCE)

(1) Initialization

This IC has no power-on reset function when power is turned on. Accordingly, the IC internal status is indefinite when the power has been turned on. Be sure to initialize the system. If electric charge remains in the smoothing capacitor connected between the liquid crystal drive voltage output terminal (V_1 to V_5) and V_{DD} terminal, such a trouble as temporary blackening will occur when power is turned on. To avoid such a trouble, follow the steps given below:



Note 0 : (0) is a NOP command. This command has a function to clear the test mode. After resetting, it is recommended to execute this command several times before starting input. It is also recommended to execute it on a periodic basis at a proper position of the insutruction.

Note 1: (7) denotes RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM clear), use the following steps:

- DDRAM - write 20H (character code).
- CGRAM - write 00H (data "0").
- Symbol register - write 00H (data "0").

The RAM data is unspecified at the time of RES input (after power is turned on). If the data "0" is not written at this stage, unexpected display may occur to the unset position.

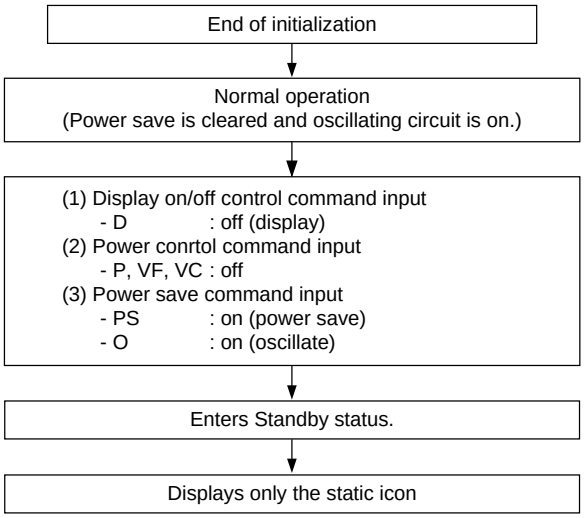
Note 2: Defined by the rising characteristics of the boosting circuit, power regulating circuit and voltage and follower circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3: The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

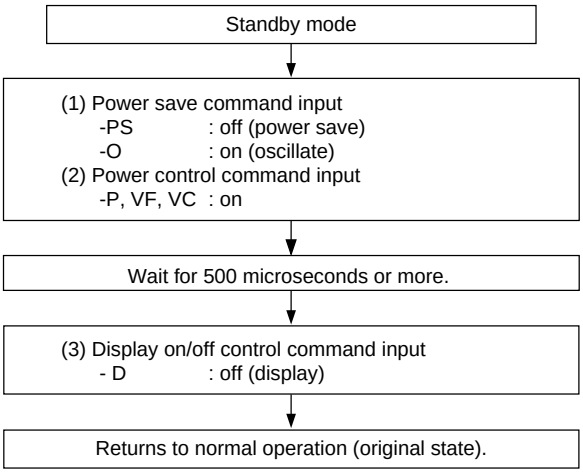
Note 4: Static icon control must be operated when the oscillating circuit is on. (This is mandatory.)

Note 5: (0) to (8) must be performed when display is off.

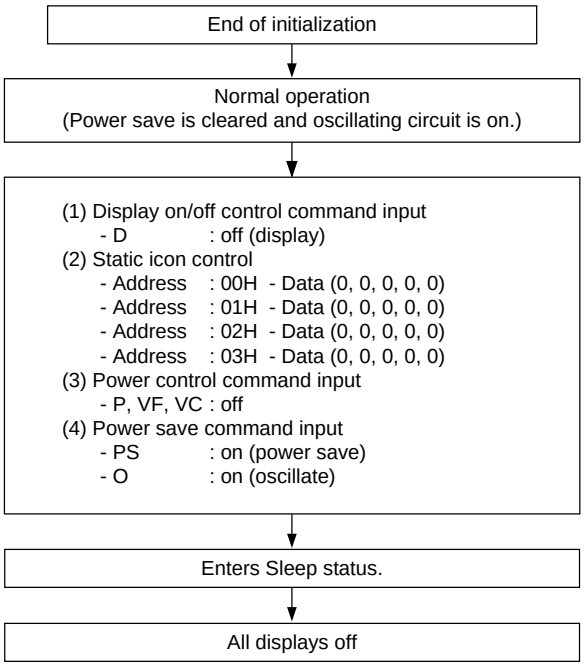
(2-1) Setting the Standby mode



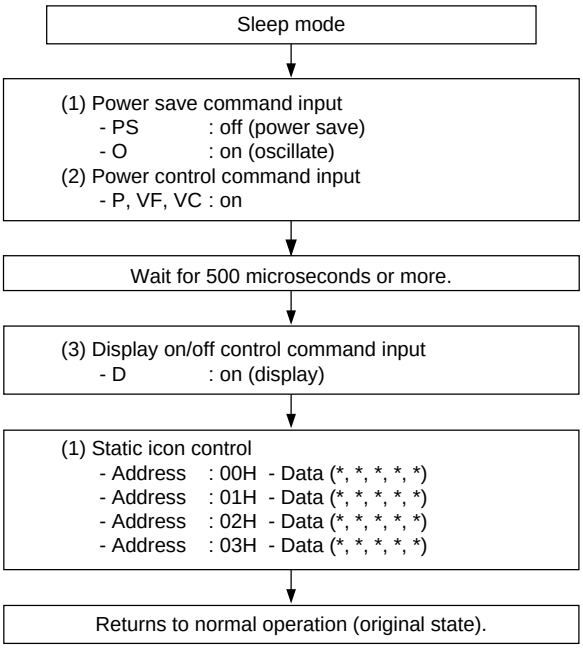
(2-1) Resetting the Standby mode



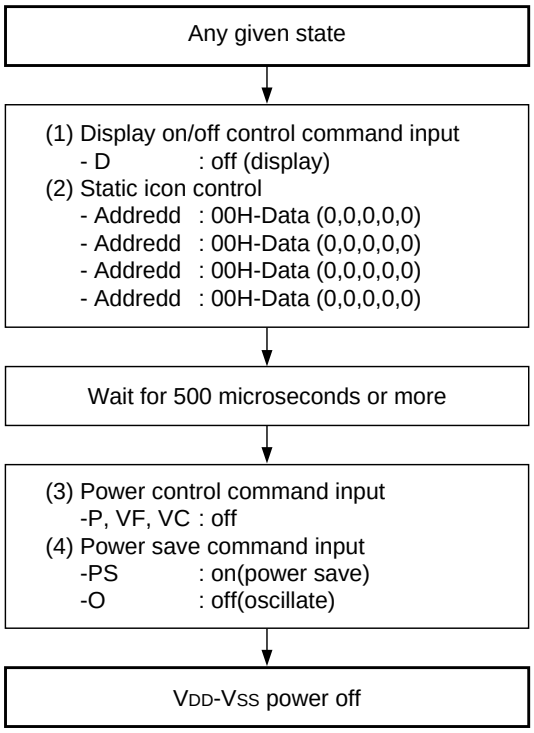
(3-1) Setting the Sleep mode



(3-1) Resetting the Sleep mode



(4) Power off sequence
Similar to the case of power on sequence, if this IC power is turned off when the built-in power is on, power supply to the built-in liquid crystal drive circuit may continue for a very little time, adversely affecting the liquid crystal panel display quality. To prevent this, strictly follow the power off sequence.



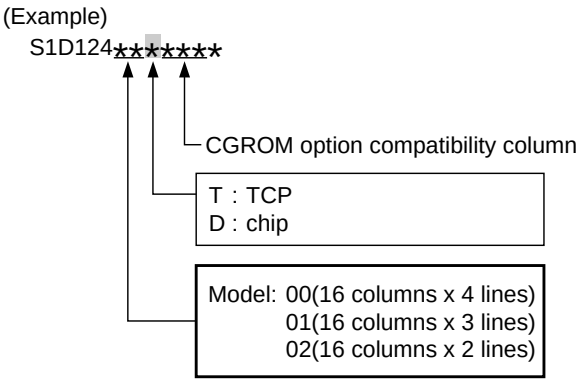
Note: This IC is configured as a logic circuit with a power supply of V_{DD}–V_{SS} which controls the LCD power supply V_{DD}–V_5 driver. Therefore, if the power supply V_{DD}–V_{SS} is shut down while voltage remains in the LCD power supply V_{DD}–V_5, the driver (COM and SEG) may output an uncontrolled voltage. When shutting the power off, be sure to observe the following operation procedure.

- Turn the internal power supply off, confirm that the voltage levels of the internal voltage follower outputs V_1, V_2, V_3 and V_4 have dropped below the LCD panel threshold voltage values, then turn the power of this IC (V_{DD}–V_{SS}) off.

16. OPTIONS LIST

The S1D 12400 series has the following options. Options are available exclusively for users. Please contact our Sales Department.

○ The following shows how to define the name of the product compatible with options:



Character Generator ROM (CGROM) Specifications

The S1D12400 series is provided with a character generator ROM for up to 544 types of characters. Each character size is of a structure of 5 × 7 (8) dots.

This CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

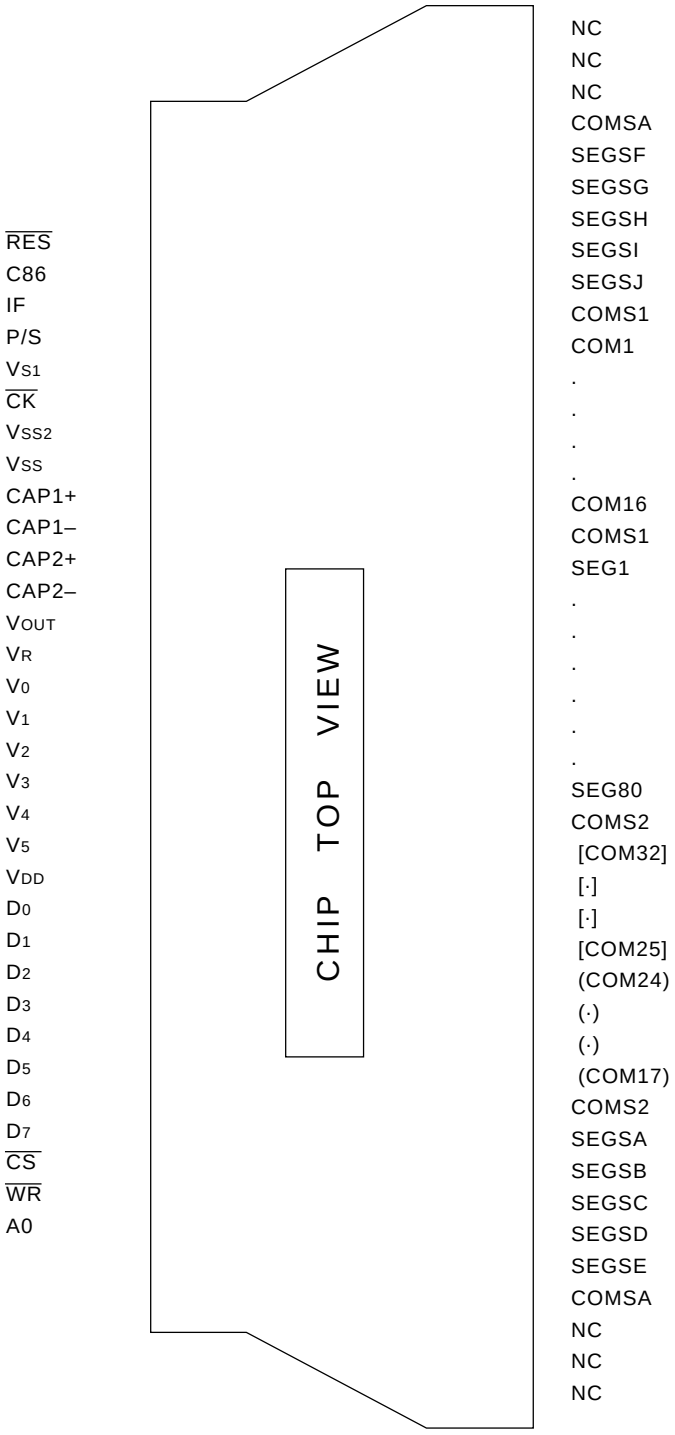
TCP Specifications

The S1D12400 series is compatible with the TCP specifications exclusive to the user, in addition to our standard TCP. Please contact our Sales Department for information.

17. EXAMPLE OF TCP ARRANGEMENT

Note: The following does not specify the TCP external view.

REFERENCE

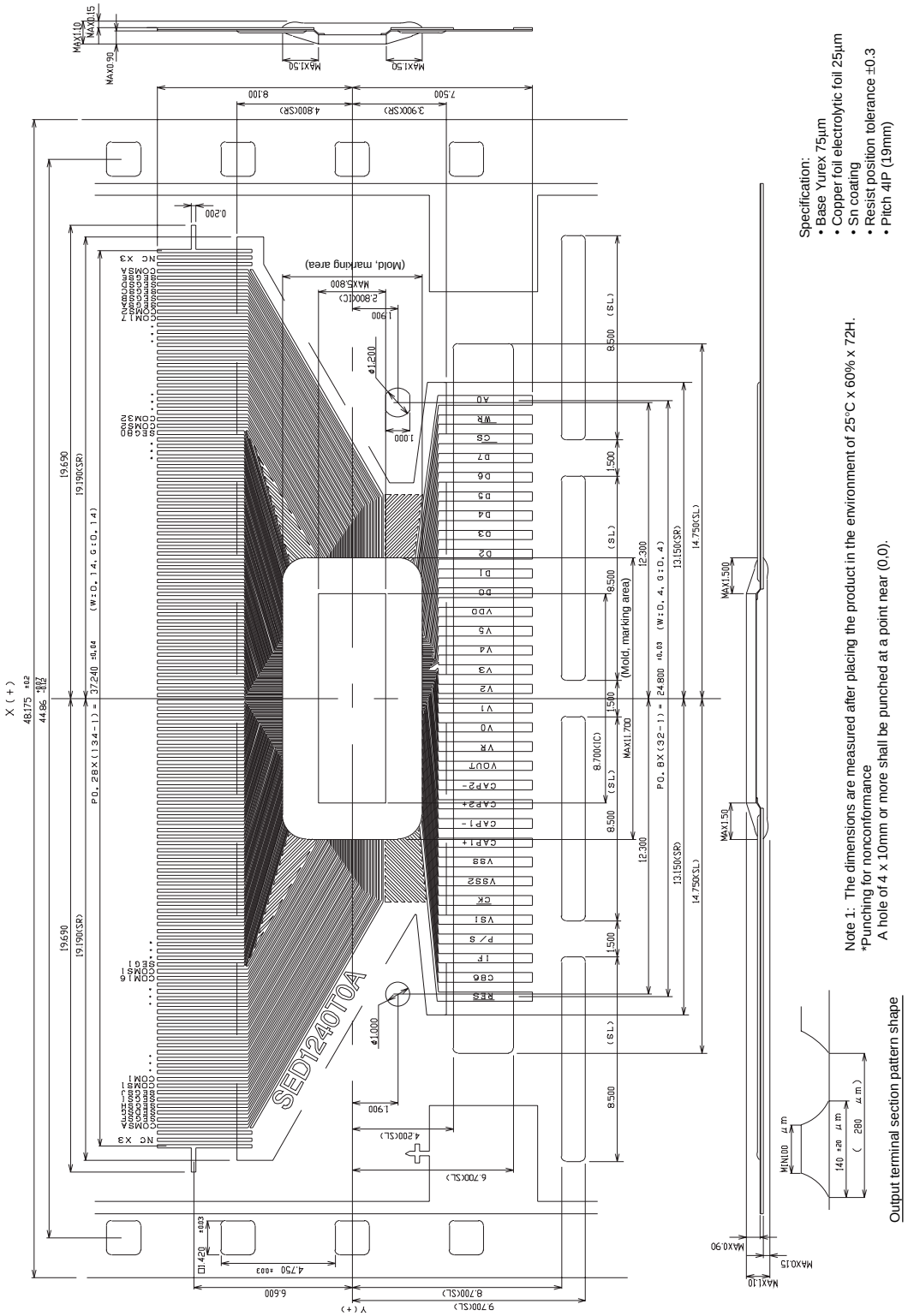


S1D12400T∗∗∗∗: COM1 to 16, (COM17 to 24) and [COM25 to 32] are used.
S1D12401T∗∗∗∗: COM1 to 16 and (COM17 to 24) are used. [COM25 to 32] is for NC.
S1D12402T∗∗∗∗: COM1 to 16 is used. (COM17 to 24) and [COM25 to 32] are for NC.

18. EXAMPLE OF TCP

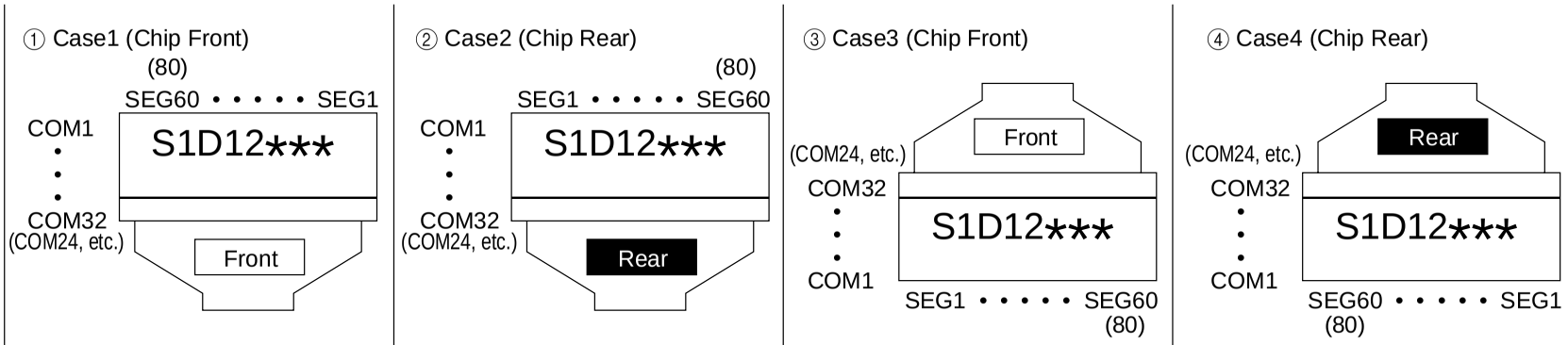
TCP External View

REFERENCE



S1D12200/12205/12400 Example of System Setup Depending on Mount Direction

Reference



	① Case1 (Chip Front)	② Case2 (Chip Rear)	③ Case3 (Chip Front)	④ Case4 (Chip Rear)
S1D12200	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
S1D12205	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
S1D12400	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "S1D12***" from the first digit of the first line shall be 3FH and 3EH, in this order.

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