Power Operational Amplifiers

FEATURES

- Low Cost Integrated Solution
- Output Current >10A Within SOA
- Internal Power Dissipation 35 W Per Channel
- 167V/µS Slew Rate

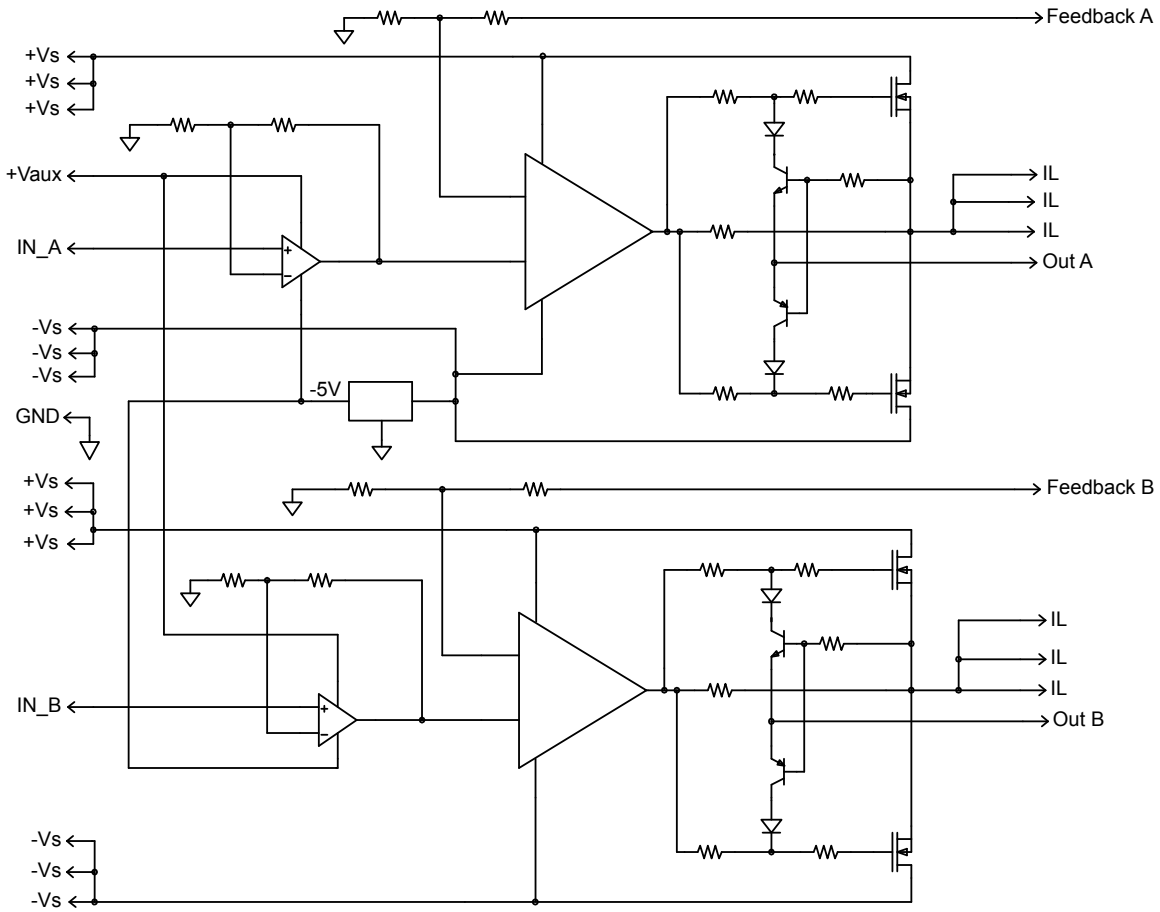
APPLICATIONS

- Piezoelectric Actuation For Ink Jet Printer Nozzles

GENERAL DESCRIPTION

The MP103 is a high voltage, high output current dual channel operational amplifier for driving capacitive loads such as piezo devices use in ink jet printing applications. The MP103 utilizes proprietary IC's combined with discrete semiconductor and passive elements on a thermally conductive insulated metal substrate, delivering very high power from a compact module. The amplifier gain is fixed at 65 V/V when the feedback pin is connected to the V_{OUT} pin. Internal compensation provides optimum slew rate and insures stability. The only external components required are the current limit resistors R_{LIM}, a series isolation resistor R_S and the power supply bypass capacitors.

EQUIVALENT CIRCUIT DIAGRAM



CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	$+V_S$ to $-V_S$		200	V
SUPPLY VOLTAGE, $-V_S$	$-V_S$	-30		V
SUPPLY VOLTAGE, $+V_{AUX}$	$+V_{AUX}$		30	V
OUTPUT CURRENT, pk, per Channel (Within SOA)	$I_{O(PK)}$		15	A
POWER DISSIPATION, internal, Each Channel	P_D		35	W
INPUT VOLTAGE	V_{IN}	-5	V_{AUX}	V
TEMPERATURE, pin solder, 10s			225	°C
TEMPERATURE, junction (Note 2)	T_J		150	°C
TEMPERATURE RANGE, storage	T_S	−40	105	°C

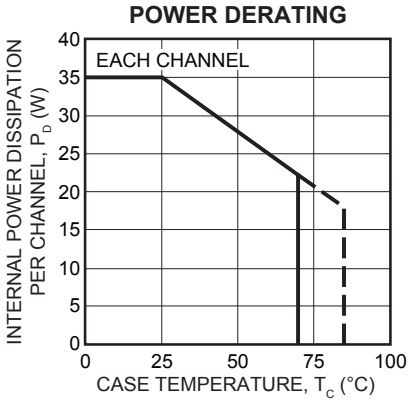
SPECIFICATIONS

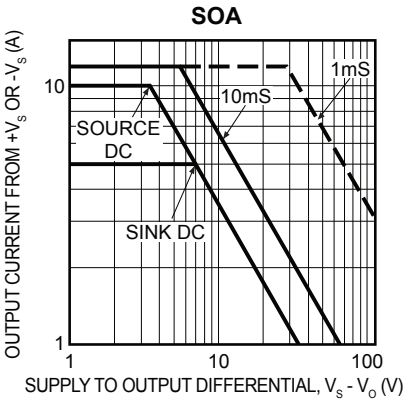
Parameter	Test Conditions	Min	Typ	Max	Units
INPUT (Each Channel)					
OFFSET VOLTAGE		-6.7	±2	6.7	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		±2		µV/°C
BIAS CURRENT, initial (Note 3)		-6.6	±3.3	6.6	µA
INPUT RESISTANCE, DC			300		KΩ
INPUT CAPACITANCE			1.5		pF
INPUT VOLTAGE RANGE		-3.4		$+V_{AUX}$ - 2	V
NOISE	f = 10KHz		600		nV/√Hz
GAIN (Each Channel)					
FIXED GAIN	Feedback connected to V_{OUT}	63.5	65	66.5	V/V
GAIN BANDWIDTH, -3db	C_L = 47nF		230		KHz
POWER BANDWIDTH, $130V_{P-P}$	$+V_S$ = 145V, $-V_S$ = -15V		230		KHz
OUTPUT (Each Channel)					
VOLTAGE SWING	I_O = 10A	$+V_S$ - 15	$+V_S$ - 9		V
VOLTAGE SWING	I_O = -5A	$-V_S$ + 15	$-V_S$ + 14		V
CURRENT, Peak, Source			12		A
SLEW RATE	R_S=1.0Ω, C_L=47nF, $V_{IN} \geq 8V_{P-P}$	167			V/µS
POWER SUPPLY (Note 4)					
VOLTAGE, $-V_S$		-7	-15	-20	V
VOLTAGE, $+V_{AUX}$			24	25	V
VOLTAGE, $+V_S$		$-V_S$ + 20	145	$-V_S$ + 200	V
CURRENT, quiescent, $-V_S$			19	26	mA
CURRENT, quiescent, $+V_{AUX}$			13.5	15	mA
CURRENT, quiescent, $+V_S$			1	5	mA

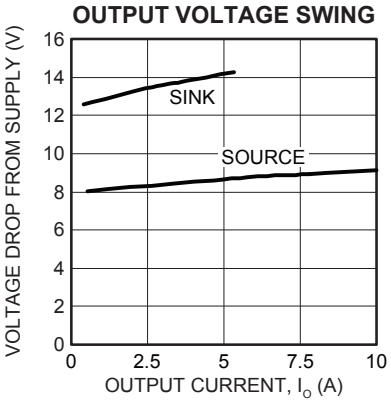
Parameter	Test Conditions	Min	Typ	Max	Units
THERMAL					
RESISTANCE, AC, junction to case (Note 5)	Full temperature range, f ≥ 60Hz		1.5	1.75	°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz		3.1	3.6	°C/W
RESISTANCE, junction to air	Full temperature range		12.5	14	°C/W
TEMPERATURE RANGE, case		0		70	°C

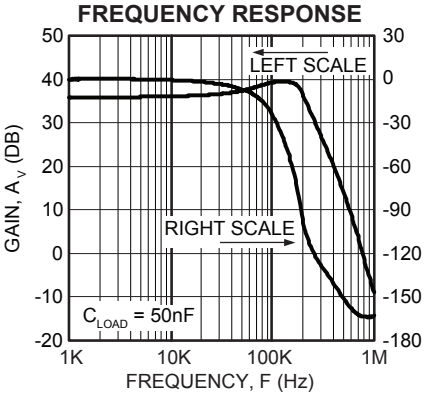
NOTES:

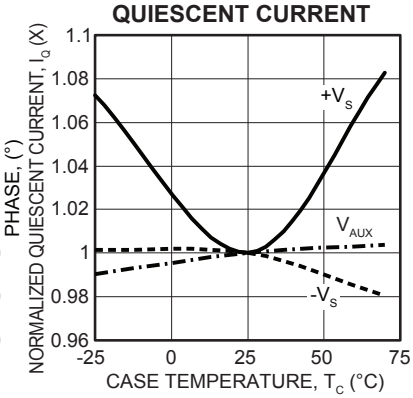
1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stages. $+V_{AUX}$ denotes the positive supply voltage to the input stages.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

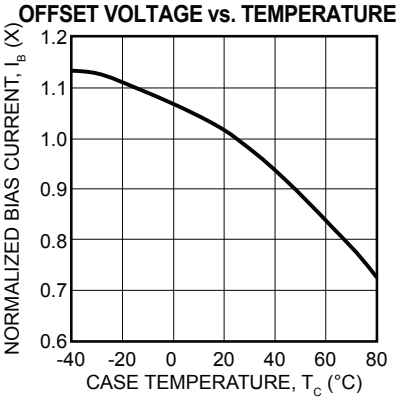


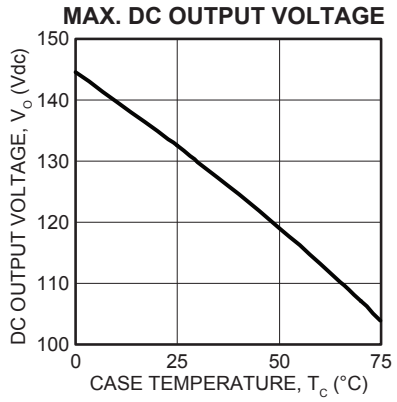


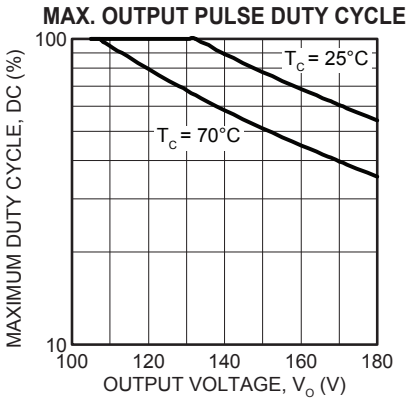


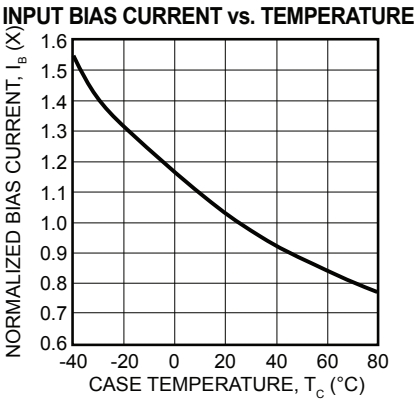


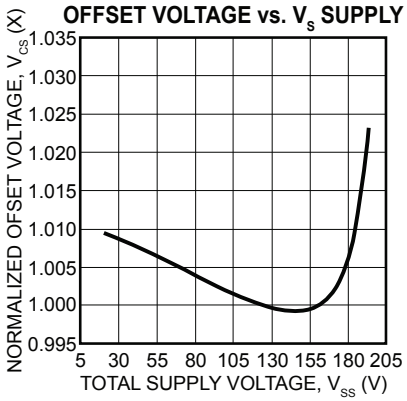


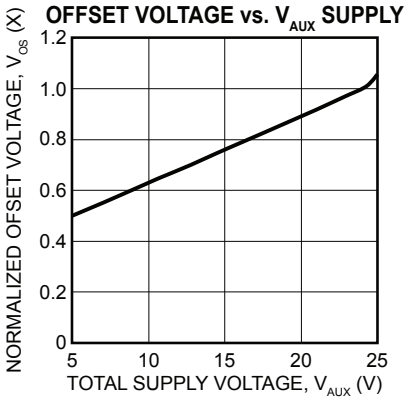


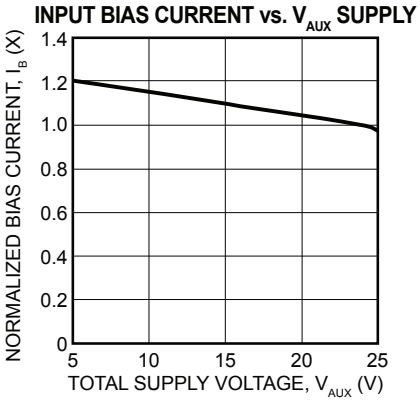


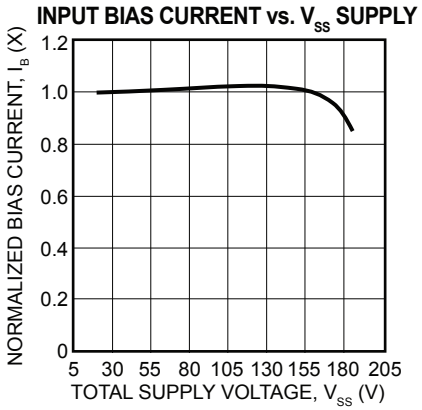


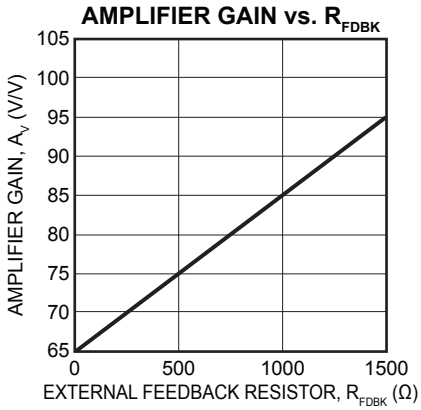


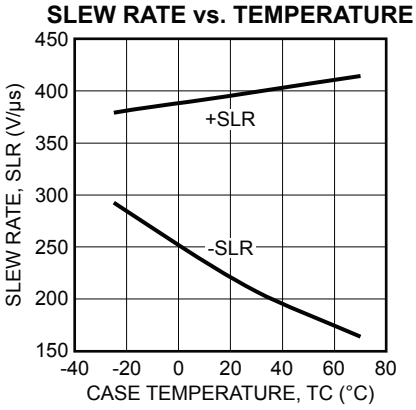




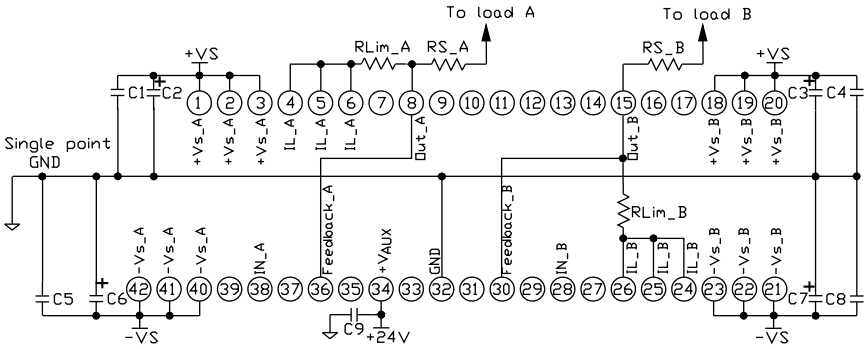


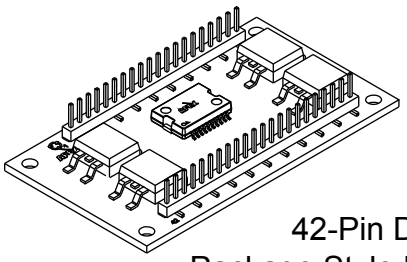






EXTERNAL CONNECTIONS





42-Pin DIP
Package Style FC

PIN DESCRIPTIONS

Pin #	Pin name	Description
1,2,3	$+V_S$_A	Positive high voltage power supply pins for channel A.
4,5,6	I_L_A	High current output pins for channel A. A current limit resistor must be placed between these pins and the output pin 8.
8	Out_A	Output pin for channel A.
15	Out_B	Output pin for channel B.
18,19,20	$+V_S$_B	Positive high voltage power supply pins for channel B.
21,22,23	$-V_S$_B	Negative power supply pins for channel B.
24,25,26	I_L_B	High current output pins for channel B. A current limit resistor must be placed between these pins and the output pin 15.
28	IN_B	Input pin for channel B.
30	Feedback_B	Feed back pin for channel B. This pin must be connected to output B pin 15 to close the feedback loop. When connected directly to pin 15 the closed loop voltage gain of channel B is 65 V/V. The gain can be increased by inserting a 1/4 W resistor between pins 30 and 15.
32	GND	Ground
34	$+V_{AUX}$	+24V voltage power supply pin. A 24 V power supply is required for operation of front end small signal circuitry of each channel.
36	Feedback_A	Feed back pin for channel A. This pin must be connected to output A pin 8 to close the feedback loop. When connected directly to pin 8 the closed loop voltage gain of channel A is 65 V/V. The gain can be increased by inserting a 1/4 W resistor between pins 36 and 8.
38	IN_A	Input pin for channel A.
40,41,42	$-V_S$_A	Negative power supply pins for channel A.

GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power’s complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

AMPLIFIER GAIN

When the feedback pin for each channel is connected to the corresponding OUT pin, the gain of the amplifier is internally set to 65 V/V. The amplifier gain can be increased by connecting a resistor between the feedback and Out pin. The amplifier gain will be increased approximately 1 V/V for each additional 49.9Ω added between the feedback and OUT pin.

SAFE OPERATING AREA

The MOSFET output stage of the MP103 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP103. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. Duplicate the supply bypass for the supply terminals of each amplifier channel. A bypass capacitor of 0.1µF or greater is recommended for the $+V_{AUX}$ terminal.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30Ω. The current limit function can be disabled by shorting the I_L pin to the OUT pin.

$$R_{LIM} = 0.7/I_{LIM}$$

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

SERIES ISOLATION RESISTOR, R_S

To insure stability with all capacitive loads a series isolation resistor should be included between the output and the load as shown in the external connections drawing. A 1Ω resistor works well for capacitive loads between 135pF and 44nF. The resistor will affect the rise and fall time of the output pulse at the capacitive load. This can be compensated for on the input signal.

BACKPLATE GROUNDING

The substrate of the MP103 is an insulated metal substrate. It is required that it be connected to signal ground. This is accomplished when the ground pin (Pin 32) is properly connected signal ground.

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
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