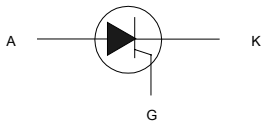
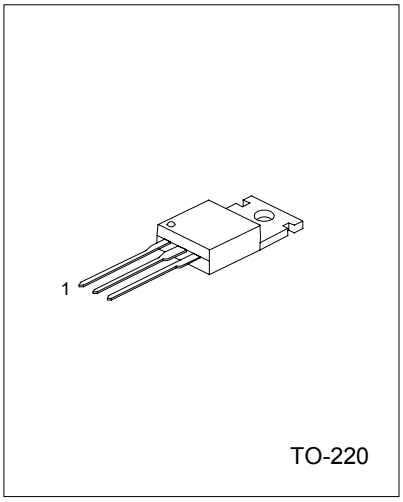
SCRs

DESCRIPTION

Thanks to highly sensitive triggering levels, the UTC US104S is suitable for all applications where the available gate current is limited, such as motor control for hand tools, kitchen aids, overvoltage crowbar protection for low power supplies, ... Available in through-hole or surface-mount packages, they provide an optimized performance in a limited space area.

SYMBOL





1: CATHODE 2: ANODE 3: GATE

ABSOLUTE RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Repetitive peak off-state voltages and Repetitive peak reverse voltage US104S/N-4 US104S/N-6 US104S/N-8	V_{DRM}, V_{RRM}	 400 600 800	V
RMS on-state current (180° conduction angle) (Tc = 115°C)	$I_{T(RMS)}$	4	A
Average on-state current (180° conduction angle) (Tc = 115°C)	$I_{T(AV)}$	2.5	A
Non repetitive surge peak on-state current (Tj = 25°C) tp=8.3ms tp=10ms	I_{TSM}	 33 30	A
I^2t Value for fusing (tp = 10 ms, Tj = 25°C)	I^2t	4.5	A^2S
Critical rate of rise of on-state current (IG = 2 x IGT , tr ≤ 100 n s, F= 60 Hz ,Tj = 125°C)	dI/dt	50	A/μs
Peak gate current (tp=20μs, Tj = 125°C)	I_{GM}	1.2	A
Average gate power dissipation (Tj = 125°C)	$P_{G(AV)}$	0.2	W
Storage junction temperature range	Tstg	-40 ~ +150	°C
Operating junction temperature range	Tj	-40 ~ +125	°C

UTC US104S(SENSITIVE) ELECTRICAL CHARACTERISTICS

(Tj=25℃unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I_{GT}	V_D = 12 V, R_L =33Ω		200	μA
Gate trigger Voltage	V_{GT}	V_D = 12 V, R_L=33Ω		0.8	V
Gate non-trigger voltage	V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, R_{GK} = 220Ω Tj = 125°C	0.1		V
Reverse gate voltage	V_{RG}	I_{RG} = 10 μA	8		V
Holding Current	I_H	I_T = 50 mA, R_{GK} = 1 kΩ		5	mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Latching Current	I_L	I_G = 1 mA ,R_{GK} = 1 kΩ		6	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V_D = 67 % V_{DRM} ,R_{GK} = 220 Ω Tj = 125°C	5		V/μs
On-state voltage	V_{TM}	I_{TM} = 8 A, t_p = 380 μs Tj = 25°C		1.6	V
Threshold Voltage	V_{t0}	Tj = 125°C		0.85	V
Dynamic Resistance	R_d	Tj = 125°C		90	mΩ
Off-state Leakage Current	I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}, R_{GK} = 220 Ω Tj = 25°C		5	μA
		V_{DRM} = V_{RRM}, R_{GK} = 220 Ω Tj = 125°C		1	mA

UTC US104N(STANDARD) ELECTRICAL CHARACTERISTICS

(Tj=25℃unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I_{GT}	V_D = 12 V, R_L =33Ω	2	15	mA
Gate trigger Voltage	V_{GT}	V_D = 12 V, R_L=33Ω		1.3	V
Gate non-trigger voltage	V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, Tj = 125°C	0.2		V
Holding Current	I_H	I_T = 100 mA, Gate open		30	mA
Latching Current	I_L	I_G = 1.2 I_{GT}		60	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V_D = 67 % V_{DRM} , Gate open,Tj = 125°C	100		V/μs
On-state voltage	V_{TM}	I_{TM} =8A, t_p = 380 μs, Tj = 25°C		1.6	V
Threshold Voltage	V_{t0}	Tj = 125°C		0.85	V
Dynamic Resistance	R_d	Tj = 125°C		62	mΩ
Off-state Leakage Current	I_{DRM} I_{RRM}	V_{DRM} = V_{RRM} Tj = 25°C Tj = 125°C		5 2	μA mA

THERMAL RESISTANCES

PARAMETER	SYMBOL	VALUE	UNIT
Junction to case (DC)	Rth(j-c)	3.0	K/W
Junction to ambient (DC)	Rth(j-a)	60	K/W

Fig.1:Maximum average power dissipation vs average on-state current

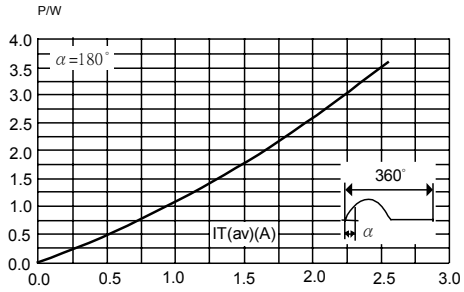


Figure.2:Average and D.C. on-state current vs case temperature

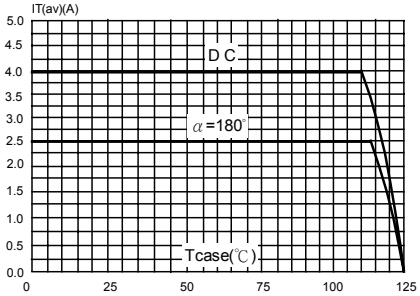


Figure.3:Relative variation of gate trigger current and holding current vs junction temperature.

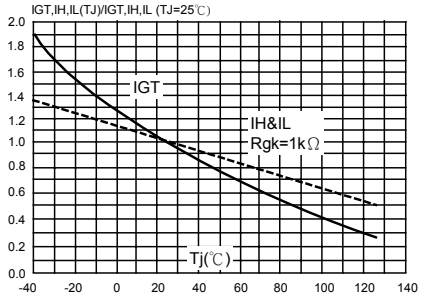


Figure.4:Relative variation of holding current vs gate-cathode vesistance(typical values).

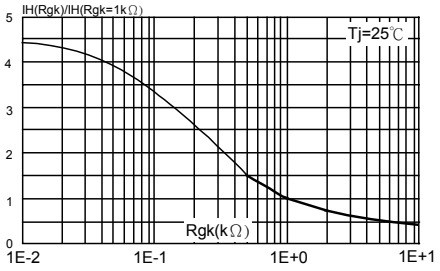


Fig.5: Relative variation of dV/dt immunity vs gate-cathode resistance(typical values).

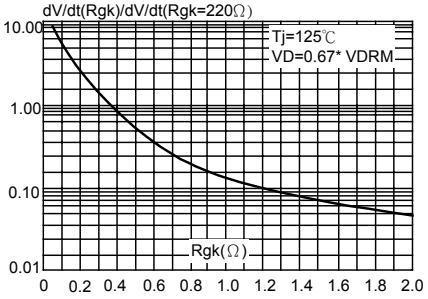


Fig.6: Relative variation of dV/dt immunity vs gate-cathode resistance(typical values).

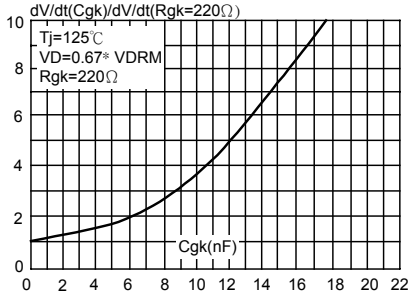


Figure.7: Surge peak on-state current vs number of cycles.

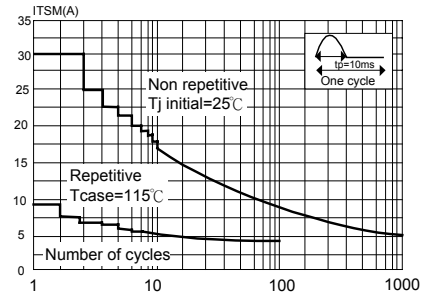


Fig.8:Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding values of I^2t.

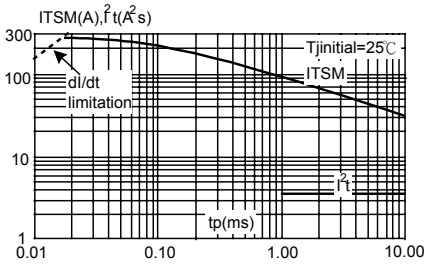


Fig.9: On-state characteristics(maximum values).