

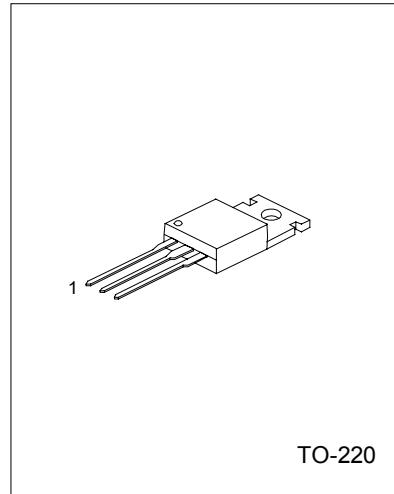
# UTC US112S/N

# SCR

## SCRs

### DESCRIPTION

The UTC US112S/N is suitable to fit all modes of control found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, in-rush current limiting circuits, capacitive discharge ignition, voltage regulation circuits...



TO-220

1: CATHODE    2: ANODE    3: GATE

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING		UNIT
		US112S	US112N	
Repetitive peak off-state voltages US112S/N-4 US112S/N-6 US112S/N-8	$V_{DRM}$ $V_{RRM}$	400 600 800		V
RMS on-state current (180° conduction angle) (T <sub>c</sub> = 105°C)	I <sub>T(RMS)</sub>	12		A
Average on-state current (180° conduction angle) (T <sub>c</sub> = 105°C)	I <sub>T(AV)</sub>	8		A
Non repetitive surge peak on-state current (T <sub>j</sub> = 25°C) tp=8.3ms tp=10ms	I <sub>TSM</sub>	146 140		A
I <sup>2</sup> t Value for fusing (tp = 10 ms, T <sub>j</sub> = 25°C)	I <sup>2</sup> t	98		A <sup>2</sup> S
Critical rate of rise of on-state current (IG = 2 x IGT, tr ≤ 100 n s, F = 60 Hz, T <sub>j</sub> = 125°C,)	dI/dt	50		A/μs
Peak gate current (tp=20μs, T <sub>j</sub> = 125°C)	I <sub>GM</sub>	4		A
Maximum peak reverse gate voltage	V <sub>RGPM</sub>		5	V
Average gate power dissipation (T <sub>j</sub> = 125°C)	P <sub>G(AV)</sub>	1		W
Storage junction temperature range	T <sub>stg</sub>	-40 ~ +150		°C
Operating junction temperature range	T <sub>j</sub>	-40 ~ +125		°C

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## UTC US112S(SENSITIVE) ELECTRICAL CHARACTERISTICS

(T<sub>j</sub>=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 140Ω		200	µA
Gate trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 140Ω		0.8	V
Gate non-trigger voltage	V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 kΩ, R <sub>GK</sub> = 1 kΩ T <sub>j</sub> = 125°C	0.1		V
Reverse gate voltage	V <sub>RG</sub>	I <sub>RG</sub> = 10 µA	8		V
Holding Current	I <sub>H</sub>	I <sub>T</sub> = 50 mA, R <sub>GK</sub> = 1 kΩ		5	mA
Latching Current	I <sub>L</sub>	I <sub>G</sub> = 1 mA, R <sub>GK</sub> = 1 kΩ		6	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> , R <sub>GK</sub> = 220 Ω T <sub>j</sub> = 125°C	5		V/µs
On-state voltage	V <sub>TM</sub>	I <sub>TM</sub> = 24A, t <sub>p</sub> = 380 µs, T <sub>j</sub> = 25°C		1.6	V
Threshold Voltage	V <sub>t0</sub>	T <sub>j</sub> = 125°C		0.85	V
Dynamic Resistance	R <sub>d</sub>	T <sub>j</sub> = 125°C		30	mΩ
Off-state Leakage Current	I <sub>IDRM</sub> I <sub>IRRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> , R <sub>GK</sub> = 220 Ω T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C		5 2	µA mA

## UTC US112N(STANDARD) ELECTRICAL CHARACTERISTICS

(T<sub>j</sub>=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 33Ω	2	15	mA
Gate trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 33Ω		1.3	V
Gate non-trigger voltage	V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 kΩ, T <sub>j</sub> = 125°C	0.2		V
Holding Current	I <sub>H</sub>	I <sub>T</sub> = 500 mA, Gate open		30	mA
Latching Current	I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>		60	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> , Gate open, T <sub>j</sub> = 125°C	200		V/µs
On-state voltage	V <sub>TM</sub>	I <sub>TM</sub> = 24A, t <sub>p</sub> = 380 µs, T <sub>j</sub> = 25°C		1.6	V
Threshold Voltage	V <sub>t0</sub>	T <sub>j</sub> = 125°C		0.85	V
Dynamic Resistance	R <sub>d</sub>	T <sub>j</sub> = 125°C		30	mΩ
Off-state Leakage Current	I <sub>IDRM</sub> I <sub>IRRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> , T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C		5 2	µA mA

## THERMAL RESISTANCES

PARAMETER	SYMBOL	VALUE	UNIT
Junction to case (DC)	R <sub>th(j-c)</sub>	1.3	K/W
Junction to ambient	R <sub>th(j-a)</sub>	60	K/W

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Figure.1:Maximum average power dissipation vs average on-state current.

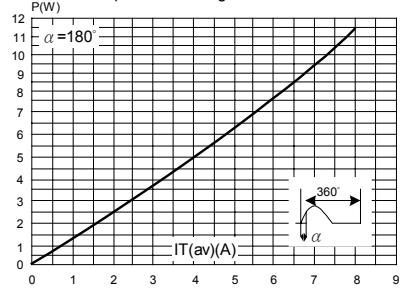


Figure.2:Average and D.C. on-state current vs case temperature

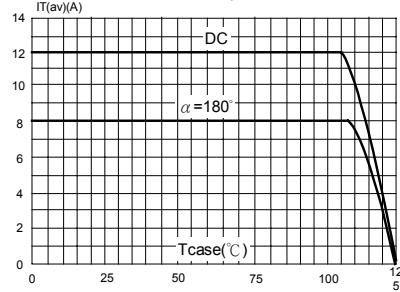


Fig.3-1:Relative variation of thermal impedance junction to case vs pulse duration.

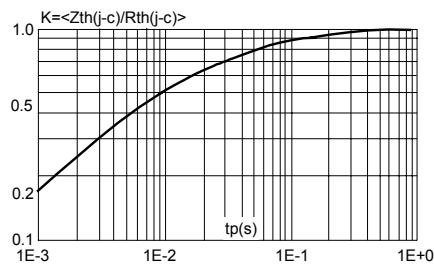


Fig.3-2:Relative variation of thermal impedance junction to ambient vs pulseduration (recommended pad layout,FR4 PC board)

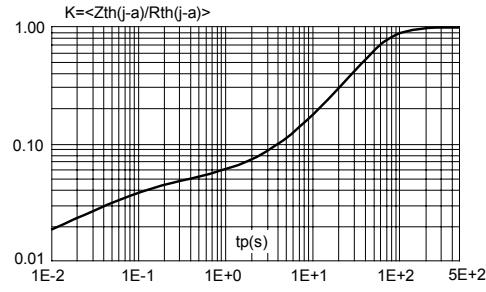


Figure.4-1:Relative variation of gate trigger current,holding current and latching vs junction temperature (US112S)

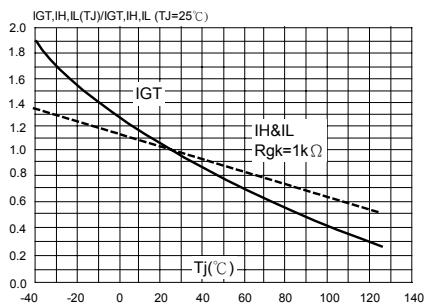


Figure.4-2: Relative variation of gate trigger current,holding current and latching current vs junction temperature (US112N).

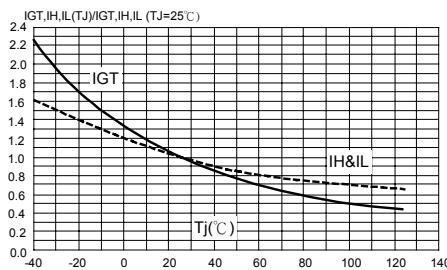


Figure 5: Relative variation of holding current vs gate-cathode resistance(typical values) (US112S)

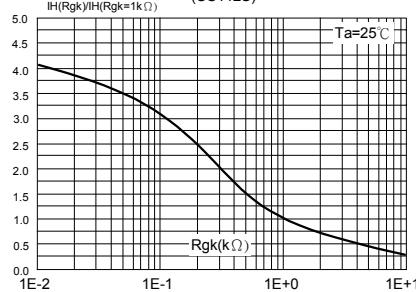


Fig.6: Relative variation of dV/dt immunity vs gate-cathode resistance(typical values) (US112S)

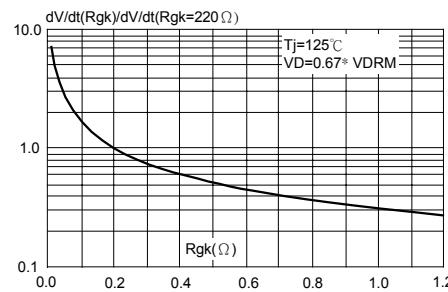


Fig.7: Relative variation of dV/dt immunity vs gate-cathode capacitance(typical values) (US112S)

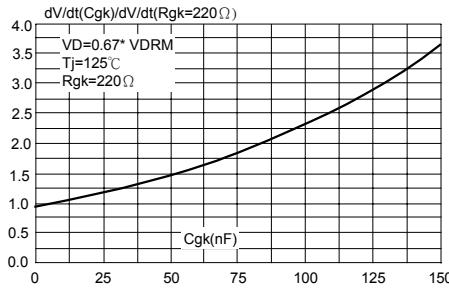


Fig.8: Surge peak on-state current vs number of cycles

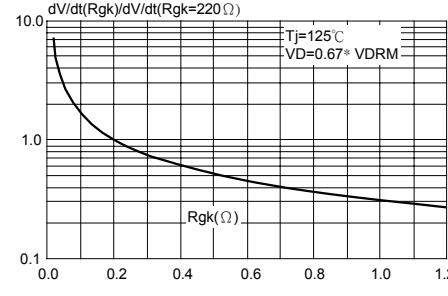


Fig.9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding values of  $I^2t$ .

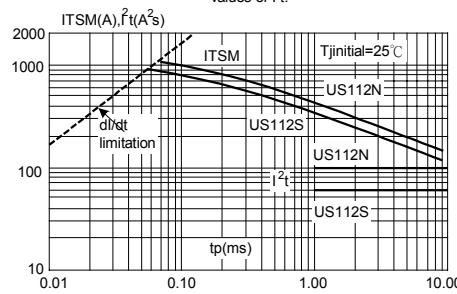
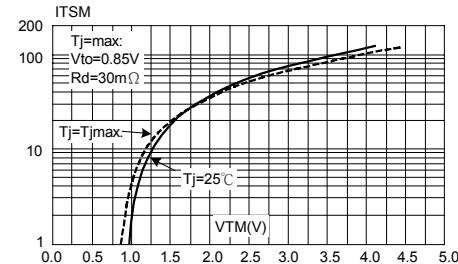


Fig.10: On-state characteristics(maximum values).



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