

**Monolithic IC for ATM to Ethernet Interworking at GE Wire Speed**

**FEATURES**

- The S/UNI DUPLEX GE is a monolithic integrated circuit supporting wire speed ATM to Ethernet inter-working at GE rates. It provides the AAL5 SARing, queuing/buffering, traffic management, address translation, and multicast functions necessary for interfacing an ATM Utopia Level 2/POS-PHY Level 2 interface to 10/100/1000 Ethernet interfaces.
- The extended (up to 144 ports) Utopia Level 2 bus is designed to accommodate the higher line densities typical of ADSL DSLAMs. The dual Ethernet integrated SERDES accommodates backplane applications where a 1:1 redundant Ethernet interface is required. A separate parallel Ethernet port creates the high performance local interface needed for packet add/drop applications such as IGMP snooping.

**APPLICATIONS**

- Ethernet DSLAM: ADSL/VDSL line cards and WAN uplink card
- ATM DSLAM: FE or GE WAN uplink
- ATM multi-service switch: GE interface cards
- Router: ATM line cards
- Wireless base station: ATM to Ethernet interworking.

**INTERFACES**

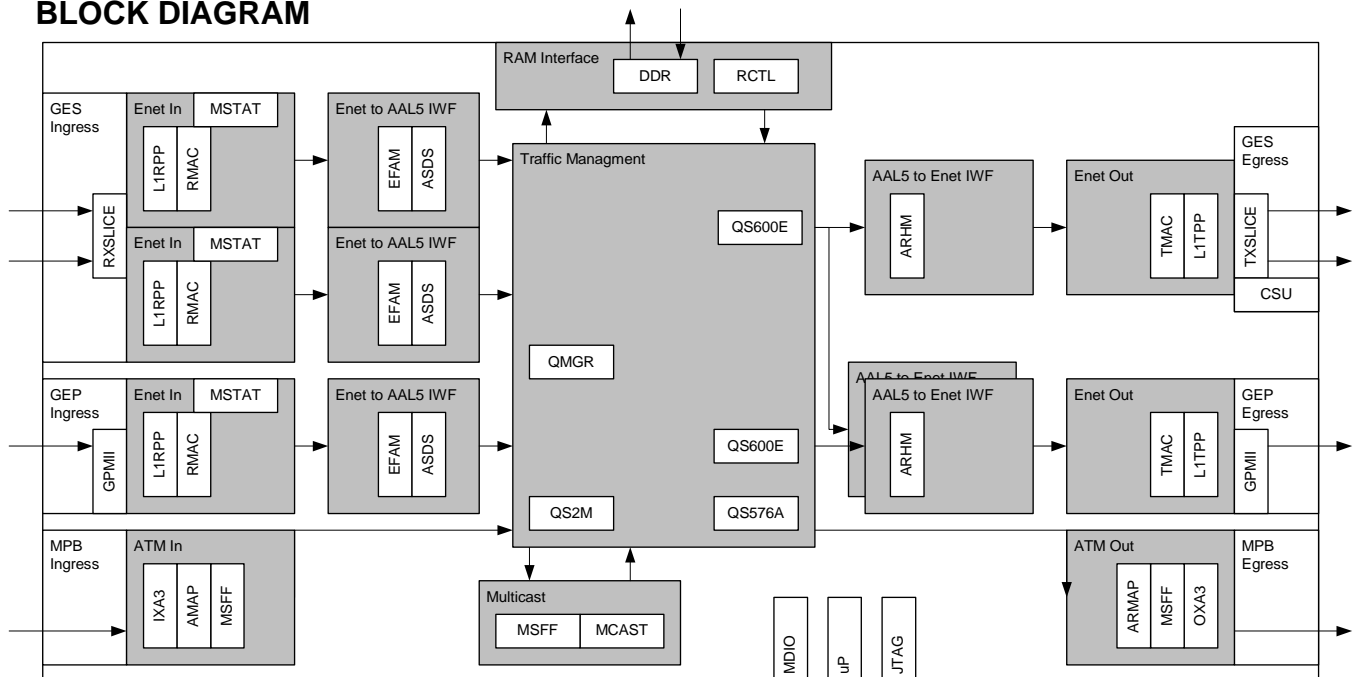
- Dual fully integrated, 1.25Gbit/s, 8B10B encoded 4-wire LVDS SERDES interface for connecting the internal GE MACs directly to a high-speed, redundant serial back-plane or external PHY.
- An additional (R)GMII / (R)MII parallel Ethernet interface, which can also be configured as two RMII interfaces.
- One 52 MHz, 16 bit Utopia Level 2 interface (Tx and Rx), extended to support up to 144 PHYs as per ATM Forum Utopia Level 2 specification af-phy-0039.000, Appendix 1. This interface is also configurable as a SATURN compliant 52-MHz, 16-bit POS-PHY Level 2 interface (Tx and Rx)
- One asynchronous 16 bit CPU interface for device configuration and alarm/status monitoring.
- One 32-bit SDRAM interface supporting up to 2 Gbits of packet buffering. Configurable as either DDR-I or DDR-II.

- Uses VLAN tag (802.1q VLAN address + 802.1p QoS bits) to identify traffic as unicast or multicast, and to identify destination port and class.
- SERDES to UL2/PL2, parallel Ethernet to UL2/PL2, SERDES to parallel Ethernet and parallel Ethernet to SERDES switching are all supported.
- For traffic directed to the UL2/PL2 interface, performs RFC2684 compliant AAL5 segmentation for origination of up to 576 ATM AAL5 VCs. Ethernet to ATM VCI/VPI mapping provided via a software configurable internal lookup table.
- Performs IP/Ethernet packet level multicast using wire-speed packet replication. Unicast and multicast traffic is queued independently and is merged onto the egress port via the egress traffic scheduler. Head of line blocking is avoided completely.
- Software configurable congestion management policies implementing Early Packet Discard & Partial Packet Discard (EPD/PPD) or weighted random early packet discard (WRED) during periods of egress port congestion.

**ETHERNET TO ATM PROCESSING**

- Receives Ethernet frames from both SERDES interfaces and the parallel interface simultaneously. Uses frame filtering to drop redundant traffic received on the protection SERDES interface.

**BLOCK DIAGRAM**



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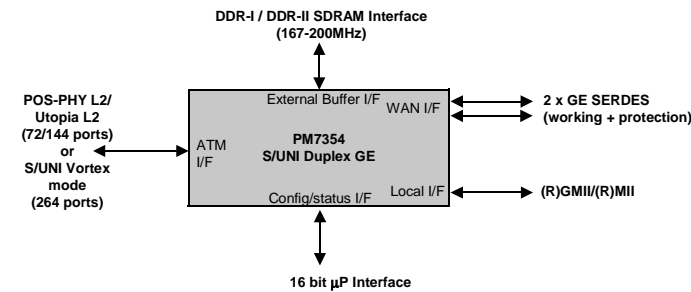
- Software configurable, QoS aware egress traffic scheduling from the 576 unicast or multicast traffic queues into 72 UL2 ports, up to 8 queues per port. Optionally configurable to 144 ports, 4 queues per port.
- Supports a "cells in frames" mode on a per VLAN basis in which received Ethernet frames have their 53 byte PDU extracted and used directly as the ATM cell to be queued at the UL2 interface.
- RFC2684 compliant AAL5 reassembly of Ethernet PDUs. Termination of up to 576 ATM AAL5 VCs. 8 reassembly queues per UL2 port for 72 ports, 4 reassembly queues per port for 144 ports.
- Reassembled packets can be directed to either the parallel or SERDES Ethernet interfaces, selectable on a per reassembly queue basis.
- All traffic sent to the SERDES interfaces is duplicated and sent to both SERDES links as required, for a 1:1 protected backplane.
- Optionally, traffic sent to the two SERDES interfaces can be replicated and sent to the parallel Ethernet interface. Inline filtering can then be performed to drop/pass packets on a selective basis. The parallel and SERDES interfaces have independent filtering.
- Software configurable, QoS aware and source port fairness aware egress traffic scheduling from the 576 packet reassembly queues into the Ethernet interfaces.
- Configurable congestion management policies implementing Early Packet Discard & Partial Packet Discard (EPD/PPD) or weighted random early packet discard (WRED) during periods of congestion on the Ethernet port.
- OAM cells arriving at the UL2/PL2 receive interface can be dropped or wrapped in their own Ethernet frame and sent to the parallel or SERDES Ethernet interfaces.
- Supports a "cells in frames" mode on a per-VC basis where each received ATM cell is wrapped in its own Ethernet frame and sent to either the SERDES or parallel Ethernet.

**ATM TO ETHERNET PROCESSING**

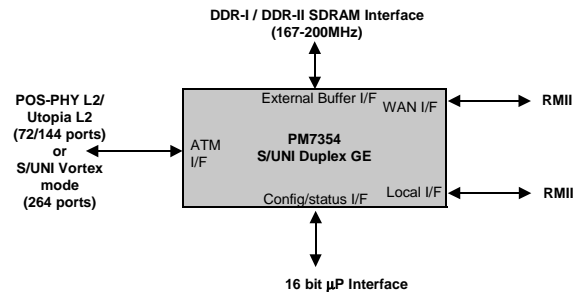
- Polls and receives ATM traffic from up to 144 logical ports on the UL2 interface.

**TYPICAL APPLICATIONS**

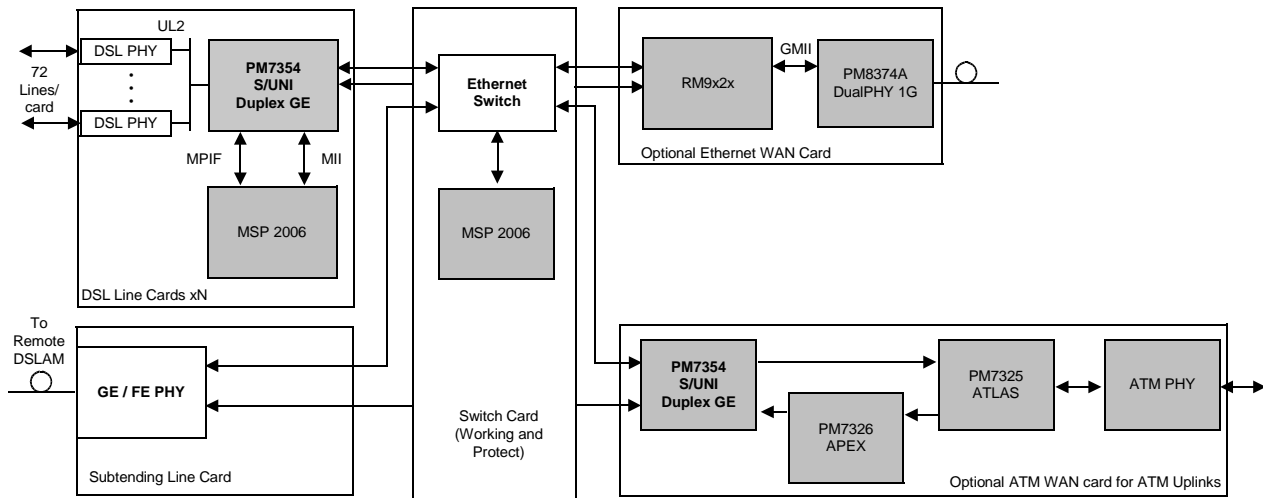
**S/UNI DUPLEX GE INTERFACES IN GE MODE**



**S/UNI DUPLEX GE INTERFACES IN FE MODE**



**S/UNI DUPLEX GE BASED MODULAR IP DSLAM ARCHITECTURE**



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