

Description

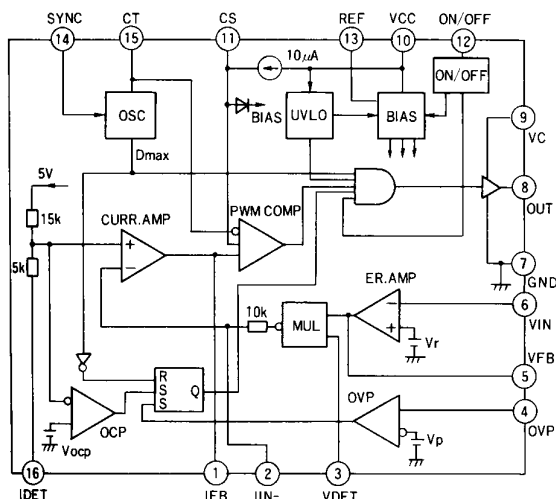
FA5331P(M) and FA5332P(M) are control ICs for a power factor correction system. These ICs use the average current control system to ensure stable operation. With this system, a power factor of 99% or better can be achieved.

FA5331P(M) is a 1st generation IC and FA5332P(M) is 2nd generation IC which light-load characteristics are improved.

Features

- Drive circuit for connecting a power MOS-FET ($I_o = \pm 1.5A$)
- Pulse-by-pulse overcurrent and overvoltage limiting function
- Output ON/OFF control function by external signals
- External synchronizing signal terminal for synchronous operation with other circuits
- Undervoltage malfunction prevention function
- Low standby current (90 μA typical) for simple start-up circuit
- 16-pin package (DIP/SOP)
- $\pm 2\%$ accuracy reference voltage for setting DC output and overvoltage protection [FA5332P(M) only]
- When there is a possibility of light-load operation, FA5332P(M) is suitable.

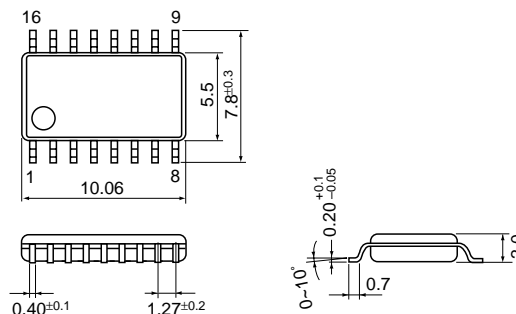
Block diagram



| Pin No. | Pin symbol | Description |
|---------|------------|--|
| 1 | IFB | Current error amplifier output |
| 2 | IIN- | Inverting input to current error amplifier |
| 3 | VDET | Multiplier input |
| 4 | OVP | Overvoltage protection input |
| 5 | VFB | Voltage error amplifier output |
| 6 | VIN- | Inverting input to voltage error amplifier |
| 7 | GND | Ground |
| 8 | OUT | Output |
| 9 | VC | Power supply to output circuit |
| 10 | VCC | Power supply |
| 11 | CS | Soft-start |
| 12 | ON/OFF | Output ON/OFF control input |
| 13 | REF | Reference voltage |
| 14 | SYNC | Oscillator synchronization input |
| 15 | CT | Oscillator timing capacitor and resistor |
| 16 | IDET | Non-inverting input to current error amplifier |

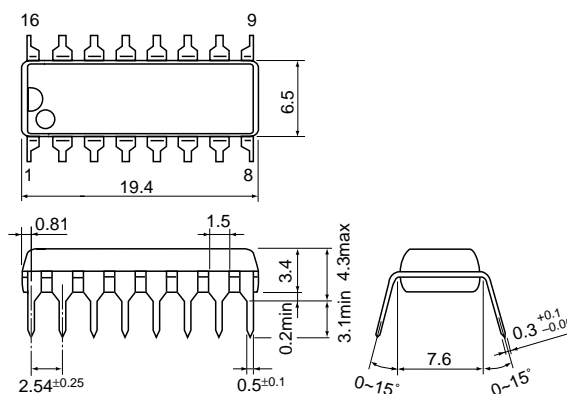
Dimensions, mm

SOP-16

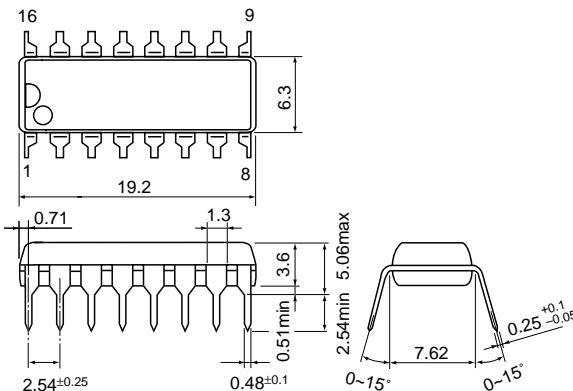


DIP-16

FA5331P



FA5332P



■ Absolute maximum ratings

| Item | Symbol | Rating | | Unit |
|---|---|-----------------|-----------------|------------------|
| | | FA5331P(M) | FA5332P(M) | |
| Supply voltage | V_{CC}, V_C | 30 | 30 | V |
| Output current | I_O | ± 1.5 | ± 1.5 | A |
| Input voltage | $V_{SYNC}, V_{ON/OFF}, V_{VIN-}, V_{VDET}, V_{OVP}$ | -0.3 to +5.3 | -0.3 to +5.3 | V |
| | V_{IDET} | -10.0 to +5.3 | -10.0 to +5.3 | V |
| Total power dissipation ($T_a=25^\circ\text{C}$) | P_d | 850 (DIP-16) *1 | 850 (DIP-16) *1 | mW |
| | | 650 (SOP-16) *2 | 650 (SOP-16) *2 | |
| Operating temperature | T_{opr} | -30 to +85 | -30 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -40 to +150 | -40 to +150 | $^\circ\text{C}$ |

Notes:

*1 Derating factor $T_a > 25^\circ\text{C}$: 6.8mW/ $^\circ\text{C}$ (on PC board)*2 Derating factor $T_a > 25^\circ\text{C}$: 5.2mW/ $^\circ\text{C}$ (on PC board)

■ Recommended operating conditions

| Item | Symbol | FA5331P(M) | | FA5332P(M) | | Unit |
|--|---------------|------------|------|------------|------|------------|
| | | Min. | Max. | Min. | Max. | |
| Supply voltage | V_{CC}, V_C | 10 | 28 | 10 | 28 | V |
| IDET terminal input voltage | V_{IDET} | -1.0 | 0 | -1.0 | 0 | V |
| VDET terminal input voltage | V_{VDET} | 0 | 2.0 | 0 | 2.4 | V |
| VDET terminal peak input voltage | V_{PVDET} | 0.65 | 2.0 | 0.65 | 2.4 | V |
| Oscillator timing capacitance | C_T | — | — | 330 | 1000 | pF |
| Oscillator timing resistance | R_T | — | — | 10 | 75 | k Ω |
| Oscillation frequency | f_{osc} | 10 | 220 | 15 | 150 | kHz |
| Noise filter resistance connected to IDET terminal | R_n | 0 | 100 | 0 | 27 | Ω |

■ Electrical characteristics ($T_a=25^\circ\text{C}$, $C_T=470\text{pF}$, $R_T=22\text{k}\Omega$, $V_{CC}=V_C=18\text{V}$)

Oscillator section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|--|------------|--|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Oscillation frequency | f_{osc} | $C_T=470\text{pF}$ $R_T=22\text{k}\Omega$ | 68 | 75 | 82 | 68 | 75 | 82 | kHz |
| Frequency variation 1 (due to supply voltage change) | f_{dv} | $V_{CC}=10$ to 30V | | 1 | | | 1 | 3 | % |
| Frequency variation 1 (due to temperature change) | f_{dT} | $T_a=-30$ to $+85^\circ\text{C}$ | | 5 | | | 5 | 8 | % |
| Output peak voltage | V_{osc} | | | 3.55 | | | 3.55 | | V |
| Synchronizing input peak voltage | V_{SYNC} | SYNC terminal voltage | 1.5 | | | 1.5 | | | V |

Voltage error amplifier section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|------------------------|-----------|--------------------|------------|------|------|------------|-------|-------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Reference voltage | V_r | | 1.48 | 1.54 | 1.60 | 1.519 | 1.550 | 1.581 | V |
| Input bias current | I_{BE} | | -500 | -50 | | -500 | -50 | | nA |
| Open-loop voltage gain | A_{VE} | | 80 | | | 80 | | | dB |
| Output voltage | V_{OE+} | No load | 3.5 | 3.8 | | 3.5 | 3.8 | | V |
| | V_{OE-} | | | 50 | 200 | | 50 | 200 | mV |
| Output source current | I_{OE+} | $V_{OE}=0\text{V}$ | | -900 | | | -900 | | μA |

Current error amplifier section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|-------------------------|----------------|---|------------|------|------|------------|------|------|---------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Input threshold voltage | $V_{TH\ IDET}$ | $V_{DET}=0V$ $V_{FB}=V_i$, $R_n=30\Omega$ | – | – | – | 0 | 30 | 60 | mV |
| Input bias current | I_{BC} | $I_{DET}=0V$ | –350 | –230 | | –350 | –250 | –150 | μA |
| Open-loop voltage gain | A_{VC} | | 80 | | | 80 | | | dB |
| Output voltage | V_{OC+} | No load | 3.5 | 3.8 | | 3.5 | 3.8 | | V |
| | V_{OC-} | | | 50 | 200 | | 50 | 200 | mV |
| Output source current | I_{OC+} | $V_{IFB}=0V$ | | –900 | | | –900 | | μA |

Reference voltage section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|---|-----------|-----------------------|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Output voltage | V_{REF} | | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | V |
| Voltage variation 1 (by supply voltage variation) | V_{RDV} | $V_{CC}=10$ to $30V$ | | | 25 | | | 25 | mV |
| Voltage variation 2 (by load change) | V_{RDT} | $I_{OR}=0.1$ to $2mA$ | | 2 | | | 2 | 5 | mV |

Multiplier section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|----------------------------------|-------------|----------------|------------|------|------|------------|------|------|---------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| V_{DET} terminal input voltage | V_{MVDET} | | 0 | | 2.0 | 0 | | 2.4 | V |
| V_{FB} terminal input voltage | V_{MVFB} | | 1.5 | | 3.5 | 1.5 | | 3.5 | V |
| Output current | I_M | $V_{IIN}=0V$ | | –65 | | | –65 | | μA |
| Output voltage coefficient | K | | | –1.0 | | | –1.0 | | – |

Pulse width modulation circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|--------------------|-----------|----------------|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Maximum duty cycle | D_{MAX} | | 89 | 92 | 95 | 89 | 92 | 95 | % |

Output circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|----------------|----------|------------------------------|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Output voltage | V_{OL} | $I_o=100mA$ | | 1.3 | 1.8 | | 1.3 | 1.8 | V |
| | V_{OH} | $I_o=-100mA$ $V_{CC}=18V$ | 15.5 | 16.5 | | 15.5 | 16.5 | | V |
| Rise time | t_r | No load | | 300 | | | 300 | | ns |
| Fall time | t_f | No load | | 200 | | | 200 | | ns |

Soft-start circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|-------------------------|-------------|-----------------------|------------|------|------|------------|------|------|---------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Input threshold voltage | V_{THCSO} | Duty cycle=0% | | 0.1 | | | 0.1 | | V |
| | V_{THCSM} | Duty cycle= D_{MAX} | | 3.55 | | | 3.55 | | V |
| Charge current | I_{CHG} | CS terminal=0V | | –10 | | | –10 | | μA |

Overvoltage protection circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|--|-------------|----------------------|------------|------|------|------------|-------|-------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Input threshold voltage | V_{THOVP} | OVP terminal voltage | 1.56 | 1.64 | 1.72 | 1.617 | 1.650 | 1.683 | V |
| Input threshold voltage/reference voltage(V_{THOVP}/V_r) | α | | — | — | — | 1.044 | 1.065 | 1.086 | — |
| Delay time | T_{PDOVP} | | | 200 | | | 200 | | ns |

Overcurrent limiting circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|-------------------------|-------------|-----------------------|------------|-------|-------|------------|-------|-------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Input threshold voltage | V_{THOCP} | IDET terminal voltage | −1.25 | −1.15 | −1.05 | −1.20 | −1.10 | −1.00 | V |
| Delay time | T_{PDOCP} | | | 200 | | | 200 | | ns |

Output ON/OFF circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|---------------------|---------------|--|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Threshold voltage | $V_{THONOFF}$ | Ta=−30°C | — | — | — | 3.7 | | 4.3 | V |
| | | Ta=+25°C | 2.0 | | 3.5 | 2.8 | | 3.4 | V |
| | | Ta=+85°C | — | — | — | 1.5 | | 2.8 | V |
| Input current at ON | I_{THON} | ON/OFF terminal voltage=3.5V | | 60 | 120 | | — | — | μA |
| | | ON/OFF terminal voltage= $V_{THONOFF}$ | | — | — | | 10 | 40 | μA |

Undervoltage lockout circuit section

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|-----------------------------|--------------|----------------|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| OFF to ON threshold voltage | V_{THUON} | | 14.3 | 15.3 | 16.3 | 14.6 | 15.3 | 16.0 | V |
| ON to OFF threshold voltage | I_{THUOFF} | | 7.6 | 8.3 | 9.0 | 7.6 | 8.3 | 9.0 | V |
| Voltage hysteresis | V_{UHYS} | | | 7.0 | | | 7.0 | | V |

Overall device

| Item | Symbol | Test condition | FA5331P(M) | | | FA5332P(M) | | | Unit |
|--------------------------------|-------------|----------------|------------|------|------|------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Standby current | I_{CCST} | $V_{CC}=14V$ | | 90 | 140 | | 90 | 140 | μA |
| Operating-state supply current | I_{CCOP} | | | 10 | 15 | | 10 | 15 | mA |
| OFF-state supply current | I_{CCOFF} | Pin 12=0V | | 1.1 | 1.8 | | 1.1 | 1.8 | mA |

■ Description of each circuit

1. Oscillator section

This section outputs sawtooth waves oscillating between 0.15 and 3.55V using the capacitor charge and discharge characteristics. Figure 1 shows how to connect the required external components to this circuit. The oscillation frequency is determined by the C_T and R_T values. The relationship between the C_T and R_T values is shown in characteristic curves. Pin 14 (SYNC) is a synchronizing input terminal whose threshold voltage is about 1V. As Fig. 1 shows, input rectangular synchronizing signal waves to pin 14 through an RC circuit. Set the free-running frequency about 10% lower than the synchronizing signal frequency. Connect a clamp diode (D1) to prevent an unwanted current inside the IC.

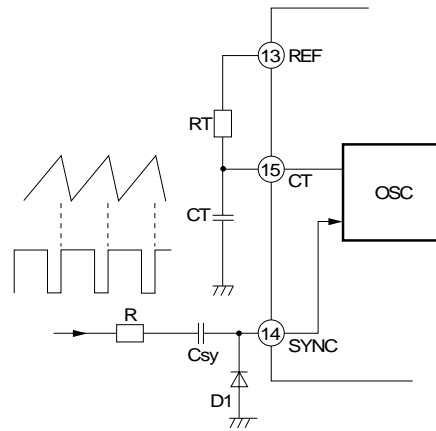


Fig. 1 Oscillator

2. Voltage error amplifier and overvoltage limiting circuit

The voltage error amplifier forms a voltage feedback loop to keep the output voltage stable. The positive input terminal of this amplifier is connected to the reference voltage (V_r). Fig. 2 shows how to connect the required external components to this circuit.

The output voltage (V_o) is as follows:

$$V_o = \frac{R_1 + R_2}{R_1} \cdot V_r \quad (1)$$

FA5331: $V_r = 1.54V$ (typ.)

FA5332: $V_r = 1.55V$ (typ.)

Connect a resistor and a capacitor in parallel across error amplifier output pin 5 and error amplifier negative input pin 6 to set the voltage gain (A_v).

The A_v value is as follows:

$$A_v = \frac{R_4}{R_3 (1 + j\omega C_1 \cdot R_4)} \quad (2)$$

Error amplifier cutoff frequency (f_c) is as follows:

$$f_c = \frac{1}{2\pi C_1 \cdot R_4} \quad (3)$$

If 100 or 120Hz ripples appear at the error amplifier output, the active filter does not operate stably. To ensure stable operation, set the f_c value to about 1Hz.

An overvoltage detection comparator (C1) is built in to limit the voltage if the output voltage exceeds the design value. The reference input voltage (V_p) is as follows:

$$V_p = \alpha \cdot V_r \quad (4)$$

$\alpha \approx 1.065$

The connections shown in Fig. 2 limit the output voltage to α times the design value.

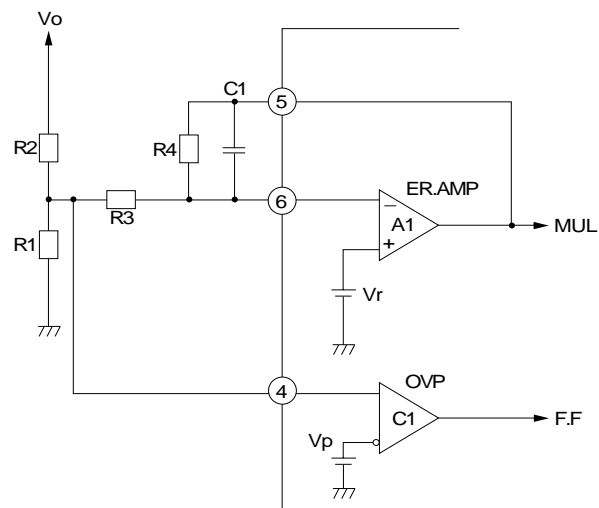


Fig. 2 Voltage error amplifier and overvoltage limiting circuit

3. Current error amplifier and overcurrent limiting circuit

The current error amplifier forms a current loop to change the input circuit current into sinusoidal waves. As Fig. 3 shows, the multiplier output is connected to pin 2 (IIN –) through a resistor (RA) to input the reference current signal. Pin 16 (IDET) is a current input terminal. Design the circuit so that the voltage at pin 16 will be within the range from 0 (GND potential) to –1.0V. Connect a phase correction resistor and capacitors across pin 1 (amplifier output) and pin 2. See Fig. 4 for the expected gain characteristics of the circuit shown in Fig. 3.

Here,

$$Z = \frac{1}{2\pi R5 \cdot C3} \quad \text{..... (5)}$$

$$p = \frac{1}{2\pi R5 \cdot C} \quad \text{..... (6)}$$

$$C = \frac{C2 \cdot C3}{C2 + C3}$$

The voltage gain (G1) between Z and P of the circuit (gain between pins 16 and 1) is given as follows:

$$G1 = 20 \cdot \log_{10} \left\{ 0.75 \left(\frac{R5}{RA} + 1 \right) \right\} \quad \text{..... (7)}$$

Ensure an adequate phase margin by selecting C1 and C2 so that the p/z ratio is about 10. The current error amplifier output is used as an input to the comparator for PWM.

The overcurrent detection comparator (C2) limits an overcurrent. The threshold voltage for overcurrent detection at pin 16 is –1.15V for FA5331 and –1.10V for FA5332. Connect noise filters Rn and Cn to prevent the voltage at pin 16 from fluctuating due to noise, causing the comparator to malfunction. For Rn, select a resistor of up to 100Ω for FA5331 and up to 27Ω for FA5332. (See P64, 4. No-load operation)

4. Comparator for PWM

Figure 5 shows the comparator for PWM. When the oscillator output (Va) is smaller than the current error amplifier output (Vc), the comparator output is high and the output ON signal is generated at pin 8. Pin 11 (CS) is a terminal for soft start. This terminal charges capacitor C4 with the internal constant current (10μA) for a soft start. Priority is given to Vb and Vc whichever is lower.

5. Multiplier

The multiplier generates a reference current signal. Input a fully rectified sinusoidal signal voltage into pin 3 (VDET). Design the circuit to keep the peak voltage at pin 3 within a range from 0.65V to 2V for FA5331 and 0.65V to 2.4V for FA5332. The multiplier output voltage (Vm) is roughly given as follows (see Fig. 6):

$$Vm = 1.25 - (Ve - 1.55) \cdot Vs \quad \text{..... (8)}$$

As Fig. 3 shows Vm is internally connected to pin 2 (IIN –) of the current error amplifier A2 through a 10kΩ resistor. (See the characteristic curve, page 66 for the input and output characteristics of the multiplier.)

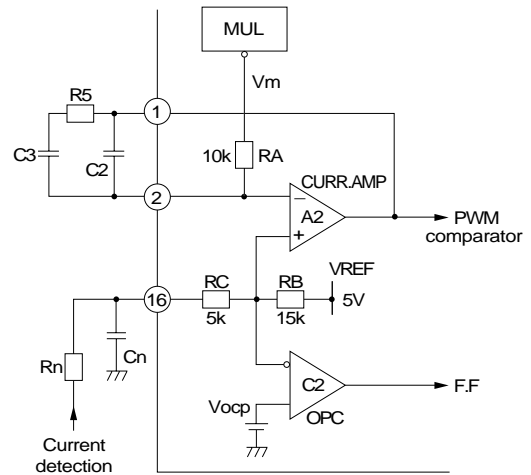


Fig. 3 Current error amplifier and overcurrent limiting circuit

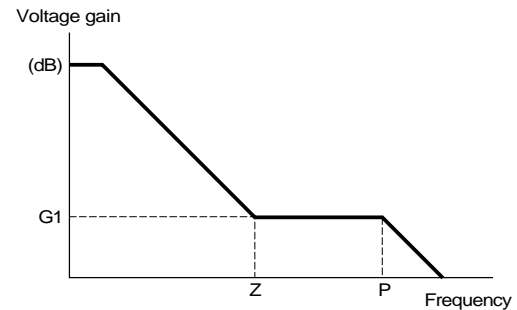


Fig. 4 Voltage gain-frequency

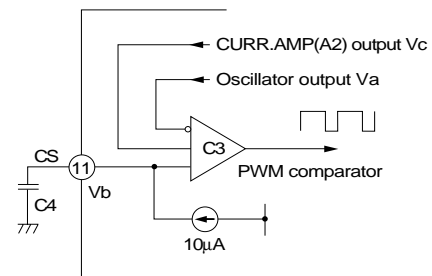


Fig. 5 PWM comparator

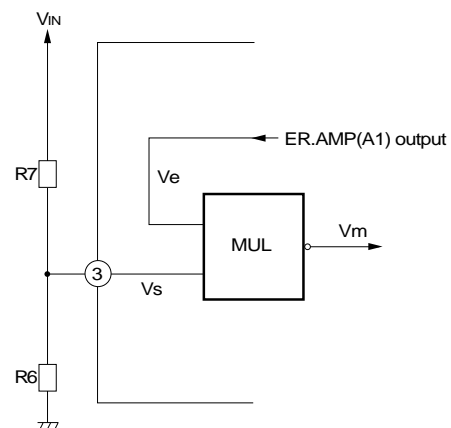


Fig. 6 Multiplier

6. ON/OFF control input circuit

Figure 7 shows the ON/OFF control input circuit. If pin 12 is set to the high level (enable), this IC outputs pulses from the OUT pin. If pin 12 is set to the low level (disable), the internal bias power (reference voltage) goes off and the IC current consumption becomes about 1/10 that of its ON state. The output level of pin 11 (CS for soft start) also goes low.

7. Output circuit

As Fig. 8 shows, pin 9 is configured as the high power terminal (VC), independent of the IC power terminal (VCC). This pin allows an independent drive resistance when the power MOSFET is ON and OFF. If the drive resistances in the ON and OFF states are Rg (on) and Rg (off), the following formulas can be used to determine the total gate resistance

Rg:

$Rg\ (on) = Rg1 + Rg2 \dots\dots\dots (9)$

$Rg\ (off) = Rg2 \dots\dots\dots (10)$

In the standby state, the output level of pin 8 is held low. If the potential at the drain terminal of the power MOSFET fluctuates, the gate-drain capacitance may drive the IC output voltage at pin 8 to below 0. Once the voltage at pin 8 reaches -0.6V, an unwanted current flows in the IC and a large abnormal current flows in the output circuit when the output transistor is turned on. To prevent this, connect a Schottky diode across the gate and source of the power MOSFET.

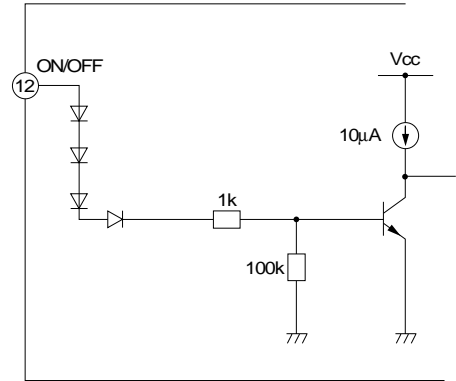


Fig. 7 ON/OFF control input circuit

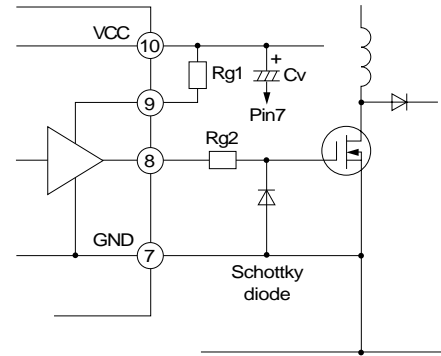


Fig. 8 Output circuit

■ Design advice

1. Start circuit

Figure 9 shows a sample start circuit. Since the IC current while the Vcc pin voltage rises from 0V to V_{THON} is as small as 90μA (typ.), the power loss in resistor R_A is small. If an additional winding is prepared in the voltage step-up inductor (L), power to the control circuit can be supplied from this circuit. However, the voltage must be stabilized by a regulator circuit (REG) to prevent an excess rise of the IC supply voltage (Vcc). Use fast or ultra-fast rectifier diodes for the rectifier circuit (DB1) of the winding for high-frequency operation.

2. Current sensing resistor

The current sensing resistor (R_s) detects the current in the inductor. R_s is used to make the input current sinusoidal. The current in the inductor produces a negative voltage across R_s. The voltage is input to IC pin 16 (IDET). Determine the value of R_s so that the peak voltage of the IDET pin is -1V.

$$R_s = \frac{V_{in}}{\sqrt{2} \cdot P_{in}} \quad (11)$$

V_{in}: Minimum AC input voltage (effective value) [V]
P_{in}: Maximum input power [W]

Since the threshold voltage of the overcurrent limiting circuit (pin 16) is -1.15V for FA5311 for and -1.10V for FA5332, the peak input current limit (i_p) is determined by:

$$\text{FA5331: } i_p = \frac{1.15}{R_s} \quad (12)$$

$$\text{FA5332: } i_p = \frac{1.10}{R_s}$$

3. Voltage step-up type converter

Figure 9 shows the basic circuit of a voltage step-up type converter which is used as a power factor correction.

(a) Output voltage

For stable operation, set the output voltage to be 10V or more over the peak value of the maximum input voltage. When using this IC for an active filter, set the output voltage (V_o) as follows:

$$V_o \geq \sqrt{2} \cdot V_{in} + 10V \quad (13)$$

V_{in}: Maximum AC input voltage [V]
(effective value of sinusoidal wave)

(b) Voltage step-up inductor

When using a voltage step-up converter in continuous current mode, the ratio of inductor current ripple to the input peak current is set to about 20%. Determine the inductance as follows:

$$L \geq \frac{V_{in}^2 (V_o - \sqrt{2} \cdot V_{in})}{\gamma \cdot f_s \cdot P_{in} \cdot V_o} \quad (14)$$

V_{in}: Minimum AC input voltage (effective value) [V]
γ: Ratio of inductor current ripple (peak to peak value) to the input peak current (about 0.2)
f_s: Switching frequency [Hz]
P_{in}: Converter's maximum input power [W]

As the characteristic curves on page 66 show, the peak voltage at pin 3 should be at least 0.65V, even when the AC input voltage is minimal. Considering this, determine R₆ and R₇ shown in Fig. 6.

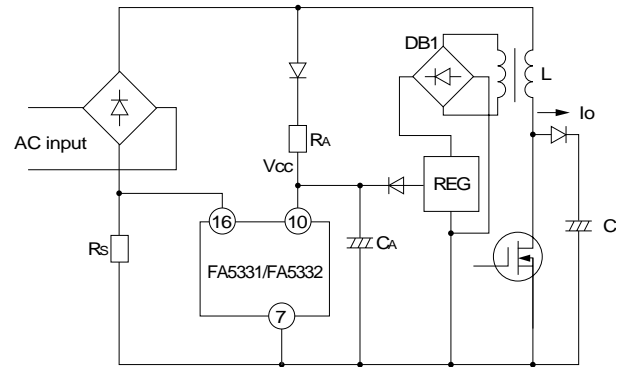


Fig. 9 Start circuit

Example: FA5332

When V_{in} is 85V and P_{in} is 300W, the formulas of (11) and (12) can be calculated as:

$$R_s = \frac{85}{\sqrt{2} \cdot 300} = 0.2 \text{ [} \Omega \text{]}$$

$$i_p = \frac{1.10}{0.2} = 5.5 \text{ [A]}$$

And,

$$\sqrt{2} \cdot 85 \cdot \frac{R_6}{R_6 + R_7} = 0.65 \text{ [V]}$$

If R₆ is set to 2.7kΩ to satisfy these formulas, R₇ becomes 480kΩ.

Example:

When V_{in} is 85V, V_o is 385V, and γ is 0.2, the formula of (14) can be calculated as:

$$L \geq \frac{2.48 \times 10^4}{f_s \cdot P_{in}} \text{ [H]} \quad (15)$$

(c) Smoothing capacitor

When a voltage step-up converter is used in a power factor correction circuit, the input current waveform is regulated to be in-phase with the input voltage waveform. Therefore, ripple noise of twice the input line frequency appears at the output. The output voltage (v_o) is represented as:

$$v_o = V_o - \frac{I_o}{2 \cdot \omega_o \cdot C} \cdot \sin 2 \omega_o t \quad (16)$$

V_o: Average output voltage
I_o: Output current
ω_o: 2π f_o (f_o: Input power frequency, 50 or 60Hz)
C: Smoothing capacitor value

Therefore, the peak-to-peak value of the output ripple voltage V_{rp} is given by:

$$V_{rp} = \frac{I_o}{\omega_o C} \quad (17)$$

Using formula (17), determine the necessary C value.

4. No-load operation

The following condition should be met to prevent from overvoltage and audible noise during no-load or light-load operation.

For FA5331 (Fig.10)

$$0.85 \cdot \alpha \leq R_{OFST}(k\Omega) \leq \alpha$$

$$\text{where, } \alpha = \frac{(3.5 \cdot 10^3 - 0.26 \cdot R_n) \cdot 12}{42 + 0.26 \cdot R_n}$$

and, $R_n \leq 100\Omega$

and, Rx: don't connect.

- You must not connect Rx which reduces DC gain of current error amplifier.
- You can connect R5 which is series with capacitor C3.

For FA5332 (Fig.11)

$$R_n \leq 27\Omega$$

and, Rx: don't connect.

- You must not connect Rx which reduces DC gain of current error amplifier.
- You can connect R5 which is series with capacitor C3.
- If you connect ROFST, dead time of AC input current will extend.

5. How to prevent from intermittent switching of low frequency

An intermittent switching, which frequency is lower than 10Hz, occurs in some applications.

In this case, it is possible to prevent from this intermittent switching to reduce feedback gain by decreasing the resistance of R4. (See Fig. 2)

You must check the effect thoroughly because this intermittent switching depends on load, temperature and input condition.

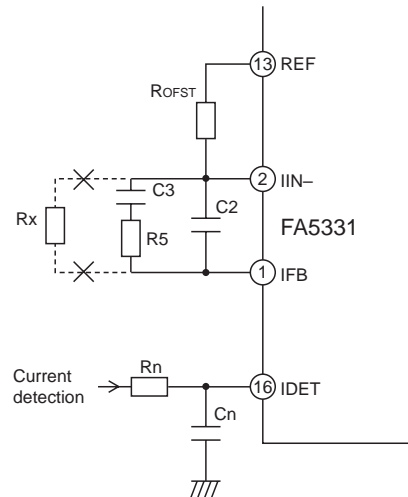


Fig.10

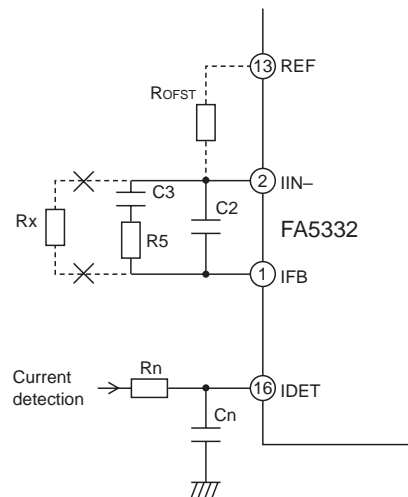
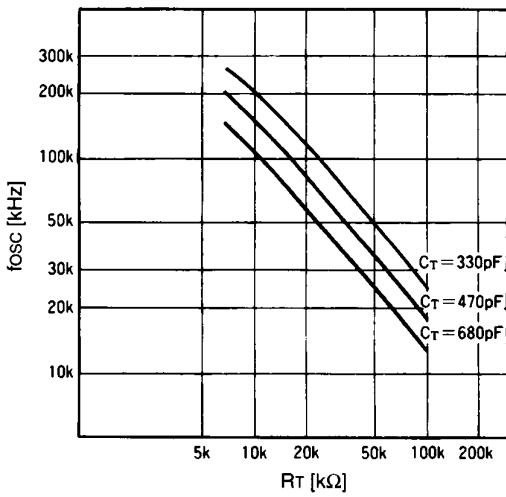


Fig.11

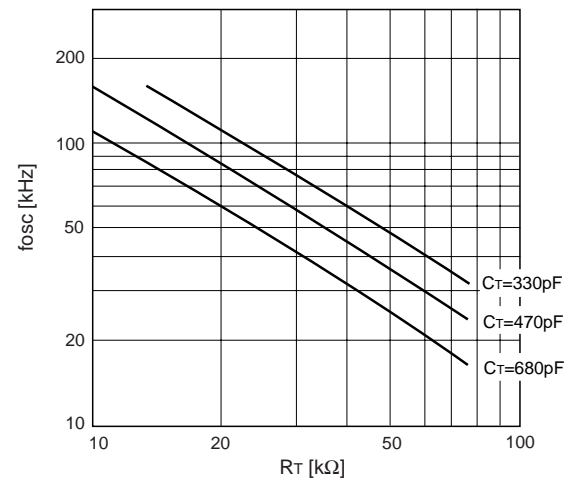
■ Characteristic curves (Ta = 25°C)

Oscillation frequency (fosc) vs.
timing resistor resistance (RT)

FA5331

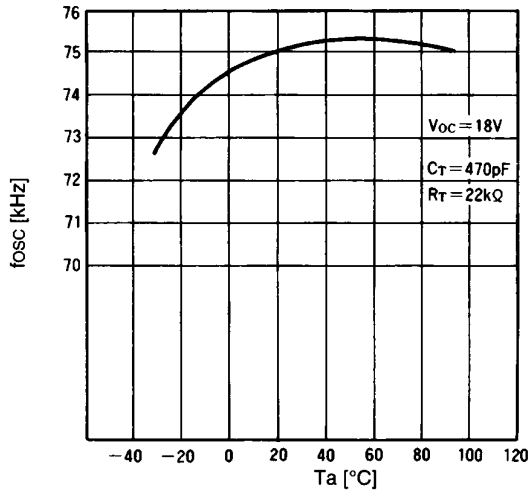


FA5332

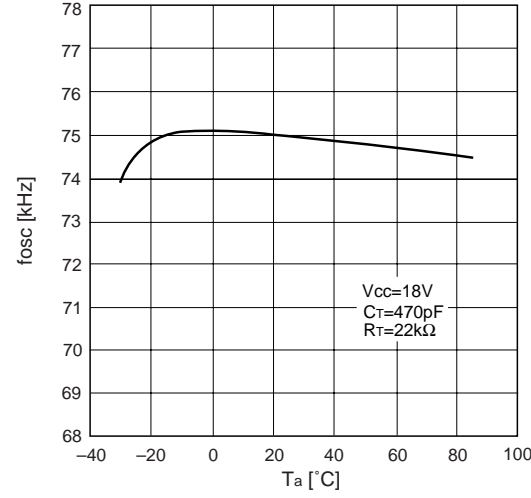


Oscillation frequency (fosc) vs.
ambient temperature (Ta)

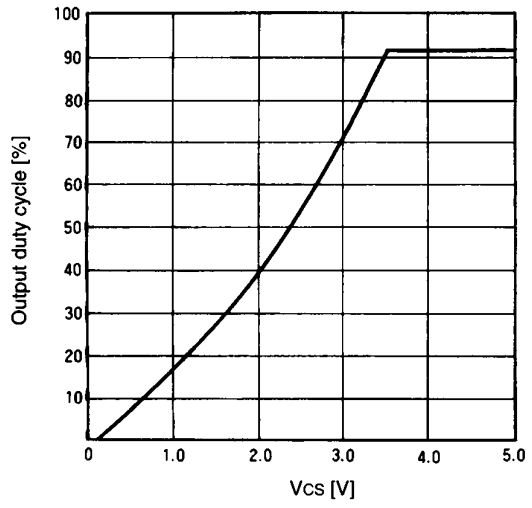
FA5331



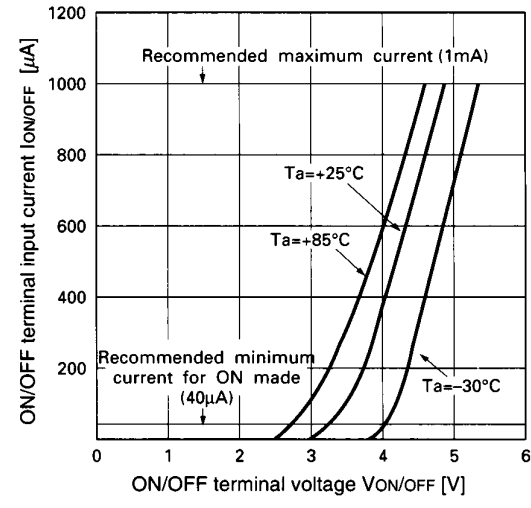
FA5332



Output duty cycle vs. CS terminal voltage (Vcs)



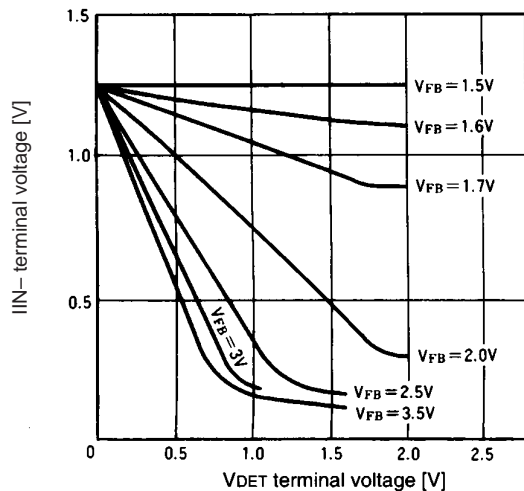
ON/OFF control terminal current vs.
ON/OFF control terminal voltage



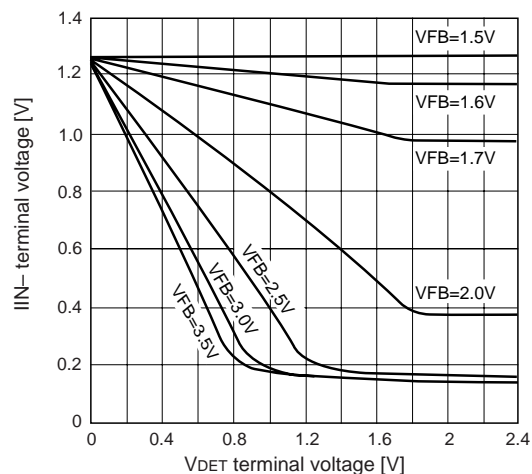
IIN– terminal voltage vs. VDET terminal voltage

Multiplier I/O

FA5331



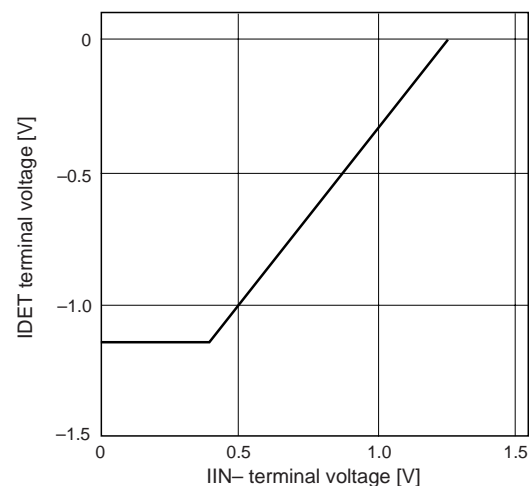
FA5332



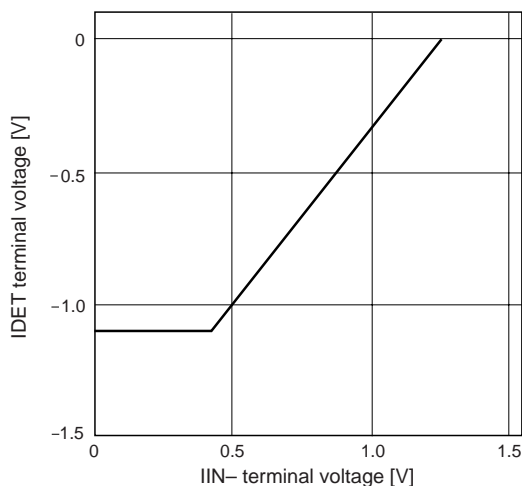
IDET terminal voltage vs. IIN– terminal voltage

Normal operation

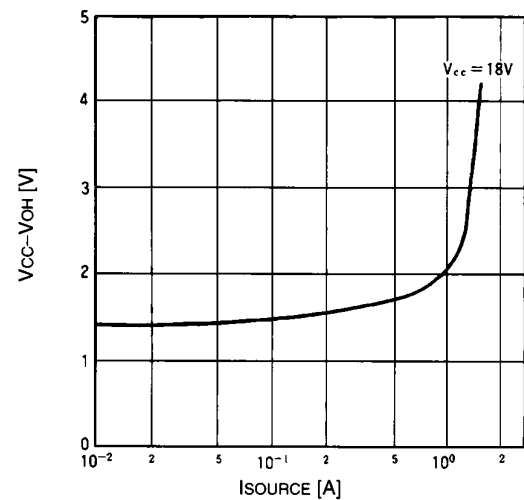
FA5331



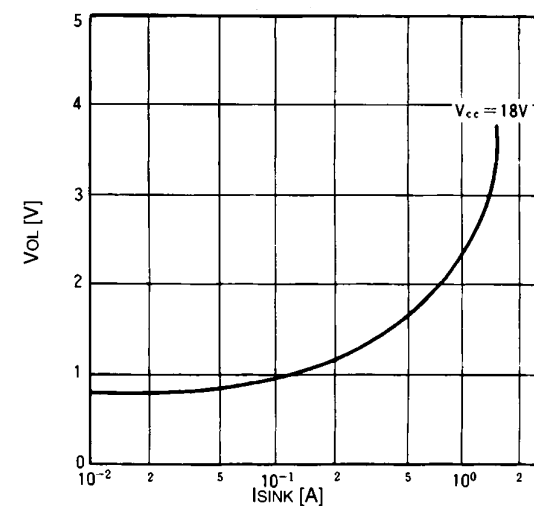
FA5332



H-level output voltage (VOH) vs. output source current (ISOURCE)

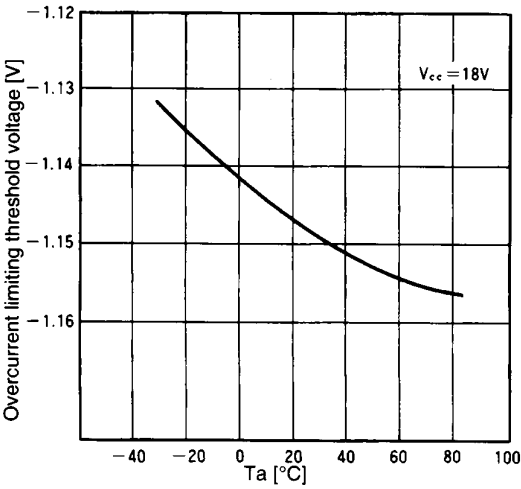


L-level output voltage (VOL) vs. output sink current (ISINK)

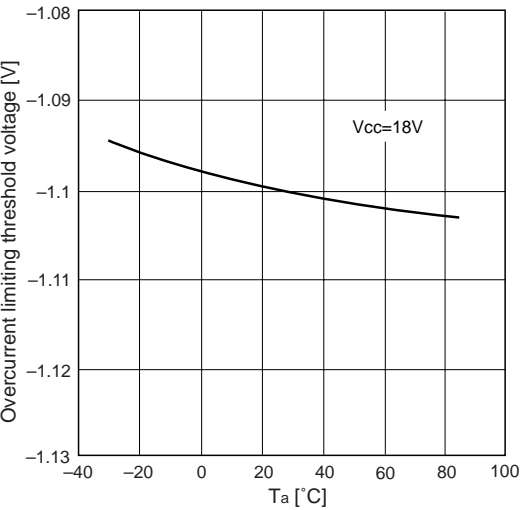


Overcurrent limiting threshold voltage vs. ambient temperature (Ta)

FA5331

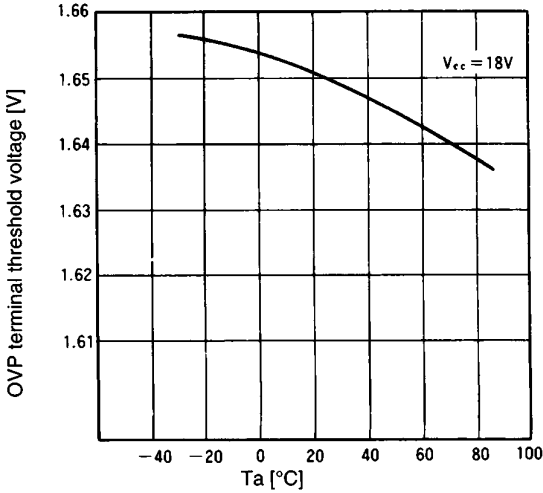


FA5332

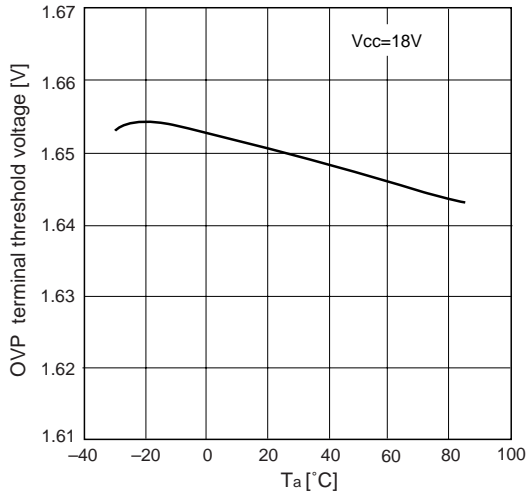


OVP terminal threshold voltage vs. ambient temperature (Ta)

FA5331

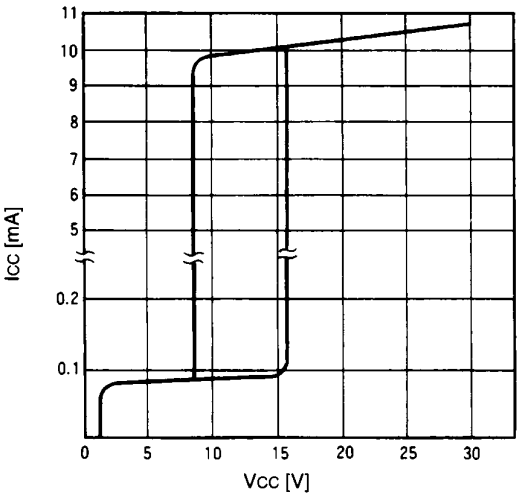


FA5332



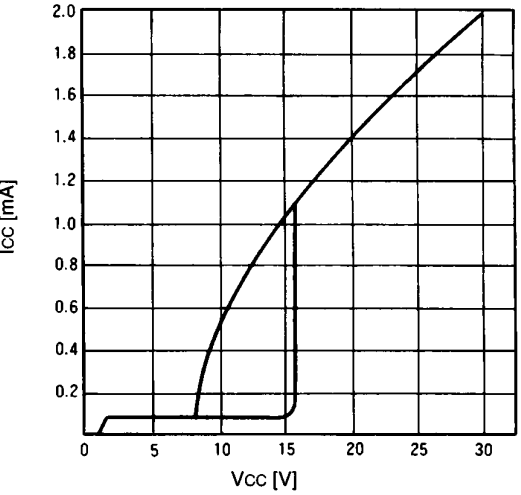
Supply current (Icc) vs. supply voltage (Vcc)

Normal operation



Supply current (Icc) vs. supply voltage (Vcc)

OFF mode



- **Example of FA5331 application circuit**