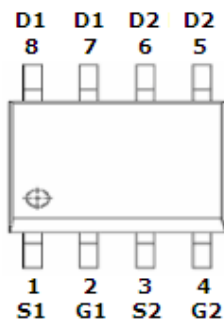


DESCRIPTION

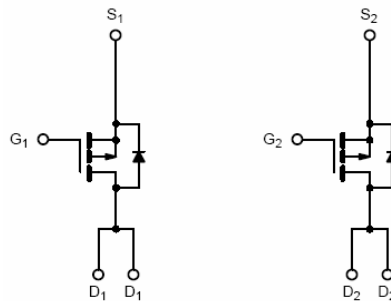
STP4925 is the dual P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management, and other battery powered circuits where high-side switching

**PIN CONFIGURATION
SOP-8**

FEATURE

- -30V/-7.2A, $R_{DS(ON)} = 25m\Omega$ (Typ.) @ $V_{GS} = -10V$
- -30V/-5.6A, $R_{DS(ON)} = 40m\Omega$ @ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING
SOP-8**


Y: Year Code A: Process Code





STP4925 

Dual P Channel Enhancement Mode MOSFET
-7.2A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

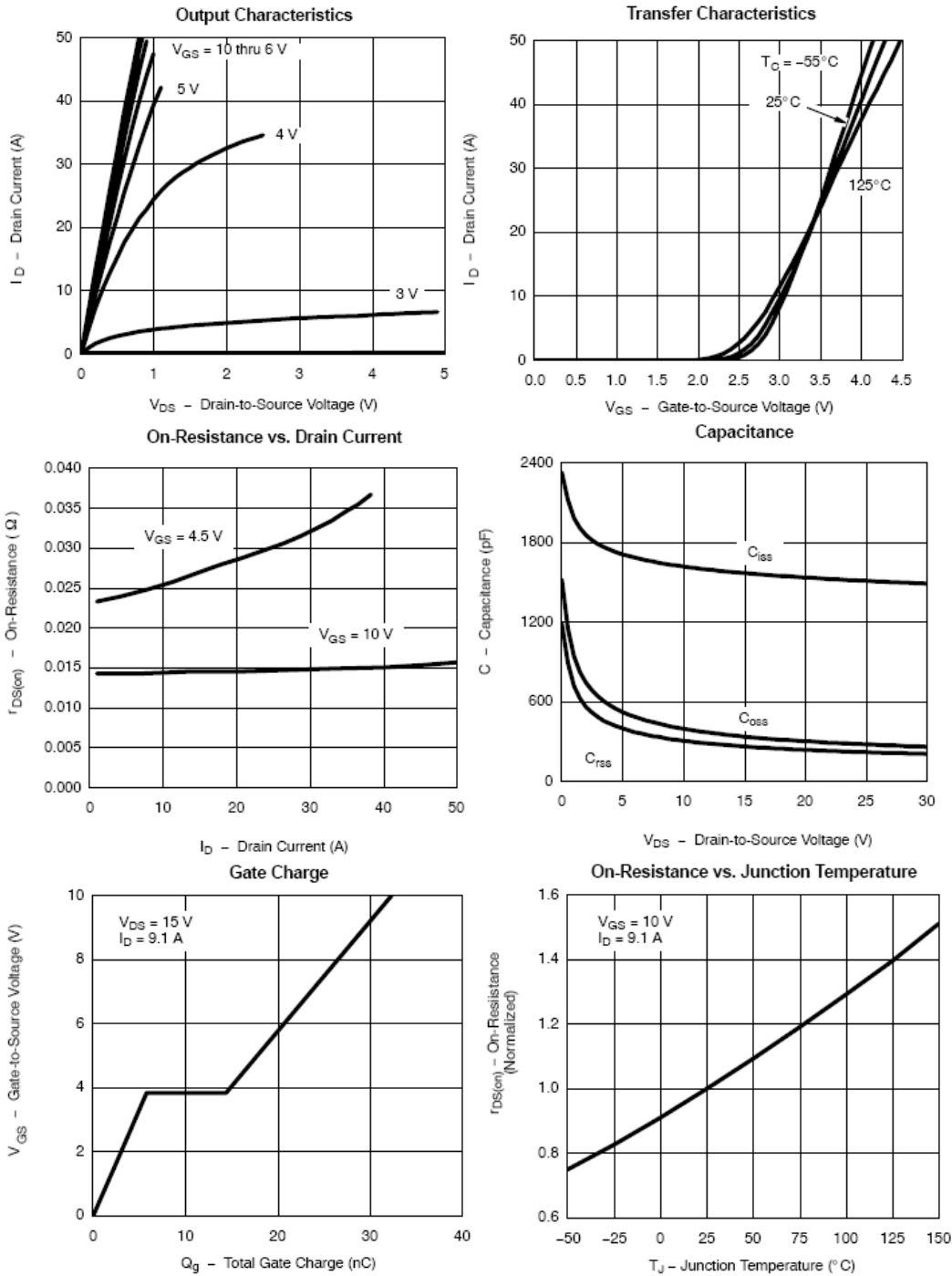
Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C -7.2	A
		T _A =70°C -5.6	
Pulsed Drain Current	I _{DM}	-20	A
Continuous Source Current (Diode Conduction)	I _S	-2.3	A
Power Dissipation	P _D	T _A =25°C 2.8	W
		T _A =70°C 1.8	
Operation Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	70	°C/W

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

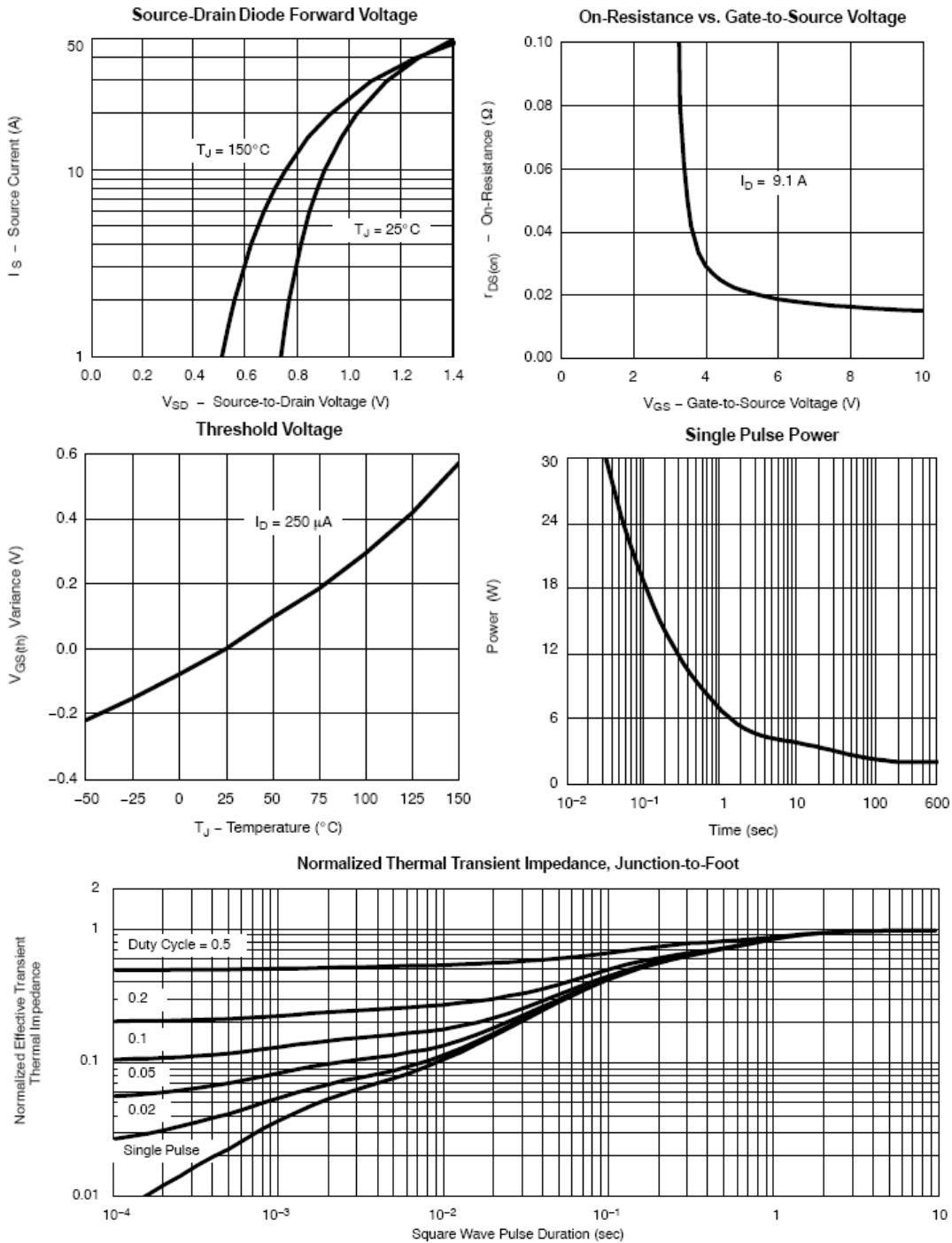
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STP4925 2009. V1

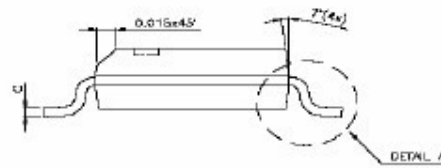
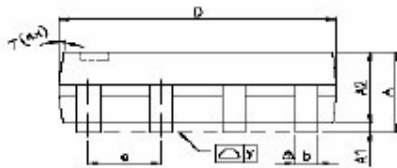
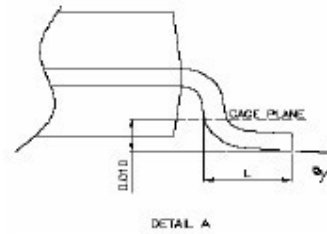
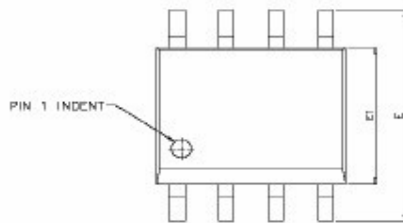
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=85^\circ C$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=4.5V$	-40			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-7.2A$		0.022	0.025	Ω
		$V_{GS}=-4.5V, I_D=-5.6A$		0.030	0.040	
Forward Tran Conductance	g_{fs}	$V_{DS}=-10V, I_D=-9.0A$		24		S
Diode Forward Voltage	V_{SD}	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-9.0A$		16	24	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		1650		pF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			235		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		16	30	nS
				17	30	
Turn-Off Time	$t_{d(off)tf}$			65	110	
				35	80	

TYPICAL CHARACTERISTICS (25°C Unless Note)


TYPICAL CHARACTERISTICS (25°C Unless Note)



SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°