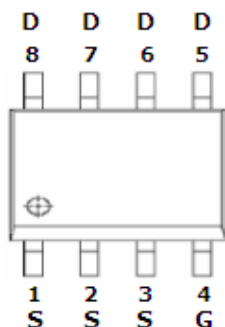
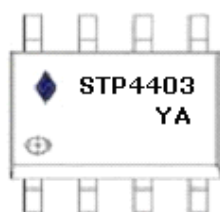


DESCRIPTION

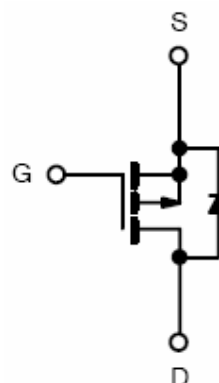
STP4403 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION
SOP-8**

FEATURE

- -20V/-10.0A, $R_{DS(ON)} = 20m\Omega$
@ $V_{GS} = -4.5V$
- -20V/-8.6A, $R_{DS(ON)} = 25m\Omega$
@ $V_{GS} = -2.5V$
- -20V/-7.6A, $R_{DS(ON)} = 35m\Omega$
@ $V_{GS} = -1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING
SOP-8**


Y:Year Code
A:Process Code





STP4403 

P Channel Enhancement Mode MOSFET

- 10.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	-20	V
Gate-Source Voltage	VGSS	±12	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C -10.0	A
		TA=70°C -8.0	
Pulsed Drain Current	IDM	-30	A
Continuous Source Current (Diode Conduction)	IS	-2.3	A
Power Dissipation	PD	TA=25°C 2.8	W
		TA=70°C 1.8	
Operation Junction Temperature	TJ	-55/150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	70	°C/W

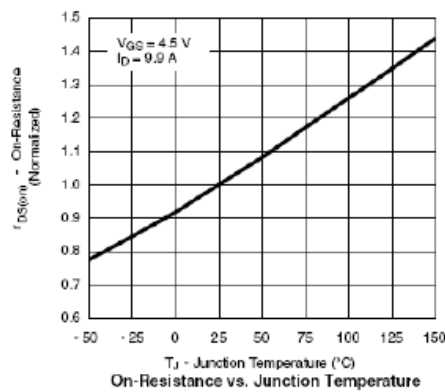
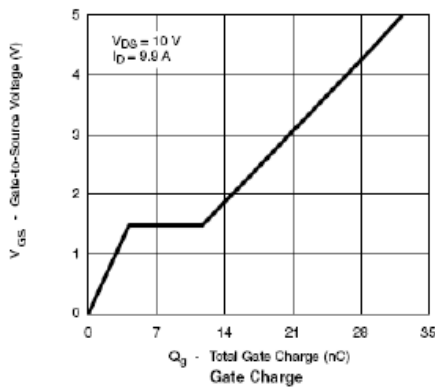
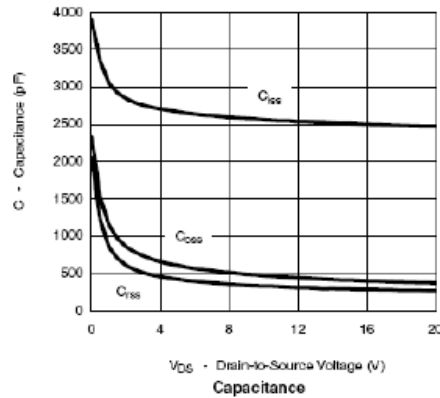
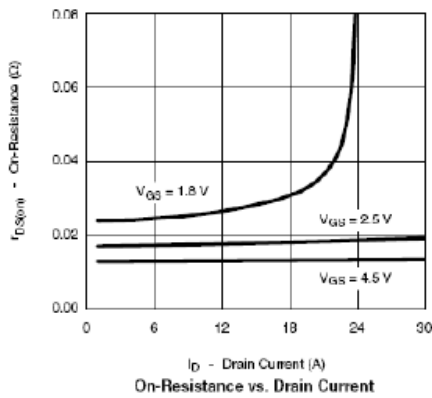
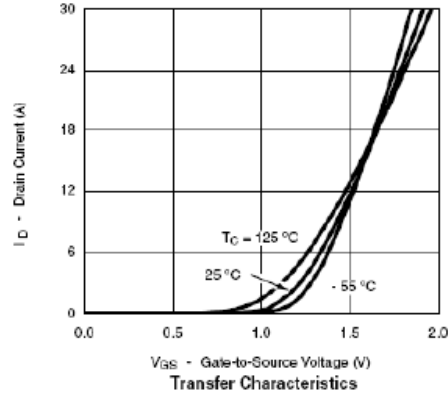
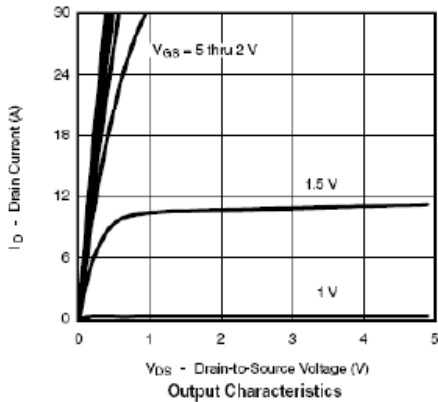
STANSON TECHNOLOGY
 120 Bentley Square, Mountain View, Ca 94040 USA
 www.stansontech.com

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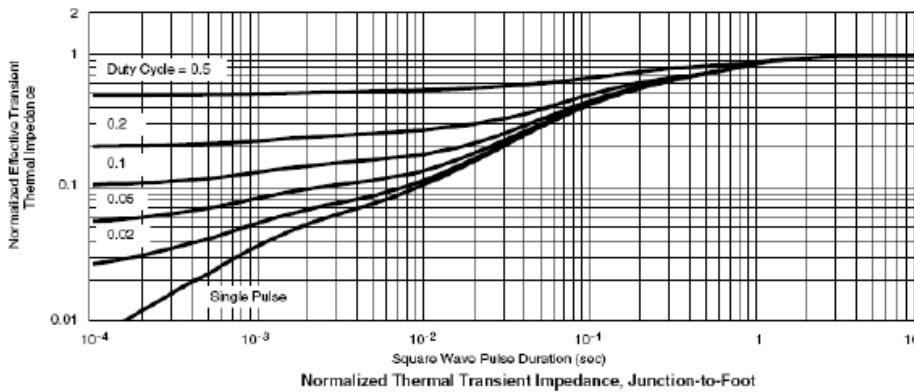
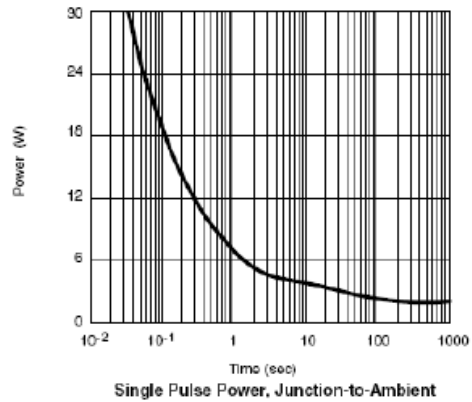
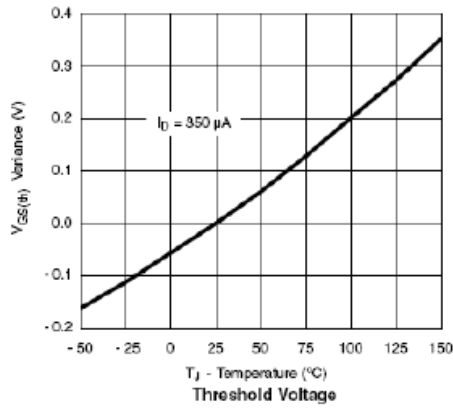
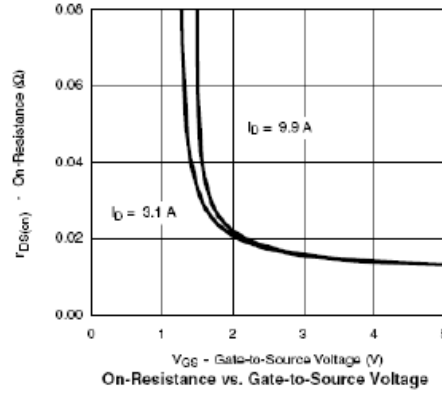
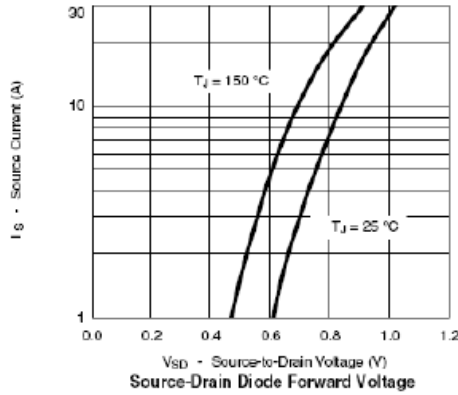
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

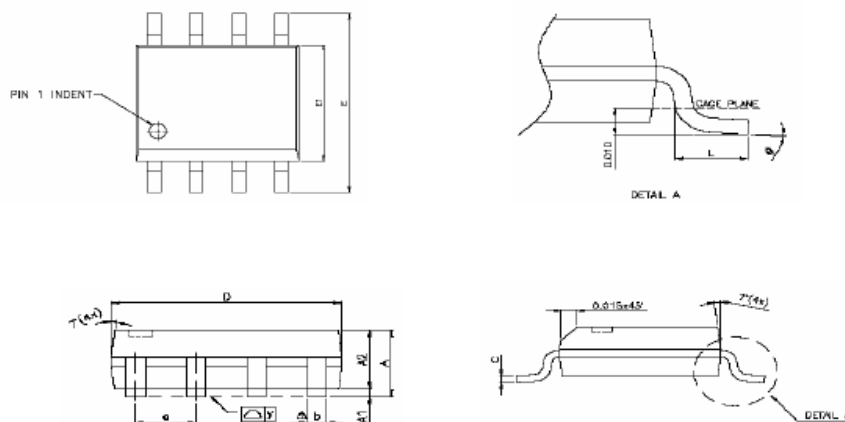
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.9	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 10 0	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-20			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-10A$ $V_{GS}=-2.5V, I_D=-8.6A$ $V_{GS}=-1.8V, I_D=-7.6A$		16 20 28	20 25 35	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-10A$		36		S
Diode Forward Voltage	V_{SD}	$I_S=-2.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V, V_{GS}=-5V$ $I_D=-10.0A$		30	45	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			8.0		
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V$ $f=1MHz$		2670		pF
Output Capacitance	C_{oss}			520		
Reverse Transfer Capacitance	C_{rss}			480		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=15\Omega$ $I_D=-1A, V_{GEN}=-4.5V$ $R_G=6\Omega$		25	40	nS
	t_r			45	70	
Turn-Off Time	$t_{d(off)}$			145	240	
	t_f			70	115	

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



PACKAGE OUTLINE SOP-8P


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
ϕ	0°	—	8°	0°	—	8°