PM5381

S/UNI-2488

SATURN USER NETWORK INTERFACE FOR 2488 M/BITS

Datasheet

Proprietary and Confidential

Released

Issue 4: June 2002

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PMC-2000489 (R4)

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Patents

Granted

The technology discussed is protected by one or more of the following patent grants:

U.S. Patent Numbers: 5,606,563; 5,640,398; 5,835,602; 5,883,545; 6,052,073; 6,054,884; 6,150,965; 6,188,692; 6,301,318

Canadian Patent Numbers: 2,149,076; 2,159,763; 2,161,921; 2,194,919; 2,226,610; 2,227,097

U.K. Patent Number 2,290,438

Other relevant patent grants may also exist.

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Detailed Revision History

Issue No.	Issue Date	Details of Change
Issue 4	June, 2002	Document issued for production release and Revision D of the device. Removed reference to FIFO_CLOCK in LINE_LOOP_BACK register bit description in register 0x0013. Corrected RRMP framing algorithm 2 description in 2nd paragraph of Section 10.3 Receive Regenerator and Multiplexer Processor (RRMP). Modified block diagrams in Section 6. Replaced STSI block with Frame Counter block. Modified INTE[4:1] register desriptions in registers 0x0005, 0x0006, and 0x0007. Changed TPRGM to PRGM. Removed references to TSTSI in register 0x0004. Replaced TSTSI with PRGM. Modified register bit descriptions for A_RSTB, RX_ENB, and DRU_ENB for registers 0x0843, 0x084B, 0x0853, and 0x085B. Modified register bit descriptions for ARSTB, TXLV_ENB, and APISO_ENB for registers 0x0865, 0x086D, 0x0875, and 0x087D. Added max and typical RMS jitter specs. Updated jitter tolerance graph. Added jitter transfer graphs. Modified TX2488_MODE[2:0] register bit configuration descriptions in register 0x0020. Updated REFCLK_P/N pin description. Removed note about single-ended PECL from “Notes on Pin Description”. Removed Ambient Temperature under Bias. Changed 2.97V to 3.14V. Modified FRlvds specs. Modified thermal resistance values. Modified junction-to-top thermal resistance. Upated Patent list. Changed “POS” to “POS-PHY’ in numerous places to more accurately reference the PL3 interface rather than Packet Over SONET. In register 0x0080, A2A2EN, Z0DEF, J0Z0INCEN bit descriptions were corrected to refer to TRMP Aux4 Configuration register instead of TRMP Aux1 Configuration register. In features list, change SONET/SDH signal defect/fail to B2 byte instead of B1 byte. Change “erred” and “errored” to “erroneous” throughout the document. TTOH and RTOH overhead pin descriptions modified to state all TOH bytes including undefined ones are included.

Issue No.	Issue Date	Details of Change
		Change TRSTB pin description to “TRSTB must be asserted at some point after power up and before the device registers are accessed.” Added pull-up resistance on input pads with pull-ups (30 to 50 kOhm). Modified device ID for rev D in register 0x0000 and JTAG description. Modified RCA pin description to remove erroneous info regarding early deassertion of RCA (4 or 0 bytes available in FIFO). Corrected RVAL description. Corrected TCA description. Updated limit for maximum allowable skew between APS links in Section 14.1, Incoming APS Serial TelecomBus. Updated functional timing diagrams for APSI and APSO links in Section 14.1, Incoming APS Serial TelecomBus, and 14.2, Outgoing APS Serial TelecomBus. Changed default state of TRAIN, DOOLV, and ROOLV in register 0x0013 to ‘X’. Modified RPAISINS_EN register bit description in register 0x0902 to indicate PAIS can be asserted on detection of LAIS, PAIS, or LOP using this register bit. Added to RHPP’s status bits (NEWPTR, ILLJREQ, PAISV, PLOPV, NDF, INVNDF, DISCOPA) to indicate they are only valid for master timeslots. Changed ILLPTR register bit to Unused. in register RHPP Indirect Register 5. Modified INVCNT description to state it must be set to logic 1 for SONET compliant behaviour. Bit 3 of register 0x780 must be set to logic 1 to improve PL3 output propagation time to meet timing specification. Modified C0_CRU/C1_CRU and C0_CSU/C1_CSU pin description to state that external capacitors are required in all configurations.
Issue 3	April 2002	Document issued for Revision C of the device. Filled out the Loopback description in the Operations Section. Updated mechanical diagram. Added 2.488Gb/s output jitter specs. Added new registers 0x0900 to 0x90F. Changed device ID code in JTAG and in register 0 for rev C. Added AC Timing for SONET Overhead signals. Added typical AC timing. Reduced the Tx ECL/PECL output levels to match the new 2.5G transmitter. Added statement to recommend setting CSU_MODE[2] register bit in register 0x0021 to logic 1 for optimal non-loop-timed intrinsic jitter performance.

Issue No.	Issue Date	Details of Change
		Added minimum RSTB pulse width in AC timing section. G1[7:0] register bits in THPP Transmit G1 POH and H4 Mask register now reference SRCG1 register bit as the enabling bit rather than SRCREI and SRCRDI bits. Changed recommended external CRU capacitor value to 10nF and external CSU capacitor value to 100nF. Updated internal resistance values and descriptions for CRU2488 and CSU2488 that are selected via CRU_MODE and CSU_MODE register bits. Removed CRU DC-offset and self narrowbanding modes. Modified FSBEN register bit in THPP Control Register (indirect register 0) to identify which timeslots are valid. Removed CSU_CLOCK register bit in register 0x0010. It is unused since the JAT CSU is to be permanently reset and bypassed. Corrected CRU_CLOCK description in register 0x010 to reference register 0x010 instead of 0x00. TXPHY's INBANDADDR register bit renamed to Reserved0 and added comment that its default value of logic 1 must be cleared to logic 0 for proper operation. Added Z0DEF register bit must be set to logic 0. Added Section 13.17 to describe using the SARC. Added jitter requirement for APSIFPCLK. Highlighted need to assert SARC's PAISPTREN to enable AIS-P consequential actions. Updated analog power supply filtering. Added typical jitter numbers in RCLK and TCLK pin descriptions. Added comments about CSU and CRU lock-up conditions. Added comment to set bit 0 of register 0038H to logic 1. Removed registers 0x20E and 0x2F from register map. Removed TSLDEL register bit. Removed statement about DCC input pins. Modified microprocessor AC timing diagrams to include WCIMODE = 1 feature. Modified statement regarding control circuitry for SONET wander transfer, holdover, and stability. Included reset start-up procedure to overcome the potential pmon counter lock-up condition in the RHPPs and SDQs. Enhanced desription for K.28.0 character of serial TeleCombus mapping in Sections 13.1.10 and 13.1.11. Added statement in Section 13.2 that states that consequential action of asserting RDI-P is not supported. Updated B3E signal description to state that it is only valid for OC48c

Issue No.	Issue Date	Details of Change
		mode of operation. Included SVCA indirect register access description in Section 13.19. Commented that SVCA's PJPMON and NJPMON counters values are only valid for master timeslots. Enhanced Diag_NDFREQ register bit description to state that this bit should be asserted and cleared whenever the corresponding SVCA timeslots are reconfigured.
2	June 2001	Document issued for Revision B of the device. Definition table added Pin Diagram inserted Pin Description tables updated Normal mode registers updated with final TSB EngDocs. Updated functional descriptions. Register Memory Map updated Added JTAG Test Port section. Added Boundary Scan Cells section. Added UL3/PL3 and associated info to Operations and Functional Timing sections. Added operations for PRGM, indirect register access, PMON servicing, and interrupt servicing. Modified analog interfacing information and register descriptions. Also revised DC Characteristics section - AVDH, VDDO, QAVD typical values read +/-5% and Vvddo, Vqavd values read 3.14 V min/3.47 V max
1	March 2000	Document Created.

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1 Definitions

The following table defines the abbreviations for the S/UNI-2488.

AIS	Alarm Indication Signal
APISO	APS Parallel to Serial Converter
APS	Automatic Protection Switching
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CRU	Clock Recovery Unit
CSU	Clock Synthesis Unit
DCC	Data Communication Channel
DRU	Data Recovery Unit
ECL	Emitter-Coupled Logic
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
FEBE	Far-End Block Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Controller
JAT	Jitter Attenuator
LCD	Loss of Cell Delineation
LFSR	Linear Feedback Shift Register
LOF	Loss of Frame
LOP	Loss of Pointer
LOS	Loss of Signal
LVDS	Low Voltage Differential Signaling
LVTTL	Low-Voltage Transistor-Transistor Logic
NC	No Connect, indicates an unused pin
NDF	New Data Flag
NNI	Network-Network Interface
ODL	Optical Data Link
OOF	Out of Frame
PECL	Pseudo-ECL

PISO	Parallel-In-Serial-Out (Parallel to Serial Converter)
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PRBS	Pseudo-Random Bit Sequence
PRGM	SONET/SDH PRBS Generator/Monitor Block
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RCFP	Receive Cell and Frame Processor Block for STS-48c (STM-16c) channel
RDI-L	Line Remote Defect Indication
RHPP	Receive High Order Path Processor
RRMP	Receive Regenerator and Multiplexer Processor
RTTP	Receive Tail Trace Processor
RXPHY	Receive PHY Interface
RXSDQ	Receive Scalable Data Queue FIFO
RDI	Remote Defect Indication
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Rate Monitor
SD	Signal Detect
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SIPO	Serial-In Parallel-Out (Serial to Parallel Converter)
SIRP	SONET/SDH Inband Error Report Processor
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelopes
STLI	SONET/SDH Transmit Line Interface
STSI	Space and Timeslot Interchange
SVCA	SONET/SDH Virtual Container Aligner
TCFP	Transmit Cell and Frame Processor for STS-48c (STM-16c) channel
THPP	Transmit High Order Path Processor
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable
TOH	Transport Overhead
TRMP	Transmit Regenerator Multiplexer Processor
TTTP	Transmit Tail Trace Processor
TXPHY	Transmit PHY Interface
TXSDQ	Transmit Scalable Data Queue FIFO
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VCXO	Voltage Controlled Crystal (Xtal) Oscillator

VPI	Virtual Path Indicator
WAN	Wide Area Network
XOR	Exclusive OR logic operator

2 Features

2.1 General

- Single chip ATM and POS User-Network Interface operating at 2488.32 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).
- Processes bit-serial 2488.32 Mbit/s STS-48 (STM-16-16c) data streams with on-chip clock and data recovery and clock synthesis.
- Complies with Bellcore GR-253-CORE jitter tolerance, jitter transfer and RMS intrinsic jitter criteria.
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.
- Provides UTOPIA Level 3 32-bit wide System Interface (clocked up to 104 MHz) with parity support for ATM applications.
- Provides SATURN POS-PHY Level 3™ 32-bit System Interface (clocked up to 104 MHz) for Packet over SONET (POS), or ATM applications.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from the line side transmit stream to the line side receive stream interface.
- Provides support for automatic protection switching via a 4-bit LVDS 777.76 MHz port.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3V compatible.
- Wide operating temperature range (-40°C to +85°C).
- 416 pin UBGA package.

2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the received stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Extracts and optionally inserts on dedicated pins the SONET/SDH transport overhead for an STS-48c/STM-16c frame.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream. Inserts the synchronization status message (S1) byte into the transmit stream.
- Extracts a 64 byte (Bellcore compatible) or 16 byte (ITU compatible) section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 64 byte or 16 byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.
- Configurable to force Line AIS in the transmit stream.
- Provides automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Provides automatic DROP bus line AIS insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Supports Automatic Protection Switching (APS) via a mate protection port.

2.3 SONET Path / SDH High Order Path

- Interprets the received payload pointer (H1, H2) and extracts the STS-48c/STM-16c synchronous payload envelope and path overhead.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Extracts and inserts the entire SONET/SDH path overhead to and from dedicated pins. The path overhead bytes may be sourced from internal registers or from the bit serial path overhead input stream. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ) and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.

- Extracts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 64 byte or 16 byte path trace (J1) message using an internal register bank for the transmit stream.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path remote error indications (REI's) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI).

2.4 The Receive ATM Processor

- Extracts ATM cells from the received STS-48c/STM-16c channel payloads using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection, and idle/unassigned cell filtering.
- Detects out of cell delineation (OCD) and loss of cell delineation (LCD) alarms.
- Counts the number of received cells, idle cells, erroneous cells and dropped cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support to read extracted cells from an internal 48 cell FIFO buffer.

2.5 The Receive POS Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing.
- Performs self-synchronous POS data de-scrambling on the received STS-48c/STM16c-16c payloads using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS frames.
- Performs frame check sequence (FCS) validation for CRC-CCITT and CRC-32 polynomials.
- Performs control escape de-stuffing or byte de-stuffing of the POS stream.
- Detects packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as erroneous.
- Permits FCS stripping on the POS-PHY output data stream.

- Provides a SATURN POS-PHY Level 3™ compliant 32-bit datapath interface (clocked up to 104 MHz) with parity support to read packet data from an internal 192x16-byte FIFO buffer.

2.6 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Optionally provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts the number of transmitted cells.
- Provides UTOPIA Level 3 and POS-PHY Level 3 32-bit wide datapath interfaces (clocked up to 104 MHz) with parity support for writing cells into an internal 48 cell FIFO.

2.7 The Transmit POS Processor

- Supports any packet based link layer protocol using byte synchronous and bit synchronous framing like PPP, HDLC and Frame Relay.
- Performs self-synchronous POS data scrambling using the $1+X^{43}$ polynomial.
- Encapsulates packets within a POS/HDLC frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Optionally performs frame check sequence generation using the CRC-CCITT and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.
- Provides a SATURN® POS-PHY Level 3™ compliant 32-bit wide datapath (clocked up to 104 MHz) with parity support to an internal 192x16-byte FIFO buffer.

3 Applications

- ATM and Multi-service Switches, routers, and switch/routers
- SONET/SDH Add/Drop Multiplexers with data processing capabilities
- Uplink cards
- SONET/SDH ATM/POS Test Equipment

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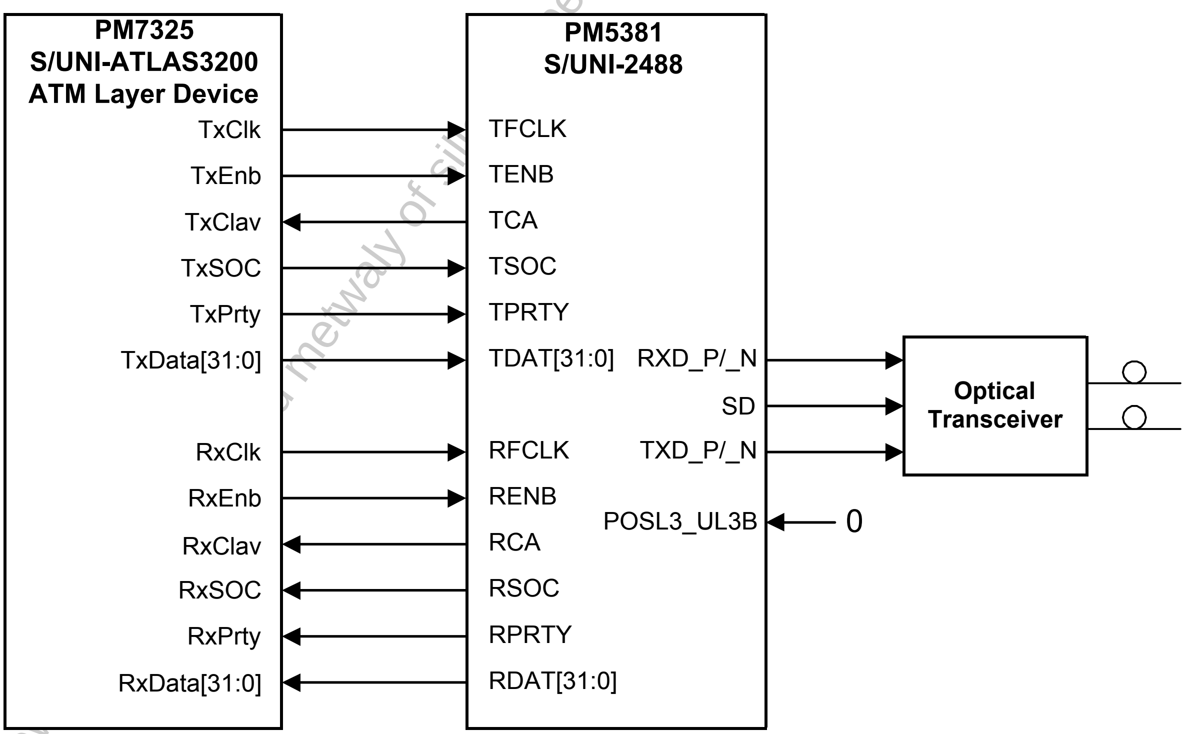
5 Application Examples

The PM5381 S/UNI-2488® device is applicable to equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), as well as Packet over SONET (POS) interfaces. The POS interface can support several packet based protocols including the Point-to-Point Protocol (PPP). The S/UNI-2488 may find application at either end of switch-to-switch links, router to router links, switch to router links or switch-to-terminal links in public and private wide area networks (WAN). The S/UNI-2488 provides a comprehensive feature set as well as compatibility with WAN synchronization requirements. The S/UNI-2488 performs the mapping of either ATM cells or POS frames into the SONET/SDH STS-48 (STM-16-16c) synchronous payload envelope (SPE) and processes applicable SONET/SDH section, line and path overheads.

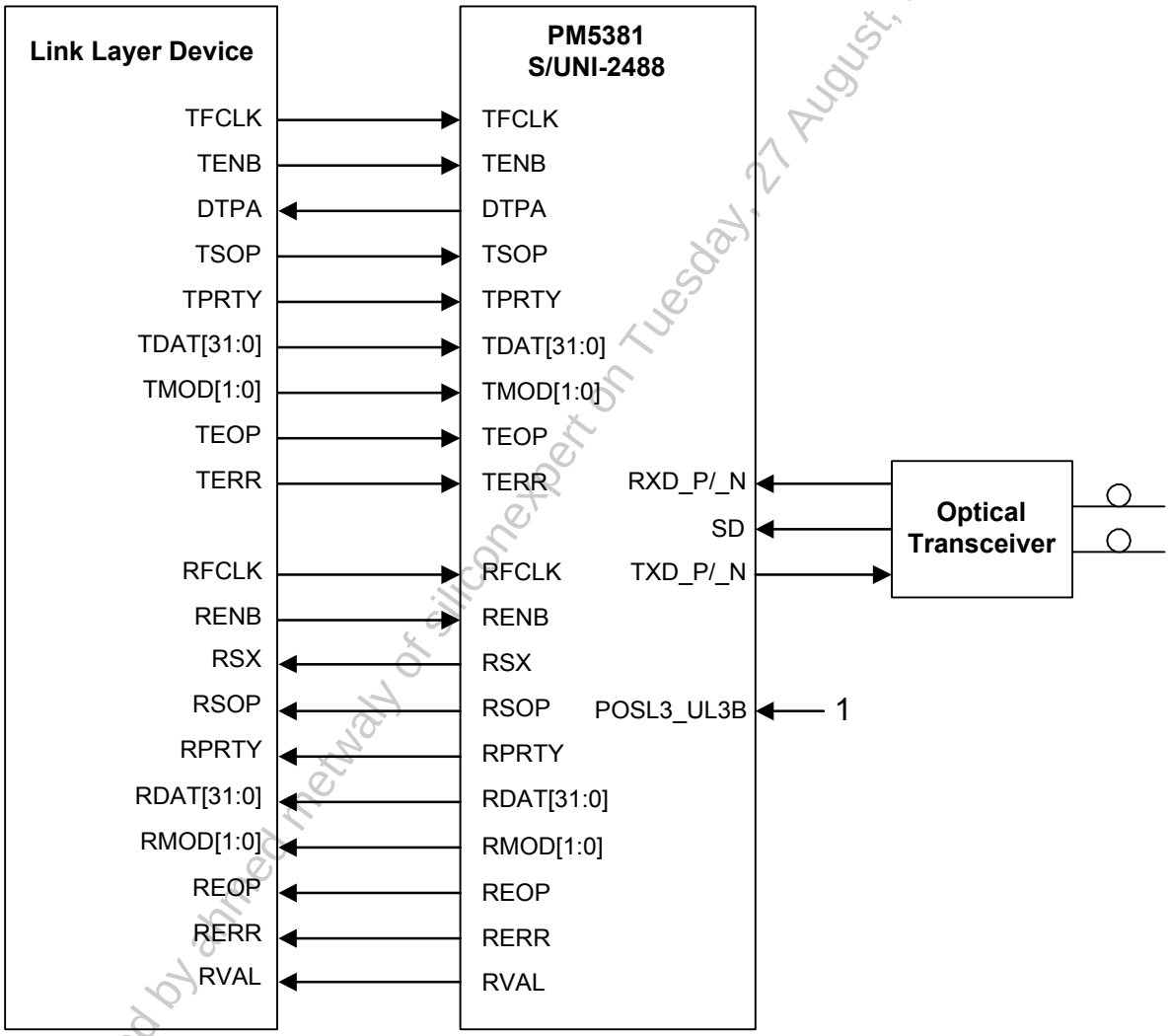
In a typical STS-48 (STM-16-16c) ATM application, the S/UNI-2488 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-2488 interfaces directly with ATM layer processors and switching or adaptation functions using a UTOPIA Level 3 compliant 32-bit (clocked up to 104 MHz) synchronous FIFO style interface. An application with a UTOPIA Level 3 system side interface is shown in Figure 1. The initial configuration and ongoing control and monitoring of the S/UNI-2488 are normally provided via a generic microprocessor interface.

Figure 1 STS-48 (STM-16-16c) ATM (UTOPIA Level 3) Switch Port Application



In a typical Packet over SONET application (i.e. using the PPP protocol) the S/UNI-2488 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-2488 interfaces directly with a data link layer processor using a SATURN POS-PHY Level 3™ 32-bit (clocked up to 104 MHz) synchronous FIFO interface over which packets are transferred. The initial configuration and ongoing control and monitoring of the S/UNI-2488 are normally provided via a generic microprocessor interface.

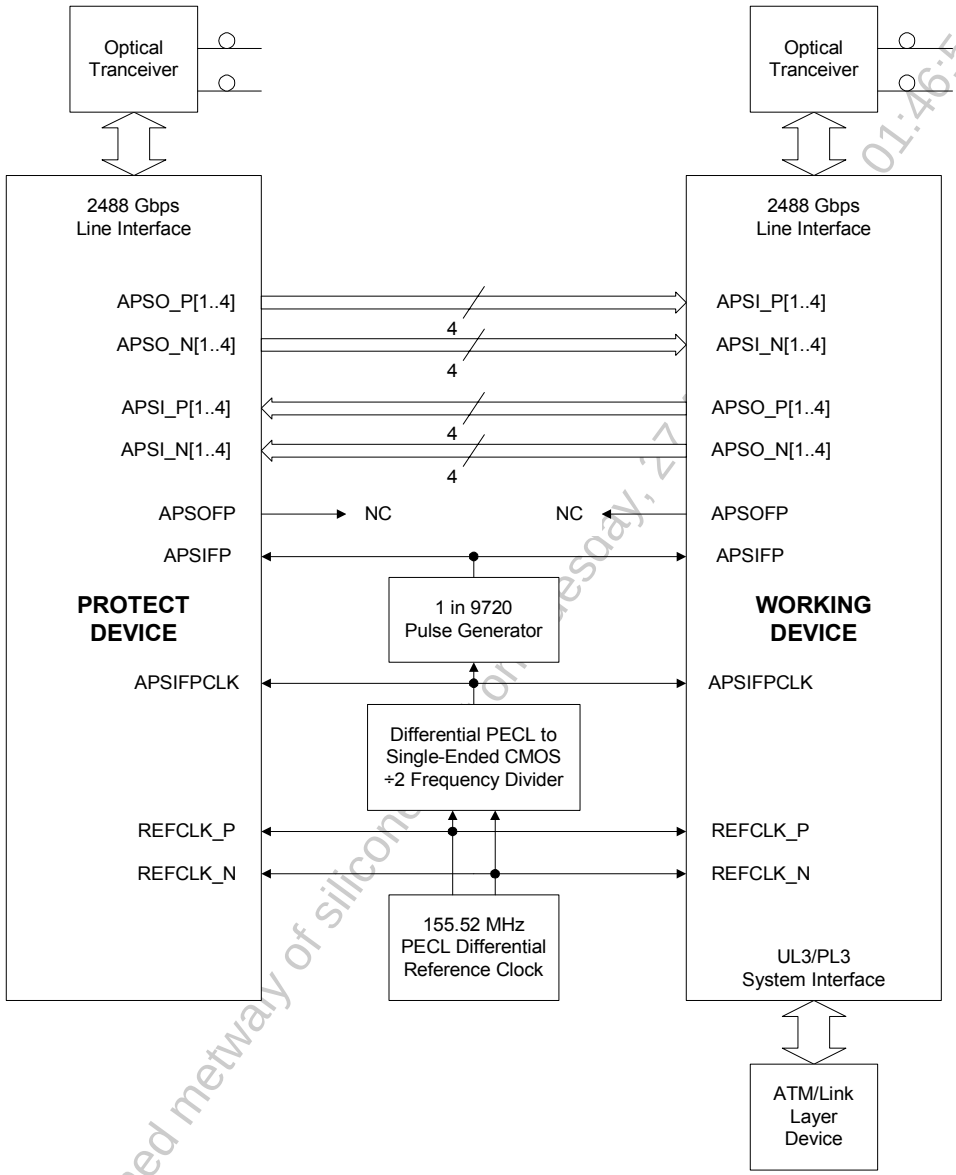
Figure 2 STS-48 (STM-16-16c) Packet Over SONET (POS-PHY Level 3) Router Application



The S/UNI-2488 supports Automatic Protection Switching. APS mode allows the S/UNI-2488 to switch over to a second S/UNI-2488 in the middle of the data-path to transmit and receive over a second optical connection. The example below is a 1+1 configuration (one working, plus one protection), with the normal "working" device switching over to the "protect" device in response to an interruption on the working chip's line side. It illustrates the connections between the two chips.

The single-ended 77.76MHz APSIFPCLK is generated directly from the common 155.52MHz PECL Differential Reference Clock. This clocks the common frame pulse generator. This is the way these signals are intended to be generated. Note that APSOFP is not used, as this is a diagnostic port only. APSOFP should not be connected to APSIFP.

Figure 3 APS Connection Example – 1+1 Architecture



6 Block Diagram

Figure 4 Normal Operation

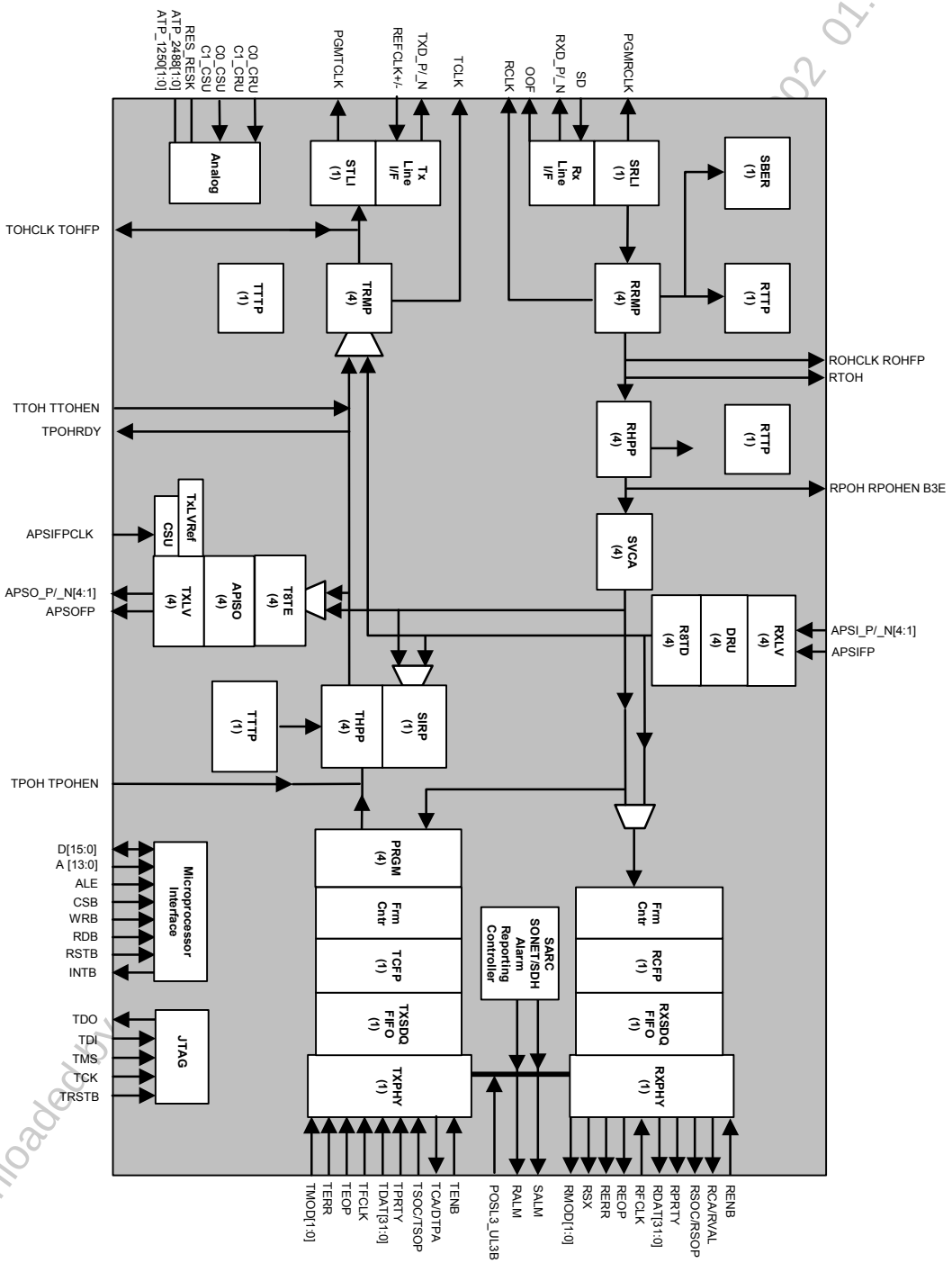


Figure 5 Loopback Modes

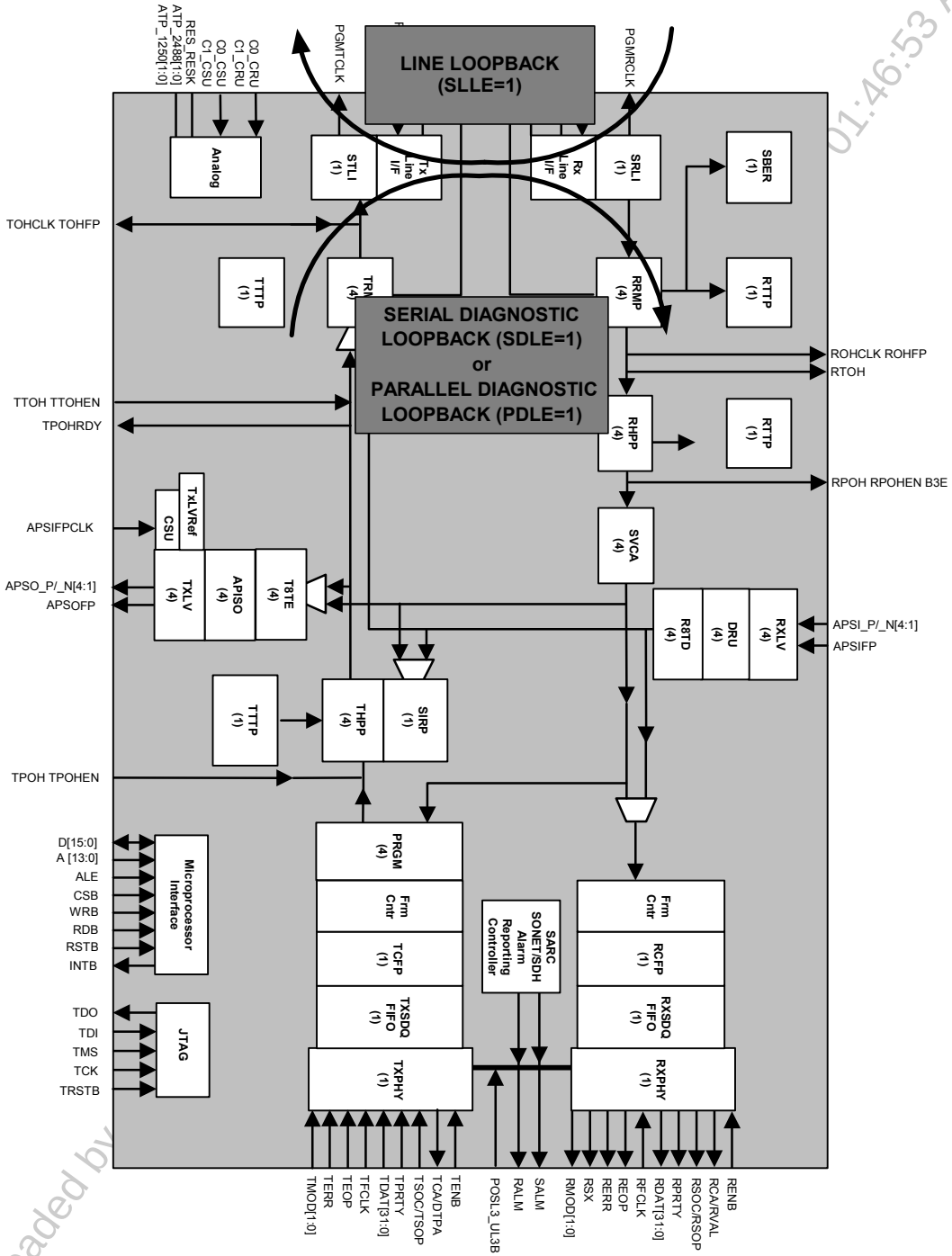


Figure 6 APS Working

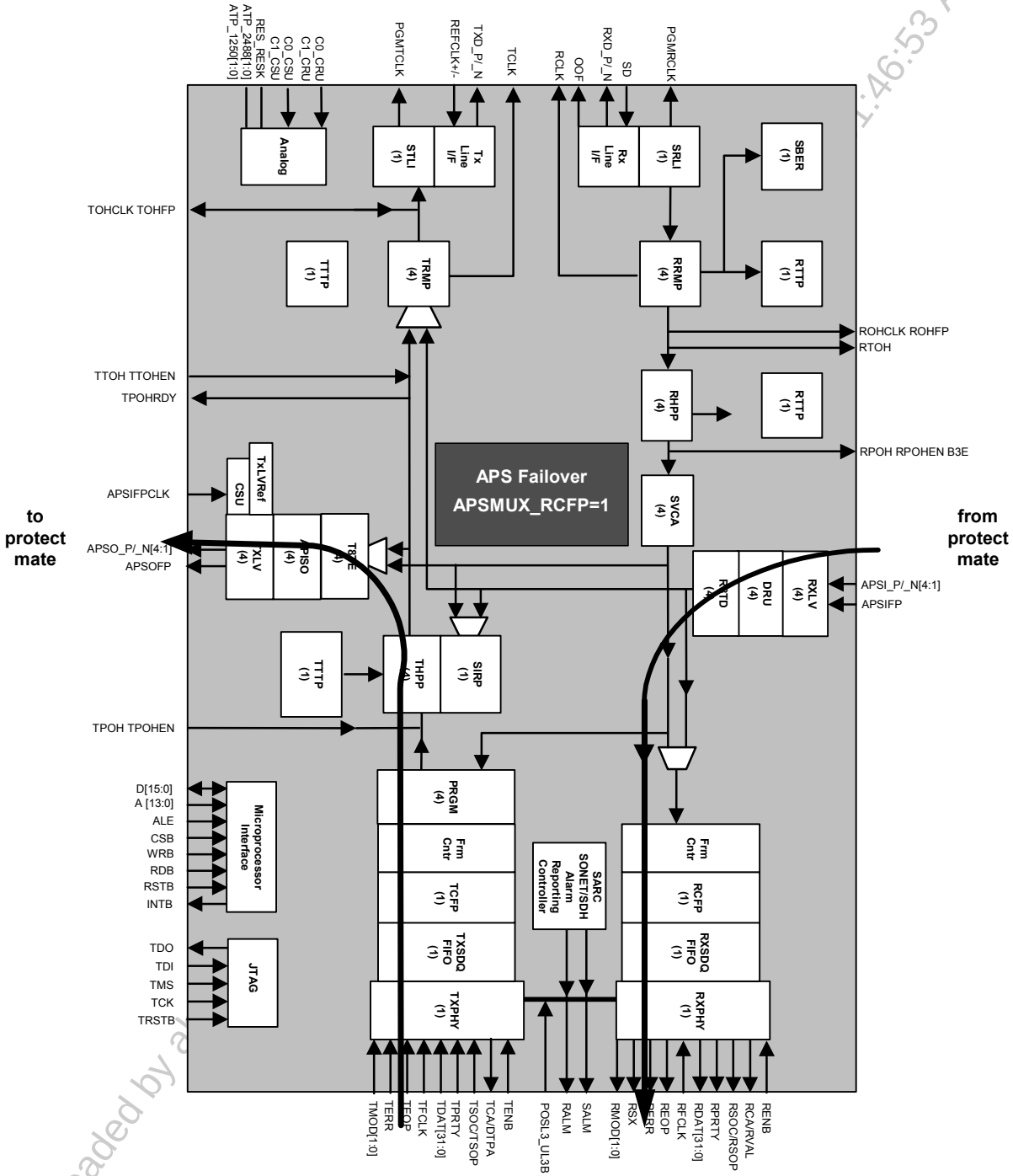
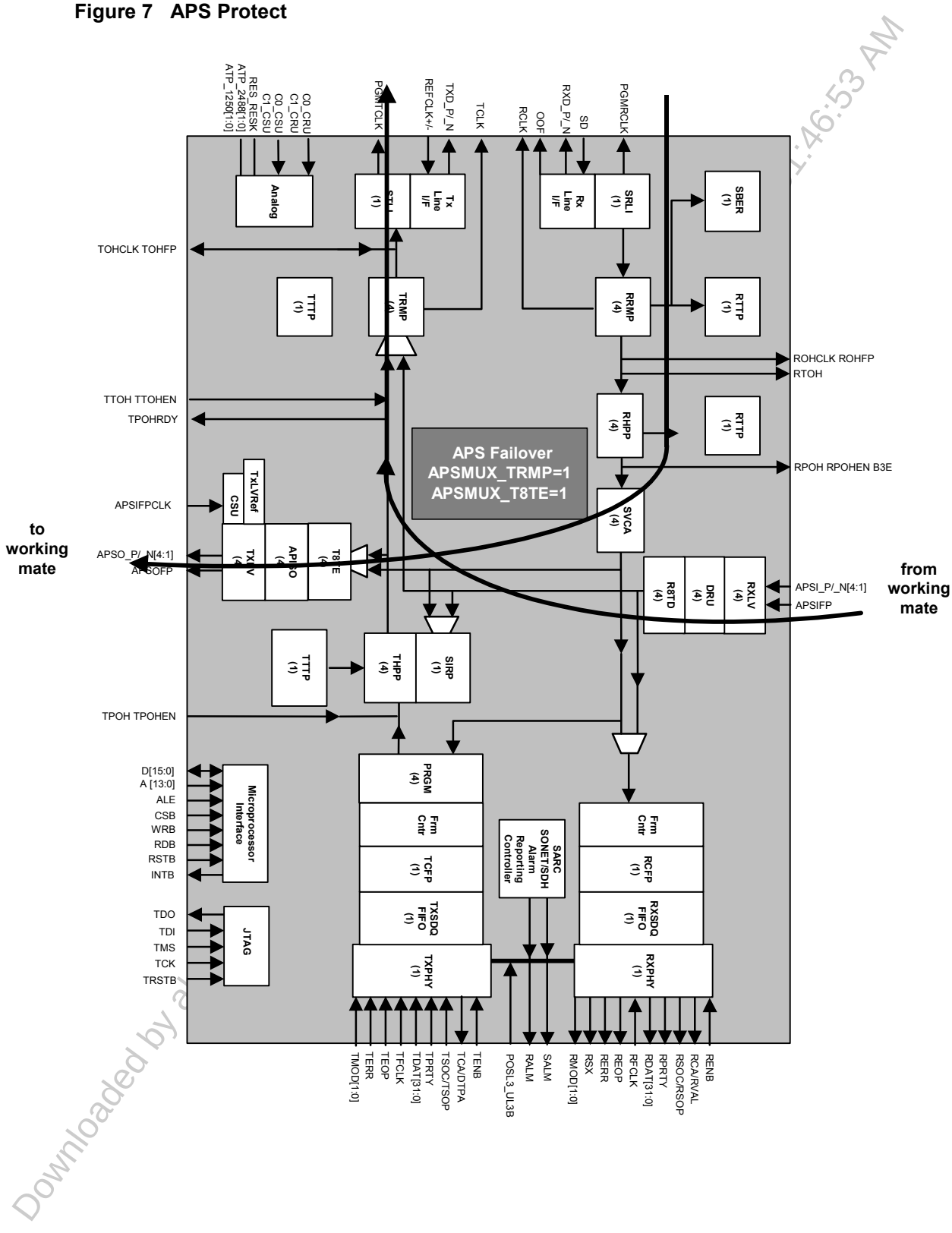


Figure 7 APS Protect



7 Description

The PM5381 S/UNI-2488 SATURN User Network Interface is a monolithic integrated circuit that implements SONET/SDH processing, ATM mapping and Packet over SONET mapping functions at the STS-48 (STM-16-16c) 2488.32 Mbit/s rate.

The S/UNI-2488 receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. The S/UNI-2488 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI-2488 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cells or POS frames.

When used to implement an ATM UNI or NNI, the S/UNI-2488 frames to the ATM payload using cell delineation. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of a header check sequence error. The ATM cell payloads are descrambled and are written to a 48-cell FIFO buffer (programmable FIFO depth). The received cells are read from the FIFO using a 32-bit wide UTOPIA Level 3 (clocked up to 104 MHz) datapath interface. Counts of received ATM cell headers that are erroneous are accumulated independently for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI-2488 extracts Packet over SONET (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive 192x16-byte FIFO (programmable FIFO depth – all packets are 16 byte block aligned). The received packets are read from the FIFO through a 32-bit POS-PHY Level 3 (clocked up to 104 MHz) system side interface. Valid packet and erroneous packet counts are provided for performance monitoring. The S/UNI-2488 Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

The S/UNI-2488 transmits SONET/SDH streams using a bit serial interface. The S/UNI-2488 synthesizes the transmit clock from a 155.52MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI-2488 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM or POS frames. The S/UNI-2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

When used to implement an ATM UNI or NNI, ATM cells are written to an internal 48 cell FIFO (programmable FIFO depth) using a 32-bit wide UTOPIA Level 3 (clocked up to 104 MHz) datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI-2488 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH link, the S/UNI-2488 inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 192x16-byte FIFO (programmable FIFO depth – all packets are 16 byte block aligned) through a 32-bit SATURN POS-PHY Level 3™ (clocked up to 104 MHz) system side interface. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

No line rate clocks are required directly by the S/UNI-2488 as it synthesizes the transmit clock and recovers the receive clock using a 155.52 MHz reference clock. The S/UNI-2488 outputs a differential PECL line data (TXD_P/ TXD_N).The S/UNI-2488 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI-2488 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-2488 is implemented in low power, +1.8 Volt, CMOS technology. It has LVTTL/CMOS compatible digital inputs and LVTTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3V compatible pseudo-ECL (PECL). The S/UNI-2488 is packaged in a 416 pin UBGA package.

8 Pin Diagram

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A	VSS	VSS	VSST	VSST	VSST	VSST	VSST	VSST	VSST	vddi	VSST	tenb	tmod[0]	terr	VSS
B	VSS	VDD	VSS	VSST	VSST	VSST	VSST		VSST	VSST	VSST	posl3_ul3b	tfclk	tmod[1]	teop
C	tck	VSS	VDD		VSST	VSST	VSST	VSST		VSST	VSST	VSST	vddi	vddi	vddi
D	rdat[31]	vddi	trstb	VDD	VSST	VSST		VSST	VSST	vddi	VDD	VSST	tdo	tca_dtpa	tsoc_tsop
E	rdat[27]	rdat[30]	rfclk	tms											
F	rdat[23]	rdat[26]	rdat[29]	tdi											
G	rdat[20]	vddi	rdat[25]	rdat[28]											
H	rdat[17]	rdat[19]	rdat[22]	rdat[24]											
J	rdat[13]	rdat[16]	rdat[18]	rdat[21]											
K	rdat[10]	vddi	rdat[15]	VDD											
L	rdat[7]	rdat[9]	rdat[12]	rdat[14]											
M	rdat[3]	rdat[5]	rdat[8]	rdat[11]											
N	rdat[1]	vddi	rdat[4]	rdat[6]											
P	reop	rprty	rdat[0]	rdat[2]											
R	VSS	rsx	rsoc_rsop	VDD											
T	VSS	rerr	rmod[1]	rmod[0]											
U	rca_rval	vddi	renb	rohfp											
V	rohclk	rtoh	rpohen	rpoh											
W	vddi	b3e	VSST	VSST											
Y	VSST	VSST	VSST	VDD											
AA	VSST	VSST	vddi	VSST											
AB	VSST		VSST	VSST											
AC		VSST	VSST	VSST											
AD	VSST	VSST	VSST	VSST											
AE	VSST		VSST	VSST											
AF	VSST	VSST	VSST	VSST											
AG	VSST	VSST		VDD	salm	tohfp	vddi	rclk	csuclko	AVDL	QAVD	AVDH	c0_cru	AVDH	VSS
AH	VSST	VSS	VDD	oof	vddi	tpoh	sd	pgmtclk		AVDL	QAVD	AVDH	c1_cru	AVDH	VSS
AJ	VSS	VDD	VSS	tohclk	ttohen	tpohrdy	tclk	cruclko		AVDL	c0_csu	AVDH	atp_2488[0]	AVDH	VSS
AK	VSS	VSS	ralm	ttoh	tpohen	pgmrclk	csuclki	VSS	VSS	AVDL	c1_csu	AVDH	atp_2488[1]	VSS	rxd_p
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

S/UNI 2488
Left Quadrants
Upper & Lower

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	tdat[1]	vddi	tdat[6]	tdat[10]	tdat[12]	vddi	tdat[19]	tdat[22]	tdat[25]	tdat[29]	VSST	VSST	VSS	VSS	A
tprty	tdat[2]	tdat[5]	tdat[8]	vddi	tdat[15]	tdat[18]	tdat[21]	tdat[24]	tdat[28]	tdat[31]	VSST	VSS	VDD	VSS	B
tdat[0]	tdat[3]	tdat[7]	tdat[11]	tdat[14]	tdat[17]	tdat[20]	vddi	tdat[27]	vddi	VSST	VSST	VDD	VSS	wrb	C
VDD	tdat[4]	tdat[9]	tdat[13]	tdat[16]	VDD	tdat[23]	tdat[26]	tdat[30]	VSST	VSST	VDD	intb	rdb	a[0]	D
											rstb	ale	a[1]	a[3]	E
											csb	vddi	a[4]	a[7]	F
											a[2]	a[5]	a[8]	vddi	G
											a[6]	a[9]	a[11]	d[0]	H
											a[10]	a[12]	d[1]	d[3]	J
											a[13]	d[2]	d[4]	d[6]	K
											VDD	vddi	d[7]	d[9]	L
											d[5]	d[8]	d[11]	d[12]	M
											d[10]	vddi	d[13]	d[15]	N
											d[14]	apsifpclk	apsifp	apsofp	P
											vddi			VSS	R
											VDD		vddi	VSS	T
											AVDH	AVDH	apso_n[4]	apso_p[4]	U
											apso_n[3]	apso_p[3]	apso_n[2]	apso_p[2]	V
											AVDH	apso_n[1]	apso_p[1]	VSS	W
											apsi_p[4]	apsi_n[4]	apsi_p[3]	apsi_n[3]	Y
											AVDL	apsi_p[2]	apsi_n[2]	VSS	AA
											apsi_p[1]	apsi_n[1]		csu_avdh	AB
											AVDH	VSS	VSS	VSS	AC
											AVDL	AVDL	VSS	VSS	AD
											res			VSS	AE
											AVDH	atp_1250[1]	AVDL		AF
VSS	AVDH	VSS	VSS	VSS	AVDH	AVDH	QAVD	vddi	AVDL	AVDL	VSS	AVDH	atp_1250[0]	resk	AG
VSS	AVDH	VSS	VSS	VSS	AVDH	AVDH	QAVD	vddi	AVDL	AVDL	VSS	VSS	AVDH	VSS	AH
VSS	AVDH	VSS	VSS	VSS	AVDH	AVDH	VSS	vddi	AVDL	AVDL	VSS	VSS	VSS	AVDH	AJ
rxd_n	VSS	txd_n	txd_p	VSS	refclk_p	refclk_n	VSS	vddi	AVDL	AVDL	VSS	VSS	VSS	VSS	AK
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

S/UNI 2488
Right Quadrants
Upper & Lower

9 Pin Description

9.1 Serial Line Side Interface Signals (7)

Pin Name	Type	Pin No.	Function
REFCLK_P REFCLK_N	Differential PECL - compatible Input	AK10 AK9	The differential **reference clock** inputs (REFCLK_P / REFCLK_N) provides a 155.52 MHz reference clock for both the clock recovery and the clock synthesis circuits. The two PECL inputs are internally terminated with differential 100-Ω termination. In practice, jitter on REFCLK_P / REFCLK_N inputs must be less than 1 psec RMS in 12KHz to 20MHz band in order for S/UNI2488 to comply with Bellcore GR-253 intrinsic jitter specs on transmit data outputs. Note: Any jitter on REFCLK_P / REFCLK_N up to about 20 MHz will also appear at the transmit data output. Please refer to the Operation section for a discussion of PECL interfacing issues.
RXD_P RXD_N	Differential PECL-compatible Input	AK16A K15	The **receive differential data** PECL-compatible inputs (RXD_P/ RXD_N) contain the 2488.32 Mbit/s NRZ bit serial receive stream. The two receive inputs are internally terminated with differential 100-Ω termination. The receive clock is recovered from the RXD_P/ RXD_N bit stream. Please refer to the Operation section for a discussion of PECL interfacing issues.
SD	TTL Input	AH24	The **receive signal detect** TTL input (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A logic high indicates the presence of valid data. A logic low indicates a loss of signal. Unless SD detection is disabled, deassertion of SD will cause the 2488 CRU to go into training mode where it locks to REFCLK_P/REFCLK_N. Please refer to the Operation section for a discussion of interfacing issues
TXD_P TXD_N	Differential, CML - compatible Output	AK12 AK13	The **transmit differential data** CML-compatible outputs (TXD_P/ TXD_N) contain the 2488.32 Mbit/s transmit stream. The TXD_P/ TXD_N outputs are driven using the synthesized clock from the CSU. Please refer to the Operation section for a discussion of the voltage swing levels.

9.2 Clocks and Alarms (7)

Pin Name	Type	Pin No.	Function
PGMRCLK	Output	AK25	The **programmable receive clock** (PGMRCLK) signal provides timing reference for the receive line interface. PGMRCLK is a divided version of the recovered clock. When the PGMRCLKSEL register bit is set low, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock. When the PGMRCLKSEL register bit is set high, PGMRCLK is a nominal 8 KHz, 50% duty cycle clock. The PGMRCLK output can be disabled and held low by programming the PGMRCLKEN bit in the SRLI PGM Clock Configuration register.
RCLK	Output	AG23	The **receive clock** (RCLK) signal provides timing reference for the receive interface. This pin is driven by a digital pad and is not intended to be used as a clock source. An external PLL is required to smooth this clock if it is desired to be used as a clock source. Jitter on this clock is typically about 450ps. RCLK is a nominal 77.76 MHz 50% duty cycle clock. The RCLK output can be disabled and held low by programming the RCLKEN bit in the SRLI Clock Configuration register. OOF and SALM are updated on the rising edge of RCLK.
PGMTCLK	Output	AH23	The **programmable transmit clock** (PGMTCLK) signal provides timing reference for the transmit line interface. PGMTCLK is a divided version of the reference clock. When the PGMTCLKSEL register bit is set low, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock. When the PGMTCLKSEL register bit is set high, PGMTCLK is a nominal 8 KHz, 50% duty cycle clock. The PGMTCLK output can be disabled and held low by programming the PGMTCLKEN bit in the STLI PGM Clock Configuration register.
TCLK	Output	AJ24	The **transmit clock** (TCLK) signal provides timing reference for the transmit interface. This pin is driven by a digital pad and is not intended to be used as a clock source. An external PLL is required to smooth this clock if it is desired to be used as a clock source. Jitter on this clock is typically about 450ps. TCLK is a nominal 77.76MHz 50% duty cycle clock. The TCLK output can be disabled and held low by programming the TCLKEN bit in the STLI Clock Configuration register.

Pin Name	Type	Pin No.	Function
OOF	Output	AH27	The active high **out of frame** (OOF) signal indicates when an out of frame condition is declared by the framing block. OOF is set high while the framing block is out of frame. An out of frame condition is declared when four consecutive erroneous framing patterns (A1 and A2 bytes) have been detected. OOF is set low while the framing block is in frame. OOF is updated on the rising edge of RCLK.
SALM	Output	AG26	The **section alarm** (SALM) signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the S/UNI-2488 SARC Section SALM Enable registers. SALM is set low when none of the enabled alarms are active. Section Alarms can only be extracted from the first STS-12 slice in this manner. SALM is updated on the rising edge of RCLK.
RALM	Output	AK28	The **Receive Alarm** (RALM) signal is the output of alarms of the receive path. Each alarm represents the logical OR of the SALM, LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PSLM, PDI-P, TIU-P, TIM-P status of the path. The selection of alarms to be reported is controlled by the S/UNI-2488 SARC Path RALM Enable registers. Receive Alarms can only be extracted from the first STS-12 slice in this manner. RALM is updated on the falling edge of ROHCLK. Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm.
CSUCLKO	Output	AG22	The JAT-**CSU output clock** (CSUCLKO) is used for PMC test purposes only. It must be left as a no-connect (NC) during the normal mode of operation.
CSUCLKI	Input	AK24	The JAT-**CSU input clock** (CSUCLKI) is used for PMC test purposes only. It must be tied to VSS during the normal mode of operation.
CRUCLKO	Output	AJ23	The **CRU output clock** (CRUCLKO) is used for PMC test purposes only. It must be left as a no-connect (NC) during the normal mode of operation.

9.3 Receive Section/Line/Path Overhead Extraction Signals (6)

Pin Name	Type	Pin No.	Function
ROHCLK	Output	V30	The **receive overhead clock** (ROHCLK) signal provides timing for the receive section, line and path overhead extraction. ROHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. ROHCLK has a 33% high duty cycle. ROHFP, RTOH, RPOH, RPOHEN, B3E, and RALM are updated on the falling edge of ROHCLK.
ROHFP	Output	U27	The **receive overhead frame pulse** (ROHFP) signal provides timing for the receive section, line and path overhead extraction. ROHFP is used to indicate the most significant bit (MSB) on RTOH, RPOH and the first possible path BIP error on B3E. ROHFP can be sampled on the rising edge of ROHCLK. ROHFP is updated on the falling edge of ROHCLK.
RTOH	Output	V29	The **receive transport overhead** (RTOH) signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2, and all undefined transport overhead) extracted from the first STS-12 (RRMP #1 only) of the incoming stream. RTOH is updated on the falling edge of ROHCLK.
RPOH	Output	V27	The **receive path overhead** (RPOH) signal contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the STS-48c/STM16c SONET/SDH path overhead. Path overhead can only be extracted from the first STS-12 slice in this manner. The RPOHEN signal is set high to indicate valid path overhead bytes on RPOH. RPOH is updated on the falling edge of ROHCLK.
RPOHEN	Output	V28	The **receive path overhead enable** (RPOHEN) signal indicates valid path overhead bytes on RPOH When the RPOHEN signal is set high, the corresponding path overhead byte presented on RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on RPOH is invalid. RPOHEN is updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
B3E	Output	W29	The **bit interleaved parity error** (B3E) signal carries the path BIP-8 errors detected for the STS-48c SONET payload. This signal is not valid for non-STS-48c configurations. B3E is set high for one ROHCLK clock cycle for each STS-48c path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E is set high for one ROHCLK clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. B3E is updated on the falling edge of ROHCLK.

9.4 Transmit Section/Line/Path Overhead Insertion Signals (7)

Pin Name	Type	Pin No.	Function
TOHCLK	Output	AJ27	The **transmit overhead clock** (TOHCLK) signal provides timing for the transmit section, line and path overhead insertion. TOHCLK is a nominal 20.736MHz clock generated by gapping a 25.92MHz clock. TOHCLK has a 33% high duty cycle. TOHFP and TPOHRDY are updated on the falling edge of TOHCLK. TTOH, TTOHEN, TPOH and TPOHEN are sampled on the rising edge of TOHCLK.
TOHFP	Output	AG25	The **transmit overhead frame pulse** (TOHFP) signal provides timing for the transmit section, line and path overhead insertion. TOHFP is used to indicate the most significant bit (MSB) on TTOH and TPOH. TOHFP is set high when the MSB of the: First A1 byte should be present on TTOH. First J1 byte should be present on TPOH. TOHFP can be sampled on the rising edge of TOHCLK. TOHFP is updated on the falling edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TTOH	Input	AK27	The **transmit transport overhead** (TTOH) signal contains all transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2, and all undefined transport overhead) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. Transport overhead can only be inserted into the first STS-12 slice in this manner. TTOH should be grounded if it is not used. TTOH is sampled on the rising edge of TOHCLK.
TTOHEN	Input	AJ26	The **transmit transport overhead insert enable** (TTOHEN) signal controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN is high during the most significant bit of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, E2, and all undefined transport overhead bytes). When TTOHEN is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. When TTOHEN is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH, the sampled TOH byte is logically XORed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH byte allows the incoming bit to go through while a bit set to logic high will toggle the outgoing bit. A low level on TTOHEN during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN should be grounded if it is not used. Transport overhead can only be inserted into the first STS-12 slice in this manner. TTOHEN is sampled on the rising edge of TOHCLK.
TPOH	Input	AH25	The **transmit path overhead** (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in the STS-48c SONET path overhead and the error masks to be applied on B3 and H4. Path overhead can only be inserted within the first STS-12 slice in this manner. A path overhead byte is accepted for transmission when the external source indicates a valid byte (TPOHEN set high) and the S/UNI-2488 indicates ready (TPOHRDY set high). The S/UNI-2488 will ignore the byte on TPOH when TPOHEN is set low. The TPOHRDY is set low to indicate that the S/UNI-2488 is not ready and the byte must be re-presented at the next opportunity. TPOH should be grounded if it is not used. TPOH is sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
TPOHRDY	Output	AJ25	The **transmit path overhead insert ready** (TPOHRDY) signal indicates if the S/UNI-2488 is ready to accept the byte currently on TPOH. TPOHRDY is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH input. This byte will be accepted if TPOHEN is also set high. If TPOHEN is set low, the byte is invalid and is ignored. TPOHRDY is set low to indicate that the S/UNI-2488 is unable to accept the byte on TPOH and expects the byte to be re-presented at the next opportunity. TPOHRDY is updated on the falling edge of TOHCLK.
TPOHEN	Input	AK26	The **transmit path overhead insert enable** (TPOHEN) signal controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. TPOHEN is set high during the most significant bit of a POH byte to indicate valid data on the TPOH input. This byte will be accepted for transmission if TPOHRDY is also set high. If TPOHRDY is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes) for the master STS-12 slice only. The byte on TPOH is ignored when TPOHEN is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH is accepted, it is used as an error mask to modify the corresponding transmit the B3 or H4 path overhead byte, respectively. The accepted error mask is XORed with the corresponding B3 or H4 byte before it is transmitted. TPOHEN should be grounded if it is not used. TPOHEN is sampled on the rising edge of the TOHCLK.

9.5 System Side UTOPIA and POS-PHY Signals (84)

Pin Name	Type	Pin No.	Function
POSL3_UL3B	Input		The **UTOPIA/POS-PHY interface select (**POSL3_UL3B**)** selects between UTOPIA Level 3 and POS-PHY Level 3 modes for the system side interface. When POSL3_UL3B is low, the UTOPIA Level 3 interface is selected. When POSL3_UL3B is high, the POS-PHY Level 3 interface is selected.
RFCLK	Input	E28	The UTOPIA **receive FIFO read clock** (RFCLK) signal is used to read ATM cells from the receive cell FIFO. RFCLK is expected to cycle at 104 MHz.

Pin Name	Type	Pin No.	Function
			The POS-PHY **receive FIFO read clock** (RFCLK) signal is used to read packet data from the receive packet FIFO. RFCLK is expected to cycle at 104 MHz.
RPRTY	Output	P29	The UTOPIA **receive parity** (RPRTY) signal indicates the parity of the RDAT[31:0] bus. Odd or even parity may be selected. RPRTY is valid only when RENB has been sampled low in the previous clock cycle. RPRTY is updated on the rising edge of RFCLK.
			The POS-PHY **receive parity** (RPRTY) signal indicates the parity of the RDAT[31:0] bus. Odd or even parity may be selected. RPRTY is valid only when either RVAL or RSX are asserted. RPRTY is updated on the rising edge of RFCLK.
RDAT[31] RDAT[30] RDAT[29] RDAT[28] RDAT[27] RDAT[26] RDAT[25] RDAT[24] RDAT[23] RDAT[22] RDAT[21] RDAT[20] RDAT[19] RDAT[18] RDAT[17] RDAT[16] RDAT[15] RDAT[14] RDAT[13] RDAT[12]	Output	D30 E29 F28 G27 E30 F29 G28 H27 F30 H28 J27 G30 H29 J28 H30 J29 K28 L27 J30 L28	The UTOPIA **receive cell data** (RDAT[31:0]) bus carries the ATM cell octets that are read from the receive FIFO. RDAT[31:0] is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]		L28 M27 K30 L29 M28 L30 N27 M29 N28 M30 P27 N30 P28	The POS-PHY **receive packet data** (RDAT[31:0]) bus carries the POS packet octets that are read from the receive FIFO. The RDAT[31:0] signals are valid when RVAL and RENB are asserted. RDAT[31:0] is updated on the rising edge of RFCLK.
RENB	Input	U28	The UTOPIA **receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. The system may de-assert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
			The POS-PHY **receive read enable** (RENB) signal is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. A read is not performed and RDAT[31:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[31:0] bus is read from the receive FIFO and RDAT[31:0] changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
RSOC	Output	R28	The UTOPIA **receive start of cell** (RSOC) signal marks the start of a cell structure on the RDAT[31:0] bus. The first word of the cell structure is present on the RDAT[31:0] bus when RSOC is high. RSOC is updated on the rising edge of RFCLK.
RSOP			The POS-PHY **receive start of packet** (RSOP) signal indicates the start of a packet on the RDAT[31:0] bus. RSOP is set high for the first word of a packet on RDAT[31:0]. RSOP is updated on the rising edge of RFCLK

Pin Name	Type	Pin No.	Function
RCA	Output	U30	The UTOPIA **receive cell available** (RCA) signal provides direct status indication when a cell is available in the receive FIFO. RCA is updated on the rising edge of RFCLK.
RVAL	Output	U30	The POS-PHY **receive data valid** (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT[31:0], RPRTY, RSOP, REOP, RMOD[1:0], and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will be high when there is valid data on the RDAT[31:0] bus. RVAL will transition low when the FIFO does not have data to give. RVAL will remain low until a programmable minimum number of bytes or an end-of-packet (EOP) exists in the receive FIFO. The threshold is configurable. RVAL is updated on the rising edge of RFCLK.
RERR	Output	T29	The POS-PHY **receive error** (RERR) signal indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received abort. RERR may only assert when REOP is asserted marking the last word of the packet. RERR is only used in POS-PHY mode and is updated on the rising edge of RFCLK.
REOP	Output	P30	The POS-PHY **receive end of packet** (REOP) signal marks the end of packet on the RDAT[31:0] bus. It is legal for RSOP to be high at the same time REOP is high. REOP is set high to mark the last word of the packet presented on the RDAT[31:0] bus. When REOP is high, RMOD[1:0] specifies if the last word has 1, 2, 3, or 4 valid bytes of data. REOP is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RMOD[1] RMOD[0]	Output	T28 T27	The POS-PHY **receive modulo** (RMOD[1:0]) bus indicates the size of the current word when configured for packet mode. During a packet transfer, every word on RDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by RMOD[1:0]. RMOD[1:0] = “00” RDAT[31:0] valid RMOD[1:0] = “01” RDAT[31:8] valid RMOD[1:0] = “10” RDAT[31:16] valid RMOD[1:0] = “11” RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL is asserted. RMOD[1:0] is only used for POS-PHY operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RSX	Output	R29	The POS-PHY **receive start of transfer** (RSX) signal indicates the start of a packet transfer. When RSX is high, the channel number being transferred is given on RDAT[31:0]. RSX is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
TFCLK	Input	B18	The UTOPIA **transmit FIFO write clock** (TFCLK) signal is used to write ATM cells to the transmit FIFO. TFCLK is expected to cycle at a 104 MHz rate.
			The POS-PHY **transmit FIFO write clock** (TFCLK) signal is used to write packet data into the transmit packet FIFO. TFCLK is expected to cycle at a 104 MHz rate.
TDAT[31] TDAT[30] TDAT[29] TDAT[28] TDAT[27] TDAT[26] TDAT[25] TDAT[24] TDAT[23] TDAT[22] TDAT[21] TDAT[20] TDAT[19] TDAT[18] TDAT[17] TDAT[16] TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	B5 D7 A5 B6 C7 D8 A6 B7 D9 A7 B8 C9 A8 B9 C10 D11 B10 C11 D12 A10 C12 A11 D13 B12 C13 A12 B13 D14 C14 B14 A14 C15	The UTOPIA **transmit cell data** (TDAT[31:0]) bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[31:0] is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK.
			The POS-PHY **transmit packet data** (TDAT[31:0]) bus carries the POS packet octets that are written to the transmit FIFO. The TDAT[31:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[31:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	B15	The UTOPIA **transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
		B15	The POS-PHY **transmit bus parity** (TPRTY) signal indicates the parity on the TDAT[31:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are still inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity may be selected. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
TSOC	Input	D16	The UTOPIA **transmit start of cell** (TSOC) signal marks the start of a cell structure on the TDAT[31:0] bus. The first word of the cell structure is present on the TDAT[31:0] bus when TSOC is high. TSOC must be present for each cell. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP			The POS-PHY **transmit start of packet** (TSOP) signal indicates the start of a packet on the TDAT[31:0] bus. TSOP is required to be present at all instances for proper operation. TSOP must be set high for the first word of a packet on TDAT[31:0]. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.
TENB	Input	A19	The UTOPIA **transmit write enable** (TENB) signal is an active low input which is used to initiate writes to the transmit FIFO. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY and TSOC signals are invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY and TSOC signals is valid and is written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB (continued)	Input	A19	The POS-PHY **transmit write enable** (TENB) signal is an active low input which is used to initiate writes to the transmit FIFOs. When TENB is sampled high, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals is invalid. When TENB is sampled low, the information sampled on the TDAT[31:0], TPRTY, TSOP, TEOP, TMOD[1:0], and TERR signals is valid and is written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
TCA	Output	D17	The UTOPIA **transmit cell available** (TCA) signal provides direct status indication of when cell space is available in the transmit FIFO. When set high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. TCA is set low to indicate either that the transmit FIFO is full. TCA is updated on the rising edge of TFCLK.
DTPA			The POS-PHY **direct transmit packet available** (DTPA) signal provides status indication on the fill status of the transmit FIFO. Note that regardless of what level DTPA is set to indicate "full", the transmit packet processors still have full FIFO capacity to store data. When DTPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When DTPA transitions low, it indicates that the transmit FIFO is either full or near full as configured. DTPA is updated on the rising edge of TFCLK.
TEOP	Input	B16	The POS-PHY **transmit end of packet** (TEOP) signal marks the end of packet on the TDAT[31:0] bus when configured for packet data. The TEOP signal marks the last word of a packet on the TDAT[31:0] bus. The TMOD[1:0] signal indicates how many bytes are in the last word. It is legal to set TSOP high at the same time as TEOP high in order to support 1, 2, 3, or 4 byte packets. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for **POS-PHY** operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TERR	Input	A17	The POS-PHY **transmit error** (TERR) signal is used to indicate that the current packet must be aborted. Packets marked with TERR will have the abort sequence appended when transmitted. TERR should only be asserted during the last word of the packet being transferred on TDAT[31:0]. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is only used for **POS-PHY** operation and is sampled on the rising edge of TFCLK.
TMOD[1:0]	Input	B17 A18	The POS-PHY **transmit word modulo** (TMOD[1:0]) bus indicates the size of the current word when configured for packet mode. During a packet transfer, every word on TDAT[31:0] must contain four valid bytes of packet data except at the end of the packet where the word is composed of 1, 2, 3, or 4 valid bytes. The number of valid bytes in this last word is specified by TMOD[1:0] TMOD[1:0] = "00" TDAT[31:0] valid TMOD[1:0] = "01" TDAT[31:8] valid TMOD[1:0] = "10" TDAT[31:16] valid TMOD[1:0] = "11" TDAT[31:24] valid TMOD[1:0] is considered valid only when TENB is simultaneously asserted. TMOD[1:0] is only used for **POS-PHY** operation and is sampled on the rising edge of TFCLK.

9.6 APS Serial Data Interface (20)

Pin Name	Type	Pin No.	Function
APSIFPCLK	Input	P3	The **APS input frame pulse clock** (APSIFPCLK) provides a jitter-free reference clock used to sample the APS input frame pulse (APSIFP). The 777.76 MHz Clock Synthesis Unit of the APS Port also uses this clock as its reference. APSIFPCLK is expected to cycle at a 77.76 MHz rate, and must be synchronous with respect to REFCLK_P / REFCLK_N to ensure that APSIFPCLK is an exact divide-by-two in frequency, compared to REFCLK_P / REFCLK_N.

Pin Name	Type	Pin No.	Function
APSI_P[4] APSI_N[4] APSI_P[3] APSI_N[3] APSI_P[2] APSI_N[2] APSI_P[1] APSI_N[1]	Analog LVDS Input	Y4 Y3 Y2 Y1 AA3 AA2 AB4 AB3	The differential **APSI** input (APSI_P/ APSI_N[4:1]) serial data links carry SONET/SDH OC-48 frame data from a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. Data on APSI_P/ APSI_N[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and bit 'j' is transmitted last. When in working mode, set using the APSMUX_RCFP, APSMUX_T8TE and APSMUX_TRMP register bits in the S/UNI-2488 Master Reset, Configuration and Loopback register, the APSI_P/ APSI_N[4:1] signals carry the receive data from the protect mate. When in protect mode, the APSI_P/ APSI_N[4:1] signals carry the transmit data from the working mate. The four differential pairs in APSI_P/ APSI_N[4:1] are frequency locked but not phase locked. APSI_P/ APSI_N[4:1] are nominally 777.6 Mbps data streams. If the Input APS Port is not used, the APSI_P/ APSI_N[4:1] must be tied to ground or left floating. If left floating, the RXLV and DRU must be disabled via the R8TD APS1-4 Analog Control registers.
APSIFP	Input	P2	The **APS input frame pulse** signal (APSIFP) provides system timing of the APS input serial interface. APSIFP is set high once every 9720 APSIFPCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (APSI_P/ APSI_N[4:1]). APSIFP is sampled on the rising edge of APSIFPCLK.
APSO_P[4] APSO_N[4] APSO_P[3] APSO_N[3] APSO_P[2] APSO_N[2] APSO_P[1] APSO_N[1]	Analog LVDS Output	U1 U2 V3 V4 V1 V2 W2 W3	The differential **APS output** (APSO_P/ APSO_N[4:1]) serial data links carry SONET/SDH OC-48 frame data to a mate in bit serial format. Each differential pair carries a constituent OC-12 of the data stream. Data on APSO_P/ APSO_N[4:1] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is received first and bit 'j' is received last. When in working mode, as set using the APSMUX_RCFP, APSMUX_T8TE and APSMUX_TRMP register bits of the S/UNI-2488 Master Reset, Configuration and Loopback register, the APSO_P/ APSO_N[4:1] signals carry the transmit data to the protect mate. When in protect mode, the APSO_P/ APSO_N[4:1] signals carry the receive data to the working mate. The four differential pairs in APSO_P/ APSO_N[4:1] are frequency locked but not phase locked. APSO_P/ APSO_N[4:1] are nominally 777.6 Mbps data streams.

Pin Name	Type	Pin No.	Function
APSOFP	Output	P1	The **APS output frame pulse** signal (APSOFP) provides system timing of the APS output serial interface. APSOFP is set high once every 9720 APSIFPCLK cycles, or multiple thereof, to indicate the approximate location of the J0 frame boundary 8B/10B character on the differential LVDS bus (APSO_P/ APSO_N[4:1]). This signal must not be used as a source for APSIFP. APSOFP is updated on the rising edge of APSIFPCLK.

9.7 Microprocessor Interface Signals (37)

Pin Name	Type	Pin No.	Function
CSB	Input	F4	The active low **chip select** (CSB) signal is low during S/UNI-2488 register accesses. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	D2	The active low **read enable** (RDB) signal is low during S/UNI-2488 register read accesses. The S/UNI-2488 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	C1	The active low **write strobe** (WRB) signal is low during S/UNI-2488 register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	N1P4N 2M1M2 N4L1M 3L2K1 M4K2J 1K3J2 H1	The bi-directional **data bus**, D[15:0], is used during S/UNI-2488 read and write accesses.
A[13]/TRS	Input	K4	The **test register select** signal (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS may be tied low.

Pin Name	Type	Pin No.	Function
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	J3H2J4 H3G2F 1H4G3 F2E1G 4E2D1	The **address** bus (A[12:0]) selects specific registers during S/UNI-2488 register accesses.
RSTB	Schmidt TTL Input	E4	The active low **reset** (RSTB) signal provides an asynchronous S/UNI-2488 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input	E3	The **address latch enable** (ALE) is an active-high signal and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. ALE allows the S/UNI-2488 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	D3	The active low **interrupt** (INTB) signal is set low when a S/UNI-2488 enabled interrupt source is active. The S/UNI-2488 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.8 JTAG Test Access Port (TAP) Signals (5)

Pin Name	Type	Pin No.	Function
TCK	Input	C30	The **test clock** (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	E27	The **test mode select** (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	F27	When the S/UNI-2488 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the S/UNI-2488 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	D18	The **test data output** (TDO) signal carries test data out of the S/UNI-2488 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when scanning of data is in progress.

Pin Name	Type	Pin No.	Function
TRSTB	Schmidt TTL Input	D28	The active low **test reset** (TRSTB) signal provides an asynchronous S/UNI-2488 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. TRSTB must be asserted at some point after power up and before the device registers are accessed.

9.9 Analog Miscellaneous Signals (10)

Pin Name	Type	Pin No.	Function
ATP_2488[0] ATP_2488[1] ATP_1250[0] ATP_1250[1]	Analog	AJ18 AK18 AG2 AF3	Four **analog test ports** are provided for production testing only. These pins must be tied to analog ground (AVS) during normal operation. ATP_2488[1:0] are the test ports for the 2488 Mbps analog circuitry. ATP_1250[1:0] are the test ports for the 777.76 MHz LVDS analog circuitry.
C0_CRU C1_CRU	Analog	AG18A H18	The analog C0_CRU and C1_CRU pins are reserved for an external capacitor for the clock recovery unit. A 10nF non-polarized capacitor across the two pins is required for all applications. The C0_CRU and C1_CRU pins must not be left floating (no connection).
C0_CSU C1_CSU	Analog	AJ20 AK20	The analog **C0_CSU** and **C1_CSU** pins are provided for an external capacitor for the clock synthesis unit. A 100nF capacitor must be placed between these two pins for all applications. The C0_CSU and C1_CSU pins must not be left floating (no connection).
RES RESK	Analog	AE4 AG1	**Reference Resistor Connection.** (RES/RESK) An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK for the APS port LVDS reference. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252µA of current to flow through the resistor. RESK is electrically connected to AVSS within the block, but should not be connected to AVSS, either on-chip or off-chip.

9.10 Analog Power and Ground (105)

Pin Name	Pin Type	PIN No.	Function
AVDH (25)	Analog Power	AH17 AH14 AH10 AH9 AG9 AJ9 AJ10 AJ14 AJ17 AJ19 AK19 AB1 AG10 AH19 AG19 AG17 AG14 AG3 AH2 AJ1 U3 U4 W4 AC4 AF4	The **analog power** (AVDH) pins for the analog core. The AVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDL(16)	Analog Power	AG5 AG6 AH5 AH6 AJ5 AJ6 AK5 AK6 AG21 AH21 AJ21 AK21 AA4 AD3 AD4 AF2	The **analog power** (AVDL) pins for the analog core. The AVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
QAVD	Analog Power	AG20 AH20 AG8 AH8	The **quiet power** (QAVD) pins for the analog core. QAVD should be connected to a well-decoupled analog +3.3V supply. These power pins should be decoupled separately from the analog power pins (AVDH).

9.11 Digital Power and Ground

Pin Name	Pin Type	PIN No.	Function
VDDI	Core Power	D29 G29 K29 N29 U29 W30 AA28 AG7 AH7 AJ7 AK7 AH26 AG24 T2 R4 N3 L3 G1 F3 C6 C8 A9 B11 A13 C16 C17 C18 A21 D21	The core power (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.

Pin Name	Pin Type	PIN No.	Function
VDDO	I/O power	B29 C28 D27 D10 D15 D20 L4 T4 B2 C3 D4 AG27 AH28 AJ29 K27 R27 Y27	**I/O power (VDDO).** The VDDO pins should be connected to a well-decoupled +3.3 V power supply.

9.11.1 Digital Ground

Pin Name	Pin Type	PIN No.				Function
VSS (124)	Digital Ground	A1 B1 C2 R1 T1 W1 AA1 AC1 AC2 AC3 AD1 AD2 AE1 AH1 AK1 AJ2 AK2 AK14 AG15 AH15 AJ15 AG16 AH16 AJ16 AK17 AK22	A15 B3 A2 AH3 AJ3 AK3 AG4 AH4 AJ4 AK4 AJ8 AK8 AG11 AH11 AJ11 AK11 AG12 AH12 AJ12 AG13 AH13 AJ13 AK30 AJ30 AH29 T30	A3 A4 B4 C4 C5 D5 D6 A20 A22 A23 A24 A25 A26 A27 A28 B20 B21 B22 B24 B25 B26 B27 C19 C20 C21 C23	D23 D25 D26 W27 W28 Y28 Y29 Y30 AA27 AA29 AA30 AB27 AB28 AB30 AC27 AC28 AC29 AD27 AD28 AD29 AD30 AE27 AE28 AE30 AF27 AF28	The **ground** (VSS) pins should be connected to a low inductance ground plane connected to both the digital and analog power supplies. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.				Function
		AK23 AJ28 AK29 B28 A16	R30 C29 B30 A30 A29	C24 C25 C26 D19 D22	AF29 AF30 AG29 AG30 AH30	

9.11.2 No Connects

N/C (17)	No Connect	C27 D24 B23 C22 AB29 AC30 AE29 AG28 AH22 AJ22 R2 R3 T3 AB2 AE2 AE3 AF1	No connect

9.12 Pad Summary

Interface	Inputs	Outputs	Bidir	Analog	Total
Serial Line Side Interface				7	7
Clocks and Alarms		7			7
Receive Section/Line/Path Overhead Insertion		6			6
Transmit Section/Line/Path Overhead Insertion	4	3			7
System Side Utopia and POS	42	41			83
APS port	3			16	19
Microprocassor	20	1	16		37
JTAG Test Access Port	4	1			5
Analog misc				10	10
Analog power/gnd				75	75
Totals	73	59	16	108	256

Notes on Pin Description:

All S/UNI-2488 inputs and bidirectionals present minimum capacitive loading and operate at CMOS/LVTTL logic levels except the REFCLK_P / REFCLK_N, RXD_P/ RXD_N, TXD_P/ TXD_N pins which operate at pseudo-ECL (PECL) logic levels and the APSI_P/ APSI_N[4:1], APSO_P/ APSO_N[4:1] pins which operate at LVDS logic levels.

The S/UNI-2488 digital outputs and bidirectionals which have 8 mA drive capability are: TDO, INTB, D[15:0], TPOHRDY, TOHFP, TOHCLK, B3E, RPOHEN, RPOH, RTOH, ROHFP, ROHCLK, RALM, SALM, and OOF

The S/UNI-2488 digital outputs and bidirectionals which have 12 mA drive capability are: APSOFP, TCA/DTPA, RSX, RMOD[1:0], REOP, RERR, RCA/RVAL, RSOC/RSOP, RDAT[31:0], RPRTY, TCLK, PGMTCLK, RCLK, and PGMRCLK.

The S/UNI-2488 digital outputs and bidirectionals which have 16 mA drive capability are: CRUCLKO and CSUCLKO

The S/UNI-2488 digital inputs are 3.3V tolerant. The SD digital input is 5V (TTL) tolerant.

Inputs ALE, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.

It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.

It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.

All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operation section.

On power-up, all 3.3V power supplies (QAVD, AVDH, VDDO) must be on before the 1.8V supplies (AVDL and VDDI).

On power-down, all 1.8V power supplies (AVDL and VDDI) must be off before the 3.3V supplies (QAVD, AVDH, VDDO).

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing listed in point numbers 9 and 10.

Follow recommendations in Section 16.3 for analog power supply filtering.

Do not exceed 100 mA of current on any pin during the power-up or power-down sequence.

Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10 Functional Description

10.1 Receive Line Interface

The Receive Line Interface allows direct interface of the S/UNI-2488 to optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery on the incoming 2488.32 Mbit/s data stream and SONET A1/A2 pattern framing.

The clock recovery unit recovers the clock from the incoming bit serial data stream and is compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep-alive purposes. The clock recovery unit utilizes a 155.52 MHz reference clock. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

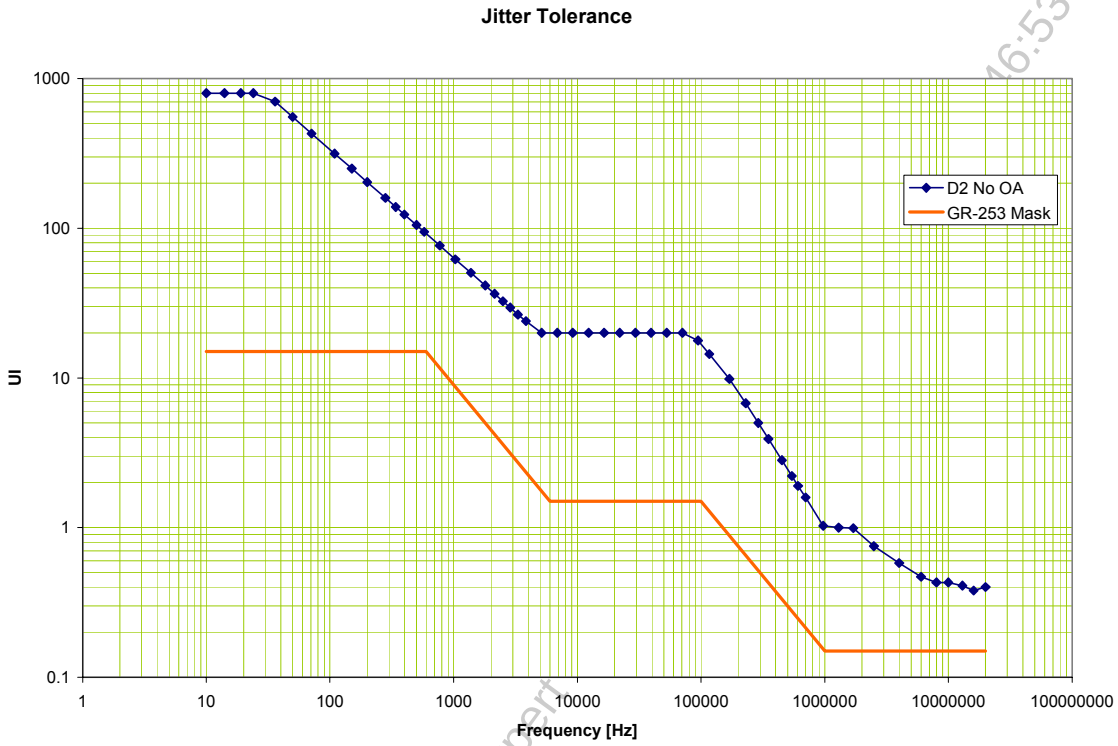
Initially upon start-up, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is close enough to that of the reference clock (approx. +/-488 ppm), the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 128 bit[1] bit periods or if the recovered clock drifts beyond 1000 ppm of the reference clock. In order to avoid bit error due to lack of edges, a transition density of approximately 50% over 1 second is required. This is generally assured when using SONET scrambling.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of signal condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within ±4.6 ppm. When not loop timed, the REFCLK accuracy may be relaxed to ±20 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET equipment by GR-253-CORE. Please refer to the figure below.

[1] This number is programmable through LOS_COUNT[4:0] in Register 0013H.

Figure 8 Typical STS-48c (STM-16c) Jitter Tolerance



An unframed PRBS pattern can optionally be monitored on the receive line. The PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) and is implemented by a Linear Feedback Shift Register (LFSR).

10.2 SONET/SDH Receive Line Interface (SRLI)

The SONET/SDH receive line interface block performs byte and frame alignment on the incoming 2488 Mbit/s data stream based on the SONET/SDH A1/A2 framing pattern.

While out of frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the RRMP framer block when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out of frame.

10.3 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and processes the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when the 12 A1 and the 12 A2 bytes are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16-16c) stream. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when only the first A1 byte and the first four bits of the last A2 byte are seen error-free in the first STS-12 (STM-4) of the STS-48c (STM-16c) . Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment algorithm used in the SRLI which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame) there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP errors can be accumulated.

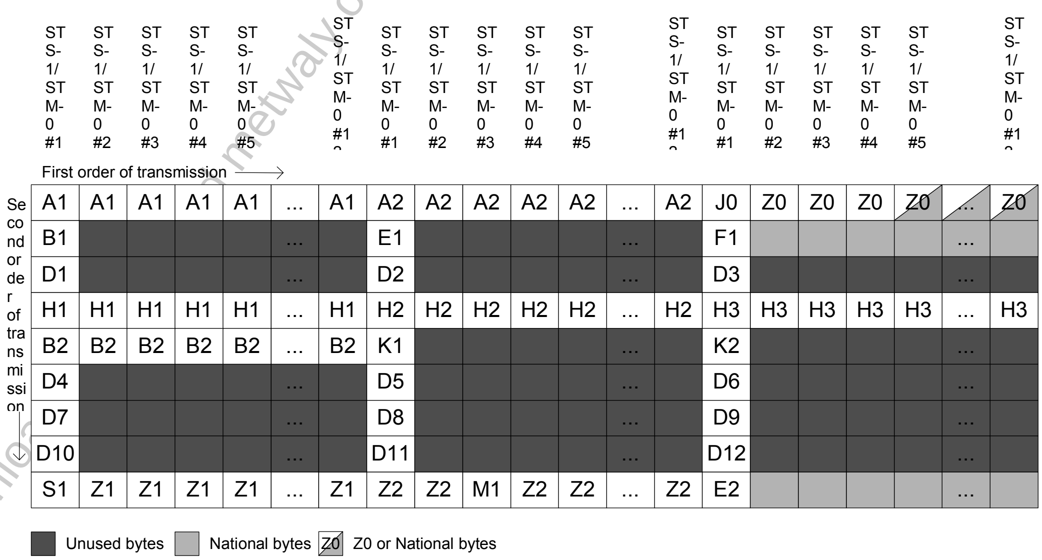
The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH output. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). RTOHCLK is the generated output clock used to provide timing for the RTOH output. RTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RTOHFP high with the rising edge of RTOHCLK identifies the MSB of the first A1 byte.

Figure 9 STS-48c (STM-16-16c) on RTOH



A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

10.4 Receive Tail Trace Processor (RTTP)

The Receive Tail Trace Processor (RTTP) block monitors the tail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect.

The synchronization mechanism is different for a 16 byte message and for a 64 byte message. When the message is 16 bytes, the synchronization is based on the MSB of the tail trace byte. Only one of the 16 bytes has MSB set high. The byte with MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = ODh, LF = OAh) characters of the tail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

Three tail trace algorithms are defined.

The first algorithm is BELLCORE compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected tail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the tail trace message is all zeros. TIM is always 0. Note that TIM is not used in BELLCORE compliance.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. The current tail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes to the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP should be set to synchronize to the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent tail trace message is declared when an identical message is received for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match tail trace message when the accepted message is all zeros.

The third algorithm is not BELLCORE/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous tail trace byte. Only TIU is used in the third algorithm. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames.

A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM). TIM is always 0.

10.5 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

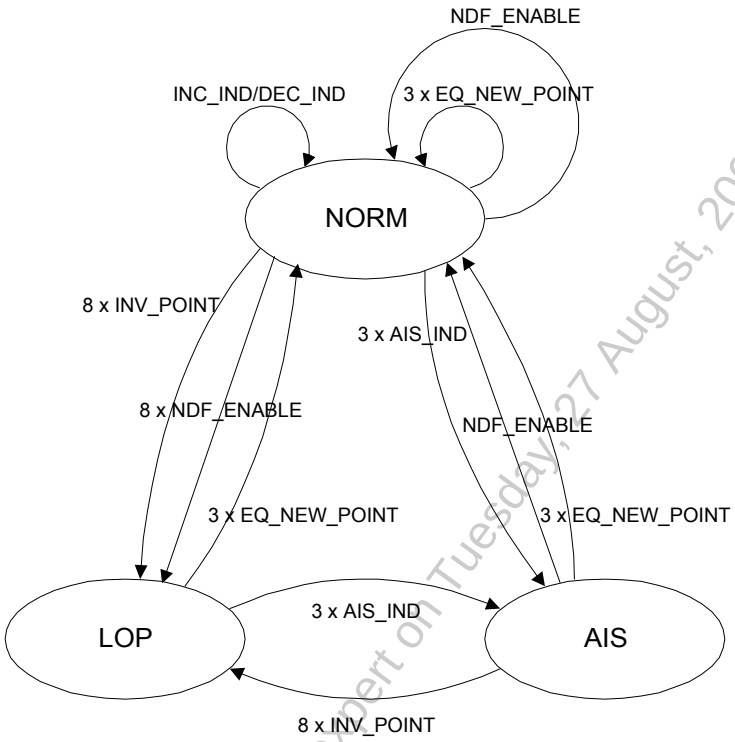
10.5.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and the synchronous payload envelop bytes (SPE) of the constituent STS-48c (VC-16-16c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process the STS-48c (AU-16-16c) pointer. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 10 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

DEC_IND: disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

INV_POINT: not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Note 1: active offset is defined as the accepted current phase of the PE (VC) in the NORM_state and is undefined in the other states.

Note 2: enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

Note 3: disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.

Note 4: the remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.

Note 5: ss bits are unspecified in SONET and have bit pattern 10 in SDH.

Note 6: the use of ss bits in definition of indications may be optionally disabled.

Note 7: the requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.

Note 8: NEW_POINT is also an INV_POINT.

Note 9: the requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.

Note 10: LOP is not declared if all the following conditions exist:
- the received pointer is out of range (>782),
- the received pointer is static,
- the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
- When the received pointer returns to an in-range value, the S/UNI-2488 will interpret it correctly.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE: single NDF_ENABLE indication

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

8 x NDF_ENABLE	eight consecutive NDF_ENABLE indications
Note 1:	the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
Note 2:	3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.
Note 3:	all three offset values received in 3 x Q_NEW_POINT must be identical.
Note 4:	"consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications

PAIS is declared on entry to the AIS_state after three consecutive AIS indications

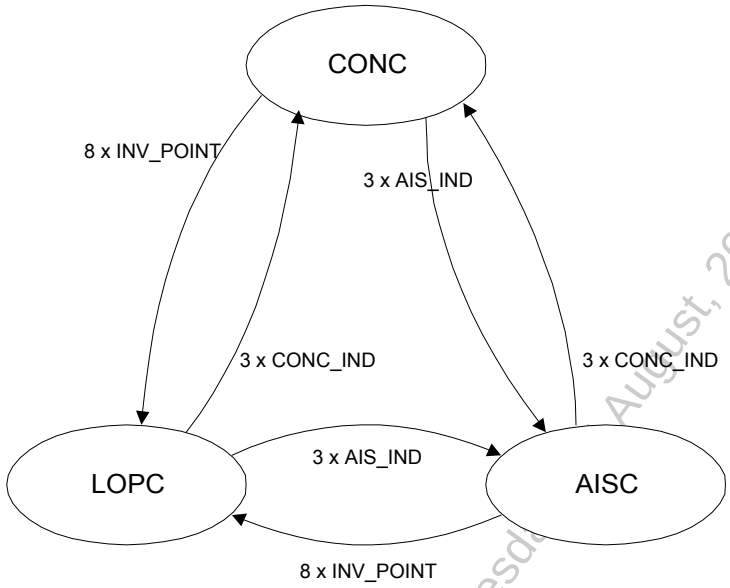
10.5.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. Within the pointer interpretation algorithm three states are defined as shown below.

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 11 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

CONC_IND: enabled NDF + dd + "1111111111"

AIS_IND: H1 = FFh + H2 = FFh

INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Note 1: enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

Note 2: the remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.

Note 3: dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: three consecutive CONC indications

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

Note 1: "consecutive event counters" are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications

PAISC is declared on entry to the AISC_state after three consecutive AIS indications

10.5.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the SONET (SDH) payloads. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of the STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously accepted PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 1. PLM-P is removed when the accepted PSL match the expected PSL according to Table 1. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. The PDI-P defect is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 2 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 1 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Mismatch	Inactive	Defect
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Unequipped	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Defect
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Unequipped	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	$=_{exp}$PSL	Match	Inactive	Inactive
				$!=_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Defect
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive

Table 2 Expected PDI Defect Based on PDI and PDI Range Values

PDI Register Value	PDI Range Register Value	Exp PDI	PDI Register Value	PDI Range Register Value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3

PDI Register Value	PDI Range Register Value	Exp PDI	PDI Register Value	PDI Range Register Value	Exp PDI
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RPOHFP high with the rising edge of RPOHCLK identifies the MSB of the first J1 byte.

10.6 SONET/SDH Virtual Container Aligner (SVCA)

The SONET (SDH) Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET (SDH) data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

10.6.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

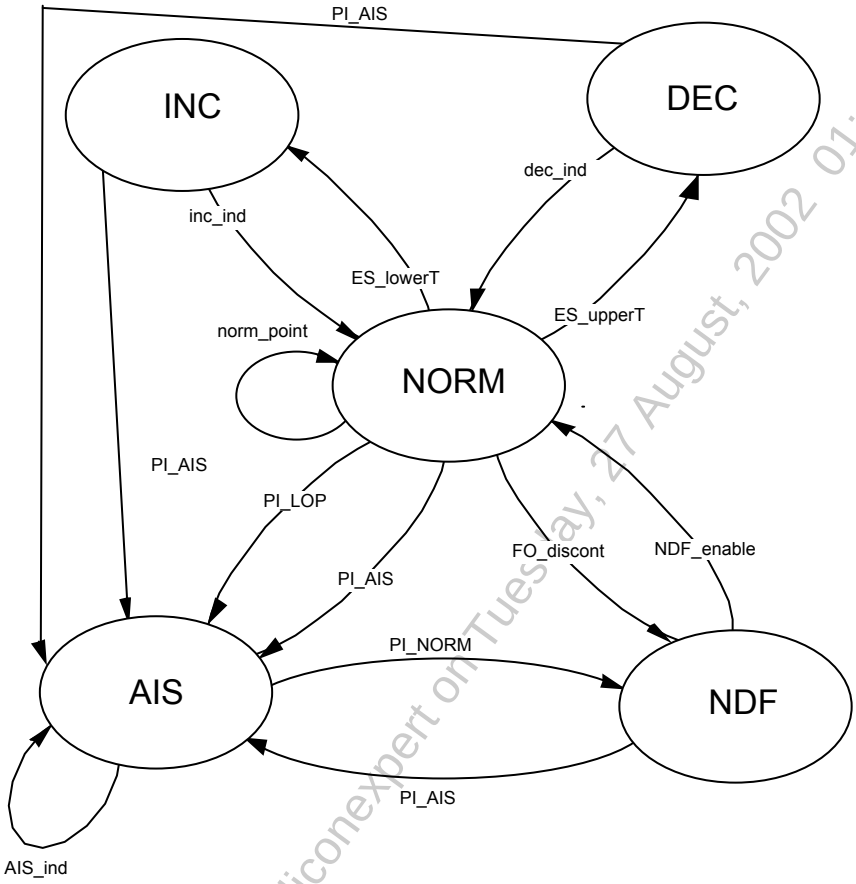
10.6.2 Pointer Generator

The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelope bytes (SPE) of the STS-48c (VC16-16c) payloads. Within the pointer generator algorithm, five states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- NDF_state (NDF)
- INC_state (INC)
- DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store block. The transition to/from the AIS state are controlled by the pointer interpreter in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 12 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT:	ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.
ES_upperT:	ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.
FO_discont:	frame offset discontinuity
PI_AIS:	PI in AIS state
PI_LOP:	PI in LOP state
PI_NORM:	PI in NORM state
Note 1:	A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind:	transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.
dec_ind:	transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.
NDF_enable:	accept new offset as active offset, transmit the pointer with NDF enabled and new offset.
norm_point:	transmit the pointer with NDF disabled and active offset.
AIS_ind:	active offset is undefined, transmit an all-1's pointer and payload.
Note 1:	active offset is defined as the phase of the SPE (VC).
Note 2:	the ss bits are undefined in SONET, and has bit pattern 10 in SDH
Note 3:	enabled NDF is defined as the bit pattern 1001.
Note 4:	disabled NDF is defined as the bit pattern 0110.

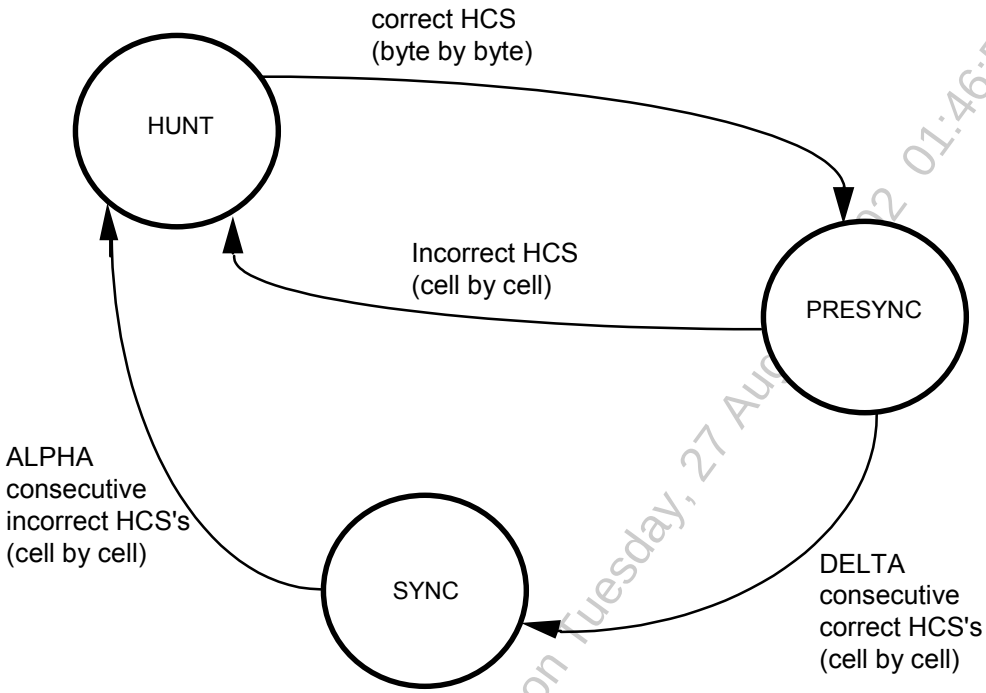
10.7 Receive Cell and Frame Processor (RCFP)

The Receive Cell and Frame Processor (RCFP) performs both ATM and PPP processing. It has the capability to process a single STS-48c (STM-16c) channel.

10.7.1 ATM Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in below.

Figure 13 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 2 µs for the STS-48c (STM-16c) rate.

10.7.2 ATM Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

10.7.3 ATM Cell Filter

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RCFP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if HCS errors are detected, or if the header contents match the pattern contained in the RCFP Idle Cell Header and Mask register. Idle cell filtering is accomplished by writing the appropriate cell header pattern into the RCFP Idle Cell Header and Mask Pattern register. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RCFP Idle Cell Header and Mask register allows filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RCFP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result.

10.7.4 ATM Performance Monitor

The Performance Monitor consists of an 8-bit saturating HCS error counter and a 32-bit saturating receive cell counter. A 32-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

10.7.5 POS Overhead Removal

The overhead removal consists of stripping SONET/SDH overhead bytes from the data stream. Once overhead bytes are removed, the data stream consists of PPP/HDLC frame octets that can be fed directly to the descrambler or the PPP/HDLC Frame Delineation block.

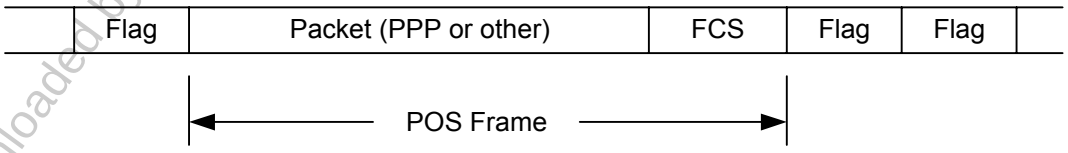
10.7.6 POS Descrambler

When enabled, the self-synchronous descrambler operates on the PPP Frame data, descrambling the data with the polynomial $x^{43}+1$. Descrambling is performed on the raw data stream, before any PPP frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.7.7 POS PPP/HDLC Frame Delineation

The PPP/HDLC Frame Delineation is performed on the descrambled data and consists of arranging the framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag and Idle Sequences and passes the data onto the Byte Destuffing block. The PPP/HDLC Frame format is shown in the figure below.

Figure 14 PPP/HDLC Over SONET Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of PPP/HDLC data resumes when a Start of Packet is encountered and the FIFO level is below a programmable Reception Initialization Level.

10.7.8 POS Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in the table below are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XOR'ed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-2488.

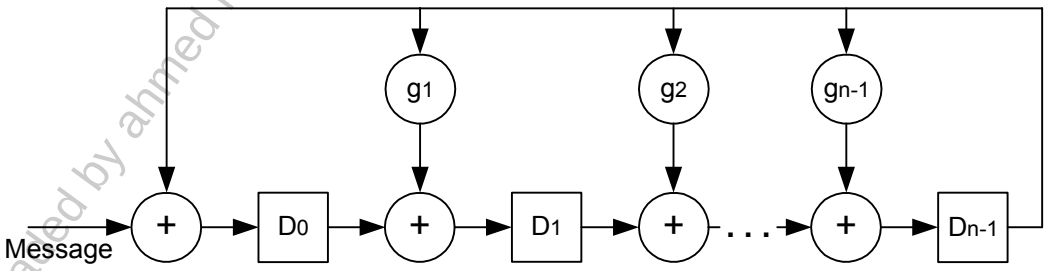
Table 3 Byte Destuffing

Original	Escaped
7E (Flag Sequence)	7D-5E
7D (Control Escape)	7D-5D
Aborted Packet	7D-7E

10.7.9 POS FCS Check

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. . Packets with FCS errors are marked as such and should be discarded by the system.

Figure 15 CRC Decoder



10.7.10 POS Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters, one 32-bit saturating received good packet counter, and one 40-bit counter for accumulating packet bytes. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 32-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RCFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets, that is packets that do not at least contain four bytes, are discarded and will be counted as a minimum packet size violation. When the packet size exceeds MAXPL[16:0], the packet is marked with an error and the bytes beyond the maximum count are discarded.

10.8 Receive Scalable Data Queue (RXSDQ)

The RXSDQ provides a FIFO to separate the line-side timing from the higher layer ATM/POS link layer timing. The RXSDQ has two modes of operations, ATM and POS.

10.8.1 Receive ATM FIFO

The RXSDQ is responsible for holding up to 48 cells until they are read by the Receive System Interface.

Receive FIFO management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO discards the current cell and discards the incoming cells until there is room in the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error.

10.8.2 Receive POS FIFO

The RXSDQ contains 192 sixteen-byte blocks for FIFO storage, along with management circuitry for reading and writing the FIFO. Note that packets always begin at the beginning of a block and will not use up left-over space in a block used by a previous packet. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and discards the current incoming bytes until there is room in the FIFO. Once enough room is available, as defined by the BT[7:0] register bit settings, the RXSDQ will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error. A FIFO underrun is caused when the System Interface tries to read more data words while the FIFO is empty. This action will be detected and reported through the FUDRI interrupt, but it is not considered a system error. The system will continue to operate normally. In that situation, RVAL can be used by the Link Layer device to find out if valid or invalid data is provided on the System Interface.

10.9 Receive Phy Interface (RXPHY)

The S/UNI-2488 receive system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit Receive UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-2488. When configured for POS applications, the system interface provides either a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI-2488. The link layer device can implement various protocols, including PPP and HDLC.

10.9.1 Receive UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA signal indicates when a cell is available for transfer on the receive data bus RDAT[31:0]. The RPRTY signal reports the parity on the RDAT[31:0] bus (selectable as odd or even parity). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA is deasserted will output invalid data.

10.9.2 Receive POS-PHY Level 3

The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the receive FIFO (using the rising edge of the RFCLK). The start of packet RSOP marks the first byte of receive packet data on the RDAT[31:0]. The RPRTY signal determine the parity on the RDAT[31:0] bus (selectable as odd or even parity). The end of a packet is indicated by the REOP signal. Signal RERR is provided to indicate that an error in the received packet has occurred (the error may have several causes include an abort sequence or an FCS error). The RVAL signal is used to indicate when RSOP, REOP, RERR and RDAT[31:0] are valid. Read accesses while RVAL is logic 0 are ignored and will output invalid data. RSX indicates the start of a transfer and marks the clock cycle where the in-band channel address is given on the RDAT bus. The RXPHY performs the polling procedure to select which PHY address is serviced.

10.10 Transmit Line Interface

The Transmit Line Interface allows the S/UNI-2488 to directly interface with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion of the incoming outgoing 2488.32 Mbit/s data stream.

The transmit clock is synthesized from a 155.52. MHz reference. The transfer function yields a typical low pass corner of 20 MHz above which reference jitter is attenuated at –12 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter-free 155.52MHz reference, the intrinsic jitter is less than 0.01 UI RMS when measured using a band-pass filter with 12KHz – 20MHz cutoff corner frequencies. In practice, jitter on REFCLK_P / REFCLK_N must be less than 1 psec RMS in 12KHz – 20MHz band in order for S/UNI2488 to comply with GR-253-CORE intrinsic jitter specification. The REFCLK reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

When configured in loop-timed mode, the S/UNI-2488 meets the jitter transfer requirements. The results of jitter transfer tests are shown in Figure 16 and Figure 17.

Figure 16 Jitter transfer results

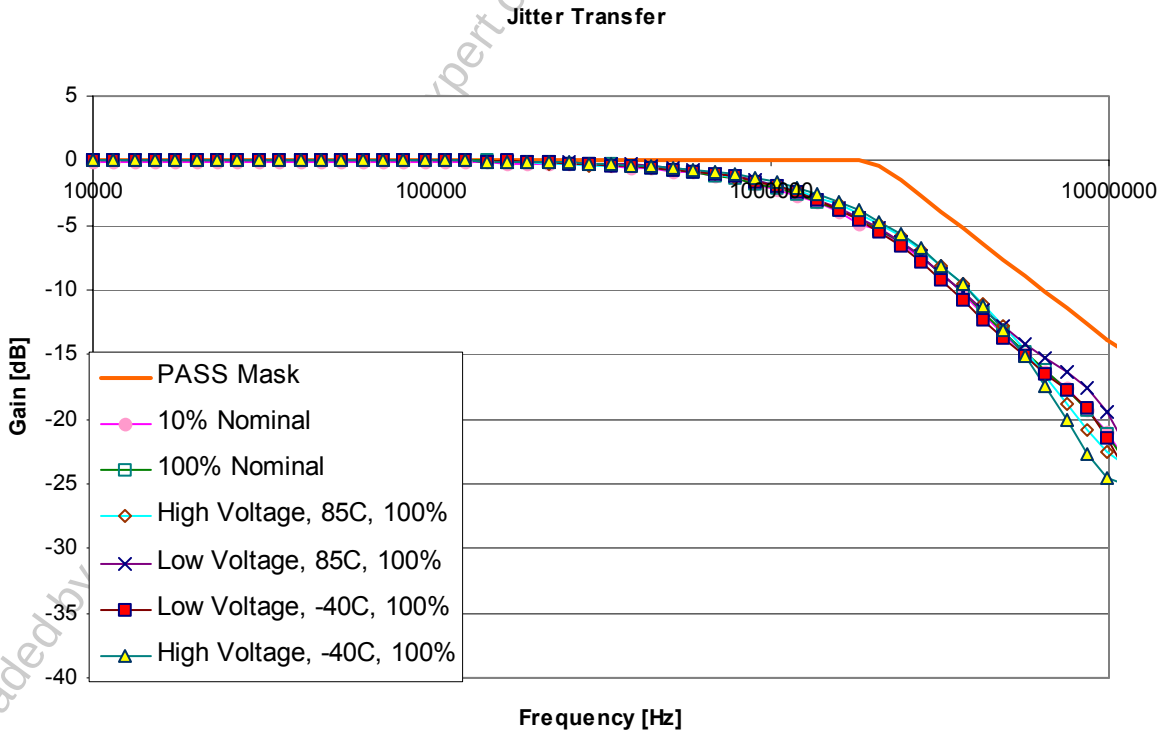
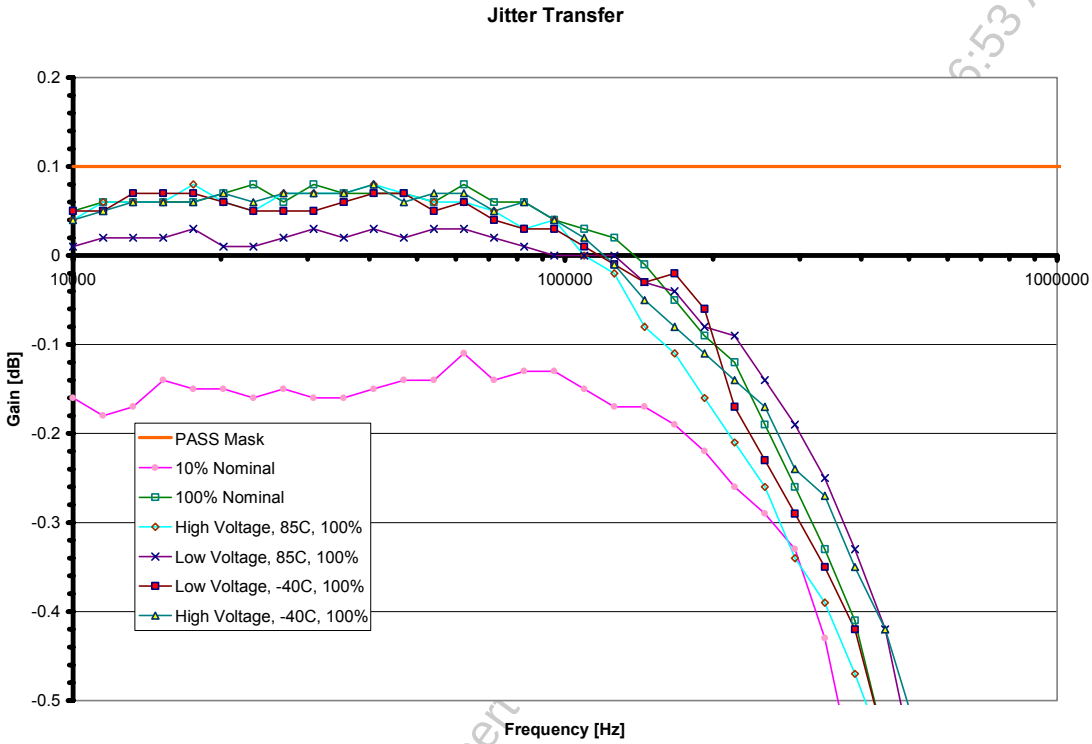


Figure 17 Jitter transfer for the low frequency region



The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD_P/ TXD_N PECL outputs.

An unframed PRBS pattern can optionally be inserted on the transmit line. The PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) and is implemented by a Linear Feedback Shift Register (LFSR).

10.11 SONET/SDH Transmit Line Interface (STLI)

The SONET/SDH transmit line interface block properly formats the outgoing 2488 Mbit/s data stream. This block interfaces the TRMP to the Tx Line Interface block.

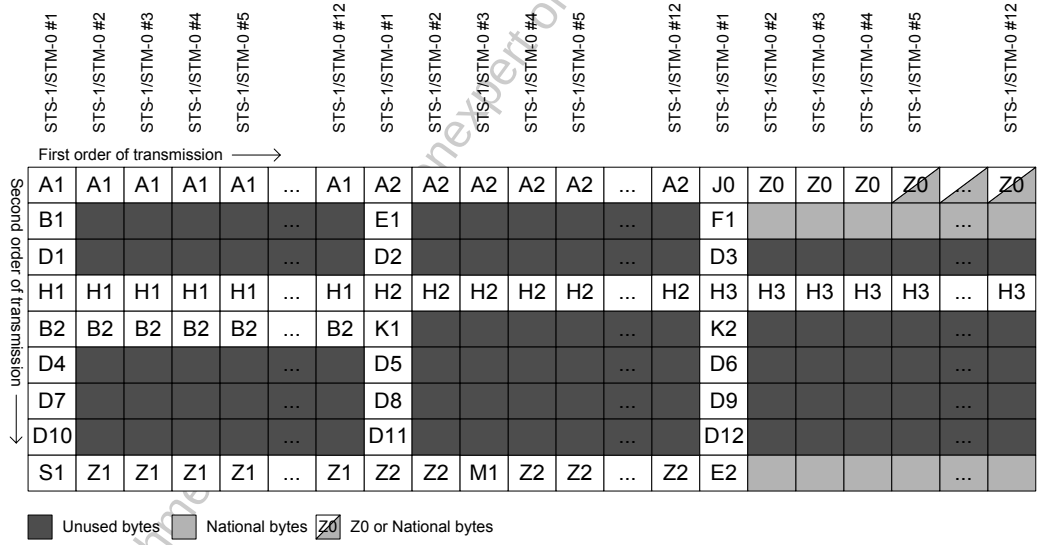
10.12 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two line BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-L and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated. For STS-48c (STM-16c), the maximum single BIP-8 error count is 0xFF while the maximum block BIP-24 error count is 0x10.

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Figure 18 STS-48c (STM-16-16c) On TTOH



Note, only the overhead from the first STS-12 (STM-4) of the STS-48c (STM-16c) can be sourced. Overhead from the other three STS-12s (STM-4s) are internally generated assigned or are assigned default values as described below.

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 4 before being inserted into the data stream.

Table 4 TOH Insertion Priority

Byte	Highest Priority						Lowest Priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1	B1 pass through (B1DISABLE=1)			Calculated B1 XOR TTOH (TTOHEN=1 & B1MASKEN=1)			Calculated B1 XOR B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)			
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	all 1's or all 0's (TSLDEN=1)		D1-D3 pass through
H1				H1 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1)			H1 pass through XOR H1MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H2				H2 pass through XOR TTOH (TTOHEN=1 & HMASKEN=1)			H2 pass through XOR H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H3				TTOH (TTOHEN=1)			H3 pass through
B2	B2 pass through (B2DISABLE=1)			Calculated B2 XOR TTOH (TTOHEN=1 & B2MASKEN=1)			Calculated B2 XOR B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)			
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	all 1's or 0's (TSLDEN=1)	all 1's or 0's (TLDEN=1)	D4-D12 pass through

Byte	Highest Priority						Lowest Priority
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)			Z1 pass through
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)			Z2 pass through
M1		Force to 0x0. (TLREIINS=0)	LREI[7:0] from RRMP (LREIEN=1)	TTOH (TTOHEN=1)			M1 pass through
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)			E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)			National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)			Unused pass through
PLD							PLD pass through

The Z0 bytes are defined according to BELLCORE as shown in Table 5. Z0DEF must be set to logic 0.

Table 5 Z0 Bytes Definition for Row #1

TRMP Mode	Type	Z0DEF = 0
STS-48c (STM-16) slave mode	Z0	From STS-1/STM-0 #1 to #12
	National	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK, B1MASK and B2MASK register bits of the TRMP Error Insertion register. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XOR with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling. The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.13 Transmit Tail Trace Processor (TTTP)

The Transmit Tail Trace Processor (TTTP) block generates the tail trace messages to be transmitted. The TTTP can generate a 16 or 64-byte tail trace message. The message is source from an internal RAM and must have been previously written by an external microprocessor. Optionally, the tail trace message can be reduced to a single continuous tail trace byte.

The tail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16-byte message and for a 64 byte message. When the message is 16 bytes, the synchronization is based on the MSB of the tail trace byte. Only one of the 16 bytes has its MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of tail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

10.14 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one or two path BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3 and N1). TOHCLK is the generated output clock used to provide timing for the TPOH port. TOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TPOHRDY high with the rising edge of TOHCLK identifies the MSB of the first J1 byte. TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

Since there are multiple sources for the same overhead byte, the POH bytes must be prioritized according to Table 6 before being inserted into the data stream.

Table 6 Path Overhead Byte Source Priority

Byte	Highest Priority					Lowest Priority
J1	J1 pass through (PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		TPOH (TPOHEN=1)	J1 pass through
B3	B3 pass through (PAIS=1)			Calculated B3 XOR TPOH (TPOHEN=1 AND B3MASKEN=1)	TPOH (TPOHEN=1)	Calculated B3 XOR B3MASK
C2	C2 pass through (PAIS=1)	C2 ind. reg. (SRCC2=1)			TPOH (TPOHEN=1)	C2 pass through
G1	G1 pass through (PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC=1)	G1 ind. reg. (SRCG1=1)		TPOH (TPOHEN=1)	G1 pass through
F2	F2 pass through (PAIS=1)	F2 ind. reg. (SRCF2=1)			TPOH (TPOHEN=1)	F2 pass through
H4	H4 pass through (PAIS=1)	H4 pass through XOR H4 ind. reg. (SRCH4=1 AND ENH4MASK=1)	H4 ind. reg. (SRCH4=1)	H4 pass through XOR TPOH (TPOHEN=1 AND H4MASK=1)	TPOH (TPOHEN=1)	H4 pass through
Z3	Z3 pass through (PAIS=1)	Z3 ind. reg. (SRCZ3=1)			TPOH (TPOHEN=1)	Z3 pass through
Z4	Z4 pass through (PAIS=1)	Z4 ind. reg. (SRCZ4=1)			TPOH (TPOHEN=1)	Z4 pass through
Z5	Z5 pass through (PAIS=1)	Z5 ind. reg. (SRCZ5=1)			TPOH (TPOHEN=1)	Z5 pass through

10.15 Transmit Cell and Frame Processor (TCFP)

The Transmit Cell and Frame Processor (TCFP) performs both ATM and PPP processing. It has the capability to process a single STS-48c (STM-16c) channel. In ATM mode, the TCFP performs provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. In POS mode, the TCFP provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions.

10.15.1 ATM Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

10.15.2 ATM Scrambler

The Scrambler scrambles the 48-octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler (x^{43} + 1 polynomial) described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

10.15.3 ATM HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.15.4 POS PPP/HDLC Frame Generator

The PPP/HDLC Frame Generator runs off of the SONET sequencer to create the POS frames to be transmitted. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

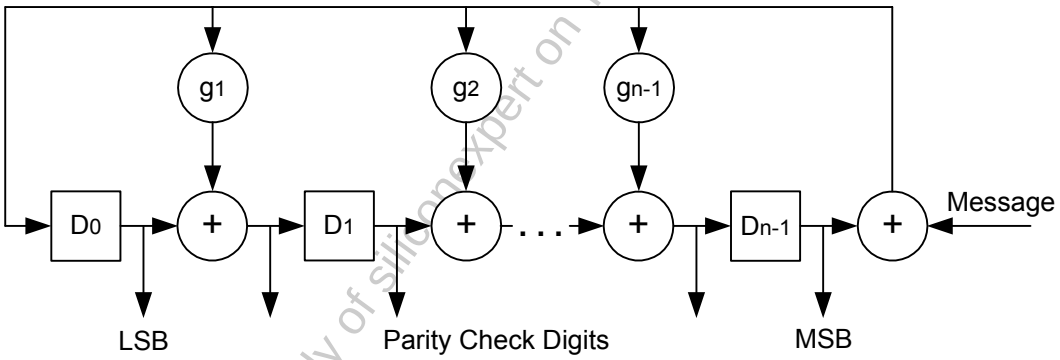
In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The PPP Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. If an overflow occurs, the packet being transmitted will also be aborted and the same abort sequence will be added. Transmission of data resumes when a Start of Packet is encountered in the FIFO data stream.

The POS Frame Generator also performs Inter Packet Gapping. This operation consists of inserting a programmable number of Flag and Idle Sequence characters between each PPP/HDLC Frame transmission. This feature allows one to control the system effective data transmission rate if required.

10.15.5 POS FCS Generator

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(X) = 1 + X^5 + X^{12} + X^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 19 CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

10.15.6 POS Byte Stuffing

The PPP Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 7 Byte Stuffing

Original	Escaped
7E (Flag Sequence)	7D-5E

7D (Control Escape)	7D-5D
Abort Sequence	7D-7E

10.15.7 Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.16 Transmit Scalable Data Queue (TXSDQ)

The TXSDQ provides a FIFO to separate the line-side timing from the higher layer ATM/POS link layer timing. The TXSDQ has two modes of operations, ATM and POS.

10.16.1 Transmit ATM FIFO

The TXSDQ is responsible for holding up to 48 cells until they can be read and transmitted. The cells are written in with a single 32-bit data bus running off TFCLK and are read out at the channel rate. Internal read and write pointers track the cells and indicate the fill status of the Transmit FIFO. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing (TFCLK).

10.16.2 Transmit POS FIFO

The TXSDQ contains 192 sixteen-byte blocks for FIFO storage, along with management circuitry for reading and writing the FIFO. Octets are written in with a single 32-bit data bus running off TFCLK and are read out with a single 32-bit data bus. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing. Packets always begin at the beginning of a block and will not use up left-over space in a block used by a previous packet.

Internal read and write pointers track the insertion and removal of octets, and indicate the fill status of the Transmit FIFO. These status indications are used to detect underrun and overrun conditions, abort packets as appropriate on both System and Line sides, control flag insertion and to generate the DTPA output.

10.17 Transmit Phy Interfaces (RXPHY and TXPHY)

The S/UNI-2488 transmit system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides a 32-bit transmit UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-2488. When configured for POS applications, the system interface provides a 32-bit POS-PHY Level 3 compliant bus for the transfer of ATM cells and data packets between the link layer device and the S/UNI-2488. The link layer device can implement various protocols, including PPP and HDLC.

10.17.1 Transmit UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be configured from the TXSDQ. If the programmed depth is less than the TXSDQ FIFO capacity, more than one cell may be written after TCA is deasserted as the TXSDQ FIFO still allows the "maximum" cells to be stored in its FIFO. The interface provides the transmit cell available status (TCA) which can transition from "available" to "unavailable" when the transmit FIFO is near full or when the FIFO is full and can accept no more writes. The TCFP cell processor automatically transmit idle cells until a full cell is available to be transmitted.

10.17.2 Transmit POS-PHY Level 3 Interface

The POS-PHY Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of packet (TSOP) indication, the end of packet (TEOP) indication, erroneous packet (TERR) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). The TPA signal notifies that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO). The TMOD signal (Transmit Mod) is provided to indicate whether 1, 2, 3, or 4 bytes are valid of the final word transfer (TEOP is asserted). A packet may be aborted by asserting the TERR signal at the end of the packet. The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TCFP HDLC processor automatically transmits idle flag characters until sufficient data is available in the transmit TXSDQ to start transmission.

10.18 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate monitoring circuits (BERM block). It is used to monitor the Line BIP (B2) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block utilizes a sliding window based algorithm.

10.19 SONET/SDH Alarm Reporting Controller (SARC)

The SARC block receives all the section, line, and path defects detected by the receive overhead processors and, according to user specific configuration, generates consequent action indications.

- Receive section alarm (RSALM) indication: RSALM is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

- Receive line AIS insertion (RLAISINS) indication: RLAISINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to remove any defect from the previous enumeration.
- Transmit line RDI insertion (TLRDIINS) indication: TLRDIINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to remove any defect from the previous enumeration.
- Receive path alarm (RPALM) indication: RPALM is asserted when a RSALM, MSRSALM, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.
- Receive path alarm insertion (RPAISINS) indication: RPAISINS is asserted when a RLAISINS, MSRLAISINS, AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

10.20 SONET/SDH Inband Error Report Processor (SIRP)

The SIRP block is used for error reporting from a remote APS protect mate when operating as the working mate under a failure condition. When in the failure condition, the remote protect mate performs section, line and path termination and passes the expected P-REI and P-RDI indications back to the working mate in-band in the G1 byte via its output APS port. The SIRP block processes remote alarm indications in the SONET/SDH data stream from the Input APS port. The SIRP in the companion working mate can be configured to extract remote defect indications (RDI) and remote error indications (REI) from a STS-48c (STM-4c) incoming data stream. Accumulated remote error indications and remote defect indications are reported to the THPP block. Both RDI and extended RDI modes are available. The RDI report can be configured to be maintained asserted for at least 10 frames or 20 frames.

10.21 APS Serial Data Interface

The APS Serial Data Interface consists of a input and output 777.76 Mbps serial TelecomBus used to communicate between a working and protect mate for APS applications.

10.21.1 Output APS Serial Data Interface (T8TE, APISO, TXLV)

The Output APS Serial Data Interface uses the four sets of T8TE, APISO and TXLV blocks to transmit a SONET (SDH) stream to a working or protect mate. The SONET (SDH) OC-48 stream is selected from either the THPP or SVCA block and serialized on a 777.76 Mbps serial TelecomBus. When the S/UNI-2488 is configured as the working mate, the Output APS Serial Data Interface selects the transmit path processed SONET (SDH) stream from the THPP block and transmits it through the 4 differential LVDS pairs, APSO_P/ APSO_N[4:1] to the protect mate where the stream is line and section processed. When the S/UNI-2488 is configured as the protect mate, the Output APS Serial Data Interface selects receive path terminated SONET (SDH) stream from the SVCA block and transmit it through the 4 differential LVDS pairs, APSO_P/ APSO_N[4:1] to the working mate. The working mate will then process the SONET (SDH) payload (ATM or POS) and pass the results to the system via the UTOPIA Level 3 or POSPHY Level 3 interface.

There are four sets of T8TE, APISO and TXLV blocks. Each set implements one of four serial streams that make up the output serial TelecomBus. The T8TE block takes a SONET (SDH) stream and 8B/10B encodes it. The APISO block performs a parallel to serial conversion. The TXLV block is a differential LVDS transmitter.

10.21.2 Input APS Serial Data Interface (RXLV, DRU, R8TD)

The Input APS Serial Data Interface uses the four sets of RXLV, DRU and R8TD blocks to receive a SONET (SDH) stream from a working or protect mate via a serial TelecomBus. The received SONET (SDH) OC-48 stream is passed to either the RCFP or TRMP block for further processing. When the S/UNI-2488 is configured as the working mate and when a failure condition exists, a receive path processed SONET (SDH) stream is expected from the protect mate on the 4 differential LVDS pairs, APSI_P/ APSI_N[4:1]. The S/UNI-2488 will pass this received stream to the RCFP for ATM or POS payload processing. When the S/UNI-2488 is configured as the protect mate and when a failure condition exists, a transmit path processed SONET (SDH) stream is expected from the working mate on the 4 differential LVDS pairs, APSI_P/ APSI_N[4:1]. The S/UNI-2488 will pass this received stream to the TRMP for SONET line and section insertion before it is transmitted.

There are four sets of RXLV, DRU and R8TD blocks. Each set implements one of four serial streams that make up the input serial TelecomBus. The RXLV block is a differential LVDS receiver. The DRU recovers the 777.76 Mbps 8B/10B encoded serial stream and deserializes it for the R8TD block. The R8TB block converts the deserialized 8B/10B stream into the a SONET (SDH) stream.

10.21.3 LVDS Transmit Reference (TXREF)

The TXLVREF provides an on-chip bandgap voltage reference (1.20V ±5%) and a precision current to the TXLVs. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude. The precision currents are generated by forcing the reference voltage across an external, off-chip 3.16KΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

10.21.4 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for the usage by the transmitter. The APFIFPCLK is used as a jitter-free reference clock to the CSU.

10.22 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-2488 identification code is 053810CD hexadecimal.

10.23 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the S/UNI-2488. The normal mode registers are used during normal operation to configure and monitor the S/UNI-2488. The test mode registers are used to enhance the testability of the S/UNI-2488. The register set is accessed as shown below. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 8 Register Memory Map

Address	Register Description
0000	S/UNI-2488 Identity and Global Performance Monitor Update
0001	S/UNI-2488 Master Reset, Configuration, and Loopback
0002	S/UNI-2488 Transmit Control Register
0003	S/UNI-2488 Clock Monitors
0004	S/UNI-2488 Master Interrupt Status #1
0005	S/UNI-2488 Master Interrupt Status #2
0006	S/UNI-2488 Master Interrupt Status #3
0007	S/UNI-2488 Master Interrupt Status #4
0008	S/UNI-2488 Master Interrupt Status #5
0009	S/UNI-2488 Master Interrupt Status #6
000A	S/UNI-2488 Master Interrupt Status #7
000B	Software General Purpose (FREE[12:0])
000C	S/UNI-2488 APS Input TelecomBus Synchronization Delay
000D	Reserved
000E	S/UNI-2488 Diagnostics
000F	S/UNI-2488 Identification Register
0010	Rx2488 Analog Interrupt Status
0011	Rx2488 Analog Interrupt Control
0012	Rx2488 Analog CRU Control
0013	Rx2488 Analog CRU Clock Training Configuration and Status

Address	Register Description
0014	Rx2488 Analog PRBS Control
0015	Rx2488 Reserved
0016-001F	Rx2488 Reserved
0020	Tx2488 Analog Control/Status
0021	Tx2488 ABC Control
0022	Tx2488 Pattern Register
0023-002F	Tx2488 Analog Reserved
0030	SRLI Clock Configuration
0031	SRLI PGM Clock Configuration
0032-0037	SRLI Reserved
0038	STLI Clock Configuration
0039	STLI PGM Clock Configuration
003A-003F	STLI Reserved
0040	RRMP Configuration
0041	RRMP Status
0042	RRMP Interrupt Enable
0043	RRMP Interrupt Status
0044	RRMP Receive APS
0045	RRMP Receive SSM
0046	RRMP AIS Enable
0047	RRMP Section BIP Error Counter
0048	RRMP Line BIP Error Counter (LSB)
0049	RRMP Line BIP Error Counter (MSB)
004A	RRMP Line REI Error Counter (LSB)
004B	RRMP Line REI Error Counter (MSB)
004C-004F	RRMP Reserved 1
0050	RRMP Aux2 Configuration
0051-0055	RRMP Reserved 2
0056	RRMP Aux2 AIS Enable
0057-005F	RRMP Reserved 2
0060	RRMP Aux3 Configuration
0061-0065	RRMP Reserved 3
0066	RRMP Aux3 AIS Enable
0067-006F	RRMP Reserved 3
0070	RRMP Aux4 Configuration
0071-0075	RRMP Reserved 4
0076	RRMP Aux4 AIS Enable
0077-007F	RRMP Reserved 4
0080	TRMP Configuration
0081	TRMP Register Insertion

Address	Register Description
0082	TRMP Error Insertion
0083	TRMP Transmit J0 and Z0
0084	TRMP Transmit E1 and F1
0085	TRMP Transmit D1D3 and D4D12
0086	TRMP Transmit K1 and K2
0087	TRMP Transmit S1 and Z1
0088	TRMP Transmit Z2 and E2
0089	TRMP H1 and H2 Mask
008A	TRMP B1 and B2 Mask
008B-009F	TRMP Reserved 1
00A0	TRMP Aux2 Configuration
00A1	TRMP Aux2 Register Insertion
00A2	TRMP Aux2 Error Insertion
00A3	TRMP Aux2 Transmit Z0
00A4-00A6	TRMP Aux2 Reserved 1
00A7	TRMP Aux2 Transmit Z1
00A8	TRMP Aux2 Transmit Z2
00A9-00BF	TRMP Aux2 Reserved 2
00C0	TRMP Aux3 Configuration
00C1	TRMP Aux3 Register Insertion
00C2	TRMP Aux3 Error Insertion
00C3	TRMP Aux3 Transmit Z0
00C4-00C6	TRMP Aux3 Reserved 1
00C7	TRMP Aux3 Transmit Z1
00C8	TRMP Aux3 Transmit Z2
00C9-00DF	TRMP Aux3 Reserved 2
00E0	TRMP Aux4 Configuration
00E1	TRMP Aux4 Register Insertion
00E2	TRMP Aux4 Error Insertion
00E3	TRMP Aux4 Transmit Z0
00E4-00E6	TRMP Aux4 Reserved 1
00E7	TRMP Aux4 Transmit Z1
00E8	TRMP Aux4 Transmit Z2
00E9-00FF	TRMP Aux4 Reserved 2
0100	SBER Configuration
0101	SBER Status
0102	SBER Interrupt Enable
0103	SBER Interrupt Status
0104	SBER SF BERM Accumulation Period (LSB)
0105	SBER SF BERM Accumulation Period (MSB)

Address	Register Description
0106	SBER SF BERM Saturation Threshold (LSB)
0107	SBER SF BERM Saturation Threshold (MSB)
0108	SBER SF BERM Declaring Threshold (LSB)
0109	SBER SF BERM Declaring Threshold (MSB)
010A	SBER SF BERM Clearing Threshold (LSB)
010B	SBER SF BERM Clearing Threshold (MSB)
010C	SBER SD BERM Accumulation Period (LSB)
010D	SBER SD BERM Accumulation Period (MSB)
010E	SBER SD BERM Saturation Threshold (LSB)
010F	SBER SD BERM Saturation Threshold (MSB)
0110	SBER SD BERM Declaring Threshold (LSB)
0111	SBER SD BERM Declaring Threshold (MSB)
0112	SBER SD BERM Clearing Threshold (LSB)
0113	SBER SD BERM Clearing Threshold (MSB)
0114-012F	SBER Reserved
0130	RTTP SECTION Indirect Address
0131	RTTP SECTION Indirect Data
0132	RTTP SECTION Trace Unstable Status
0133	RTTP SECTION Trace Unstable Interrupt Enable
0134	RTTP SECTION Trace Unstable Interrupt Status
0135	RTTP SECTION Trace Mismatch Status
0136	RTTP SECTION Trace Mismatch Interrupt Enable
0137	RTTP SECTION Trace Mismatch Interrupt Status
0138	TTTP SECTION Indirect Address
0139	TTTP SECTION Indirect Data
013A-013B	TTTP SECTION Reserved
013C-01FF	S/UNI-2488 Reserved
0200	RHPP STS-1/STM-0 #1 through #12 Indirect Address
0201	RHPP STS-1/STM-0 #1 through #12 Indirect Data
0202	RHPP Payload Configuration
0203	RHPP Counters Update
0204	RHPP Path Interrupt Status
0205	Point Concatenation Processing
0206-0207	RHPP Reserved
0208	RHPP STS-1/STM-0 #1 Pointer Interpreter Status
0209	RHPP STS-1/STM-0 #1 Pointer Interpreter Interrupt Enable
020A	RHPP STS-1/STM-0 #1 Pointer Interpreter Interrupt Status
020B	RHPP STS-1/STM-0 #1 Error Monitor Status
020C	RHPP STS-1/STM-0 #1 Error Monitor Interrupt Enable
020D	RHPP STS-1/STM-0 #1 Error Monitor Interrupt Status

Address	Register Description
020E-020F	RHPP Reserved
0210	RHPP STS-1/STM-0 #2 Pointer Interpreter Status
0211	RHPP STS-1/STM-0 #2 Pointer Interpreter Interrupt Enable
0212	RHPP STS-1/STM-0 #2 Pointer Interpreter Interrupt Status
0213	RHPP STS-1/STM-0 #2 Error Monitor Status
0214	RHPP STS-1/STM-0 #2 Error Monitor Interrupt Enable
0215	RHPP STS-1/STM-0 #2 Error Monitor Interrupt Status
0216-0217	RHPP Reserved
0218	RHPP STS-1/STM-0 #3 Pointer Interpreter Status
0219	RHPP STS-1/STM-0 #3 Pointer Interpreter Interrupt Enable
021A	RHPP STS-1/STM-0 #3 Pointer Interpreter Interrupt Status
021B	RHPP STS-1/STM-0 #3 Error Monitor Status
021C	RHPP STS-1/STM-0 #3 Error Monitor Interrupt Enable
021D	RHPP STS-1/STM-0 #3 Error Monitor Interrupt Status
021E-021F	RHPP Reserved
0220	RHPP STS-1/STM-0 #4 Pointer Interpreter Status
0221	RHPP STS-1/STM-0 #4 Pointer Interpreter Interrupt Enable
0222	RHPP STS-1/STM-0 #4 Pointer Interpreter Interrupt Status
0223	RHPP STS-1/STM-0 #4 Error Monitor Status
0224	RHPP STS-1/STM-0 #4 Error Monitor Interrupt Enable
0225	RHPP STS-1/STM-0 #5 Error Monitor Interrupt Status
0226-0227	RHPP Reserved
0228	RHPP STS-1/STM-0 #5 Pointer Interpreter Status
0229	RHPP STS-1/STM-0 #5 Pointer Interpreter Interrupt Enable
022A	RHPP STS-1/STM-0 #5 Pointer Interpreter Interrupt Status
022B	RHPP STS-1/STM-0 #5 Error Monitor Status
022C	RHPP STS-1/STM-0 #5 Error Monitor Interrupt Enable
022D	RHPP STS-1/STM-0 #5 Error Monitor Interrupt Status
022E-022F	RHPP Reserved
0230	RHPP STS-1/STM-0 #6 Pointer Interpreter Status
0231	RHPP STS-1/STM-0 #6 Pointer Interpreter Interrupt Enable
0232	RHPP STS-1/STM-0 #6 Pointer Interpreter Interrupt Status
0233	RHPP STS-1/STM-0 #6 Error Monitor Status
0234	RHPP STS-1/STM-0 #6 Error Monitor Interrupt Enable
0235	RHPP STS-1/STM-0 #6 Error Monitor Interrupt Status
0236-0237	RHPP Reserved
0238	RHPP STS-1/STM-0 #7 Pointer Interpreter Status
0239	RHPP STS-1/STM-0 #7 Pointer Interpreter Interrupt Enable
023A	RHPP STS-1/STM-0 #7 Pointer Interpreter Interrupt Status
023B	RHPP STS-1/STM-0 #7 Error Monitor Status

Address	Register Description
023C	RHPP STS-1/STM-0 #7 Error Monitor Interrupt Enable
023D	RHPP STS-1/STM-0 #7 Error Monitor Interrupt Status
023E-023F	RHPP Reserved
0240	RHPP STS-1/STM-0 #8 Pointer Interpreter Status
0241	RHPP STS-1/STM-0 #8 Pointer Interpreter Interrupt Enable
0242	RHPP STS-1/STM-0 #8 Pointer Interpreter Interrupt Status
0243	RHPP STS-1/STM-0 #8 Error Monitor Status
0244	RHPP STS-1/STM-0 #8 Error Monitor Interrupt Enable
0245	RHPP STS-1/STM-0 #8 Error Monitor Interrupt Status
0246-0247	RHPP Reserved
0248	RHPP STS-1/STM-0 #9 Pointer Interpreter Status
0249	RHPP STS-1/STM-0 #9 Pointer Interpreter Interrupt Enable
024A	RHPP STS-1/STM-0 #9 Pointer Interpreter Interrupt Status
024B	RHPP STS-1/STM-0 #9 Error Monitor Status
024C	RHPP STS-1/STM-0 #9 Error Monitor Interrupt Enable
024D	RHPP STS-1/STM-0 #9 Error Monitor Interrupt Status
024E-024F	RHPP Reserved
0250	RHPP STS-1/STM-0 #10 Pointer Interpreter Status
0251	RHPP STS-1/STM-0 #10 Pointer Interpreter Interrupt Enable
0252	RHPP STS-1/STM-0 #10 Pointer Interpreter Interrupt Status
0253	RHPP STS-1/STM-0 #10 Error Monitor Status
0254	RHPP STS-1/STM-0 #10 Error Monitor Interrupt Enable
0255	RHPP STS-1/STM-0 #10 Error Monitor Interrupt Status
0256-0257	RHPP Reserved
0258	RHPP STS-1/STM-0 #11 Pointer Interpreter Status
0259	RHPP STS-1/STM-0 #11 Pointer Interpreter Interrupt Enable
025A	RHPP STS-1/STM-0 #11 Pointer Interpreter Interrupt Status
025B	RHPP STS-1/STM-0 #11 Error Monitor Status
025C	RHPP STS-1/STM-0 #11 Error Monitor Interrupt Enable
025D	RHPP STS-1/STM-0 #11 Error Monitor Interrupt Status
025E-025F	RHPP Reserved
0260	RHPP STS-1/STM-0 #12 Pointer Interpreter Status
0261	RHPP STS-1/STM-0 #12 Pointer Interpreter Interrupt Enable
0262	RHPP STS-1/STM-0 #12 Pointer Interpreter Interrupt Status
0263	RHPP STS-1/STM-0 #12 Error Monitor Status
0264	RHPP STS-1/STM-0 #12 Error Monitor Interrupt Enable
0265	RHPP STS-1/STM-0 #12 Error Monitor Interrupt Status
0265-027F	RHPP Reserved
0280	RHPP STS-1/STM-0 #13 through #24 Indirect Address
0281	RHPP STS-1/STM-0 #13 through #24 Indirect Data

Address	Register Description
0282	RHPP Payload Configuration
0283	RHPP Counters Update
0284	RHPP Path Interrupt Status
0285	Pointer Concatenation Processing
0286-0287	Reserved
0288	RHPP STS-1/STM-0 #13 Pointer Interpreter Status
0289	RHPP STS-1/STM-0 #13 Pointer Interpreter Interrupt Enable
028A	RHPP STS-1/STM-0 #13 Pointer Interpreter Interrupt Status
028B	RHPP STS-1/STM-0 #13 Error Monitor Status
028C	RHPP STS-1/STM-0 #13 Error Monitor Interrupt Enable
028D	RHPP STS-1/STM-0 #13 Error Monitor Interrupt Status
028E-028F	RHPP Reserved
. . . . .	. . . . .
02E0	RHPP STS-1/STM-0 #24 Pointer Interpreter Status
02E1	RHPP STS-1/STM-0 #24 Pointer Interpreter Interrupt Enable
02E2	RHPP STS-1/STM-0 #24 Pointer Interpreter Interrupt Status
02E3	RHPP STS-1/STM-0 #24 Error Monitor Status
02E4	RHPP STS-1/STM-0 #24 Error Monitor Interrupt Enable
02E5	RHPP STS-1/STM-0 #24 Error Monitor Interrupt Status
02E6-02FF	RHPP Reserved
0300	RHPP STS-1/STM-0 #25 through #36 Indirect Address
0301	RHPP STS-1/STM-0 #25 through #36 Indirect Data
0302	RHPP Payload Configuration
0303	RHPP Counters Update
0304	RHPP Path Interrupt Status
0305	Pointer Concatenation Processing
0306-0307	Reserved
0308	RHPP STS-1/STM-0 #25 Pointer Interpreter Status
0309	RHPP STS-1/STM-0 #25 Pointer Interpreter Interrupt Enable
030A	RHPP STS-1/STM-0 #25 Pointer Interpreter Interrupt Status
030B	RHPP STS-1/STM-0 #25 Error Monitor Status
030C	RHPP STS-1/STM-0 #25 Error Monitor Interrupt Enable
030D	RHPP STS-1/STM-0 #25 Error Monitor Interrupt Status
030E-030F	RHPP Reserved
. . . . .	. . . . .
0360	RHPP STS-1/STM-0 #36 Pointer Interpreter Status
0361	RHPP STS-1/STM-0 #36 Pointer Interpreter Interrupt Enable
0362	RHPP STS-1/STM-0 #36 Pointer Interpreter Interrupt Status
0363	RHPP STS-1/STM-0 #36 Error Monitor Status
0364	RHPP STS-1/STM-0 #36 Error Monitor Interrupt Enable

Address	Register Description
0365	RHPP STS-1/STM-0 #36 Error Monitor Interrupt Status
0365-036F	RHPP Reserved
0380	RHPP STS-1/STM-0 #37 through #48 Indirect Address
0381	RHPP STS-1/STM-0 #37 through #48 Indirect Data
0382	RHPP Payload Configuration
0383	RHPP Counters Update
0384	RHPP Path Interrupt Status
0385	Pointer Concatenation Processing
0386-0387	Reserved
0388	RHPP STS-1/STM-0 #37 Pointer Interpreter Status
0389	RHPP STS-1/STM-0 #37 Pointer Interpreter Interrupt Enable
038A	RHPP STS-1/STM-0 #37 Pointer Interpreter Interrupt Status
038B	RHPP STS-1/STM-0 #37 Error Monitor Status
038C	RHPP STS-1/STM-0 #37 Error Monitor Interrupt Enable
038D	RHPP STS-1/STM-0 #37 Error Monitor Interrupt Status
038E-038F	RHPP Reserved
. . . . .	. . . . .
03E0	RHPP STS-1/STM-0 #48 Pointer Interpreter Status
03E1	RHPP STS-1/STM-0 #48 Pointer Interpreter Interrupt Enable
03E2	RHPP STS-1/STM-0 #48 Pointer Interpreter Interrupt Status
03E3	RHPP STS-1/STM-0 #48 Error Monitor Status
03E4	RHPP STS-1/STM-0 #48 Error Monitor Interrupt Enable
03E5	RHPP STS-1/STM-0 #48 Error Monitor Interrupt Status
03E6-03FF	RHPP Reserved
0400	THPP STS-1/STM-0 #1 through #12 Indirect Address
0401	THPP STS-1/STM-0 #1 through #12 Indirect Data
0402	THPP Payload Configuration
0402-047F	THPP Reserved 1
0480	THPP STS-1/STM-0 #13 through #24 Indirect Address
0481	THPP STS-1/STM-0 #13 through #24 Indirect Data
0482-04FF	THPP Reserved 2
0500	THPP STS-1/STM-0 #25 through #36 Indirect Address
0501	THPP STS-1/STM-0 #25 through #36 Indirect Data
0502-057F	THPP Reserved 3
0580	THPP STS-1/STM-0 #37 through #48 Indirect Address
0581	THPP STS-1/STM-0 #37 through #48 Indirect Data
0582-05FF	THPP Reserved 4
0600	SVCA Indirect Address
0601	SVCA Indirect Data
0602	SVCA Payload Configuration

Address	Register Description
0603	SVCA Positive Justification Interrupt Status
0604	SVCA Negative Justification Interrupt Status
0605	SVCA FIFO Overflow Interrupt Status
0606	SVCA FIFO Underflow Interrupt Status
0607	SVCA Pointer Justification Interrupt Enable
0608	SVCA FIFO Interrupt Enable
0609	SVCA Pointer Justification Thresholds
060A	SVCA MISC Register
060B	Reserved
060C-061F	SVCA Reserved 1
0620-063F	SVCA slave SVCA #2
0640-065F	SVCA slave SVCA #3
0660-067F	SVCA slave SVCA #4
0700	RTTP PATH Indirect Address
0701	RTTP PATH Indirect Data
0702	RTTP PATH Trace Unstable Status
0703	RTTP PATH Trace Unstable Interrupt Enable
0704	RTTP PATH Trace Unstable Interrupt Status
0705	RTTP PATH Trace Mismatch Status
0706	RTTP PATH Trace Mismatch Interrupt Enable
0707	RTTP PATH Trace Mismatch Interrupt Status
0708	TTTP PATH Indirect Address
0709	TTTP PATH Indirect Data
070A-070B	TTTP PATH Reserved
070C-071F	S/UNI-2488 Reserved
0720	SARC Path Register Enable
0721	SARC Reserved
0722	SARC Section Configuration
0723	SARC Section SALM
0724	SARC Section RLAISINS Enable
0725	SARC Section TLRDIINS Enable
0726-0727	SARC Reserved
0728	SARC Path Configuration
0729	SARC Path RALM Enable
072A	SARC Path RPAISINS Enable
072B-072F	SARC Reserved
0730	SARC LOP Pointer Status
0731	SARC LOP Pointer Interrupt Enable
0732	SARC LOP Pointer Interrupt Status
0733	SARC AIS Pointer Status

Address	Register Description
0734	SARC AIS Pointer Interrupt Enable
0735	SARC AIS Pointer Interrupt Status
0736-073F	SARC Reserved
0740	RCFP Configuration
0741	RCFP Interrupt Enable
0742	RCFP Interrupt Indication and Status
0743	RCFP Minimum Packet Length
0744	RCFP Maximum Packet Length
0745	RCFP LCD Count Threshold
0746	RCFP Idle Cell Header and Mask
0747	RCFP Receive Byte/Idle Cell Counter (LSB)
0748	RCFP Receive Byte/Idle Cell Counter
0749	RCFP Receive Byte/Idle Cell Counter (MSB)
074A	RCFP Packet/Cell Counter (LSB)
074B	RCFP Receive Packet/ATM Cell Counter (MSB)
074C	RCFP Receive Erroneous FCS/HCS Counter
074D	RCFP Receive Aborted Packet Counter
074E	RCFP Receive Minimum Length Packet Error
074F	RCFP Receive Maximum Length Packet Error Counter
0750	TCFP Configuration
0751	TCFP Interrupt Indication
0752	TCFP Idle/Unassigned ATM Cell Header
0753	TCFP Diagnostics
0754	TCFP Transmit Cell/Packet Counter (LSB)
0755	TCFP Transmit Cell/Packet Counter (MSB)
0756	TCFP Transmit Byte Counter (LSB)
0757	TCFP Transmit Byte Counter
0758	TCFP Transmit Byte Counter (MSB)
0759	TCFP Aborted Packet Counter
075A-075F	TCFP Reserved
0760	RXSDQ FIFO Reset
0761	RXSDQ FIFO Interrupt Enable
0762	RXSDQ Reserved
0763	RXSDQ FIFO Overflow Port and Interrupt Indication
0764	RXSDQ Reserved
0765	RXSDQ Reserved
0766	RXSDQ Reserved
0767	RXSDQ Reserved
0768	RXSDQ FIFO Indirect Address
0769	RXSDQ FIFO Indirect Configuration

Address	Register Description
076A	RXSDQ FIFO Indirect Data Available Threshold
076B	RXSDQ FIFO Indirect Cells and Packets Count
076C	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
076D	RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
076E	RXSDQ FIFO Cells and Packets Dropped Aggregate Count
076F	RXSDQ Reserved
0770	TXSDQ FIFO Reset
0771	TXSDQ FIFO Interrupt Enable
0772	TXSDQ Reserved
0773	TXSDQ FIFO Overflow Port and Interrupt Indication
0774	TXSDQ FIFO EOP Error Port and Interrupt Indication
0775	TXSDQ FIFO SOP Error Port and Interrupt Indication
0776	TXSDQ Reserved
0777	TXSDQ Reserved
0778	TXSDQ FIFO Indirect Address
0779	TXSDQ FIFO Indirect Configuration
077A	TXSDQ FIFO Indirect Data and Buffer Available Thresholds
077B	TXSDQ FIFO Indirect Cells and Packets Count
077C	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)
077D	TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)
077E	TXSDQ FIFO Cells and Packets Dropped Aggregate count
077F	TXSDQ Reserved
0780	RXPHY Configuration
0781	RXPHY Interrupt Status
0782	RXPHY Interrupt Enable
0783	RXPHY Indirect Burst Size
0784	RXPHY Calendar Length
0785	RXPHY Calendar Indirect Address Data
0786	RXPHY Data Type Field
0787	RXPHY Reserved
0788	TXPHY Configuration
0789	TXPHY Interrupt Status
078A	TXPHY Interrupt Enable
078B	TXPHY Data Type Field
078C-078F	TXPHY Reserved
0790	SIRP Configuration Timeslot
0791-079B	SIRP Reserved 1
079C	SIRP Configuration
079D-079F	SIRP Reserved 2
07A0-07FF	S/UNI-2488 Reserved

Address	Register Description
0800	PRGM Indirect Address
0801	PRGM Indirect Data
0802	PRGM Generator Payload Configuration
0803	PRGM Monitor Payload Configuration
0804	PRGM Monitor Byte Error Interrupt Status
0805	PRGM Monitor Byte Error Interrupt Enable
0806	PRGM Reserved
0807	PRGM Reserved
0808	PRGM Reserved
0809	PRGM Monitor Synchronization Interrupt Status
080A	PRGM Monitor Synchronization Interrupt Enable
080B	PRGM Monitor Synchronization Status
080C	PRGM Performance Counters Transfer Trigger
080D-080F	PRGM Reserved
0810	PRGM Aux2 Indirect Address
0811	PRGM Aux2 Indirect Data
0812	PRGM Aux2 Generator Payload Configuration
0813	PRGM Aux2 Monitor Payload Configuration
0814	PRGM Aux2 Monitor Byte Error Interrupt Status
0815	PRGM Aux2 Monitor Byte Error Interrupt Enable
0816-0818	PRGM Aux2 Reserved
0819	PRGM Aux2 Monitor Synchronization Interrupt Status
081A	PRGM Aux2 Monitor Synchronization Interrupt Enable
081B	PRGM Aux2 Monitor Synchronization Status
081C	PRGM Aux2 Performance Counters Transfer Trigger
081D-081F	PRGM Aux2 Reserved
0820	PRGM Aux3 Indirect Address
0821	PRGM Aux3 Indirect Data
0822	PRGM Aux3 Generator Payload Configuration
0823	PRGM Aux3 Monitor Payload Configuration
0824	PRGM Aux3 Monitor Byte Error Interrupt Status
0825	PRGM Aux3 Monitor Byte Error Interrupt Enable
0826-0828	PRGM Aux3 Reserved
0829	PRGM Aux3 Monitor Synchronization Interrupt Status
082A	PRGM Aux3 Monitor Synchronization Interrupt Enable
082B	PRGM Aux3 Monitor Synchronization Status
082C	PRGM Aux3 Performance Counters Transfer Trigger
082D-082F	PRGM Aux3 Reserved
0830	PRGM Aux4 Indirect Address
0831	PRGM Aux4 Indirect Data

Address	Register Description
0832	PRGM Aux4 Generator Payload Configuration
0833	PRGM Aux4 Monitor Payload Configuration
0834	PRGM Aux4 Monitor Byte Error Interrupt Status
0835	PRGM Aux4 Monitor Byte Error Interrupt Enable
0836-0838	PRGM Aux4 Reserved
0839	PRGM Aux4 Monitor Synchronization Interrupt Status
083A	PRGM Aux4 Monitor Synchronization Interrupt Enable
083B	PRGM Aux4 Monitor Synchronization Status
083C	PRGM Aux4 Performance Counters Transfer Trigger
083D-083F	PRGM Aux4 Reserved
0840	R8TD APS1 Control and Status
0841	R8TD APS1 Interrupt Status
0842	R8TD APS1 Line Code Violation Count
0843	R8TD APS1 Analog Control 1
0844	R8TD APS1 Analog Control 2
0845	R8TD APS1 Analog Control 3
0846-0847	R8TD APS1 Reserved
0848	R8TD APS2 Control and Status
0849	R8TD APS2 Interrupt Status
084A	R8TD APS2 Line Code Violation Count
084B	R8TD APS2 Analog Control 1
084C	R8TD APS2 Analog Control 2
084D	R8TD APS2 Analog Control 3
084E-084F	R8TD APS2 Reserved
0850	R8TD APS3 Control and Status
0851	R8TD APS3 Interrupt Status
0852	R8TD APS3 Line Code Violation Count
0853	R8TD APS3 Analog Control 1
0854	R8TD APS3 Analog Control 2
0855	R8TD APS3 Analog Control 3
0856-0857	R8TD APS3 Reserved
0858	R8TD APS4 Control and Status
0859	R8TD APS4 Interrupt Status
085A	R8TD APS4 Line Code Violation Count
085B	R8TD APS4 Analog Control 1
085C	R8TD APS4 Analog Control 2
085D	R8TD APS4 Analog Control 3
085E-085F	R8TD APS4 Reserved
0860	T8TE APS1 Control and Status
0861	T8TE APS1 Interrupt Status

Address	Register Description
0862	T8TE APS1 TelecomBus Mode #1
0863	T8TE APS1 TelecomBus Mode #2
0864	T8TE APS1 Test Pattern
0865	T8TE APS1 Analog Control
0866	T8TE APS1 DTB Bus
0867	T8TE APS1 Reserved
0868	T8TE APS2 Control and Status
0869	T8TE APS2 Interrupt Status
086A	T8TE APS2 TelecomBus Mode #1
086B	T8TE APS2 TelecomBus Mode #2
086C	T8TE APS2 Test Pattern
086D	T8TE APS2 Analog Control
086E	T8TE APS2 DTB Bus
086F	T8TE APS2 Reserved
0870	T8TE APS3 Control and Status
0871	T8TE APS3 Interrupt Status
0872	T8TE APS3 TelecomBus Mode #1
0873	T8TE APS3 TelecomBus Mode #2
0874	T8TE APS3 Test Pattern
0875	T8TE APS3 Analog Control
0876	T8TE APS3 DTB Bus
0877	T8TE APS3 Reserved
0878	T8TE APS4 Control and Status
0879	T8TE APS4 Interrupt Status
087A	T8TE APS4 TelecomBus Mode #1
087B	T8TE APS4 TelecomBus Mode #2
087C	T8TE APS4 Test Pattern
087D	T8TE APS4 Analog Control
087E	T8TE APS4 DTB Bus
087F	T8TE APS4 Reserved
0880	RXDLL Configuration
0881	RXDLL Vernier Control
0882	RXDLL Delay Tap Status/DLL Reset
0883	RXDLL Control Status
0884	TXDLL Configuration
0885	TXDLL Vernier Control
0886	TXDLL Delay Tap Status/DLL Reset
0887	TXDLL Control Status
0888	CSTR Control
0889	CSTR Interrupt Enable and APS CSU Lock Status

Address	Register Description
088A	CSTR APS CSU Lock Interrupt Indication
088B	CSTR Reserved
088C-088F	S/UNI-2488 Reserved
0890-0897	S/UNI-2488 Rx STSI Reserved
0898-089F	S/UNI-2488 Tx STSI Reserved
08A0-8FFF	S/UNI-2488 Reserved
0900	Rx APS J0 Interrupt Enable
0901	Rx APS J0 FIFO Interrupt Status
0902	S/UNI-2488 Miscellaneous Defect Configuration
0903-090D	S/UNI-2488 Reserved
090E-090F	S/UNI-2488 Reserved
0910-1FFF	S/UNI-2488 Reserved
2000-2FFF	S/UNI-2488 Test – see section 12.

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI-2488. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-2488 to determine the programming state of the device.

3. Writable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-2488 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-2488 operates as intended, reserved register bits must only be written with the logic level as specified. Writing other values to reserved registers should be avoided.

Register 0000H: S/UNI-2488 Identity and Global Performance Monitor Update

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R	TYPE[4]	0
Bit 7	R	TYPE[3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	1

This register allows the revision number of the S/UNI-2488 to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-2488.

In addition, writing to the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H) performs a global performance monitor update by simultaneously loading all the performance meter registers in the RHPP, RRMP, RCFP, RXSDQ, SVCA, PRGM, TXSDQ, TCFP, R8TD, and T8TE blocks.

ID[3:0]

The ID bits can be read to provide a binary S/UNI-2488 revision number. A value of 0x0 means the device is a revision A S/UNI-2488. A value of 0x1 means the device is a revision B S/UNI-2488. A value of 0x2 means the device is a revision C S/UNI-2488. A value of 0x3 means the device is a revision D S/UNI-2488.

TYPE[4:0]

The TYPE bits can be read to distinguish the S/UNI-2488 from the other members of the S/UNI family of devices. The TYPE[4:0] register for the PM5381 S/UNI-2488 is 00010.

TIP

The TIP bit is set to logic one when the performance meter registers are being loaded. Writing to this register with DRESET equal to logic 0 initiates an accumulation interval transfer and loads all the performance meter registers in the S/UNI-2488.

TIP remains high while the transfer is in progress, and is set to logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0001H: S/UNI-2488 Master Reset, Configuration, and Loopback

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET_APS	0
Bit 13	R/W	ARESET_LINE	0
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	XCONNECTMODE	0
Bit 5	R/W	APSMUX_RCFP	0
Bit 4	R/W	APSMUX_T8TE	0
Bit 3	R/W	APSMUX_TRMP	0
Bit 2	R/W	PDLE	0
Bit 1	R/W	WCIMODE	0
Bit 0	R/W	PL3EN	0

This register allows the configuration of S/UNI-2488 features.

PL3EN

The POS-PHY Level 3 Select bit (PL3EN) is OR'ed with the POSL3_UL3B pin to select POS-PHY Level 3 mode on the system interface. When PL3EN or POSL3_UL3B are logic 1, the system bus operates in POS-PHY Level 3 mode. When both PL3EN and POSL3_UL3B are logic 0, the bus operates as a UTOPIA Level 3™ bus. Reading this bit gives the mode of the bus, (i.e., the OR of the pin and the bit). The default state of this register bit is logic 0.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read.

PDLE

The Parallel Diagnostic Loopback, PDLE bit enables the S/UNI-2488 diagnostic loopback where the STLI block is directly connected to its SRLI block. When PDLE is logic one, loopback is enabled. Under this operating condition, the S/UNI-2488 continues to operate normally in the transmit direction. When PDLE is logic zero, the S/UNI-2488 operates normally.

APSMUX_TRMP

The APS MUX_TRMP register bit controls whether data received by the TRMP is sourced from the THPP (normal operation) or from the R8TD (APSI_P/ APSI_N[4:1]) APS port (when the S/UNI-2488 is configured as a protect device). When APSMUX_TRMP is a logic 0, the TRMP (normal mode of operation) receives data from the THPP. When APSMUX_TRMP is a logic 1 (S/UNI-2488 is configured as a protect device), the TRMP receives data from the R8TD (APSI_P/ APSI_N[4:1]) APS port. Under this mode of operation the input APS port is expected to contain a bridged transmit SONET stream from a working mate device. In addition, the S/UNI-2488 will output a received SONET stream on the output APS port to the same mate device.

APSMUX_T8TE

The APS MUX_T8TE register bit controls whether or not data from the THPP (normal operation) or the SVCA (when configured as the protect device) are transmitted over the T8TE (APSO_P/ APSO_N[4:1]) port. When APSMUX_T8TE is a logic 0, the T8TE receives data from the THPP (normal mode of operation). When APSMUX_T8TE is a logic 1, the T8TE receives data from the SVCA (S/UNI-2488 is configured as a protect device). These data are transmitted over the APSO_P/ APSO_N[4:1] port. In this mode, the S/UNI-2488 receives a SONET stream from a protect mate via the input APS port and presents the payload out through the POS-PHY Level 3 or UTOPIA Level 3™ interface. The S/UNI-2488 transmits data from its POS-PHY Level 3 or UTOPIA Level 3™ interface out through its output APS port to a protect mate device. It is assumed that the mate device will transmit data onto the line.

APSMUX_RCFP

The APS MUX1_RCFP register bit controls whether or not the RCFP receives data from the SVCA (normal operation) or from the R8TD (APSI_P/ APSI_N[4:1]) APS Port (when configured as a working mate during an APS switchover). When APSMUX_RCFP is a logic 0, the RCFP receives data normally from the SVCA. When APSMUX_RCFP is a logic 1, the RCFP receives data from the R8TD APS Port. This register bit would be set if the S/UNI-2488 is configured as a working device during an APS failure condition.

XCONNECTMODE

The Cross Connect mode (XCONNECTMODE) bit enables the S/UNI-2488 to operate in a mode where granularity down to the STS-1 / STM-0 level is supported in the device. In the normal mode of operation, the S/UNI-2488 will process an STS-48c payload only, however when in XCONNECT mode the S/UNI-2488 allows for independent configuration of the four RHPP and SVCA blocks in the device. These blocks can be configured so as to allow the processing of a mixture of payloads within an STS-48 frame. When set to logic 0, the S/UNI-2488 operates normally and processes an STS-48c frame carrying ATM or POS payloads. When set to logic 1, the S/UNI-2488 can process payloads down to STS-1 granularity and will work in conjunction with a cross connect switch like the PM5372 TSE. The operation of the POS-PHY Level 3 / UTOPIA Level 3™ interface is not defined in this mode of operation. Please refer to the Operation section for more information.

The SRLI Loopback enable (SRLILE) bit enables the S/UNI-2488 diagnostic loopback in which the SRLI output is directly connected to the STLI block. When SRLILE is logic one, the loopback is enabled. When SRLILE is logic zero, the S/UNI-2488 operates normally. This register bit is only used for test purposes.

Reserved

Must be set to the default value.

ARESET_LINE

The ARESET_LINE bit allows the 2488 Mbps analog circuitry in the S/UNI-2488 to be reset under software control. If the ARESET_LINE bit is a logic one, 2488 Mbps analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the 2488 Mbps analog blocks out of reset. Holding the ARESET_LINE in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET_LINE bit, thus negating the analog software reset.

ARESET_APS

The ARESET_APS bit allows the APS Port analog circuitry in the S/UNI-2488 to be reset under software control. If the ARESET_APS bit is a logic one, APS Port analog circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the APS Port analog blocks out of reset. Holding the ARESET_APS in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET_APS bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the S/UNI-2488 to be reset under software control. If the DRESET bit is a logic one, all the S/UNI-2488 digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-2488 out of reset A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 0002H: S/UNI-2488 Transmit Control Register

Bit	Type	Function	Default
Bit 15	R/W	CXUCLKO_OEB	1
Bit 14	R/W	TREQ_ADVANCE[6]	1
Bit 13	R/W	TREQ_ADVANCE[5]	0
Bit 12	R/W	TREQ_ADVANCE[4]	0
Bit 11	R/W	TREQ_ADVANCE[3]	1
Bit 10	R/W	TREQ_ADVANCE[2]	1
Bit 9	R/W	TREQ_ADVANCE[1]	0
Bit 8	R/W	TREQ_ADVANCE[0]	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TPAIS_EN	0
Bit 2	R/W	DIAGSHORT	0
Bit 1	R/W	RESYNC_EN	1
Bit 0	R/W	Reserved	1

The reserved bit 0 must be set to logic one for normal operation of the S/UNI 2488.

RESYNC_EN

The RESYNC_EN bit is used to tie the transmit frame's J0 position with the incoming APSIFP. This is to ensure a deterministic latency through the device as required for interfacing to another S/UNI-2488 or potentially a CHESS device via the APS ports. Initially, the framing is arbitrary. If RESYNC_EN is logic '1', then the S/UNI-2488 will compare the internal frame pulse location to that of the APSIFP. If they ever differ by the number of clock cycles specified in the APSIFP_THRESH[7:0] field in register 000EH, then the frame pulse will snap to the position indicated by the APSIFP input. If RESYNC_EN is logic '0', the frame pulse will internally flywheel in its current alignment. Note that even if RESYNC_EN is set low, it is still necessary to provide a proper APSIFP signal as the receive APS side is not affected by the resynchronization logic. This register bit should always be set to logic 1 for normal operation of the S/UNI-2488.

DIAGSHORT

The diagnostic short frame (DIAGSHORT) bit sets a reduced frame size. This register bit is for test purposes only.

TPAIS_EN

The Transmit Path AIS Enable bit controls the insertion of Transmit Path AIS. When logic 0, the S/UNI-2488 does not generate Transmit Path AIS. When logic 1, the S/UNI-2488 will generate Transmit Path AIS. In order for proper transmit path AIS to be generated, the TS1_PROV bit (bit 0 in register 0790H) must be set to logic 0 when TPAIS_EN is set to logic 1.

SS_CONCAT[1:0]

These register bits control the value of the SS field of the H1 concatenation pointer indication for STS-48c / STM-16c for the transmit frame.

SS_H1[1:0]

These register bits control the value of the SS field of the H1 pointer of the transmit frame.

TREQ_ADVANCE[6:0]

Reserved. This field must be left in its default configuration for normal operation of the S/UNI-2488.

CXUCLKO_OEB

This register bit is used for PMC test purposes only and must be left in its default state for the normal operation of the S/UNI-2488.

Register 0003H: S/UNI-2488 Clock Monitors

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	APSIFPCLKA	X
Bit 3	R	RCLKA	X
Bit 2	R	TCLKA	X
Bit 1	R	RFCLKA	X
Bit 0	R	TFCLKA	X

TFCLKA

The TFCLK active (TFCLKA) bit monitors for low to high transitions on the TFCLK transmit FIFO clock input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA

The RFCLK active (RFCLKA) bit monitors for low to high transitions on the RFCLK receive FIFO clock input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

RCLKA

The RCLK active (RCLKA) bit monitors for low to high transitions on the internal receive system clock (RCLK). RCLKA is set high on a rising edge of RCLK, and is set low when this register is read. This bit is not affected by RCLKEN (Register 0030H, bit 1).

TCLKA

The TCLK active (TCLKA) bit monitors for low to high transitions on the internal transmit system clock (TCLK). TCLKA is set high on a rising edge of TCLK, and is set low when this register is read. This bit is not affected by TCLKEN (Register 0038H, bit 1).

APSIFLCLKA

The APSIFPCLK active (APSIFPCLKA) bit monitors for low to high transitions on the APSIFPCLK input. APSIFPCLKA is set high on a rising edge of APSIFPCLK, and is set low when this register is read.

Register 0004H: S/UNI-2488 Master Interrupt Status #1

Bit	Type	Function	Default
Bit 15	R/W	INTE[1]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PRGMI[1]	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R	SARCI[1]	X
Bit 7	R	SVCAI[1]	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PATHRTTPI[1]	X
Bit 3	R	RHPPI[1]	X
Bit 2	R	SBERI[1]	X
Bit 1	R	SECTIONRTTPI[1]	X
Bit 0	R	RRMPI[1]	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RRMPI[1]…PRGMI[1]

The RRMPI[1] to PRGMI[1] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[1]

The interrupt enable (INTE[1]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[1], the RRMP[1]…PRGM[1] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[1], the RRMP[1]…PRGM[1] pending interrupt will not assert the interrupt (INTB) output.

Register 0005H: S/UNI-2488 Master Interrupt Status #2

Bit	Type	Function	Default
Bit 15	R/W	INTE[2]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PRGMI[2]	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SVCAI[2]	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RHPPI[2]	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	Reserved	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RHPPI[2]… PRGMI[2]

The RHPPI[2] to PRGMI[2] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[2]

The interrupt enable (INTE[2]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[2], the RRMP[2]…PRGM[2] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[2], the RRMP[2]…PRGM[2] pending interrupt will not assert the interrupt (INTB) output.

Register 0006H: S/UNI-2488 Master Interrupt Status #3

Bit	Type	Function	Default
Bit 15	R/W	INTE[3]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PRGMI[3]	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	Unused	X
Bit 8		Unused	X
Bit 7	R	SVCAI[3]	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RHPPI[3]	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	Reserved	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RHPPI[3]… PRGMI[3]

The RHPPI[3] to PRGMI[3] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[3]

The interrupt enable (INTE[3]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[3], the RRMP[3]…PRGM[3] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[3], the RRMP[3]…PRGM[3] pending interrupt will not assert the interrupt (INTB) output.

Register 0007H: S/UNI-2488 Master Interrupt Status #4

Bit	Type	Function	Default
Bit 15	R/W	INTE[4]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PRGMI[4]	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SVCAI[4]	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RHPPI[4]	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	Reserved	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RHPPI[4]… PRGMI[4]

The RHPPI[4] to PRGMI[4] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[4]

The interrupt enable (INTE[4]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[4], the RRMP[4]…PRGM[4] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[4], the RRMP[4]…PRGM[4] pending interrupt will not assert the interrupt (INTB) output.

Register 0008H: S/UNI-2488 Master Interrupt Status #5

Bit	Type	Function	Default
Bit 15	R/W	INTE[5]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	RXPHYI	X
Bit 8	R	RXSDQI	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RCFPI	X

This register is used to indicate interrupts generated from blocks associated with the receive UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

RCFPI

The RCFP interrupt event indication (RCFPI) transitions to logic 1 when a hardware interrupt event is sourced from RCFP block. This bit is cleared to logic 0 when the interrupt is cleared.

RXSDQI

The RXSDQ interrupt event indication (RXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO RXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

RXPHYI

The RXPHY interrupt event indication (RXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system UTOPIA/POS-PHY interface RXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[5]

The interrupt enable (INTE[5]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[5], the RCFPI, RXSDQI or RXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 0009H: S/UNI-2488 Master Interrupt Status #6

Bit	Type	Function	Default
Bit 15	R/W	INTE[6]	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	TXPHYI	X
Bit 8	R	TXSDQI	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TCFPI	X

This register is used to indicate interrupts generated from blocks associated with the transmit UTOPIA/POS-PHY interfaces, FIFO, and cell/frame processors.

TCFPI

The TCFP interrupt event indication (TCFPI) transitions to logic 1 when a hardware interrupt event is sourced from TCFP block. This bit is cleared to logic 0 when the interrupt is cleared.

TXSDQI

The TXSDQ interrupt event indication (TXSDQI) transitions to logic 1 when a hardware interrupt event is sourced from the receive system FIFO TXSDQ block. This bit is cleared to logic 0 when the interrupt is cleared.

TXPHYI

The RXPHY interrupt event indication (TXPHYI) transitions to logic 1 when a hardware interrupt event is sourced from the transmit system UTOPIA/POS-PHY interface TXPHY block. This bit is cleared to logic 0 when the interrupt is cleared.

INTE[6]

The interrupt enable (INTE[6]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[6], the TCFPI, TXSDQI or TXPHYI pending interrupt will not assert the interrupt (INTB) output.

Register 000AH: S/UNI-2488 Master Interrupt Status #7

Bit	Type	Function	Default
Bit 15	R/W	INTE[7]	0
Bit 14		Unused	X
Bit 13	R	RX_APSI	X
Bit 12	R	CSTRI	X
Bit 11	R	T8TE4I	X
Bit 10	R	T8TE3I	X
Bit 9	R	T8TE2I	X
Bit 8	R	T8TE1I	X
Bit 7	R	TXANALOGI	X
Bit 6	R	RXANALOGI	X
Bit 5	R	DLL_TFCLKI	X
Bit 4	R	DLL_RFCLKI	X
Bit 3	R	R8TD4I	X
Bit 2	R	R8TD3I	X
Bit 1	R	R8TD2I	X
Bit 0	R	R8TD1I	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

R8TD1I, R8TD2I, R8TD3I, R8TD4I

The R8TDxI interrupt event indication (R8TDxI) transitions to logic 1 when a hardware interrupt event is sourced from the R8TD1, R8TD2, R8TD3 or R8TD4 blocks. This bit is cleared when the interrupt is cleared.

DLL_RFCLKI, DLL_TFCLKI

The DLL_RFCLKI and DLL_TFCLKI interrupt event indications transition to logic 1 when a hardware interrupt event is sourced from the DLL_RFCLK or DLL_TFCLK, respectively. This bit is cleared when the interrupt is cleared.

RXANALOGI, TXANALOGI

The RXANALOGI and TXANALOGI interrupt event indications transition to logic 1 when a hardware interrupt event is sourced from the Rx2488 or Tx2488 blocks respectively. This bit is cleared when the interrupt is cleared.

T8TE1I, T8TE2I, T8TE3I, T8TE4I

The T8TExI interrupt event indication (T8TExI) transitions to logic 1 when a hardware interrupt event is sourced from the T8TE1, T8TE2, T8TE3 or T8TE4 blocks. This bit is cleared when the interrupt is cleared.

CSTRI

The CSTRI interrupt event indication (CSTRI) transitions to logic 1 when a hardware interrupt event is sourced from the CSTR block (analog control for the APS Port). This bit is cleared when the interrupt is cleared.

RX_APSI

The RX_APSI interrupt event indication (RX_APSI) transitions to logic 1 when one of the APS J0 character to APSIFP alignment interrupts is detected (register 0901H). This bit is cleared when the interrupt is cleared.

INTE[7]

The interrupt enable (INTE[7]) bit controls the assertion of the interrupt (INTB) output. When a logic 1 is written to INTE[7], the R8TDxI, DLL_RFCLKI, DLL_TFCLKI, RXANALOGI, TXANALOGI T8TexI or CSTRI pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[6], the R8TDxI, DLL_RFCLKI, DLL_TFCLKI, RXANALOGI, TXANALOGI T8TexI or CSTRI pending interrupt will not assert the interrupt (INTB) output.

Register 000BH: Software General Purpose (FREE[12:0]) Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	FREE[12]	0
Bit 11	R/W	FREE[11]	0
Bit 10	R/W	FREE[10]	0
Bit 9	R/W	FREE[9]	0
Bit 8	R/W	FREE[8]	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

All reserved bits in this register should be set to logic 0 for normal operation.

FREE[12:0]

General-purpose register bits. These do not affect the operation of the device in any way but will hold a value written to them.

Register 000CH: APS Input TelecomBus Synchronization Delay

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	AIJ0DLY[13]	0
Bit 12	R/W	AIJ0DLY[12]	0
Bit 11	R/W	AIJ0DLY[11]	0
Bit 10	R/W	AIJ0DLY[10]	0
Bit 9	R/W	AIJ0DLY[9]	0
Bit 8	R/W	AIJ0DLY[8]	0
Bit 7	R/W	AIJ0DLY[7]	0
Bit 6	R/W	AIJ0DLY[6]	0
Bit 5	R/W	AIJ0DLY[5]	1
Bit 4	R/W	AIJ0DLY[4]	0
Bit 3	R/W	AIJ0DLY[3]	0
Bit 2	R/W	AIJ0DLY[2]	0
Bit 1	R/W	AIJ0DLY[1]	0
Bit 0	R/W	AIJ0DLY[0]	0

This register controls the delay from the APSIFP input signal to the time when the S/UNI-2488 may safely process the J0 characters delivered by the APS Input serial data links (APSI_P/ APSI_N[4:1]).

AIJ0DLY[13:0]

The APS Input transport frame delay bits (AIJ0FP[13:0]) controls the delay, in APSIFPCLK cycles, inserted by the S/UNI-2488 before processing the J0 characters delivered by the APS Input serial data links (APSI_P/ APSI_N[4:1]). AIJ0DLY is set such that after the specified delay, all active APS Input links would have delivered the J0 character. The relationships of AIJ0FP, AIJ0DLY[13:0] and the system configuration are described in the Functional Timing section.

Valid values of AIJ0DLY[13:0] are 0000H to 25F7H.

Register 000DH: Reserved

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register must be set to its default value for normal operation.

Register 000EH: S/UNI-2488 Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	APSIFP_THRESH[7]	0
Bit 14	R/W	APSIFP_THRESH[6]	0
Bit 13	R/W	APSIFP_THRESH[5]	0
Bit 12	R/W	APSIFP_THRESH[4]	1
Bit 11	R/W	APSIFP_THRESH[3]	0
Bit 10	R/W	APSIFP_THRESH[2]	0
Bit 9	R/W	APSIFP_THRESH[1]	0
Bit 8	R/W	APSIFP_THRESH[0]	0
Bit 7	R/W	LOCK0	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TLD_VAL	0
Bit 2	R/W	TSLD_VAL	0
Bit 1	R/W	DS	0
Bit 0	R/W	DD	0

The reserved bit in this register should be set to logic 0 for normal operation.

DD

The Disable Descrambling (DD) bit is used to disable SONET descrambling performed by the RRMP block. When set to logic 1, SONET descrambling is disabled. When set to logic 0, SONET descrambling is enabled. For normal operation, this bit should be set to logic zero. Note that due to the high speed integrated analog front end, there is a minimum transition density that must be maintained. This device is intended for use with an incoming data stream that has been scrambled as specified by Bellcore GR-253 Core to reduce the probability of extended periods without transitions.

DS

The Disable Scrambling (DS) bit is used to disable SONET scrambling performed by the TRMP block. When set to logic 1, SONET scrambling is disabled. When set to logic 0, SONET scrambling is enabled. For normal operation, this bit should be set to logic zero.

TSLD_VAL

The TSLD value (TSLD_VAL) bit is used to set the value optionally inserted into the section DCC (D1-D3) in the transmit data stream as configured using the TSLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted.

TLD_VAL

The TLD value (TLD_VAL) bit is used to set the value optionally inserted into the line DCC (D4-D12) in the transmit data stream as configured using the TLDEN bit in the TRMP Configuration register. When set to logic 1, ones are inserted. When set to logic 0, zeros are inserted.

LOCK0

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration (as specified by the ATM Forum). When set to logic 1, the H1 H2 pointer value is set at 0.

APSIFP_THRESH[7:0]

APSIFP_THRESH determines the amount of slack allowed in the comparison between the internal transmit frame pulse and the input APSIFP before the internal frame pulse is forced to match the APSIFP. This value is only used when RESYNC_EN in register 0002H is logic 1. The minimum value for APSIFP_THRESH is 4. This field should normally be set to the minimum value (4) to reduce the probability of synchronization problems with APSIFP.

Register 000FH: S/UNI-2488 Identification Register

Bit	Type	Function	Default
Bit 15	R	CHIPID[15]	0
Bit 14	R	CHIPID[14]	1
Bit 13	R	CHIPID[13]	0
Bit 12	R	CHIPID[12]	1
Bit 11	R	CHIPID[11]	0
Bit 10	R	CHIPID[10]	0
Bit 9	R	CHIPID[9]	1
Bit 8	R	CHIPID[8]	1
Bit 7	R	CHIPID[7]	1
Bit 6	R	CHIPID[6]	0
Bit 5	R	CHIPID[5]	0
Bit 4	R	CHIPID[4]	0
Bit 3	R	CHIPID[3]	0
Bit 2	R	CHIPID[2]	0
Bit 1	R	CHIPID[1]	0
Bit 0	R	CHIPID[0]	1

CHIPID[15:0]

The CHIPID[15:0] is set to 5381H to identify the PM5381 S/UNI-2488.

Register 0010H: Rx2488 Analog Interrupt Status

Bit	Type	Function	Default
Bit 15	R	CRU_CLOCK	1
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PRBS_SYNC_I	0
Bit 4	R	PRBS_ERR_I	0
Bit 3	R	FIFO_ERROR_I	0
Bit 2	R	LOS_I	0
Bit 1	R	DOOL_I	0
Bit 0	R	ROOL_I	0

ROOL_I

The recovered reference out of lock status (ROOL_I is logic 1) indicates that the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. At startup, ROOL_I may remain at logic 1 for several hundred milliseconds while the PLL obtains lock. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

DOOL_I

The recovered data out of lock status indicates that the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOL_I is a logic one if the divided down recovered clock frequency is not within ±1000 ppm of the REFCLK frequency or if no transitions have occurred on the RXD input for more than LOS_COUNT[4:0] bits. Note: recall that LOS_COUNT is specified as the upper 5 bits of a 9 bit number and has an accuracy of ±15. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

If the optical signal is lost, the SD input pin should be deasserted. This will cause the CRU into training mode where it will lock onto the REFCLK input. However, the state-machine which controls DOOL_I will continue to search for lock to data and is expected to toggle during this time. When the optical signal is restored and the SD input pin is asserted, the CRU will once again attempt to lock onto the data signal. Once lock is found, DOOL_I will stop toggling and DOOLV can be examined to verify the CRU is in fact locked to the data.

LOS_I

The loss of signal status indicates that the receive signal is lost or that at least LOS_COUNT consecutive ones or zeros have been received. LOS_I is a logic zero if the SDI input is high or less than LOS_COUNT consecutive ones or zeros have been received. LOS_I is a logic one if the SDI input is low or LOS_COUNT consecutive ones or zeros have been received. Note: recall that LOS_COUNT is specified as the upper 5 bits of a 9 bit number and has an accuracy of ±15. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

FIFO_ERROR_I

The FIFO Error bit provides a status indication of an underflow or overflow condition in the Rx data elastic store. When FIFO_ERROR_I is set to '1', the data in the elastic store has been corrupted and invalid data has been read from the FIFO. If WCIMODE in register 0001H is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PRBS_ERR_I

The PRBS Bit Error bit provides a status indication that a bit error has been detected in the comparison between the incoming data and the locally generated data. The PRBS_ERR_I is set high when the monitor is in the synchronized state and when an error in a PRBS word is detected. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PRBS_SYNC_I

The PRBS Synchronization bit indicates that a change in the status of the PRBS Monitor has occurred. The comparison between the incoming data and the internal PRBS^23 pattern is generated locally. The PRBS_SYNC_I is set high when the monitor is in the synchronized state and has received two consecutive erroneous words forcing the PRBS monitor to resynchronize. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

CRU_CLOCK

The CRU_CLOCK status bit monitors the state of the CRU clock. Each time Register 0010H is read, the sampling register is reset. The CRU_CLOCK is set high when the CRU clock transitions from low to high at least once. The CRU_CLOCK is reset low after Register 0010H is read and will remain low if no transitions occur on the CRU clock.

Register 0011H: Rx2488 Analog Interrupt Control

Bit	Type	Function	Default
Bit 15	R/W	SD_DISABLE	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PRBS_SYNC_EN	0
Bit 4	R/W	PRBS_ERR_EN	0
Bit 3	R/W	FIFO_ERROR_EN	0
Bit 2	R/W	LOS_EN	0
Bit 1	R/W	DOOL_EN	0
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit connects the ROOL_I status bit to the INT pin of the RCS_2488. When ROOL_EN is set to logic one, an interrupt on the INT pin is generated upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

DOOL_EN

The Data Out Of Lock Enable bit connects the DOOL_I status bit to the INT pin of the RCS_2488. When DOOL_EN is set to logic one, an interrupt on the INT is generated upon assertion of the DOOL_I register bit. When DOOL_EN is set low, a change in the DOOL_I status does not generate an interrupt.

LOS_EN

The Loss of Signal Enable bit connects the LOS_I status bit to the INT pin of the RCS_2488. When LOS_EN is set to logic one, an interrupt on the INT is generated upon assertion of the LOS_I register bit. When LOS_EN is set low, a change in the LOS_I status does not generate an interrupt.

FIFO_ERROR_EN

The FIFO Error Enable bit connects the FIFO_ERROR_I status bit to the INT pin of the RCS_2488. When FIFO_ERROR_EN is set to logic one, an interrupt on the INT is generated upon assertion of the FIFO_ERROR_I register bit. When FIFO_ERROR_EN is set low, a change in the FIFO_ERROR_I status does not generate an interrupt.

PRBS_ERR_EN

The PRBS Error Enable bit connects the PRBS_ERR_I status bit to the INT pin of the RCS_2488. When PRBS_ERR_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_ERR_I register bit. When PRBS_ERR_EN is set low, a change in the PRBS_ERR_I status does not generate an interrupt.

PRBS_SYNC_EN

The PRBS Synchronized Enable bit connects the PRBS_SYNC_I status bit to the INT pin of the RCS_2488. When PRBS_SYNC_EN is set to logic one, an interrupt on the INT is generated upon assertion of the PRBS_SYNC_I register bit. When PRBS_SYNC_EN is set low, a change in the PRBS_SYNC_I status does not generate an interrupt.

SD_DISABLE

The Signal Detect Disable bit controls the operation of the SD input pin. When SD_DISABLE is set to a logic one the SD input will be ignored and the internal signal will be forced to the active state and all down stream blocks will operate normally. When SD_DISABLE is set to logic zero the internal signal follows the state of the SD input pin and the state of SD_INV bit.

Register 0012H: Rx2488 Analog CRU Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved1	0
Bit 14	R/W	CRU_RESET	0
Bit 13	R/W	Reserved1	0
Bit 12	R/W	RX2488_ENABLE	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	LOCK_TO_REF	0
Bit 9	R/W	IDDQ_ENABLE	0
Bit 8	R/W	Reserved0	0
Bit 7	R/W	SDLE	0
Bit 6	R/W	CRU_MODE[6]	0
Bit 5	R/W	CRU_MODE[5]	1
Bit 4	R/W	CRU_MODE[4]	0
Bit 3	R/W	CRU_MODE[3]	1
Bit 2	R/W	CRU_MODE[2]	0
Bit 1	R/W	CRU_MODE[1]	1
Bit 0	R/W	CRU_MODE[0]	1

CRU_MODE[6:0]

Note: This field should be set to 2Bh for optimal operation.

The CRU Mode control bits are used to place the CRU in one of the following modes:

Table 9 CRU Mode Control

Mode Bits	Description
6:5	Bandwidth Selection via Internal Loop Filter Modes: 00 = Reserved 01 = 2.5 K ohm (default, recommended) 10 = 5.0 K ohm 11 = Reserved
4:3	Narrowbanding Mode: This field selects the current source for Narrowbanding of the CRU's oscillator. 00 – Reserved 01 – CSU Narrowbanding (default) 10 – Reserved 11 – Reserved
2	Override Lock to Reference. When high, forces the CRU to remain locked to the data. When low, the CRU state machine controls the CRU.
1:0	Set to 01 or 11 (equivalent) for OC48 operation. All other settings are reserved.

SDLE

The Serial Diagnostic Loopback Enable (SDLE) bit, when set to '1', loops the data from the transmit line PISO to the receive side CRU/SIPO. In the loopback mode, the CRU locks to the loopback data.

Reserved0

The Reserved0 bit must be set to logic 0 for normal operation.

IDDQ_ENABLE

The IDDQ_ENABLE bit activates the IDDQ (Quiescent Current) test mode. When set to '1', all RX2488 Analog Circuits are disabled and the IDDQ of the digital circuits can be measured. When this bit is set to '0', all RX2488 analog circuits operate normally. This bit is only used during production testing and should be set to logic 0 for normal operation.

LOCK_TO_REF

The Lock to Reference bit controls the operation of the CRU state machine. When LOCK_TO_REF is set to logic one the CRU state machine will hold the CRU in the Lock-to-Reference state. When the CRU is reset to logic zero the CRU state machine operates

RX2488_ENABLE

The 2.488GHz Receiver Enable bit provides a global power down of the RX2488 Analog Block Circuit. When set to '0', this bit forces the RX2488 to a low power state and functionality is disabled. When set to '1', the RX2488 operates in the normal mode of operation.

Reserved1

Both the Reserved1 bits must be set to logic 1 for optimal operation.

CRU_RESET

The Clock Recovery Unit Reset bit provides a complete reset of the CRU Analog Block Circuit. When set to '1', this bit forces the CRU to a known initial state. While the bit is set to '1', the functionality of the block is disabled. When set to '0', the CRU operates in the normal mode. This bit is not self-clearing. Therefore a '0' must be written to the bit to remove the reset condition.

Register 0013H: Rx2488 Analog CRU Clock Training Configuration and Status

Bit	Type	Function	Default
Bit 15	R/W	LOS_COUNT[4]	0
Bit 14	R/W	LOS_COUNT[3]	1
Bit 13	R/W	LOS_COUNT[2]	0
Bit 12	R/W	LOS_COUNT[1]	0
Bit 11	R/W	LOS_COUNT[0]	0
Bit 10	R/W	LOSEN	1
Bit 9	R/W	LINE_LOOP_BACK	0
Bit 8	R/W	SDI_INV	0
Bit 7	R/W	INV_DATA	0
Bit 6	R	DOOLV	X
Bit 5	R	ROOLV	X
Bit 4	R	TRAIN	X
Bit 3	R/W	OUTLOCK	1
Bit 2	R/W	OUTDATA	1
Bit 1	R/W	INLOCK	1
Bit 0	R/W	INDATA	1

INDATA

The clock difference detector DATA TO LOCK transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the LOCKED TO REFERENCE state to the DATA IN RANGE state. When INDATA is a logic zero, the clock difference detector must pass once before the state transition can occur. When INDATA is a logic one, the clock difference detector must pass 39 consecutive times before the state transition can occur.

INLOCK

The clock difference detector LOCKING TO DATA transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the DATA IN RANGE state to the LOCKED TO DATA state. When INLOCK is a logic zero, the clock difference detector must pass once before the state transition can occur. When INLOCK is a logic one, the clock difference detector must pass 39 consecutive times before the state transition can occur.

OUTDATA

The clock difference detector DROPPING OUT OF DATA transition configuration bit determines the number of times the clock difference detector must fail before the CRU control state machine transitions from the DATA IN RANGE state to the LOCKED TO REFERENCE state. When OUTDATA is a logic zero, the clock difference detector must fail once before the state transition can take place. When OUTDATA is a logic one, the clock difference detector must fail 39 consecutive times before the state transition can occur.

Note: This bit is recommended to be set to '1' for robust operation of the CRU/state machine in a noisy environment.

OUTLOCK

The clock difference detector DROPPING OUT OF LOCK transition configuration bit determines the number of times the clock difference detector must pass before the CRU control state machine transitions from the LOCKED TO DATA state to the DATA IN RANGE state. When OUTLOCK is a logic zero, the clock difference detector must fail once before the state transition can occur. When OUTLOCK is a logic one, the clock difference detector must fail 39 consecutive times before the state transition can occur.

Note: This bit is recommended to be set to '1' for robust operation of the CRU/state machine in a noisy environment.

TRAIN

The CRU reference training status indicates if the CRU is locking to the reference clock or the locking to the receive data. TRAIN is a logic zero if the CRU is locking or locked to the reference clock. TRAIN is a logic one if the CRU is locking or locked to the receive data. TRAIN is invalid if the CRU is not used.

When the optical signal is lost, the SD input pin is expected to be deasserted. In this state, the CRU will be forced into training mode and will lock to REFCLK. However, the state-machine which controls the TRAIN register bit will continue looking at the data and will occasionally change states. However, the CRU will remain locked to REFCLK until SD is once again asserted.

ROOLV

The recovered reference out of lock status indicates that the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. At startup, ROOLV may remain at logic 1 for several hundred milliseconds while the PLL obtains lock.

DOOLV

The recovered data out of lock status indicates that the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is logic one if the divided down recovered clock frequency is not within approximately 488ppm of the REFCLK frequency or if LOS_I interrupt has been triggered.

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the received data. When INV_DATA is set to '1', the polarity of the RXD_P/RXD_N input pins invert. When INV_DATA is set to '0', the RXD_P/RXD_N inputs operate normally.

SDI_INV

The Signal Detect Inversion INV_SD controls the polarity of the SD input pin. When INV_SD is set to '1' the polarity of the SD input pin is inverted. When INV_SD is set to '0' the polarity of the SD input remains unchanged.

LINE_LOOP_BACK

The line loop back bit selects the source of the timing for the parallel data output of the receive FIFO. When the LINE_LOOP_BACK is set to logic one, the output data of this FIFO is timed to the clock of the S/UNI-2488 transmitter. Either the S/UNI-2488 or the upstream device must be in loop-timed mode for the line-loopback mode to work properly. When reset to logic zero, the receive FIFO output data is timed using either the receive-side-CRU clock.

For chip-level line loopback, this LINE_LOOP_BACK bit and the SLLE register bit in the Tx2488 Analog Control/Status register (register 0020H) must be set to logic 1. As well, the CSU_MODE[7] register bit in the Tx2488 ABC Control register (register 0021H) must be set to logic 0.

LOSEN

The loss of signal enable bit controls the signal detection logic. The CRU uses the LOS detector along with the clock difference detector to determine if the CRU is locked to data. When LOSEN is set to logic one, the incoming signal is monitored for 1/0 transitions as determined by LOS_COUNT[4:0] register bits. If LOSEN is reset to logic zero, the 1/0 transition detector is disabled. Note: recall that LOS_COUNT is specified as the upper 5 bits of an 11 bit number and has an accuracy of ±15.

LOS_COUNT[4:0]

The Loss of Signal 1's/0's transition detector count field sets the value for the number of consecutive all-zeros or all-ones pattern that will force the CRU out of the LOCK TO DATA state. Each bit in the binary count represents sixteen ones or zeros in the pattern. (i.e. LOS_COUNT has an accuracy of ±15). For example, to set the consecutive all-ones or all-zeros pattern to 128 the LOS_COUNT should be set to "01000"b. The default value for this field is 128.

Register 0014H: Rx2488 Analog PRBS Control

Bit	Type	Function	Default
Bit 15	R	PRBS_ERR_CNT[7]	0
Bit 14	R	PRBS_ERR_CNT[6]	0
Bit 13	R	PRBS_ERR_CNT[5]	0
Bit 12	R	PRBS_ERR_CNT[4]	0
Bit 11	R	PRBS_ERR_CNT[3]	0
Bit 10	R	PRBS_ERR_CNT[2]	0
Bit 9	R	PRBS_ERR_CNT[1]	0
Bit 8	R	PRBS_ERR_CNT[0]	0
Bit 7	R/W	CLEAR_ERR_CNT	0
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	SYNC_STAT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	PRBS_ENABLE	0
Bit 0		Unused	X

PRBS_ENABLE

This bit enables the PRBS monitor of the RCS_2488. When low, the PRBS monitor is disabled. When high, the PRBS monitor is enabled and will check the incoming data stream for errors. The monitored PRBS is based on the $X^{23}+X^{18}+1$ polynomial (PRBS^23) implemented by a Linear Feedback Shift Register (LFSR).

Reserved

This bit must be set to logic 0 for proper operation.

SYNC_STAT

The Monitor Synchronization Status bit reflects the state of the monitor's state machine. When SYNC_STAT is set low, the monitor has lost synchronization. When SYNC_STAT is high, the monitor is in synchronization.

CLEAR_ERR_CNT

The Clear Error Count bit clears the PRBS word error count value. When a logic 1 is written to this bit, the PRBS word error count register is reset to zero. When set to logic 0, the counter operates normally. This bit should be written to 1 then written 0 to perform the clear counter operation.

PRBS_ERR_CNT[7:0]

The ERR_CNT[7:0] register is the number of errors in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is triggered by writing to the CLEAR_ERR_CNT bit or by writing to register 0000H, the Global Performance Monitor Update Register. PRBS_ERR_CNT[7:0] is cleared by the CLEAR_ERR_CNT bit in this register. The actual PRBS error counter is cleared immediately after a logic 1 is written to the CLEAR_ERR_CNT bit. The error counter will not wrap around after reaching FFh. The error counter will saturate to FFh.

Register 0015H: Rx2488 Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

These bits must be set to their default value for proper operation.

Register 0020H: Tx2488 Analog Control/Status

Bit	Type	Function	Default
Bit 15	R	ROOL_I	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PD_MON	X
Bit 11	R/W	Reserved1	1
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	TX2488_MODE[2]	0
Bit 7	R/W	TX2488_MODE[1]	0
Bit 6	R/W	TX2488_MODE[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	SLLE	0
Bit 2	R/W	INV_DATA	0
Bit 1	R/W	Unused	0
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit enables the ROOL_I interrupt to assert the INTB pin. When ROOL_EN is set to logic one, an interrupt on the INTB is generated upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the transmitter data. When INV_DATA is set to ‘1’, the polarity of the TXD_P/TXD_N input pins are inverted. When INV_DATA is set to ‘0’, the TXD_P/TXD_N inputs operate normally.

SLLE

The serial line loop-back enable (SLLE) bit loops the recovered data and clock to the transmit output. When this bit is set to logic 1, data from the 2488 receiver is input into the PISO and data from the SONET transmit processor is ignored.

Note: The CSU_MODE[7] bit of the CSU Control register must be set to logic 0 when SLLE is enabled.

For chip-level line loopback, the LINE_LOOP_BACK bit in the Rx2488 Analog CRU Clock Training Configuration and Status register (register 0013H) and the SLLE register bit in the Tx2488 Analog Control/Status register (register 0020H) must be set to logic 1. As well, the CSU_MODE[7] register bit in the Tx2488 ABC Control register (register 0021H) must be set to logic 0.

TX2488_MODE[2:0]

The TX2488 Mode control bits are used to place the TX2488-CML in one of the following operating modes:

Table 10 TX2488 Mode Control

TX2488_MODE [2:0] Value	Description
111	Reserved
1XX	Reserved
0XX	When MODE[2] is set low, the data from PISO-2488 is used as the input to the transmitter. The default is to use the PISO-2488 as the input.
X11	Reserved
X10	Reserved
X01	When the configuration bits MODE0 and MODE1 are set respectively high and low, limited-swing AC coupling suitable for the Lucent T48, Hitachi HTR6540, or HP HFCT-53D5 ODL transmitters is used. In this mode a 16mA bias current is generated in the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current produces a differential amplitude suitable for the Lucent T48, Hitachi HTR6540 or HP HFCT-53D5 (using double termination).
X00	When the configuration bits MODE1 and MODE0 are set low, AC coupling suitable for PECL compliant ODL transmitters (e.g. Sumitomo SDM7128-XC or Sumitomo SCM6028-GL) is used. In this mode a 30.5mA bias current is generated in the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current is adequate to produce a valid differential PECL amplitude with double termination.

Reserved1

The Reserved1 bit must be set to logic 1 for proper operation.

PD_MON

The Phase Detector Monitor bit indicates the state of the Phase Detector state machine. When PD_MON is logic 0 the CSU state machine is in the Phase & Frequency Detector state. When PD_MON is set to logic 1 the CSU state machine is in the Hogge-II Phase Detector state.

When in the Hogge-II Phase Detector state, the CSU has locked to the reference.

ROOL_I

The transmit recovered reference out of lock status indicates that the clock synthesis phase locked loop is unable to lock to the reference clock on REFCLK. At startup, ROOL_I may remain at logic 1 for several hundred milliseconds while the PLL obtains lock. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

The PD_MON register bit can be used to reveal whether the CSU is locked to the reference.

Note: When ROOL_I is set and indicates that the CSU has lost lock to the reference clock, then once the reference is restored, the CSU must be reset (using CSU_RESET in register 0x0021) before normal operation can begin.

Register 0021H: TX2488 ABC Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	PISO_RESET	0
Bit 13	R/W	CSU_RESET	0
Bit 12	R/W	RX_REF ENABLE	1
Bit 11	R/W	TX2488_ENABLE	1
Bit 10	R/W	C2C_ENABLE	1
Bit 9	R/W	Reserved1	1
Bit 8	R/W	IDDQ_ENABLE	0
Bit 7	R/W	CSU_MODE[7]	1
Bit 6	R/W	CSU_MODE[6]	1
Bit 5	R/W	CSU_MODE[5]	1
Bit 4	R/W	CSU_MODE[4]	0
Bit 3	R/W	CSU_MODE[3]	0
Bit 2	R/W	CSU_MODE[2]	0
Bit 1	R/W	CSU_MODE[1]	0
Bit 0	R/W	CSU_MODE[0]	0

CSU_MODE[7:0]

The CSU Mode control bits are used to place the CSU in one of the following operating modes:

Table 11 CSU Mode Control

Mode Bits	Description
7	CSU Input reference clock selection bit: 0 – CRU Recovered Clock (loop-time) 1 – External Reference Clock (lock to reference)
6:5	Loop filter resistor select. They allow selection of various loop filter parameters that affect bandwidth. Selection modes are: Bits 6:5 Resistor Value 11 2 x 10kΩ (Default) 10 2 x 12.5kΩ (increases bandwidth of CSU by 25% compared to default) 01 Reserved 00 2 x 2.5kΩ (reduces bandwidth for loop-timed operation) Note: The optimum resistor for PFD mode is 12.5kΩ. The optimum resistor for Hogge-II mode is 10kΩ. The optimum resistor for loop-timed operation is 2.5kΩ. See CSU_MODE[2] register bit description also.
4	Reserved

Mode Bits	Description
3	Reserved
2	Selects the type of phase detector used in the PLL after the frequency lock is achieved. 0 - Phase & Frequency Detector (a.k.a. PFD) (Default) 1 - Hogge-II Phase Detector. NOTE: PFD is the default mode for start-up. Once the frequency lock is achieved, switching to Hogge mode will reduce the intrinsic jitter by about 10%. In Hogge-II mode the resistor value must be 10KΩ. If after frequency lock, the PFD mode is continued to be used for normal operation (10% more jitter), the optimum resistor for PFD is 12.5KΩ. During start-up either 12.5KΩ or 10KΩ can be used with PFD. (For resistor value selections, see CSU_MODE[6:5])
1:0	Reserved

For a loop timed mode of operation, the CSUMODE[7] register bit must be set to logic 0. In this mode of operation, the transmitter timing is derived from the recovered clock. The S/UNI-2488 cannot be configured for loop time operation if operating with a mate device unless both received clocks are frequency locked.

IDDQ_ENABLE

The IDDQ_ENABLE bit activates the IDDQ (Quiescent Current) test mode. When set to '1', all TX2488 Analog Circuits are disabled and the IDDQ of the digital circuits can be measured. When this bit is set to '0', all TX2488 analog circuits operate normally. This bit is only used during production testing.

Reserved1:

The Reserved1 bit must be set to logic1 for proper operation.C2C_ENABLE

The CML to CMOS Interface Module Enable provides a global power down of the CML2CMOS-RX2488 Analog Block Circuit. When set to '0', this bit forces the CML to CMOS Interface Module to a low power state and functionality is disabled. When set to '1', the CML to CMOS Interface Module operates in the normal mode of operation.

TX2488_ENABLE

The 2.488GHz Transmitter Enable provides a global power down of the TX2488 Analog Block Circuit. When set to '0', this bit forces the TX2488 to a low power state and functionality is disabled. When set to '1', the TX2488 operates in the normal mode of operation.

RX_REF_ENABLE

The PECL Reference Clock Receiver Enable provides a global power down of the RX2488-PECL Analog Block Circuitry used for reference clock input. When set to '0', this bit forces the block to a low power state and functionality is disabled. When set to '1', the block operates in the normal mode of operation.

CSU_RESET

The Clock Source Unit Reset provides a complete reset of the CSU2488 Analog Block Circuit. When set to '1', this bit forces the CSU to a known initial state. While the bit is set to '1', the functionality of the block is disabled. When set to '0', the CSU operates in the normal mode of operation. This bit is not self-clearing. Therefore a '0' must be written to the bit to remove the reset condition.

When asserted, CSU_RESET must be set to logic 1 for at least 2ms.

PISO_RESET

The PISO Reset provides a complete reset of the PISO-2488 Analog Block Circuit. When set to '1', this bit forces the PISO to a known initial state. While the bit is set to '1', the functionality of the block is disabled. When set to '0', the PISO operates in the normal mode of operation. This bit is not self-clearing. Therefore a '0' must written to the bit to remove the reset condition.

Reserved

This bit must be set to logic 0 for proper operation.

Register 0022H: TX2488 Pattern Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits should be set to logic 0 for normal operation.

Register 0030H: SRLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISFRM	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RCLKEN	0
Bit 0		Unused	

The Clock Configuration Register is provided at SRLI r/w address 0030H.
All Reserved bits must be set to their default values for proper operation.

RCLKEN

The receive clock enable (RCLKEN) bit controls the gating of the RCLK output clock. When RCLKEN is set to logic 1, the RCLK output clock operates normally. When RCLKEN is set to logic 0, the RCLK output clock is held low.

DISFRM

The disable framing (DISFRM) bit disables the framing algorithm and resets the bit alignment on the RD[15:0] input bus to none. When DISFRM is set to logic 1, the framing algorithm is disabled and the bit alignment is reset to none. When DISFRM is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

Register 0031H: SRLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	PGMRCLKSEL	0
Bit 0	R/W	PGMRCLKEN	0

The PGM Clock Configuration Register is provided at SRLI r/w address 0031H.
All Reserved bits must be set to their default values for proper operation.

PGMRCLKEN

The programmable receive clock enable (PGMRCLKEN) bit controls the gating of the PGMRCLK output clock. When PGMRCLKEN is set to logic one, the PGMRCLK output clock operates normally. When PGMRCLKEN is set to logic zero, the PGMRCLK output clock is held low.

PGMRCLKSEL

The programmable receive clock frequency selection (PGMRCLKSEL) bit selects the frequency of the PGMRCLK output clock. When PGMRCLKSEL is set high, PGMRCLK is a nominal 8 KHz clock. When PGMRCLKSEL is set to logic zero, PGMRCLK is a nominal 19.44 MHz clock.

Register 0038H: STLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TCLKEN	0
Bit 0	R/W	Reserved1	0

Reserved1 **This register bit must be set to logic 1 for normal operation.**

TCLKEN

The transmit clock enable (TCLKEN) bit controls the gating of the TCLK output clock. When TCLKEN is set to logic 1, the TCLK output operates normally. When TCLKEN is set to logic 0, the TCLK output is held low.

Reserved

The Reserved bits must be left in their default values for proper operation.

Register 0039H: STLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	PGMTCLKSEL	0
Bit 0	R/W	PGMTCLKEN	0

All Reserved bits must be set to their default values for proper operation.

PGMTCLKEN

The programmable transmit clock enable (PGMTCLKEN) bit controls the gating of the PGMTCLK output clock. When PGMTCLKEN is set to logic one, the PGMTCLK output clock operates normally. When PGMTCLKEN is set to logic zero, the PGMTCLK output clock is held low.

PGMTCLKSEL

The programmable transmit clock frequency selection (PGMTCLKSEL) bit selects the frequency of the PGMTCLK output clock. When PGMTCLKSEL is set high, PGMTCLK is a nominal 8 KHz clock. When PGMTCLKSEL is set to logic zero, PGMTCLK is a nominal 19.44 MHz clock.

Register 0040H: RRMP Configuration
Register 0050H: RRMP Aux2 Configuration
Register 0060H: RRMP Aux3 Configuration
Register 0070H: RRMP Aux4 Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14		Unused	
Bit 13		Reserved	0
Bit 12	R/W	LREIBLK	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

All Reserved bits must be set to their default values for proper operation.

FOOF

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re-framing in an upstream frame detector.

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). This algorithm examines only 12 framing bits; all other framing bits are ignored. When ALGO2 is set to logic 0, the framing patterns consist of 12 A1 framing bytes and 12 A2 framing bytes.

LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LREIBLK

The line REI block (LREIBLK) bit controls the extraction of line REI errors from the M1 byte. When LREIBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

BUSY

The BUSY (BUSY) bit reports the status of the transfer of section BIP, line BIP and line REI error counters to the holding registers. BUSY is set to logic 1 upon writing to the holding register addresses or by a low to high transition on LCK. BUSY is set to logic 0 upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

Register 0041H: RRMP Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit errors in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Register 0042H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE

The interrupt enable bits control the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0043H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R	LREIEI	X
Bit 9	R	LBIPEI	X
Bit 8	R	SBIPEI	X
Bit 7	R	COSSMI	X
Bit 6	R	COAPSI	X
Bit 5	R	APSBFI	X
Bit 4	R	LRDII	X
Bit 3	R	LAISI	X
Bit 2	R	LOSI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate new APS bytes. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0044H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Register 0045H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disabled, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

Register 0046H: RRMP AIS Enable
Register 0056H: RRMP Aux2 AIS Enable
Register 0066H: RRMP Aux3 AIS Enable
Register 0076H: RRMP Aux4 AIS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	K2AIS	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

RSOHAISEN

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when a LOF or LOS condition exists. When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLOHAISEN

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when a LOF or LOS condition exists. When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when a LOF or LOS condition exists and when the SARC block is configured for this alarm consequential action. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

K2AIS

The K2 line AIS (K2AIS) bit restricts line AIS to the K2 byte. When K2AIS is set to logic 1, line AIS is only inserted in bits 6, 7 and 8 of the K2 byte. When K2AIS is set to logic 0, line AIS is inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes).

Register 0047H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H).

Register 0048H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Register 0049H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H).

Register 004AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 004BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LREIE[23:16]	XX

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H).

Register 0080H: TRMP Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	TLDEN	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	TSLDEN	0
Bit 3	R/W	TRACEEN	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

All Reserved bits must be set to their default values for proper operation.

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 4. When A1A2EN is set to logic 0, the framing bytes are not inserted.

For normal operation, the A1A2EN bits in the TRMP Aux2 Configuration register, the TRMP Aux3 Configuration register and the TRMP Aux4 Configuration register must be set to the same value as the A1A2EN bit.

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 0, the Z0 bytes are defined according to BELLCORE. The Z0 bytes are located in STS-1/STM-0 #2 to #48. **Z0DEF must be set to logic 0 for proper operation.**

For normal operation, the Z0DEF bits in the TRMP Aux2 Configuration register, the TRMP Aux3 Configuration register and the TRMP Aux4 Configuration register must be set to the same value as the Z0DEF bit.

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 4. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

For normal operation, the J0Z0INCEN bits in the TRMP Aux2 Configuration register, the TRMP Aux3 Configuration register and the TRMP Aux4 Configuration register must be set to the same value as the J0Z0INCEN bit.

TRACEEN

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the Section TTTP block is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 4. When TRACEEN is set to logic 0, the section trace from the J0[7:0] input port is not inserted.

TSLDEN

The TSLD enable (TSLDEN) bit controls the insertion of section or line DCC in the data stream. When TSLDEN is set to logic 1, the S/UNI-2488 inserts all ones or all zeros as selected using the TSLD_VAL bit in the S/UNI-2488 Diagnostics register (000EH) into the D1-D3 bytes or D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When TSLDEN is set to logic 0, the section or line DCC is not inserted.

TLDEN

The TLD enable (TLDEN) bit controls the insertion of line DCC in the data stream. When TLDEN is set to logic 1, the S/UNI-2488 inserts all ones or all zeros as selected using the TLD_VAL bit in the S/UNI-2488 Diagnostics register (000EH) into in the D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When TLDEN is set to logic 0, line DCC is not inserted.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

LREIEN

The functionality of the LREIEN register bit has been replaced with the TREIINS register bit in register 0903H. LREIEN must be left in its default state of logic 1 for proper operation.

LREIBLK

The line REI block error (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame).

Register 0081H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11		Unused	
Bit 10	R/W	E2REGEN	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	S1REGEN	0
Bit 6	R/W	D4D12REGEN	0
Bit 5	R/W	K1K2REGEN	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN	1
Bit 0	R/W	J0REGEN	1

J0REGEN

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the TRMP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 4. When J0REGEN is set to logic 0, the section trace from the TRMP Transmit J0 and Z0 register is not inserted.

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 4. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

E1REGEN

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the TRMP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When E1REGEN is set to logic 0, the section order wire from the TRMP Transmit E1 and F1 register is not inserted.

F1REGEN

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the TRMP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When F1REGEN is set to logic 0, the section user channel from the TRMP Transmit E1 and F1 register is not inserted.

D1D3REGEN

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When D1D3REGEN is set to logic 0, the section DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

K1K2REGEN

The K1K2 register enable (K1K2REGEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGEN is set to logic 1, the APS bytes from the TRMP Transmit K1 and K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When K1K2REGEN is set to logic 0, the APS bytes from the TRMP Transmit K1 and K2 register are not inserted.

D4D12REGEN

The D4 to D12 register enable (D4D12REGEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGEN is set to logic 1, the line DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 4. When D4D12REGEN is set to logic 0, the line DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

S1REGEN

The S1 register enable (S1REGEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGEN is set to logic 1, the SSM from the TRMP Transmit S1 and Z1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 4. When S1REGEN is set to logic 0, the SSM from the TRMP Transmit S1 and Z1 register is not inserted.

Z1REGEN

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 4. When Z1REGEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGEN

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 4. When Z2REGEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

E2REGEN

The E2 register enable (E2REGEN) bit controls the insertion of line order wire in the data stream. When E2REGEN is set to logic 1, the line order wire from the TRMP Transmit Z2 and E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 4. When E2REGEN is set to logic 0, the line order wire from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 4. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enabled via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enabled via the NATIONALEN register bit.

UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 4. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit.

Register 0082H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	B2DISABLE	0
Bit 7	R/W	B1DISABLE	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

B1MASKEN

The B1 mask enable (B1MASKEN) bit selects the use of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is XOR with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

B2MASKEN

The B2 mask enable (B2MASKEN) bit selects the use of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are XOR with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

HMASKEN

The H1/H2 mask enable (HMASKEN) bit selects the use of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are XOR with the path payload pointer bytes). When HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the path payload pointer bytes.

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes of the STS-12/STM-4 #1 according to the priority of Table 4. When A1ERR is set to logic 0, no framing errors are introduced.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling.

Note, this bit must be set to the same value as the other LAISINS bits in the TRMP Aux2 Error Insertion, TRMP Aux3 Error Insertion and TRMP Aux4 Error Insertion registers.

LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zeros (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

Note, this bit must be set to the same value as the other LOSINS bits in the TRMP Aux2 Error Insertion, TRMP Aux3 Error Insertion and TRMP Aux4 Error Insertion registers.

B1DISABLE

The B1 disable insertion (B1DISABLE) bit is used to set the B1 byte in a pass through mode. When B1DISABLE is set to logic one, the B1 byte value is passed through transparently without being overwritten. When B1DISABLE is set to logic zero, a valid B1 byte is inserted into the SOH.

B2DISABLE

The B2 disable insertion (B2DISABLE) bit is used to set the B2 byte in a pass through mode. When B2DISABLE is set to logic one, the B2 byte value is passed through transparently without being overwritten. When B2DISABLE is set to logic zero, a valid B2 byte is inserted into the TOH.

Register 0083H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

This register is only valid once written. The default value is not transferred.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted in the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN bit in the TRMP Register Insertion register.

Register 0084H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted in the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN bit in the TRMP Register Insertion register.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted in the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN bit in the TRMP Register Insertion register.

Register 0085H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

D4D12V[7:0]

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted in the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGEN bit in the TRMP Register Insertion register.

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted in the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN bit in the TRMP Register Insertion register.

Register 0086H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

K1V[7:0], K2V[7:0]

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted in the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGEN bit in the TRMP Register Insertion register.

Register 0087H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted in the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN bit in the TRMP Register Insertion register.

S1V[7:0]

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted in the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGEN bit in the TRMP Register Insertion register.

Register 0088H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

E2V[7:0]

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted in the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGEN bit in the TRMP Register Insertion register.

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted in the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN bit in the TRMP Register Insertion register.

Register 0089H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

H2MASK[7:0]

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted in the data stream. The H2MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

H1MASK[7:0]

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted in the data stream. The H1MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

Register 008A: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

B2MASK[7:0]

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted in the data stream. The B2MASK[7:0] is XOR'ed with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted in the data stream. The B1MASK[7:0] is XOR'ed with the calculated B1 before insertion in the B1 byte.

Register 00A0H: TRMP Aux2 Configuration
Register 00C0H: TRMP Aux3 Configuration
Register 00E0H: TRMP Aux4 Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

All reserved bits in this register should be set to logic 0 for normal operation.

A1A2EN

For normal operation, the A1A2EN should be set to the same value as the A1A2EN bit in the TRMP Configuration register.

Z0DEF

For normal operation, the Z0DEF should be set to the same value as the Z0DEF bit in the TRMP Configuration register.

J0Z0INCEN

For normal operation, the J0Z0INCEN should be set to the same value as the J0Z0INCEN bit in the TRMP Configuration register.

Register 00A1H: TRMP Aux 2 Register Insertion
Register 00C1H: TRMP Aux 3 Register Insertion
Register 00E1H: TRMP Aux 4 Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11		Unused	
Bit 10	R/W	Reserved	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Z0REGEN	1
Bit 0	R/W	Reserved	1

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 4. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

Z1REGEN

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 4. When Z1REGEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGEN

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 4. When Z2REGEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 4. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enabled via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enabled via the NATIONALEN register bit.

UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 4. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit.

Register 00A2H: TRMP Aux2 Error Insertion
Register 00C2H: TRMP Aux3 Error Insertion
Register 00E2H: TRMP Aux4 Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	B2DISABLE	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

All reserved bits in this register must be set to their default value for proper operation.

LAISINS

For normal operation, the LAISINS should be set to the same value as the LAISINS bit in the TRMP Error Insertion register.

LOSINS

For normal operation, the LOSINS should be set to the same value as the LOSINS bit in the TRMP Error Insertion register.

B2DISABLE

The B2 disable insertion (B2DISABLE) bit is used to set the B2 byte in a pass through mode. When B2DISABLE is set to logic one, the B2 byte value is passed through transparently without being overwritten. When B2DISABLE is set to logic zero, a valid B2 byte is inserted into the TOH.

Register 00A3H: TRMP Aux2 Transmit Z0
Register 00C3H: TRMP Aux3 Transmit Z0
Register 00E3H: TRMP Aux4 Transmit Z0

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

These registers are only valid once written. The default values are not transferred.

All reserved bits in this register must be set to their default value for proper operation.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

Register 00A7H: TRMP Aux 2 Transmit Z1
Register 00C7H: TRMP Aux 3 Transmit Z1
Register 00E7H: TRMP Aux 4 Transmit Z1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

All reserved bits in this register must be set to their default value for proper operation.

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted in the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN bit in the TRMP Register Insertion register.

Register 00A8H: TRMP Aux 2 Transmit Z2
Register 00C8H: TRMP Aux 3 Transmit Z2
Register 00E8H: TRMP Aux 4 Transmit Z2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted in the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN bit in the TRMP Register Insertion register.

Register 0100H: SBER Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0, the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1, the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0, the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1, the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0, the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1, the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0, the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1, the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

Register 0101H: SBER Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Register 0102H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the interrupt (INTB) output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the interrupt (INTB) output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0103H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0104H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 0105H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to Section 13.16 for the recommended settings.

Register 0106H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	FFFF

Register 0107H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[23:16]	XXFF

SFSATH[23:0]

The SFSTH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFF disables the saturation functionality. Refer to Section 13.16 for the recommended settings..

Register 0108H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Register 0109H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[23:16]	XX00

SFDECTH[23:0]

The SFDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to Section 13.16 for the recommended settings.

Register 010AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 010BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[23:16]	XX00

SFCLRTH[23:0]

The SFCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to Section 13.16 for the recommended settings.

Register 010CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 010DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to Section 13.16 for the recommended settings.

Register 010EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[15:0]	FFFF

Register 010FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[23:16]	XXFF

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to Section 13.16 for the recommended settings.

Register 0110H: SBER SD BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 0111H: SBER SD BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[23:16]	XX00

SDDECTH[23:0]

The SDDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to Section 13.16 for the recommended settings.

Register 0112H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 0113H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[23:16]	XX00

SDCLRTH[23:0]

The SDCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to Section 13.16 for the recommended settings.

Register 0130H: RTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 section is accessed by the current indirect transfer. This register should only be set to 0001 since only the STS-1/STM-0 #1 section byte is valid.

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0131H: RTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0132H: RTTP SECTION Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUV	X

All Reserved bits must be set to their default values for proper operation.

TIUV

The trace identifier unstable status (TIUV) bit indicates the current status of the TIU defect.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is received for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. BYTE_TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 0133H: RTTP SECTION Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIUE	0

All Reserved bits must be set to their default values for proper operation.

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When the bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0134H: RTTP SECTION Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUI	X

All Reserved bits must be set to their default values for proper operation.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0135H: RTTP SECTION Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMV	X

TIMV

The trace identifier mismatch status (TIMV) bit indicates the current status of the TIM defect.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0136H: RTTP SECTION Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIME	0

All Reserved bits must be set to their default values for proper operation.

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0137H: RTTP SECTION Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMI	X

All Reserved bits must be set to their default values for proper operation.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Indirect Register 00H: RTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must be received in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi frame to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero message are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered to match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP SECTION Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP SECTION Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronize. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP SECTION Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP SECTION Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP SECTION Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP SECTION Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validate the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0138H: TTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SECTION[3]	0
Bit 2	R/W	SECTION[2]	0
Bit 1	R/W	SECTION[1]	0
Bit 0	R/W	SECTION[0]	0

SECTION[3:0]

The STS-1/STM-0 section (SECTION[3:0]) bits select which STS-1/STM-0 is accessed by the current indirect transfer. SECTION[3:0] should be set to 0001.

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0139H: TTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP SECTION Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 0200H: RHPP STS-1/STM-0 #1 through #12 Indirect Address
Register 0280H: RHPP STS-1/STM-0 #13 through #24 Indirect Address
Register 0300H: RHPP STS-1/STM-0 #25 through #36 Indirect Address
Register 0380H: RHPP STS-1/STM-0 #37 through #48 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001	Path #(1, 13, 25 or 37)
0010	Path #(2, 14, 26 or 38)
0011	Path #(3, 15, 27 or 39)
0100	Path #(4, 16, 28 or 40)
0101	Path #(5, 17, 29 or 41)
0110	Path #(6, 18, 30 or 42)
0111	Path #(7, 19, 31 or 43)
1000	Path #(8, 20, 32 or 44)
1001	Path #(9, 21, 33 or 45)
1010	Path #(10, 22, 34 or 46)
1011	Path #(11, 23, 35 or47)
1100	Path #(12, 24, 36 or 48)
1101-1111	Invalid path

IADDR[2:0]

The address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address IADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	RHPP Pointer Interpreter status
0110	RHPP Path BIP Error Counter
0111	RHPP Path REI Error Counter
1000	RHPP Path Negative Justification Event Counter
1001	RHPP Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0201H: RHPP STS-1/STM-0 #1 through #12 Indirect Data
Register 0281H: RHPP STS-1/STM-0 #13 through #24 Indirect Data
Register 0301H: RHPP STS-1/STM-0 #25 through #36 Indirect Data
Register 0381H: RHPP STS-1/STM-0 #37 through #48 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Indirect Register 00H: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	

All Reserved bits must be set to their default values for proper operation.SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taken into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The "justification more than 3 frames ago disable" (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications. INVCNT must be set to logic 1 to enable behaviour compliant to GR-253 CORE.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782. This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE event counter to count towards LOP-P defect when the pointer is out of range. This configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 01H: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPECNTBLK	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at RHPP r/w indirect address 01H.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPECNTBLK

The path block BIP-8 errors count (PBIPECNTBLK) bit controls the way path BIP-8 errors are reported to the SARC. If PBIPECNTBLK is set to logic 1, BIP-8 errors are counted on a block basis, incremented only once for one or more BIP-8 errors. When PBIPECNTBLK is set to logic 0, the number of incorrect bits in the BIP-8 are reported (maximum of 8).

B3EBLK

The serial path block BIP-8 errors count (B3EBLK) bit controls the way path BIP-8 errors are reported via the RPOH extract pin. If B3EBLK is set to logic 1, BIP-8 errors are counted on a block basis, incremented only once for one or more BIP-8 errors. When B3EBLK is set to logic 0, the number of incorrect bits in the BIP-8 are reported (maximum of 8).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLKACC is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLKACC is set to logic 0, the extracted path REI errors are interpreted as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3E On RPOH (B3EONRPOH) bit controls whether the normal B3E output on RPOH should be replaced by the BIP-8 error byte. When set to logic 0, B3 is output normally. When set to logic 1, B3 is replaced by the BIP-8 error code.

Indirect Register 02H: RHPP Pointer Value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS pointer being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 03H: RHPP Captured and Accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Accepted PSL and ERDI Indirect Register is provided at RHPP r/w address 03H.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. APSLV is updated differently depending on how the ALGO2 bit in RHPP indirect register 01H is set. When ALGO2 is logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit). When ALGO2 is logic 0, APSLV is updated every time a new PSL is received. Note that there is no concept of "accepted" path signal label in Algorithm 1, so this register should only be used when ALGO2 is logic 1.

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at RHPP r/w indirect address 04H.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 1.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 2. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disabled and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 1.

Indirect Register 05H: RHPP Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	NDF	X
Bit 5	R	Unused	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	X

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable). This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times. This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received. This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication). This bit is only valid for master timeslots. It is not valid for slave (concatenated) timeslots.

Indirect Register 06H: RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The RHPP Path BIP Error Counter register is provided at RHPP r/w indirect address 06H.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 07H: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The RHPP Path REI Error Counter register is provided at RHPP r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 08H: RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The RHPP Path Negative Justification Event Counter register is provided at RHPP r/w indirect address 08H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Indirect Register 09H: RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The RHPP Path Positive Justification Event Counter register is provided at RHPP r/w indirect address 09H.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address 203H, 283H, 303H, 383H). The TIP output indicates the transfer status.

Register 0202H, 0282H, 0302H and 0382H: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

In the normal mode of operation of the S/UNI-2488, this register must not be changed from its default settings. In the cross connect mode of operation (controlled by the XCONNECT register bit), the RHPP must be configured to correctly process the various payloads that are input to the S/UNI-2488.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of an STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of an STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of an STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of an STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) master payload.

Register 0203H, 0283, 0303, 0383: RHPP Counters Update

Bit	Type	Function	Default
Bit 15	W	Unused	X
Bit 14	W	Unused	X
Bit 13	W	Unused	X
Bit 12	W	Unused	X
Bit 11	W	Unused	X
Bit 10	W	Unused	X
Bit 9	W	Unused	X
Bit 8	W	Unused	X
Bit 7	W	Unused	X
Bit 6	W	Unused	X
Bit 5	W	Unused	X
Bit 4	W	Unused	X
Bit 3	W	Unused	X
Bit 2	W	Unused	X
Bit 1	W	Unused	X
Bit 0	W	Unused	X

Any write to an RHPP Counters Update Register (address 0203H, 0283H, 0303H, 0383H) will trigger the transfer of all counter values, for that particular STS-12 slice, to their holding registers. To update all counters in this manner, all four registers must be written. This is equivalent writing to register 0000H. The TIP register bit (register 0000H) indicates the transfer status.

Register 0204H, 0284, 0304, 0384: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The RHPP Path Interrupt Status Register is provided at RHPP read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) indicates which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts. P_INT[1:12] has been added to reduce the average number of accesses required to service interrupts.

Register 0205H, 0285, 0305, 0385: RHPP Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The Pointer Concatenation Processing Disable Register is provided at RHPP r/w address 05H.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Register 0208H, 0210H, 0218H, 0220H, 0228H, 0230H, 0238H, 0240H, 0248H, 0250H, 0258H, 0260H
Register 0288H, 0290H, 0298H, 02A0H, 02A8H, 02B0H, 02B8H, 02C0H, 02C8H, 02D0H, 02D8H, 02E0H
Register 0308H, 0310H, 0318H, 0320H, 0328H, 0330H, 0338H, 0340H, 0348H, 0350H, 0358H, 0360H
Register 0388H, 0390H, 0398H, 03A0H, 03A8H, 03B0H, 03B8H, 03C0H, 03C8H, 03D0H, 03D8H, 03E0H:
RHPP STS-1/STM-0 #N (Where N=1 to 48) Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	
Bit 0		Unused	

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

This bit is only valid for RHPP STS-1/STM0 #1, except in the XCONNECT mode of operation where it is valid only for master timeslots.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

This bit is only valid for RHPP STS-1/STM0 #1, except in the XCONNECT mode of operation where it is valid only for master timeslots.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for RHPP STS-1/STM0 #2-48, except in the XCONNECT mode of operation.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

This bit is only valid for RHPP STS-1/STM0 #2-48 except in the XCONNECT mode of operation.

Register 0209H, 0211H, 0219H, 0221H, 0229H, 0231H, 0239H, 0241H, 0249H, 0251H, 0259H, 0261H
Register 0289H, 0291H, 0299H, 02A1H, 02A9H, 02B1H, 02B9H, 02C1H, 02C9H, 02D1H, 02D9H, 02E1H
Register 0309H, 0311H, 0319H, 0321H, 0329H, 0331H, 0339H, 0341H, 0349H, 0351H, 0359H, 0361H
Register 0389H, 0391H, 0399H, 03A1H, 03A9H, 03B1H, 03B9H, 03C1H, 03C9H, 03D1H, 03D9H, 03E1H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	
Bit 0	R/W	PTRJEE	0

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit controls the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1, except in the XCONNECT mode of operation.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #2-48 except in the XCONNECT mode of operation.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

This bit is only valid for RHPP STS-1/STM0 #2-48 except in the XCONNECT mode of operation.

Register 020AH, 0212H, 021AH, 0222H, 022AH, 0232H, 023AH, 0242H, 024AH, 0252H, 025AH, 0262H
Register 028AH, 0292H, 029AH, 02A2H, 02AAH, 02B2H, 02BAH, 02C2H, 02CAH, 02D2H, 02DAH, 02E2H
Register 030AH, 0312H, 031AH, 0322H, 032AH, 0332H, 033AH, 0342H, 034AH, 0352H, 035AH, 0362H
Register 038AH, 0392H, 039AH, 03A2H, 03AAH, 03B2H, 03BAH, 03C2H, 03CAH, 03D2H, 03DAH, 03E2H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Pointer Interpreter Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #1 except in the XCONNECT mode of operation.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #2-48 except in the XCONNECT mode of operation.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

This bit is only valid for RHPP STS-1/STM0 #2-48 except in the XCONNECT mode of operation.

Register 020BH, 0213H, 021BH, 0223H, 022BH, 0233H, 023BH, 0243H, 024BH, 0253H, 025BH, 0263H
Register 028BH, 0293H, 029BH, 02A3H, 02ABH, 0283H, 02BBH, 02C3H, 02CBH, 02D3H, 02DBH, 02E3H
Register 030BH, 0313H, 031BH, 0323H, 032BH, 0333H, 033BH, 0343H, 034BH, 0353H, 035BH, 0363H
Register 038BH, 0393H, 039BH, 03A3H, 03ABH, 03B3H, 03BBH, 03C3H, 03CBH, 03D3H, 03DBH, 03E3H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 1, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 1, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 1, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 1, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect. PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 1, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). A PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 1, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 1, 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 1, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect according to Table 1. PPDI is set to logic 0 when the accepted PSL is not a defect according to Table 1.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 020CH, 0214H, 021CH, 0224H, 022CH, 0234H, 023CH, 0244H, 024CH, 0254H, 025CH, 0264H
Register 028CH, 0294H, 029CH, 02A4H, 02ACH, 02B4H, 02BCH, 02C4H, 02CCH, 02D4H, 02DCH, 02E4H
Register 030CH, 0314H, 031CH, 0324H, 032CH, 0334H, 033CH, 0344H, 034CH, 0354H, 035CH, 0364H
Register 038CH, 0394H, 039CH, 03A4H, 03ACH, 03B4H, 03BCH, 03C4H, 03CCH, 03D4H, 03DCH, 03E4H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt (INTB) output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt (INTB) output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt (INTB) output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt (INTB) output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt (INTB) output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt (INTB) output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt (INTB) output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt (INTB) output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt (INTB) output.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt (INTB) output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt (INTB) output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt (INTB) output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt (INTB) output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt (INTB) output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt (INTB) output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt (INTB) output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt (INTB) output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt (INTB) output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt (INTB) output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt (INTB) output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt (INTB) output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt (INTB) output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt (INTB) output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt (INTB) output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt (INTB) output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt (INTB) output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt (INTB) output.

Register 020DH, 0215H, 021DH, 0225H, 022DH, 0235H, 023DH, 0245H, 024DH, 0255H, 025DH, 0265H
Register 028DH, 0295H, 029DH, 02A5H, 02ADH, 02B5H, 02BDH, 02C5H, 02CDH, 02D5H, 02DDH, 02E5H
Register 030DH, 0315H, 031DH, 0325H, 032DH, 0335H, 033DH, 0345H, 034DH, 0355H, 035DH, 0365H
Register 038DH, 0395H, 039DH, 03A5H, 03ADH, 03B5H, 03BDH, 03C5H, 03CDH, 03D5H, 03DDH, 03E5H:
RHPP STS-1/STM-0 #N (where N=1 to 48) Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0400H: THPP STS-1/STM-0 #1 through #12 Indirect Address
Register 0480H: THPP STS-1/STM-0 #13 through #24 Indirect Address
Register 0500H: THPP STS-1/STM-0 #25 through #36 Indirect Address
Register 0580H: THPP STS-1/STM-0 #37 through #48 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

Path[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001	Path #(1, 13, 25 or 37)
0010	Path #(2, 14, 26 or 38)
0011	Path #(3, 15, 27 or 39)
0100	Path #(4, 16, 28 or 40)
0101	Path #(5, 17, 29 or 41)
0110	Path #(6, 18, 30 or 42)
0111	Path #(7, 19, 31 or 43)
1000	Path #(8, 20, 32 or 44)
1001	Path #(9, 21, 33 or 45)
1010	Path #(10, 22, 34 or 46)
1011	Path #(11, 23, 35 or47)
1100	Path #(12, 24, 36 or 48)
1101-1111	Invalid path

IADDR[3:0]

The address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source and Pointer Control
0010	Reserved
0011	Reserved
0100	THPP B3 Mask and Fixed stuff byte
0101	THPP Transmit C2 and J1
0110	THPP Transmit H4 Mask and G1
0111	THPP Transmit F2 and Z3
1000	THPP Transmit Z4 and Z5
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0401H: THPP STS-1/STM-0 #1 through #12 Indirect Data
Register 0481H: THPP STS-1/STM-0 #13 through #24 Indirect Data
Register 0501H: THPP STS-1/STM-0 #25 through #36 Indirect Data
Register 0581H: THPP STS-1/STM-0 #37 through #48 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0402: THPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

All Reserved bits must be set to their default values for proper operation.

Indirect Register 00H: THPP Control Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	

All Reserved bits must be set to their default values for proper operation.

PREIEBLK

The path REI block error (PREIEBLK) bit controls the extraction of path REI errors in the PREI monitoring block of the STS/AU pointer. When PREIEBLK is set to logic 1, the path REI extracted represents BIP-8 block errors (a maximum of 1 error per frame). When PREIEBLK is set to logic 0, the path REI extracted represents BIP-8 errors (a maximum of 8 errors per frame).

This bit is only valid for THPP STS-1/STM0 #1.

FSBEN

When the FSBEN register bit is logic one, THPP overwrites the fixed stuff byte. The value used is that programmed in the FSB field of THPP Indirect Register 04H. Note that if the channel is unequipped, this bit may be set and the value changed to whatever value is being transmitted in the unequipped payload. This bit has no effect when TPAIS_EN is set high and Path AIS is being transmitted.

This bit is valid for and should be consistent for the first four STS-1 timeslots of each THPP as these are the only FSB bytes in an STS-48c.

Indirect Register 01H: THPP Source and Pointer Control Register

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	H4MASK	0
Bit 12	R/W	B3MASK	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	ENH4MASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

IBER

When the IBER register bit is set to logic one, the G1 byte is generated by the SIRP block. The THPP overwrites the LSB of the pass-through G1 with a zero logic value. When IBER is set to logic zero, the G1 byte can be modified by one of the THPP POH sources.

This bit is only valid for THPP STS-1/STM0 #1.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCnn bits are used to determine the source for the path overhead bytes. For example, when a logic 1 is written to SRCJ1, the J1 byte inserted can be found in the THPP Transmit C2 and J1 register. When a logic 0 is written to SRCJ1, the J1 byte source can be either the TPOH input or the TTTP PATH, depending on the value of the PTBJ1 register bit found in this register.

These bits are only valid for THPP STS-1/STM0 #1.

PTBJ1

The PTBJ1 or Path Trace Buffer J1 byte register bit is used to determine the origin of the path trace byte to be inserted. When PTBJ1 is high, the J1 byte is sourced from the TTTP PATH block; otherwise, the J1 byte is sourced either from the TPOH input or not inserted at all as it is controlled using the SRCJ1 bit.

These bits are only valid for THPP STS-1/STM0 #1.

ENH4MASK

When ENH4MASK is logic high, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is used as an error mask on the H4 byte. When ENH4MASK is logic low, the H4[7:0] byte in THPP Transmit H4 Mask and G1 register is inserted as the H4 byte.

These bits are only valid for THPP STS-1/STM0 #1.

ENG1REC

The valid high ENG1REC register bit enables the insertion of the PRDI[2:0] and PREI[3:0] of the G1 byte from the SARC block. When ENG1REC is set to logic low, the G1 byte source is other than the SARC block.

B3MASK

When B3MASK is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is to be used as a mask for an internally generated B3. When B3MASK is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted in the B3 byte if the path overhead source priority is TPOH.

H4MASK

When H4MASK is logic high, the byte received via the TPOH (valid only if TPOHEN is logic high) bit serial stream is to be used as a mask for the H4 byte. When H4MASK is logic low, the byte received on TPOH (valid only if TPOHEN is logic high) will be inserted in the H4 byte only if the path overhead source priority is TPOH.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all-one or an all-zero pattern in the payload. The path overhead and fixed stuff bytes are excluded from insertion.

The path overhead may be forced to all-zeros or all-ones using the THPP's SRC register fields in this register. Note that the Bellcore spec requires the Path Signal Label (C2) to be set to 0x00. This must be set manually. The FSBEN and FSB fields in THPP indirect registers 00H and 04H respectively may be used to set the same value in the FSB as programmed in UNEQV. Regardless, the B3 will be calculated and inserted such that the unequipped frame has a valid BIP.

When UNEQ is set to logic one, an all-one or an all-zero pattern is inserted in the payload. The UNEQV bit in this register determines the pattern. When UNEQ is set logic 0, no pattern is inserted.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the payload. When UNEQV is set to logic 1, an all-one pattern is inserted in the payload if enabled via the UNEQ register bit. When UNEQV is set to logic 0, an all-zero pattern is inserted in the payload if enabled via the UNEQ register bit.

Indirect Register 04H: THPP Fixed Stuff Byte and B3 Mask (TFSB)

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When the FSBEN bit in the THPP Control register is logic one, the THPP replaces the fixed bytes with the byte from this register. Note that if the channel is unequipped, this field may be set to the same value that is indicated by UNEQV to insert FSB that is consistent with the rest of the payload.

FSB[7:0] should be consistent for all THPP STS-1/STM0 #1 through #48.

B3MASK[7:0]

The calculated B3 parity byte is always XOR'ed with this register bit to allow the user to insert errors in B3.

B3MASK[7:0] is only valid for THPP STS-1/STM0 #1.

Indirect Register 05H: THPP Transmit J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

The J1[7:0] bits are inserted in the J1 byte position when the SRCJ1 bit of the THPP Source & Pointer Control Register is logic 0 and TPOHEN is low during the path trace bit positions in the path overhead input stream, TPOH. J1[7:0] is inserted into the J1 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

C2[7:0]

The C2[7:0] bits are inserted in the C2 byte position when the SRCC2 bit of the THPP Source & Pointer Control Register is logic 0 and TPOHEN is low during the path signal label bit positions in the path overhead input stream, TPOH. C2[7:0] is inserted into the C2 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 06H: THPP Transmit G1 POH and H4 Mask (TG1H4POH)

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

The G1[7:0] bits are inserted in the G1 byte position when the SRCG1 bit of the Source and Pointer Control Register is high and TPOHEN is low during the path status bit positions in the path overhead input stream, TPOH. G1[7:0] is inserted into the G1 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

H4[7:0]

The H4[7:0] bits are inserted in the H1 byte position when the ENH4MASK bit of the Source and Pointer Control Register is high and TPOHEN is low during the path multiframe bit positions in the path overhead input stream, TPOH. H4[7:0] is inserted into the H4 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 07H: THPP Transmit F2 and Z3 POH (TF2Z3POH)

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

Z3[7:0]

The Z3[7:0] bits are inserted in the Z3 byte position when the SRCZ3 bit of the THPP Source and Pointer Control Register is logic 0 and input TPOHEN is low during the path Z3 growth bit positions in the path overhead input stream, TPOH. Z3[7:0] is inserted into the Z3 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

F2[7:0]

The F2[7:0] bits are inserted in the F2 byte position when the SRCF2 bit of the THPP Source and Pointer Control Register is logic 0 and input TPOHEN is low during the path User Channel bit positions in the path overhead input stream, TPOH. F2[7:0] is inserted into the F2 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

Indirect Register 08H: THPP Transmit Z4 and Z5 Overhead (TZ4Z5POH)

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z5[7:0]

The Z5[7:0] bits are inserted in the Z5 byte position when the SRCZ5 bit of the THPP Source and Pointer Control Register is logic 0 and input TPOHEN is low during the path Z5 growth bit positions in the path overhead input stream, TPOH. Z5[7:0] is inserted into the Z5 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

Z4[7:0]

The Z4[7:0] bits are inserted in the Z4 byte position when the SRCZ4 bit of the THPP Source and Pointer Control Register is logic 0 and input TPOHEN is low during the path Z4 growth bit positions in the path overhead input stream, TPOH. Z4[7:0] is inserted into the Z4 position of the POH when register insertion is enabled. See Table 6 Path Overhead Byte Source Priority for details.

This field is only valid for THPP STS-1/STM0 #1.

Register 0600H, 0620H, 0640H, 0660H: SVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Refer to Section 13.19 for details on SVCA indirect register access.

Path[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1110	Invalid path
1111	Invalid path

IADDR[1:0]

The address location (IADDR[1:0]) bits select which address location is accessed by the current indirect transfer. Refer to Section 13.19 for details on SVCA indirect register access

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Pointer Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to an internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to a register. When RWB is set to logic 1, an indirect read access to a register is initiated. The data from the addressed location as indicated using the IADDR field will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to a register is initiated. The data from the Indirect Data Register will be transferred to the addressed register.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access to an internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0601H, 0621H, 0641H, 0661H: SVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an indirect register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

Register 0602H, 0622H, 0642H, 0662H: SVCA Payload Configuration Register

Bit	Type	Function	Default
Bit 15	R/W	SLAVE	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

In normal mode operation this register is reserved. Use default values.

In the XCONNECT mode of operation of the S/UNI-2488, the STS3C[4:1] register bits are defined as follows:

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

SLAVE

The STS-12c/VC-4-4c slave concatenation (SLAVE) signal enables the slave processing of an STS-12c/VC-4-4c payload. When SLAVE is logic one, the SVCA processes a slave STS-12c/VC-4-4c payload. When SLAVE is logic zero, the SVCA processes a master STS-12c/VC-4-4c payload. One master SVCA and three slave SVCA can be used to process an STS-48c/VC-4-16c payload. When SLAVE is logic one, the PTRJE output is simply the SLPTRJE input. When STS12CSL is logic zero, the PTRJE output is derived from the pointer generator state machine and the SLPTRJE input is ignored.

The SLAVE register bit is OR'ed with the SLAVE input. The SLAVE register bit has precedence over the STS3C[1:4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the STS12C input. The STS12C register bit has precedence over the STS3C[1:4] register bit.

Register 0603H, 0623H, 0643H, 0663H: SVCA Positive Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	PPJI[12]	0
Bit 10	R	PPJI[11]	0
Bit 9	R	PPJI[10]	0
Bit 8	R	PPJI[9]	0
Bit 7	R	PPJI[8]	0
Bit 6	R	PPJI[7]	0
Bit 5	R	PPJI[6]	0
Bit 4	R	PPJI[5]	0
Bit 3	R	PPJI[4]	0
Bit 2	R	PPJI[3]	0
Bit 1	R	PPJI[2]	0
Bit 0	R	PPJI[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the PPJI[12:1] register bits are defined as follows:

PPJI[12:1]

The positive pointer justification interrupt status (PPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PPJI[12:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0603H) is used. The PPJI[12:2] register bits are unused in normal mode and the PPJI[1] register bit is defined as follows:

PPJI[1]

The positive pointer justification interrupt status (PPJI[1]) bit indicates a positive pointer adjustment in the STS-48c/STM-4-4c stream. PPJI[1] is set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0604H, 0624H, 0644H, 0664H: SVCA Negative Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	NPJI[12]	0
Bit 10	R	NPJI[11]	0
Bit 9	R	NPJI[10]	0
Bit 8	R	NPJI[9]	0
Bit 7	R	NPJI[8]	0
Bit 6	R	NPJI[7]	0
Bit 5	R	NPJI[6]	0
Bit 4	R	NPJI[5]	0
Bit 3	R	NPJI[4]	0
Bit 2	R	NPJI[3]	0
Bit 1	R	NPJI[2]	0
Bit 0	R	NPJI[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the NPJI[12:1] register bits are defined as follows:

NPJI[12:1]

The negative pointer justification interrupt status (NPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. NPJI[12:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0604H) is used. The NPJI[12:2] register bits are unused in normal mode and the NPJI[1] register bit is defined as follows:

NPJI[1]

The negative pointer justification interrupt status (NPJI[1]) bit indicates a negative pointer adjustment in the STS-48c/STM-4-4c stream. NPJI[1] is set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0605H, 0625H, 0645H, 0665H: SVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FOVRI[12]	0
Bit 10	R	FOVRI[11]	0
Bit 9	R	FOVRI[10]	0
Bit 8	R	FOVRI[9]	0
Bit 7	R	FOVRI[8]	0
Bit 6	R	FOVRI[7]	0
Bit 5	R	FOVRI[6]	0
Bit 4	R	FOVRI[5]	0
Bit 3	R	FOVRI[4]	0
Bit 2	R	FOVRI[3]	0
Bit 1	R	FOVRI[2]	0
Bit 0	R	FOVRI[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the FOVRI[12:1] register bits are defined as follows:

FOVRI[12:1]

The FIFO overflow event interrupt status (FOVRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FOVRI[12:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0605H) is used. The FOVRI[12:2] register bits are unused in normal mode and the FOVRI[1] register bit is defined as follows:

FOVRI[1]

The FIFO overflow event interrupt status (FOVRI[1]) bit indicates a FIFO overflow in the SVCA. FOVRI[1] is set to logic 1 to indicate a FIFO overflow event. This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0606H, 0626H, 0646H, 0666H: SVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FUDRI[12]	0
Bit 10	R	FUDRI[11]	0
Bit 9	R	FUDRI[10]	0
Bit 8	R	FUDRI[9]	0
Bit 7	R	FUDRI[8]	0
Bit 6	R	FUDRI[7]	0
Bit 5	R	FUDRI[6]	0
Bit 4	R	FUDRI[5]	0
Bit 3	R	FUDRI[4]	0
Bit 2	R	FUDRI[3]	0
Bit 1	R	FUDRI[2]	0
Bit 0	R	FUDRI[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the FUDRI[12:1] register bits are defined as follows:

FUDRI[12:1]

The FIFO underflow event interrupt status (FUDR[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FUDRI[12:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0606H) is used. The FUDRI[12:2] register bits are unused in normal mode and the FUDRI[1] register bit is defined as follows:

FUDRI[1]

The FIFO underflow event interrupt status (FUDRI[1]) bit indicates a FIFO underflow in the SVCA. FUDRI[1] is set to logic 1 to indicate a FIFO underflow event. This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0607H, 0627H, 0647H, 0667H: SVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PJIEN[12]	0
Bit 10	R/W	PJIEN[11]	0
Bit 9	R/W	PJIEN[10]	0
Bit 8	R/W	PJIEN[9]	0
Bit 7	R/W	PJIEN[8]	0
Bit 6	R/W	PJIEN[7]	0
Bit 5	R/W	PJIEN[6]	0
Bit 4	R/W	PJIEN[5]	0
Bit 3	R/W	PJIEN[4]	0
Bit 2	R/W	PJIEN[3]	0
Bit 1	R/W	PJIEN[2]	0
Bit 0	R/W	PJIEN[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the PJIEN[12:1] register bits are defined as follows:

PJIEN[12:1]

The pointer justification event interrupt enable (PJIEN[12:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0607H) is used. The PJIEN[12:2] register bits are unused and the PJIEN[1] register bit is defined as follows:

PJIEN[1]

The pointer justification event interrupt enable (PJIEN[1]) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0608H, 0628H, 0648H, 0668H: SVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	FIEN[12]	0
Bit 10	R/W	FIEN[11]	0
Bit 9	R/W	FIEN[10]	0
Bit 8	R/W	FIEN[9]	0
Bit 7	R/W	FIEN[8]	0
Bit 6	R/W	FIEN[7]	0
Bit 5	R/W	FIEN[6]	0
Bit 4	R/W	FIEN[5]	0
Bit 3	R/W	FIEN[4]	0
Bit 2	R/W	FIEN[3]	0
Bit 1	R/W	FIEN[2]	0
Bit 0	R/W	FIEN[1]	0

In the XCONNECT mode of operation of the S/UNI-2488, the FIEN[12:1] register bits are defined as follows:

FIEN[12:1]

The FIFO event interrupt enable (ESEEN[12:1]) bits control the activation of the interrupt (INT) output for STS-1/STM-0 paths #1 to #12 caused by a FIFO overflow or a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INT) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INT) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

In the normal mode of operation of the S/UNI-2488 only the first register address (0608H) is used. The FIEN[12:2] register bits are unused in normal mode and the FIEN[1] register bit is defined as follows:

FIEN[1]

The FIFO event interrupt enable (FIEN[1]) bit controls the activation of the interrupt (INTB) output due to a FIFO overflow or a FIFO underflow. When set to logic 1, the corresponding pending interrupts will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupts will not assert the interrupt (INTB) output. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears this bit.

Register 0609H, 0629H, 0649H, 0669H: SVCA Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Reserved

All Reserved bits must be set to their default value for proper operation.

Register 060AH, 062AH, 064AH, 066AH: SVCA MISC Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	CLRFS[12]	0
Bit 10	R/W	CLRFS[11]	0
Bit 9	R/W	CLRFS[10]	0
Bit 8	R/W	CLRFS[9]	0
Bit 7	R/W	CLRFS[8]	0
Bit 6	R/W	CLRFS[7]	0
Bit 5	R/W	CLRFS[6]	0
Bit 4	R/W	CLRFS[5]	0
Bit 3	R/W	CLRFS[4]	0
Bit 2	R/W	CLRFS[3]	0
Bit 1	R/W	CLRFS[2]	0
Bit 0	R/W	CLRFS[1]	0

CLRFS

The Clear Fixed Stuff (CLRFS) enables the regeneration of fixed stuff columns (#30, #59) of an STS-1/VC-3. When set to logic one, STS-1/VC-3 incoming fixed stuff columns (#30, #59) are discarded and regenerated (set to 00h) on the outgoing stream. When set to logic 0, these fixed stuff columns are relayed through the SVCA.

Register 060BH, 062BH, 064BH, 066BH: SVCA Performance Monitor Trigger

The Performance monitor transfer register is provided at address 060BH. Any write to this register triggers a transfer of all performance monitor counters to holding registers that can be read by the microprocessor interface.

Indirect Register 00H: SVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by writing to the SVCA Performance Monitor Trigger register (0x060B, 0x062B, 0x064B, 0x066B) or the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H).

Note that the PJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 01H: SVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 3 TCLK cycles after a transfer is triggered by the SVCA Performance monitor trigger register or by writing to the S/UNI-2488 Identity and Global Performance Monitor Update register (0000H).

Note that the NJPMON[12:0] count value is only valid for STS-N master timeslots.

Indirect Register 02H: SVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[2]	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Diag_FifoAISDis	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	0

Diag_PosJust

The Diag_PosJust bit forces the SVCA to generate outgoing positive justification events. When set to 1, the SVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the SVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor. In OC-48c mode (normal mode) this bit should only be set in STS-1 #1 of 48.

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_NegJust

The Diag_NegJust bit forces the SVCA to generate outgoing negative justification events. When set to 1, the SVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Note that the SVCA will follow up with an automatic negative pointer justification if it needs to do so in order to keep its FIFO fill levels under control. The diagnostic feature has a lower priority than the FIFO monitor. In OC-48c mode (normal mode) this bit should only be set in STS-1 #1 of 48.

Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP

When set high, the Diag_LOP bit forces the SVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis

When set high, the Diag_FifoAISDis bit forces the SVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames.

Note: When Diag_FifoAISDis is enabled, any overflow or underflow will cause the SVCA to declare both FUDR and FOVR interrupts.

Diag_NDFREQ

When set high, the Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine. This bit should be set for less than one frame as multiple NDF will otherwise ensue. Consecutive NDF will cause the downstream pointer processor to declare LOP.

After any timeslot is reconfigured, the corresponding Diag_NDFREQ bit must be toggled.

PTRDD[1:0]

The PTRDD[1:0] defines the SS bits for the STS-N/AU-N concatenation pointer (may also be known as DD). ITU requires that DD be set to 10 when processing AU-4, AU-3 or TU-3. Note, BELLCORE does not specify these two bits.

JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4, AU-3 or TU-3. Note, BELLCORE does not specify these two bits. The ss bits are set to 00 when processing a slave sts-1.

PTR_RST

When set high, incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Register 0700H: RTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. This register should only be set to 0001 since only the STS-1/STM-0 #1 path byte is valid.

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0701H: RTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	DATA[7]	X
Bit 6	R/W	DATA[6]	X
Bit 5	R/W	DATA[5]	X
Bit 4	R/W	DATA[4]	X
Bit 3	R/W	DATA[3]	X
Bit 2	R/W	DATA[2]	X
Bit 1	R/W	DATA[1]	X
Bit 0	R/W	DATA[0]	X

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0702H: RTTP PATH Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUV	X

TIUV

The trace identifier unstable status (TIUV) bit indicates the current status of the TIU defect.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is received for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. BYTE_TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 0703H: RTTP PATH Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIUE	0

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When the bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0704H: RTTP PATH Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIUI	X

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit.

Register 0705H: RTTP PATH Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMV	X

TIMV

The trace identifier mismatch status (TIMV) bit indicates the current status of the TIM defect.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0706H: RTTP PATH Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TIME	0

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

Register 0707H: RTTP PATH Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	TIMI	X

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Indirect Register 00H: RTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. When LENGTH16 is set to logic 1, the tail trace message is synchronized on the MSB of the tail trace message. The byte with its MSB set high is placed in the first byte location of the captured page. When LENGTH16 is set to logic 0, the tail trace message is synchronize on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the tail trace message. The byte following the CR/LF bytes is placed in the first byte location of the captured page.

PER5

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be receive for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero message is validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered to match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP PATH Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	CTRACE[7]	X
Bit 6	R/W	CTRACE[6]	X
Bit 5	R/W	CTRACE[5]	X
Bit 4	R/W	CTRACE[4]	X
Bit 3	R/W	CTRACE[3]	X
Bit 2	R/W	CTRACE[2]	X
Bit 1	R/W	CTRACE[1]	X
Bit 0	R/W	CTRACE[0]	X

The RTTP PATH Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP PATH Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The RTTP PATH Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP PATH Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The RTTP PATH Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validate the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0708H: TTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. PATH[3:0] should be set to 0001.

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0709H: TTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP PATH Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

Register 0720H: SARC Path Register Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH_REG_EN[3]	0
Bit 2	R/W	PATH_REG_EN[2]	0
Bit 1	R/W	PATH_REG_EN[1]	0
Bit 0	R/W	PATH_REG_EN[0]	0

PATH_REG_EN[3:0]

This bit must be set to 1 to enable access to the SARC path configuration registers. For STS-48c operation, the PATH_REG_EN]3:0] register bits should be set to the value 0x1.

Please see Section 13.17 for details on setting up the SARC.

Register 0722H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	LRDI22	0
Bit 0	R/W	Reserved	0

The reserved bit in this register should be set to the default value.

LRDI22

The line remote defect indication (LRDI22) bit selects the line RDI persistence when line RDI is asserted as a result of received defects. When LRDI22 is set to logic 1, a new line RDI-L indication is transmitted for at least 22 frames. When LRDI22 is set to logic 0, a new line RDI indication is transmitted for at least 12 frames.

Register 0723H: SARC Section SALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOSEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN

The OOF enable bit allows the out of frame defect to be OR'ed into the SALM output. When the OOFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the OOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOFEN

The LOF enable bit allows the loss of frame defect to be OR'ed into the SALM output. When the LOFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOSEN

The LOS enable bit allows the loss of signal defect to be OR'ed into the SALM output. When the LOSEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LOSEN bit is set low, the corresponding defect indication does not affect the SALM output.

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be OR'ed into the SALM output. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on SALM. When the LAISEN bit is set low, the corresponding defect indication does not affect the SALM output.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to be OR'ed into the SALM output. When the LRDIEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the LRDIEN bit is set low, the corresponding defect indication does not affect the SALM output.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to be OR'ed into the SALM output. When the APSBFEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the APSBFEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be OR'ed into the SALM output. When the STIUEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the STIUEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be OR'ed into the SALM output. When the STIMEN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the STIMEN bit is set low, the corresponding defect indication does not affect the SALM output.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be OR'ed into the SALM output. When the SDBEREN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SDBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be OR'ed into the SALM output. When the SFBEREN bit is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SFBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SD/LOSEN

The SD/LOS enable bit allows the deassertion of the SD pin or the assertion of LOS to be OR'ed into the SALM output. When SD/LOSEN is set high, the corresponding defect indication is OR'ed with other defect indications and output on SALM. When the SD/LOSEN bit is set low, the corresponding defect indication does not affect the SALM output.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0724H: SARC Section RLAISINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOSEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN

The above enable bits allows for the auto insertion of in-band receive AIS-P based on any or all of the Receive Line defects listed below. A defect is a candidate for the generation if the associated enable bit is set to logic '1'. If it is set to logic '0', it will not be considered. If any bits in this register are set, bit 0, "RLAISINSEN", of register 072AH, "SARC Path RPAISINS Enable," must also be set.

- Out Of Frame (OOF) defect.
- Loss Of Frame (LOF) defect.
- Loss Of Signal (LOS) defect.
- Line Alarm Indication Signal (LAIS) defect.*
- Line Remote Defect Indication (LRDI) defect.
- APS Byte Failure (APSBF) defect.
- Section Trace Identifier Unstable (STIU) defect.
- Section Trace Identifier Mismatch (STIM) defect.
- Signal Degrade BER (SDBER) defect.
- Signal Failure BER (SFBER) defect.

-SD input pin deassertion or Loss of Signal (LOS) defect assertion

*Note that it is not possible to insert AIS-L in this direction due to the downstream pointer processor. Only AIS-P may be generated.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0725H: SARC Section TLRDIINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	SD/LOSEN	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN, LOFEN, LOSEN, LAISEN, LRDIEN, APSBFEN, STIUEN, STIMEN, SDBEREN, SFBEREN

The above enable bits allows for the auto assertion of transmit LRDI based on the following conditions:

- Out Of Frame (OOF) defect.
- Loss Of Frame (LOF) defect.
- Loss Of Signal (LOS) defect.
- Line Alarm Indication Signal (LAIS) defect.
- Line Remote Defect Indication (LRDI) defect.
- APS Byte Failure (APSBF) defect.
- Section Trace Identifier Unstable (STIU) defect.
- Section Trace Identifier Mismatch (STIM) defect.
- Signal Degrade BER (SDBER) defect.
- Signal Failure BER (SFBER) defect.

- SD input pin deassertion or Loss of Signal (LOS) defect assertion

When the bit is set high, the corresponding defect indication is OR'ed with other defect indications and the result forces transmit LRD

The GROWTH enable bit has been included to allow for future expansion of the device. Neither SONET nor SDH currently specify a defect generated on the GROWTH bytes. This register field should be considered reserved.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0728H: SARC Path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI22	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

The reserved bit in this register should be set to the default value.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, a LOP-P defect is declared when the pointer is in the LOP state and a LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, a LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and a LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, a LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and a LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

PERDI22

The path enhance remote defect indication (PERDI22) bit selects the path ERDI persistence. When PERDI22 is set to logic 1, a new path ERDI indication is transmitted by the THPP for at least 22 frames. When PERDI22 is set to logic 0, a new path ERDI indication is transmitted by the THPP for at least 12 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted by the THPP. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted by the THPP.

Register 0729H: SARC Path RALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	LCDEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RSALMEN	0

The reserved bit in this register should be set to the default value.

SALMEN, PLOPTREN, PAISPTREN, LCDEN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PPLUEN, PPLMEN

The above enable bits allows for the generation of the RALM output based on the following conditions:

- section alarm (register 06A3H)
- path loss of pointer defect
- path AIS pointer defect
- path payload label unstable defect
- path payload label mismatch defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect
- loss of cell delineation

When the bit is set high, the corresponding defect indication is XORed with other defect indications to generate RALM. When the bit is set low, the corresponding defect indication does not affect RALM.

Register 072A: SARC Path RPAISINS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RLAISINSEN	0

All Reserved bits must be set to their default values for proper operation.

RLAISINSEN, PLOPTREN, PAISPTREN, PUNEQEN, PPDIEN, PRDIEN, PERDIEN, PTIUEN, PTIMEN, PPLUEN, PPLMEN

The above enable bits allows for the generation of receive path AIS (AIS-P) based on the following conditions:

- receive LAIS (register 0724H)
- path loss of pointer defect
- path AIS pointer defect*
- path payload label unstable defect
- path payload label mismatch defect
- path payload defect indication defect
- path remote defect indication defect
- path enhanced remote defect indication defect
- path trace identifier unstable defect
- path trace identifier mismatch defect

When the bit is set high, the corresponding defect indication is OR'ed with other defect indications to generate receive AIS-P. When under receive AIS-P, an all ones pattern is inserted into the receive SPE bytes. When the bit is set low, the corresponding defect indication does not affect the assertion of AIS-P.

*Note: PAISPTREN must be enabled for AIS-P consequential action to be propagated properly.

Register 0730H: SARC LOP Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PLOPTRV	X

PLOPTRV

The path loss of pointer status (PLOPTRV) bit indicates the current status of the LOP-P defect for STS-1/STM-0. When PLOPTRCFG register bits are set to 00b, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to 01b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to 10b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV is negated when an AIS-P defect is detected.

Register 0731H: SARC LOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PLOPTRE	0

PLOPTRE

The path loss of pointer interrupt enable (PLOPTRE) bit controls the activation of the interrupt (INTB) output. When this bit is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0732H: SARC LOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PLOPTRI	X

PLOPTRI

The path loss of pointer interrupt status (PLOPTRI) bit is an event indicator for the STS-1/STM-0 path #1. PLOPTRI is set to logic 1 to indicate any changes in the status of PLOPTRV. This interrupt status bit is independent of the interrupt enable bit. PLOPTRI is cleared to logic 0 when this register is read. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0733H: SARC AIS Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PAISPTRV	X

PAISPTRV

The path AIS pointer status (PAISPTRV) bit indicates the current status of the AIS-P defect for STS-1/STM-0 #1. When PAISPTRCFG register bits are set to 00b, PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to 01b, PAISPTRV is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to 10b, PAISPTRV is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV is negated when the pointer or any of the concatenation pointers are not in the AIS state.

Register 0734H: SARC AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PAISPTRE	0

PAISPTRE

The path AIS signal pointer interrupt enable (PAISPTRE) bit controls the activation of the interrupt (INTB) output. When this bit is set to logic 1, the pending interrupt will assert the interrupt (INTB) output. When this bit is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

Register 0735H: SARC AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	PAISPTRI	X

PAISPTRI

The path AIS pointer interrupt status (PAISPTRI) bit is an event indicator for STS-1/STM-0 paths #1. PAISPTRI is set to logic 1 to indicate any changes in the status of PAISPTRV. These interrupt status bits are independent of the interrupt enable bits. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0740H: RCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	POS_SEL	0
Bit 9	R/W	INVERT	0
Bit 8	R/W	STRIP_SEL	0
Bit 7	R/W	DELINDIS	0
Bit 6	R/W	IDLEPASS	0
Bit 5	R/W	CRCPASS	0
Bit 4	R/W	CRC_SEL[1]	1
Bit 3	R/W	CRC_SEL[0]	1
Bit 2	R/W	RXOTYP	0
Bit 1	R/W	DESCRMBL	1
Bit 0	R/W	PROV	0

All Reserved bits must be set to their default values for proper operation.

PROV

The processor provision bit (PROV) is used to enable the RCFP. When PROV is logic 0, the RCFP ATM and packet processors are disabled and will not transfer any valid data to the Receive FIFO interface. When PROV is logic 1, the RCFP ATM or packet processor is enabled and will process data presented to it and transfer data to the Receive FIFO (RXSDQ).

DESCRMBL

The DESCRMBL bit controls the descrambling of the packet or ATM cell payload with the polynomial $x^{43} + 1$. When DESCRMBL is set to logic 0, frame or cell payload descrambling is disabled. When DESCRMBL is set to logic 1, payload descrambling is enabled.

RXOTYP

The RXOTYP bit determines if an incoming alarm signal (from IPAIS[x]) will stop a packet by simply asserting EOP, (RXOTYP set to logic 0), or by asserting both EOP and ERR, (RXOTYP set to logic 1). When RXOTYP is set to logic 0, premature termination of the packet will result in that packet failing a FCS check.

This bit is only valid when in POS mode. In ATM mode the RCFP will finish processing any cell in progress and then stop until the alarm signal is cleared.

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits control the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, after byte destuffing and descrambling.

Table 12 Functionality of the CRC_SEL[1:0] Register Bits

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	Reserved
01	Reserved	Reserved
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

CRCPASS

The CRCPASS bit controls the dropping of cells and packets based on the detection of an incorrect CRC.

When in ATM mode and when CRCPASS is a logic 0, cells containing an HCS error are dropped.

When CRCPASS is logic 1, cells are passed to the external FIFO interface regardless of errors detected in the HCS. Additionally, the Cell Delineation finite state machine never exits the SYNC state, and hence will never lose cell delineation. Note that HCS errors are still counted.

Note that ATM idle cells that contain HCS errors will cause the state machine to change state regardless of the setting of the IDLEPASS register bit.

When in POS mode and CRCPASS is logic 1, packets with FCS errors are not marked as such and are passed to the external FIFO interface as if no FCS error occurred. When CRCPASS is logic 0, then packets with FCS errors are marked using FIFO_ERR[x] on the EOP byte.

Regardless of the programming of this bit, ATM cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the DELINDIS bit in this register is set to logic 1.

IDLEPASS

The IDLEPASS bit controls the function of the ATM Idle Cell filter. It is only valid when in ATM mode. When IDLEPASS is written with logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is enabled, the Idle Cell Header Pattern and Mask register bits are ignored. The default state of this bit and the bits in the RCFP Idle Cell Header and Mask Register enable the dropping of Idle cells.

DELINDIS

When DELINDIS is set to logic 1, all payload data read by the RCFP is passed to the FIFO interface without the requirement of having to find cell delineation or packet delineation first.

In ATM mode the DELINDIS bit is used to disable all ATM cell filtering and ATM cell delineation. If cell alignment has been reached before DELINDIS is enabled, then the current cell alignment position is kept.

In POS mode the DELINDIS bit is used to disable the HDLC flag alignment, byte destuffing and flag removal. The data stream is arbitrarily segmented into 64 byte long packets. FCS and descrambling operations still follow how they have been set in their respective configuration registers.

When DELINDIS mode is used, the RBY_MODE bit in register 0743H must be set for proper counter operation. If this is not done, the counters will be incorrect.

STRIP_SEL

The frame check sequence stripping bit (STRIP_SEL) selects the CRC stripping mode of the RCFP. When STRIP_SEL is logic 1, CRC stripping is enabled. When STRIP_SEL is logic 0, CRC stripping is disabled. Note that CRC_SEL[1:0] must not equal "00", (no CRC) for stripping to be enabled. When stripping is enabled, the received packet FCS or ATM cell HCS byte(s) are not passed to the RXSDQ FIFO. When STRIP is disabled, the received packet FCS are transferred over the FIFO interface. When DELINDIS is enabled, packets and cells are not delineated therefore the value of STRIP_SEL is ignored. **The STRIP_SEL bit must be set to logic 1 if working in ATM mode.**

INVERT

The data inversion bit (INVERT) configures the processor to logically invert the incoming stream before processing it. When INVERT is set to logic 1, the stream is logically inverted before processing. When INVERT is set to logic 0, the stream is not inverted before processing.

POS_SEL

The Packet Over SONET (POS_SEL) bit selects the data type mode of the RCFP. When POS_SEL is logic 1, POS mode is selected. When POS_SEL is logic 0, ATM mode is selected.

Register 0741H: RCFP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	OCDV	X
Bit 8	R	LCDV	X
Bit 7	R/W	MINLE	0
Bit 6	R/W	MAXLE	0
Bit 5	R/W	ABRTE	0
Bit 4	R/W	XFERE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CRCE	0
Bit 1	R/W	OCDE	0
Bit 0	R/W	LCDE	0

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the ATM LCD state. When LCDE is set to logic 1, the interrupt is enabled.

OCDE

The OCDE bit enables the generation of an interrupt due to a change in ATM cell delineation state or packet Idle state. When OCDE is set to logic 1, the interrupt is enabled.

CRCE

The CRCE bit enables the generation of an interrupt due to the detection of an ATM HCS or packet FCS error. When CRCE is set to logic 1, the interrupt is enabled.

Reserved

The Reserved bit should be set to logic 0 for proper operation.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RCFP performance monitor counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set to logic 1, the interrupt is enabled.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set to logic 1, the interrupt is enabled.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set to logic 1, the interrupt is enabled.

LCDV

The LCDV bit gives the ATM Loss of Cell Delineation state. When LCDV is logic 1, an out of cell delineation (LCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCDV is logic 0, the RCFP has been in cell delineation for the number of cells specified in the RCFP LCD Count Threshold register. The cell time period can be varied by using the LCDC[10:0] register bits in the RCFP LCD Count Threshold register.

OCDV

The OCDV bit indicates the ATM cell delineation or packet out of frame alignment state. When OCDV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries or the packet processor is in out of frame alignment. When OCDV is logic 0, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO, or the packet processor is in frame alignment.

Register 0742H: RCFP Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	MINLI	X
Bit 6	R	MAXLI	X
Bit 5	R	ABRTI	X
Bit 4	R	XFERI	X
Bit 3	R	Reserved	X
Bit 2	R	CRCI	X
Bit 1	R	OCDI	X
Bit 0	R	LCDI	X

LCDI

The LCDI bit is set to logic 1 when there is a change in the loss of cell delineation (LCD) state. The current value of the LCD state is available through the LCDV bit in the RCFP Interrupt Enable and Status register (0x0741). This interrupt can be masked using LCDE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

OCDI

The OCDI bit is set to logic 1 when the RCFP ATM cell processor enters or exits the SYNC state or the packet processor enters or exits the frame alignment state. This interrupt can be masked using OCDE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

CRCI

The CRCI bit is set to logic 1 when an ATM HCS or packet FCS error is detected. This interrupt can be masked using CRCE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Reserved

This bit is not used.

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. Logic 1 in this bit position indicates that the RCFP performance monitor counter holding registers have been updated. This update is initiated by writing to one of the counter register locations, or by writing to address 0000H. This interrupt can be masked using XFERE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

ABRTI

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

MAXLI

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

MINLI

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0743H: RCFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MINPL[7]	0
Bit 14	R/W	MINPL[6]	0
Bit 13	R/W	MINPL[5]	0
Bit 12	R/W	MINPL[4]	0
Bit 11	R/W	MINPL[3]	0
Bit 10	R/W	MINPL[2]	1
Bit 9	R/W	MINPL[1]	0
Bit 8	R/W	MINPL[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RBY_MODE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	0

All Reserved bits must be set to their default values for proper operation.

RBY_MODE

The receive byte counter mode (RBY_MODE) bit is used to select the mode in which the RBY_IC[39:0] counters work. When RBY_MODE is logic 0, RBY_IC[39:0] will count all bytes in received packets (including FCS and Abort bytes) after the byte destuffing operation. When RBY_MODE is logic 1, RBY_IC[39:0] will count all bytes in received packets (including FCS, Abort, and stuff bytes) before the byte destuffing operation. Flag bytes will not be counted in either case. The RBY_MODE bit is only valid when working in POS mode. For correct counting, RBY_MODE must be set when using the DELINDIS mode in register 0740H.

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame after destuffing but including the FCS. The default minimum packet length is 4 octets. If STRIP_SEL in register 0740H is set to logic 1, then MINPL should be set to at least 4 plus the number of CRC bytes – i.e. either 6 or 8. If STRIP_SEL is logic 0, then MINPL should be set to a value greater than or equal to 5.

Register 0744H: RCFP Maximum Packet Length

Bit	Type	Function	Default
Bit 15	R/W	MAXPL[16]	0
Bit 14	R/W	MAXPL[15]	0
Bit 13	R/W	MAXPL[14]	0
Bit 12	R/W	MAXPL[13]	0
Bit 11	R/W	MAXPL[12]	0
Bit 10	R/W	MAXPL[11]	0
Bit 9	R/W	MAXPL[10]	1
Bit 8	R/W	MAXPL[9]	1
Bit 7	R/W	MAXPL[8]	0
Bit 6	R/W	MAXPL[7]	0
Bit 5	R/W	MAXPL[6]	0
Bit 4	R/W	MAXPL[5]	0
Bit 3	R/W	MAXPL[4]	0
Bit 2	R/W	MAXPL[3]	0
Bit 1	R/W	MAXPL[2]	0
Bit 0	R/W	MAXPL[1]	0

MAXPL[16:1]

The Maximum Packet Length (MAXPL[16:0]) bits are used to set the maximum packet length. Only the top 16 bits of this 17 bit value are programmable. MAXPL[0] is automatically set to logic 0. Packets larger than this length are terminated and marked with an error. The remainder of the packet is discarded. This Maximum Packet Length defaults to 1.5 Kbytes. The packet length used here is defined as the number of bytes encapsulated into the POS frame excluding byte stuffing but including the FCS. The default maximum packet length is 1536 octets. The maximum packet length allowed is 128 Kbytes less 2 (131070 bytes). The value of MAXPL[16:1] must be greater than or equal to 0x03 but less than or equal to 0xFFFA.

Register 0745H: RCFP LCD Count Threshold

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LCDC[10]	0
Bit 9	R/W	LCDC[9]	0
Bit 8	R/W	LCDC[8]	1
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until the receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360. For STS-48c, the average cell period is 176.9 ns and the default LCD integrate period is 63.8 μs.

Register 0746H: RCFP Idle Cell Header and Mask

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[3]	0
Bit 10	R/W	PTI[2]	0
Bit 9	R/W	PTI[1]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to this register to select the bits included in the cell filter. Logic 1 in this bit position enables the CLP bit in the pattern register to be compared. Logic 0 causes the masking of the CLP bit. The default enables the register bit comparison.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. A logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. A logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header field to select the bits included in the cell filter. Logic 1 in any bit position enables the corresponding bit in the pattern register to be compared. Logic 0 causes the masking of the corresponding bit. The default enables the register bit comparison.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bit. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header and Mask register bits. The IDLEPASS bit in the RCFP Configuration Register must be set to logic 0 to enable dropping of cells matching this pattern.

Note that an all-zeros pattern must be present in the VPI and VCI fields of the Idle or unassigned cell.

Register 0747H: RCFP Receive Byte/Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[15:0]	XXXX

Register 0748H: RCFP Receive Byte/Idle Cell Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RBY_IC[31:16]	XXXX

Register 0749H: RCFP Receive Byte/Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XXXX
Bit 7 to Bit 0	R	RBY_IC[39:32]	XXXX

RBY_IC[39:0]

When POS mode is selected, the RBY_IC[39:0] bits indicate the number of bytes received within POS frames during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes in the count is controlled by the RBY_MODE register bit. HDLC flags are not counted. In either mode, an abort sequence (0x7d7e) is counted as one byte.

When ATM mode is selected, the RBY_IC[39:0] bits indicate the number of Idle cells received and passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor counter registers loads the registers with the current counter value and resets the internal 40 bit counter to 4,3,2,1 or 0. The counter reset value is dependent on if there were counter events during the transfer of the count to RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 074AH: RCFP Packet/Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[15:0]	XXXX

Register 074BH: RCFP Receive Packet/ATM Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	RP_RC[31:16]	XXXX

RP_RC[31:0]

When POS mode is selected, the RP_RC[31:0] bits indicate the number of received good packets passed to the FIFO interface during the last accumulation interval.

When ATM mode is selected, the RP_RC[31:0] bits indicate the number of received ATM cells passed to the FIFO interface in the last accumulation interval.

A write to any one of the RCFP performance monitor Counter registers loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the RCFP performance monitor Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 074CH: RCFP Receive Erroneous FCS/HCS Counter

Bit	Type	Function	Default
Bit 15	R	EFCS[15]	X
Bit 14	R	EFCS[14]	X
Bit 13	R	EFCS[13]	X
Bit 12	R	EFCS[12]	X
Bit 11	R	EFCS[11]	X
Bit 10	R	EFCS[10]	X
Bit 9	R	EFCS[9]	X
Bit 8	R	EFCS[8]	X
Bit 7	R	EFCS[7]/EHCS[7]	X
Bit 6	R	EFCS[6]/EHCS[6]	X
Bit 5	R	EFCS[5]/EHCS[5]	X
Bit 4	R	EFCS[4]/EHCS[4]	X
Bit 3	R	EFCS[3]/EHCS[3]	X
Bit 2	R	EFCS[2]/EHCS[2]	X
Bit 1	R	EFCS[1]/EHCS[1]	X
Bit 0	R	EFCS[0]/EHCS[0]	X

EFCS[15:0]

When POS mode is selected, the EFCS[15:0] bits indicate the number of received FCS errors during the last accumulation interval. The FCS calculation will proceed independent of any errors detected upstream. Thus, under abort, max length violations, etc, one might get FCS violations as well.

EHCS[7:0]

When ATM mode is selected, the EHCS[7:0] bits indicate the number of HCS errors received in the last accumulation interval.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counters to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 074DH: RCFP Receive Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	RABR[15]	X
Bit 14	R	RABR[14]	X
Bit 13	R	RABR[13]	X
Bit 12	R	RABR[12]	X
Bit 11	R	RABR[11]	X
Bit 10	R	RABR[10]	X
Bit 9	R	RABR[9]	X
Bit 8	R	RABR[8]	X
Bit 7	R	RABR[7]	X
Bit 6	R	RABR[6]	X
Bit 5	R	RABR[5]	X
Bit 4	R	RABR[4]	X
Bit 3	R	RABR[3]	X
Bit 2	R	RABR[2]	X
Bit 1	R	RABR[1]	X
Bit 0	R	RABR[0]	X

RABR[15:0]

When POS mode is selected, the RABR[15:0] bits indicate the number of aborted packets received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Aborted Packet Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 074EH: RCFP Receive Minimum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMINL[15]	X
Bit 14	R	RMINL[14]	X
Bit 13	R	RMINL[13]	X
Bit 12	R	RMINL[12]	X
Bit 11	R	RMINL[11]	X
Bit 10	R	RMINL[10]	X
Bit 9	R	RMINL[9]	X
Bit 8	R	RMINL[8]	X
Bit 7	R	RMINL[7]	X
Bit 6	R	RMINL[6]	X
Bit 5	R	RMINL[5]	X
Bit 4	R	RMINL[4]	X
Bit 3	R	RMINL[3]	X
Bit 2	R	RMINL[2]	X
Bit 1	R	RMINL[1]	X
Bit 0	R	RMINL[0]	X

RMINL[15:0]

When POS mode is selected, the RMINL[15:0] bits indicate the number of minimum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Minimum Length Packet Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 074FH: RCFP Receive Maximum Length Packet Error Counter

Bit	Type	Function	Default
Bit 15	R	RMAXL[15]	X
Bit 14	R	RMAXL[14]	X
Bit 13	R	RMAXL[13]	X
Bit 12	R	RMAXL[12]	X
Bit 11	R	RMAXL[11]	X
Bit 10	R	RMAXL[10]	X
Bit 9	R	RMAXL[9]	X
Bit 8	R	RMAXL[8]	X
Bit 7	R	RMAXL[7]	X
Bit 6	R	RMAXL[6]	X
Bit 5	R	RMAXL[5]	X
Bit 4	R	RMAXL[4]	X
Bit 3	R	RMAXL[3]	X
Bit 2	R	RMAXL[2]	X
Bit 1	R	RMAXL[1]	X
Bit 0	R	RMAXL[0]	X

RMAXL[15:0]

When POS mode is selected, the RMAXL[15:0] bits indicate the number of maximum length packet errors received during the last accumulation interval. This counter is held at value 0 when ATM mode is selected.

A write to any one of the RCFP performance monitor registers loads the registers with the current counter value and resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Maximum Length Packet Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 0750H: TCFP Configuration

Bit	Type	Function	Default
Bit 15	R/W	FIFO_ERRE	0
Bit 14	R/W	FIFO_UDRE	0
Bit 13	R/W	XFERE	0
Bit 12		Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	DELINDIS	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	POS_SEL	0
Bit 7	R/W	CRC_SEL[1]	1
Bit 6	R/W	CRC_SEL[0]	1
Bit 5	R/W	FLAG[3]	0
Bit 4	R/W	FLAG[2]	0
Bit 3	R/W	FLAG[1]	0
Bit 2	R/W	FLAG[0]	0
Bit 1	R/W	SCRMBL	1
Bit 0	R/W	PROV	0

All Reserved bits must be set to their default values for proper operation.

PROV

The processor provision bit (PROV) is used to enable the TCFP. When PROV is logic 0, the TCFP ATM and packet processors are disabled and will not request data from the TXSDQ FIFO interface and will respond to data requests with all 1's data. When PROV is logic 1, the TCFP ATM or packet processor is enabled and will respond to data requests with valid data after requesting and processing data from the TXSDQ FIFO interface.

SCRMBL

The SCRMBL bit controls the scrambling of the packet data stream or ATM cell payload. When SCRMBL is a logic 1, scrambling is enabled. When SCRMBL is a logic 0, scrambling is disabled.

FLAG[3:0]

The flag insertion control (FLAG[3:0]) configures the minimum number of flag bytes the packet processor inserts between packets. The minimum number of flags (01111110) inserted between packets is shown in the table below. FLAG[3:0] are used only in POS mode. This register is to be a static value; it should not be modified during normal operation.

Table 13 Selection of the Number of Flag Bytes

FLAG[3:0]	Minimum Number of FLAG Bytes
0000	1 flag
0001	2 flags
0010	4 flags
0011	8 flags
0100	16 flags
0101	32 flags
0110	64 flags
0111	128 flags
1000	256 flags
1001	512 flags
1010	1024 flags
1011	2048 flags
1100	4096 flags
1101	8192 flags
1110	16384 flags
1111	32768 flags

CRC_SEL[1:0]

The CRC select (CRC_SEL[1:0]) bits allow the control of the CRC calculation according to the table below. For ATM cells, the CRC is calculated over the first four ATM header bytes. For packet applications, the CRC is calculated over the whole packet data, before byte stuffing and scrambling. For idle cells, the CRC-8 is always inserted and the coset polynomial is added.

Table 14 CRC Mode Selection

CRC_SEL[1:0]	HCS Operation	FCS Operation
00	Reserved	No FCS inserted
01	Reserved	No FCS inserted
10	CRC-8 without coset polynomial	CRC-CCITT (2 bytes)
11	CRC-8 with coset polynomial added	CRC-32 (4 bytes)

POS_SEL

The POS_SEL bit enables the POS HDLC frame processing mode. When POS_SEL is set to logic 1, POS processing will occur. When POS_SEL is set to logic 0, ATM mode is selected.

DELINDIS

The DELINDIS (POS delineation control bit) enables the carriage of unmodified POS traffic. In POS mode, flags are not inserted (unless in FIFO underrun) and stuffing is disabled. FCS insertion and scrambling are still controlled by CRC_SEL and SCRMBL.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the transmitted packet/cell counter, transmitted byte counter, and aborted packet counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

FIFO_UDRE

The FIFO_UDRE bit enables the generation of an interrupt due to a FIFO underrun. When FIFO_UDRE is set to logic 1, the interrupt is enabled and the INTB signal will be set to logic 0 whenever FIFO_UNRI is set to logic 1.

FIFO_ERRE

The FIFO_ERRE bit enables the generation of an interrupt due to a FIFO error. When FIFO_ERRE is set to logic 1, the interrupt is enabled and the INTB signal will be set to logic 0 whenever FIFO_ERRI is set to logic 1.

Register 0751H: TCFP Interrupt Indication

Bit	Type	Function	Default
Bit 15	R	FIFO_ERRI	X
Bit 14	R	FIFO_UDRI	X
Bit 13	R	XFERI	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

XFERI

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the transmitted cell/packet counter, transmitted byte counter, and aborted packet counter holding registers have been updated. This update is initiated by writing to one of the TCFP counter register locations, or initiating a global performance monitor update by writing to register 0000H. XFERI is set to logic 0 when this register is read. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

FIFO_UDRI

The FIFO_UDRI bit is set high when an attempt is made to read from the FIFO while it is empty. This is considered a system error. The FIFO_UDRI bit is set to logic 0 immediately after a read to this register. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

FIFO_ERRI

This bit is set to one when an error is detected on the read side of the FIFO. An error can be caused by an abnormal sequence of TSOP and TEOP signals or the assertion of FIFO_ERR. Such errors are normally caused by a previous FIFO overrun or underrun condition or a user asserted error from the POS-PHY L3 interface. The FIFO_ERRI bit is reset immediately after a read to this register. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0752H: TCFP Idle/Unassigned ATM Cell Header

Bit	Type	Function	Default
Bit 15	R/W	GFC[3]	0
Bit 14	R/W	GFC[2]	0
Bit 13	R/W	GFC[1]	0
Bit 12	R/W	GFC[0]	0
Bit 11	R/W	PTI[2]	0
Bit 10	R/W	PTI[1]	0
Bit 9	R/W	PTI[0]	0
Bit 8	R/W	CLP	1
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] (Idle Cell Payload) value reflects the payload bytes which will be inserted into the ATM Idle cell generated by the TCFP.

CLP

The CLP (Cell Loss Priority) bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

PTI[2:0]

The PTI[2:0] (Payload Type) bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TCFP detects that no outstanding cells are available from the external FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode.

GFC[3:0]

The GFC[3:0] (Generic Flow Control) bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TCFP detects that no outstanding cells are available from the FIFO and data is requested on the TCFP egress interface. Additionally, XOFF can be used to force the transmission of Idle/Unassigned cells in ATM mode. The all zeros pattern is transmitted in the VCI and VPI fields of the idle/unassigned cell.

Register 0753H: TCFP Diagnostics

Bit	Type	Function	Default
Bit 15	R/W	DCRC[7]	0
Bit 14	R/W	DCRC[6]	0
Bit 13	R/W	DCRC[5]	0
Bit 12	R/W	DCRC[4]	0
Bit 11	R/W	DCRC[3]	0
Bit 10	R/W	DCRC[2]	0
Bit 9	R/W	DCRC[1]	0
Bit 8	R/W	DCRC[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TX_BYTE_MODE	0
Bit 4	R/W	XOFF	0
Bit 3	R/W	INVERT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

All Reserved bits must be set to their default values for proper operation.

INVERT

The data inversion bit (INVERT) configures the ATM or packet processor to logically invert the outgoing data stream. When INVERT is set to logic 1, the outgoing data stream is logically inverted. The outgoing data stream is not inverted when INVERT is set to logic 0.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic 0, ATM cells or packets are transmitted normally. When XOFF is set to logic 1, the cell or packet currently being transmitted is completed and then transmission is suspended. When XOFF is set to logic 1, the TCFP will request data from the FIFO until its own internal FIFO is full (maximum 56 bytes). ATM Idle cells or HDLC flags will be sent on the TCFP egress interface.

TX_BYTE_MODE

The transmit byte counter mode (TX_BYTE_MODE) bit is used to select the mode in which the TX_BYTE[39:0] counters work. When TX_BYTE_MODE is logic 0, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS and Abort bytes) before the byte stuffing operation. When TX_BYTE_MODE is logic 1, TX_BYTE[39:0] will count all bytes in transmitted packets (including FCS, Abort, and stuff bytes) after the byte stuffing operation. Flag bytes will not be counted in either case. The TX_BYTE_MODE bit is only valid when working in POS mode.

DCRC[7:0]

The diagnostic CRC word (DCRC[7:0]) configures the ATM or packet processor to logically invert bits in the inserted CRC on the outgoing data stream for diagnostic purposes. When any bit in DCRC[7:0] is set to logic 1, the corresponding bit in the FCS value inserted by the POS processor or the HCS value inserted by the ATM processor is logically inverted. DCRC[7:0] is ignored when no FCS is inserted. Each DCRC[x] bit will cause a bit error in each byte of the 2 byte or 4 byte FCS.

Register 0754H: TCFP Transmit Cell/Packet Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[15:0]	XXXX

Register 0755H: TCFP Transmit Cell/Packet Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_CELL[31:16]	XXXX

TX_CELL[31:0]

The TX_CELL[31:0] bits indicate the number of cells or non-aborted packets transmitted to the TCFP egress stream during the last accumulation interval. ATM Idle cells, HDLC flags, and HDLC Abort bytes inserted into the transmission stream are not counted.

A write to any one of the TCFP Transmit Cell/Packet Counter registers loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell/Packet Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 0756H: TCFP Transmit Byte Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[15:0]	XXXX

Register 0757H: TCFP Transmit Byte Counter

Bit	Type	Function	Default
Bit 15 to Bit 0	R	TX_BYTE[31:16]	XXXX

Register 0758H: TCFP Transmit Byte Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R	TX_BYTE[39:32]	XX

TX_BYTE[39:0]

The TX_ BYTE[39:0] bits indicate the number of bytes in packets transmitted to the TCFP egress stream during the last accumulation interval. The byte counts include all user payload bytes, FCS bytes, and abort bytes. Inclusion of stuffed bytes is controlled by the TX_BYTE_MODE register bit. HDLC flags are not counted. The TX_BYTE[39:0] counters are only valid when processing packets.

A write to any one of the TCFP counter registers loads the registers with the current counter value and resets the internal 40 bit counter to between 0 and 8. The counter reset value is dependent on if there were count events during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 0759H: TCFP Aborted Packet Counter

Bit	Type	Function	Default
Bit 15	R	TX_ABT[15]	X
Bit 14	R	TX_ABT[14]	X
Bit 13	R	TX_ABT[13]	X
Bit 12	R	TX_ABT[12]	X
Bit 11	R	TX_ABT[11]	X
Bit 10	R	TX_ABT[10]	X
Bit 9	R	TX_ABT[9]	X
Bit 8	R	TX_ABT[8]	X
Bit 7	R	TX_ABT[7]	X
Bit 6	R	TX_ABT[6]	X
Bit 5	R	TX_ABT[5]	X
Bit 4	R	TX_ABT[4]	X
Bit 3	R	TX_ABT[3]	X
Bit 2	R	TX_ABT[2]	X
Bit 1	R	TX_ABT[1]	X
Bit 0	R	TX_ABT[0]	X

TX_ABT[15:0]

The TX_ ABT[15:0] bits indicate the number of aborted packets transmitted to the TCFP egress stream during the last accumulation interval. These counters are only valid when processing packets.

A write to any one of the TCFP counter registers loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled regularly to avoid saturation.

To allow for synchronization update with all other blocks, writing to register 0000H will initiate a global performance counter update.

Register 0760H: RXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	Reserved	X
Bit 0	R/W	SDQRST	1

SDQRST

SDQRST is used to reset the RXSDQ. The RXSDQ comes up in reset. It should be taken out of reset by writing a 0 to the SDQRST bit. The user can reset the SDQ at any time by writing a 1 to this bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

Register 0761H: RXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	OFLE	0

The Reserved bit must be set to its default value for proper operation.

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

Register 0763H: RXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when there is a FIFO overflow condition. This bit is cleared when read by the user when WCIMODE is set to logic 0. It is cleared when written to logic 1 when WCIMODE is set to logic 1.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO identity. This field should contain the value "000000". Otherwise, a system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0768H: RXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	1
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO for which the user is setting up or reading the setup. This register is the common address used for the three indirect setup registers: 0769H FIFO Indirect Configuration, 076AH FIFO Indirect Buffer and 076BH Data Available Thresholds plus the 076CH FIFO Indirect Cells and Packets Count. See also section 13.19: Accessing Indirect Registers.

A FIFO needs to be configured according to a set of rules defined in the Operation section. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information.

PHYID[5:0]

This field should be set to all zeros.

EMPTY

This read-only indirect-access register bit indicates if the requested FIFO is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty. Note that a read to this register bit must be preceded by a write to this register with RWB (bit 14) set to logic 1, and the PHYID set to all-zeros. Then the register may be read and the EMPTY bit checked. See Section 13.19 for the procedure to access indirect register bits.

FLUSH

This is a write-only indirect-access register bit used to discard all the current data in a specified FIFO. Typically, this should be used if a non-empty FIFO needs to be reconfigured. Note that the RWB bit (bit 14 in this register) must be written to logic 0, and the PHYID set to all-zeros, at the same time as the FLUSH bit is set to logic 1. The user should then poll the EMPTY bit (bit 15 in this register) until it is logic 1, which indicates that the FLUSH is complete. The FLUSH bit must then be cleared to logic 0 before data can be passed to the RXSDQ. See Section 13.19 for the procedure to access indirect register bits.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When the RWB bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers RXSDQ FIFO Indirect Configuration, RXSDQ FIFO Indirect Data Available Threshold and RXSDQ FIFO Indirect Cells and Packets Count. When the RWB bit is set to 0, the user is writing the configuration of a FIFO.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If BUSY is sampled 1, the update is in progress. If BUSY is sampled 0, the information for the FIFO is available in the accessed register.

Register 0769H: RXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

See section 13.8: RXSDQ and TXSDQ Data Available and Burst-Size Operation for more information on configuring the TXSDQ, RXSDQ, TXPHY, and RXPHY. This register must be accessed via an indirect register read or write via register 0768H. See also section 13.19: Accessing Indirect Registers.

BLOCK_PTR[4:0]

Set this to value 00H.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the RXSDQ FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed are given in the Operation section.

For correct operation of the S/UNI-2488, this field must be set to 11.

FIFO_NUMBER[5:0]

This should be set to 00H.

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs.

ENABLE

Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data but does continue to assert Data Available internally until it is drained completely. During operation, FIFOs must be disabled before being reconfigured.

Register 076AH: RXSDQ FIFO Indirect Data Available Threshold

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

This register is used to set the Data Available Threshold for a FIFO. This threshold is explained in the Operation section. A FIFO does not need to be enabled to set this threshold. In order to change this value for a FIFO, the user should first disable it, write in the new value, and enable it again. See section 13.8: RXSDQ and TXSDQ Data Available and Burst-Size Operation for more information on configuring the TXSDQ, RXSDQ, TXPHY, and RXPHY. This register must be accessed via an indirect register read or write via register 0768H. See also section 13.19: Accessing Indirect Registers.

All Reserved bits must be set to their default values for proper operation.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the RXSDQ FIFO Indirect Address register's PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO. The absolute maximum value is DT[7:0] +1 = 16. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be set to a value of DT[7:0] = 3 (ATM cells are 4 Blocks long). Note that the RXPHY BURST_SIZE[3:0] value must be less than or equal to DT.

Register 076BH: RXSDQ FIFO Indirect Cells and Packets Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]

This register is used to read the 4-bit FIFO counters for the enabled FIFOs, which count the number of ATM cells or POS packets currently in the FIFO, modulo 4.

These read-only bits hold the last sampled count for the FIFO requested in the RXSDQ FIFO Indirect Address register's PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. When this counter reaches its maximum count, it rolls over. This register must be accessed via an indirect register read or write via register 0768H. See also section 13.19: Accessing Indirect Registers.

The counters provided by the RXSDQ are purely for diagnostic purposes. They should be ignored in normal operation.

Register 076CH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[15:0]	X

Register 076DH: RXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[31:16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the RXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. **When this counter reaches its maximum count, it rolls over.**

Register 076EH: RXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the RXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. **When this counter reaches its maximum count, it rolls over.**

Register 0770H: TXSDQ FIFO Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	Reserved	X
Bit 0	R/W	SDQRST	1

SDQRST

This bit is used to reset the TXSDQ. The TXSDQ comes up in reset. It should be taken out of reset by writing a 0 to the SDQRST bit. The user can reset the SDQ at any time by writing a 1 to the SDQRST bit, and then writing a 0. Reset flushes all the data in the FIFOs, resets the read and write pointers and resets all counters. The configuration information is not changed by Reset.

Register 0771H: TXSDQ FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	SOPE	0
Bit 1	R/W	EOPE	0
Bit 0	R/W	OFLE	0

The Reserved bit must be set to its default value for proper operation.

OFLE

When this bit is set to 1, FIFO overflows cause the INTB output to be asserted. If this bit is set to 0, FIFO overflows do not cause INTB to be asserted.

EOPE

When this bit is set to 1, bad EOP signals cause the INTB output to be asserted. If this bit is set to 0, bad EOP signals do not cause INTB to be asserted.

SOPE

When this bit is set to 1, bad SOP signals cause the INTB output to be asserted. If this bit is set to 0, bad SOP signals do not cause INTB to be asserted.

Register 0773H: TXSDQ FIFO Overflow Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	OFL_FIFO[5]	X
Bit 12	R	OFL_FIFO[4]	X
Bit 11	R	OFL_FIFO[3]	X
Bit 10	R	OFL_FIFO[2]	X
Bit 9	R	OFL_FIFO[1]	X
Bit 8	R	OFL_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	OFLI	X

OFLI

This bit is set when there is a FIFO overflow condition. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

OFL_FIFO[5:0]

These bits are used to indicate the FIFO identity. This field should contain the value "000000". Otherwise a system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0774H: TXSDQ FIFO EOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	EOP_FIFO[5]	X
Bit 12	R	EOP_FIFO[4]	X
Bit 11	R	EOP_FIFO[3]	X
Bit 10	R	EOP_FIFO[2]	X
Bit 9	R	EOP_FIFO[1]	X
Bit 8	R	EOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	EOPI	X

EOPI

This bit is set when two EOPs arrive consecutively on the FIFO without being separated by a SOP. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

EOP_FIFO[5:0]

These bits are used to indicate the FIFO identity. This field should contain the value "000000". Otherwise a system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0775H: TXSDQ FIFO SOP Error Port and Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R	SOP_FIFO[5]	X
Bit 12	R	SOP_FIFO[4]	X
Bit 11	R	SOP_FIFO[3]	X
Bit 10	R	SOP_FIFO[2]	X
Bit 9	R	SOP_FIFO[1]	X
Bit 8	R	SOP_FIFO[0]	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	SOPI	X

SOPI

This bit is set when two SOPs arrive consecutively on the FIFO without being separated by an EOP. This bit is cleared when read by the user when WCIMODE is set to logic 0. It is cleared when written to logic 1 when WCIMODE is set to logic 1.

SOP_FIFO[5:0]

These bits are used to indicate the FIFO identity. This field should contain the value "000000". Otherwise a system error should be declared. These bits are valid only when the interrupt bit is logic 1.

Register 0778H: TXSDQ FIFO Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13	W	FLUSH	0
Bit 12	R	EMPTY	1
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PHYID[5]	0
Bit 4	R/W	PHYID[4]	0
Bit 3	R/W	PHYID[3]	0
Bit 2	R/W	PHYID[2]	0
Bit 1	R/W	PHYID[1]	0
Bit 0	R/W	PHYID[0]	0

This is an indirect register that is used to specify the address of the FIFO for which the user is setting up or reading the setup. This register is the common address used for the three indirect setup registers: 0779H FIFO Indirect Configuration, 077AH FIFO Indirect Buffer and 077BH Data Available Thresholds plus the 077CH FIFO Indirect Cells and Packets Count. See also section 13.19: Accessing Indirect Registers.

A FIFO needs to be configured according to a set of rules defined in the Operation section. In order to change the current setup of a FIFO, it is recommended that the user reads the existing setup information first, makes any modifications as required, and writes back the information.

PHYID[5:0]

This field should be set to all zeros.

EMPTY

This read-only indirect-access register bit indicates if the requested FIFO is empty. When this bit is read as 1, the FIFO number specified in PHYID[5:0] in this register is empty. Before reconfiguring a disabled FIFO, this bit needs to be sampled at logic 1 indicating that the FIFO is empty. Note that a read to this register bit must be preceded by a write to this register with RWB (bit 14) set to logic 1, and the PHYID set to all-zeros. Then the register may be read and the EMPTY bit checked. See Section 13.19 for the procedure to access indirect register bits.

FLUSH

This is a write-only indirect-access register bit used to discard all the current data in a specified FIFO. Typically, this should be used if a non-empty FIFO needs to be reconfigured. Note that the RWB bit (bit 14 in this register) must be written to logic 0, and the PHYID set to all-zeros, at the same time as the FLUSH bit is set to logic 1. The user should then poll the EMPTY bit (bit 15 in this register) until it is logic 1, which indicates that the FLUSH is complete. The FLUSH bit must then be cleared to logic 0 before data can be passed to the TXSDQ. See Section 13.19 for the procedure to access indirect register bits.

RWB

This bit is used to indicate whether the user is writing the setup of a FIFO, or reading all setup information of a FIFO. This bit is used in conjunction with the BUSY bit. When this bit is set to 1, all the available setup information of the FIFO requested in PHYID[5:0] is available in the registers TXSDQ FIFO Indirect Configuration, TXSDQ FIFO Indirect Data Available Threshold, and TXSDQ FIFO Indirect Cells and Packets Count. When this bit is set to 0, the user is writing the configuration of a FIFO.

BUSY

This is a read-only bit is used to indicate to the user that the information requested for the FIFO specified in bits PHYID[5:0] is in the process of being updated. If BUSY is sampled 1, the update is in progress. If BUSY is sampled 0, the information for the FIFO is available in the accessed register.

Register 0779H: TXSDQ FIFO Indirect Configuration

Bit	Type	Function	Default
Bit 15	R/W	ENABLE	0
Bit 14	R/W	POS_SEL	0
Bit 13	R/W	FIFO_NUMBER[5]	0
Bit 12	R/W	FIFO_NUMBER[4]	0
Bit 11	R/W	FIFO_NUMBER[3]	0
Bit 10	R/W	FIFO_NUMBER[2]	0
Bit 9	R/W	FIFO_NUMBER[1]	0
Bit 8	R/W	FIFO_NUMBER[0]	0
Bit 7	R/W	FIFO_BS[1]	0
Bit 6	R/W	FIFO_BS[0]	0
Bit 5		Unused	X
Bit 4	R/W	BLOCK_PTR[4]	0
Bit 3	R/W	BLOCK_PTR[3]	0
Bit 2	R/W	BLOCK_PTR[2]	0
Bit 1	R/W	BLOCK_PTR[1]	0
Bit 0	R/W	BLOCK_PTR[0]	0

See section 13.8: RXSDQ and TXSDQ Data Available and Burst-Size Operation for more information on configuring the TXSDQ, RXSDQ, TXPHY, and RXPHY. This register must be accessed via an indirect register read or write via register 0778H. See also section 13.19: Accessing Indirect Registers.

BLOCK_PTR[4:0]

Set this to value 00H.

FIFO_BS[1:0]

This 2-bit number denotes the size in Blocks of FIFO for the PHYID specified in the TXSDQ FIFO Indirect Address register. The bandwidth is related to the size of the FIFO that will be allocated to the PHY. The values to be programmed are given in the Operation section.

For proper operation of the S/UNI-2488, this register field must be set to 11.

FIFO_NUMBER[5:0]

Set this to value 00H.

POS_SEL

This bit is set to 1 if the FIFO needs to be configured as a packet FIFO. By default, the FIFOs are configured as ATM cell FIFOs.

ENABLE

Writing a 0 to this bit disables a FIFO. If previously enabled, a disabled FIFO does not accept any new data but continues to assert Data Available internally until it is drained completely. During operation, FIFOs must be disabled before being reconfigured.

Register 077AH: TXSDQ FIFO Indirect Data and Buffer Available Thresholds

Bit	Type	Function	Default
Bit 15	R/W	DT[7]	0
Bit 14	R/W	DT[6]	0
Bit 13	R/W	DT[5]	0
Bit 12	R/W	DT[4]	0
Bit 11	R/W	DT[3]	0
Bit 10	R/W	DT[2]	0
Bit 9	R/W	DT[1]	1
Bit 8	R/W	DT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	BT[4]	0
Bit 3	R/W	BT[3]	0
Bit 2	R/W	BT[2]	0
Bit 1	R/W	BT[1]	1
Bit 0	R/W	BT[0]	1

This register is used to set the Data and Buffer Available Thresholds for a FIFO. These thresholds are explained in the Operation section. A FIFO does not need to be enabled to set this threshold. In order to change a value for a FIFO, the user should first disable it, write in the new value, and enable it again. See section 13.8: RXSDQ and TXSDQ Data Available and Burst-Size Operation for more information on configuring the TXSDQ, RXSDQ, TXPHY, and RXPHY. This register must be accessed via an indirect register read or write via register 0778H. See also section 13.19: Accessing Indirect Registers.

BT[4:0]

These bits specify the Buffer Available threshold for the FIFO specified in PHYID[5:0] bits in the TXSDQ FIFO Indirect Address register. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to BT[4:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is BT[4:0] +1 = 32. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be set to a value of BT[4:0] = 3 since ATM cells are 4 blocks in size.

DT[7:0]

These bits specify the Data Available threshold for the FIFO selected by the TXSDQ FIFO Indirect Address register PHYID[5:0] bits. When this threshold is being set, these bits are written to by the user, and when this threshold is being read, these bits hold the previously configured data. The threshold is equal to DT[7:0] + 1.

This threshold is set in 16 byte Blocks. This threshold can never be greater than the size of the FIFO being configured, and the absolute maximum value is DT[7:0] +1 = 192. This number should be a standard fraction of the FIFO size in blocks. In the case of ATM FIFOs, this number should be set to a value of DT[7:0] = 3 (ATM cells are 4 blocks long).

The DT[7:0] threshold sets the level at which the cell/packet processors (TCFP) blocks can begin transmission of a cell or packet. Once transmission of a cell or packet begins, it cannot be stopped so this threshold should be set to a value which guarantees that the Utopia/POS-PHY interface can write to the FIFO in due time to prevent FIFO underruns. For packet data, it is recommended that DT[7:0] be set to a larger value about equal to 1/2 or 2/3 the size of the FIFO.

Register 077BH: TXSDQ FIFO Indirect Cells and Packets Count

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	COUNT[3]	X
Bit 2	R	COUNT[2]	X
Bit 1	R	COUNT[1]	X
Bit 0	R	COUNT[0]	X

COUNT[3:0]

This register is used to read the 4-bit FIFO counters for the enabled FIFOs, which count the number of ATM cells or POS packets currently in the FIFO, modulo 4.

These read-only bits hold the last sampled count for the FIFO requested in the RXSDQ FIFO Indirect Address register's PHYID[5:0] bits. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. When this counter reaches its maximum count, it rolls over. This register must be accessed via an indirect register read or write via register 0778H. See also section 13.19: Accessing Indirect Registers.

Register 077CH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[15:0]	X

Register 077DH: TXSDQ FIFO Cells and Packets Accepted Aggregate Count (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	ACOUNT[31:16]	X

ACOUNT[31:0]

These bits display the aggregate count of all the POS packets and ATM cells that are accepted by the TXSDQ. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. When this counter reaches its maximum count, it rolls over.

Register 077EH: TXSDQ FIFO Cells and Packets Dropped Aggregate Count

Bit	Type	Function	Default
Bit 15	R	DCOUNT[15]	X
Bit 14	R	DCOUNT[14]	X
Bit 13	R	DCOUNT[13]	X
Bit 12	R	DCOUNT[12]	X
Bit 11	R	DCOUNT[11]	X
Bit 10	R	DCOUNT[10]	X
Bit 9	R	DCOUNT[9]	X
Bit 8	R	DCOUNT[8]	X
Bit 7	R	DCOUNT[7]	X
Bit 6	R	DCOUNT[6]	X
Bit 5	R	DCOUNT[5]	X
Bit 4	R	DCOUNT[4]	X
Bit 3	R	DCOUNT[3]	X
Bit 2	R	DCOUNT[2]	X
Bit 1	R	DCOUNT[1]	X
Bit 0	R	DCOUNT[0]	X

DCOUNT[15:0]

These bits display the aggregate count of all the POS packets and ATM cells that are dropped by the TXSDQ due to FIFO overflows. This register is latched when register 0000H is written to for a global performance monitor update. After the count is latched into the register, the internal counter is reset to 0 and starts counting again. When this counter reaches its maximum count, it rolls over.

Register 0780H: RXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	RSXPAUSE[1]	0
Bit 12	R/W	RSXPAUSE[0]	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved1	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	RXPRST	1

All Reserved bits must be set to their default values for proper operation.

RXPRST

The RXPRST bit is used to reset the RXPHY circuitry. When RXPRST is set to logic zero, the RXPHY operates normally. When RXPRST is set to logic one, the RXPHY ignores all pin inputs but the register bits may be accessed for purposes of initialization. The RXPHY deasserts all outputs until logic zero is written to RXPRST.

ODDPARITY

The ODDPARITY bit is used to set the parity generated by the RXPHY for the UL3 or POS L3 interface. When set to logic 1, odd parity is generated. When set to logic 0, even parity is generated.

Reserved

The Reserved bits should be set to logic 0 for proper operation.

Reserved1

The Reserved1 bit should be set to logic1 for proper operation.

RSXPAUSE[1:0]

RSXPAUSE bits control the width of the RSX cycle in POS-PHY Level 3 operation. The width of the RSX pulse is equal to RSXPAUSE + 1. For example, setting of '00' will result in an RSX cycle of one cycle wide. A setting of '01' will make the RSX pulse two clock cycles wide. These bits should only be changed when the RSPRST is logic one.

Register 0781H: RXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

In UTOPIA, the RENB was detected as being deasserted before appropriate time at end of the cell transfer. The cell will continue to be transferred as per the UTOPIA Level 3™ specification, but this indicates that there may be a configuration mismatch between the RXPHY and the downstream device. A possible cause is the incorrect setting of the size of the cell expected by this interface. The RUNTCELLI bit is cleared when read by the user when WCIMODE is set to logic 0. It is cleared when written to logic 1 when WCIMODE is set to logic 1..

Register 0782H: RXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable RUNTCELLI signal to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Register 0783H: RXPHY Indirect Burst Size

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CONFIG_RWB	0
Bit 13	R/W	PHY_ADDR[5]	0
Bit 12	R/W	PHY_ADDR[4]	0
Bit 11	R/W	PHY_ADDR[3]	0
Bit 10	R/W	PHY_ADDR[2]	0
Bit 9	R/W	PHY_ADDR[1]	0
Bit 8	R/W	PHY_ADDR[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	BURST_SIZE[3]	0
Bit 2	R/W	BURST_SIZE[2]	0
Bit 1	R/W	BURST_SIZE[1]	1
Bit 0	R/W	BURST_SIZE[0]	1

The RXPHY Indirect Burst Size register is an indirect address and data register. The register is used only in POS-PHY mode of operation. See section 13.8: RXSDQ and TXSDQ Data Available and Burst-Size Operation for more information on configuring the TXSDQ, RXSDQ, TXPHY, and RXPHY.

BURST_SIZE[3:0]

The BURST_SIZE data register is provided to program the allowable burst size for the PHY. The size of a burst is BURST_SIZE + 1. For example, a BURST_SIZE[3:0] = “0000” indicates a burst size of one block. A block is equal to 16 bytes and takes 4 clocks to transfer. The 4 bits of BURST_SIZE allow the maximum burst to be 16 blocks (256 bytes), per PHY. .BURST_SIZE[3:0] must be set to a value less than or equal to the RXSDQ DT[7:0] value in Register 076AH.

This register is generally used only in POS-PHY L3 mode. However, for ATM cell transfers , it is recommended that BURST_SIZE be set to a multiple of 4 blocks to avoid cell fragmentation.

PHY_ADDR[5:0]

The PHY_ADDR bits are an indirect address that is used with BURST_SIZE data. The two allow indirect address reads and writes using a small amount of external address space. The PHY_ADDR is used with CONFIG_RWB and BUSY to command reads and writes. For the S/UNI-2488, PHY_ADDR[5:0] must be set to zero.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data for PHY_ADDR and will be placed in the BURST_SIZE register. A value of '0' means that a write of the information in BURST_SIZE will be performed for PHY channel address PHY_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate that a read or write operation is currently being executed. A value of '1' means the operation is in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further accesses.

Register 0784H: RXPHY Calendar Length

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	CALENDAR_LENGTH[6]	0
Bit 5	R/W	CALENDAR_LENGTH[5]	0
Bit 4	R/W	CALENDAR_LENGTH[4]	0
Bit 3	R/W	CALENDAR_LENGTH[3]	0
Bit 2	R/W	CALENDAR_LENGTH[2]	0
Bit 1	R/W	CALENDAR_LENGTH[1]	0
Bit 0	R/W	CALENDAR_LENGTH[0]	0

CALENDAR_LENGTH[6:0]

The CALENDAR_LENGTH register is provided to program the length of calendar used for servicing up to a maximum of 128 entries. Please see the RXPHY Calendar Indirect Address Data register. The number of entries is equal to CALENDAR_LENGTH + 1. For the S/UNI-2488, this register must be set to all zeros.

Register 0785H: RXPHY Calendar Indirect Address Data

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	CALENDAR_ADDR[6]	0
Bit 13	R/W	CALENDAR_ADDR[5]	0
Bit 12	R/W	CALENDAR_ADDR[4]	0
Bit 11	R/W	CALENDAR_ADDR[3]	0
Bit 10	R/W	CALENDAR_ADDR[2]	0
Bit 9	R/W	CALENDAR_ADDR[1]	0
Bit 8	R/W	CALENDAR_ADDR[0]	0
Bit 7	R/W	CONFIG_RWB	0
Bit 6		Unused	X
Bit 5	R/W	CALENDAR_DATA[5]	0
Bit 4	R/W	CALENDAR_DATA[4]	0
Bit 3	R/W	CALENDAR_DATA[3]	0
Bit 2	R/W	CALENDAR_DATA[2]	0
Bit 1	R/W	CALENDAR_DATA[1]	0
Bit 0	R/W	CALENDAR_DATA[0]	0

The RXPHY Calendar Indirect Address Data register is an indirect address and data register. The register is used in POS-PHY mode of operation

CALENDAR_DATA[5:0]

The CALENDAR_DATA register is provided to program the PHY address number to be serviced in the calendar sequence. The calendar consists of a maximum of 128 entries where the CALENDAR_ADDR is used to access one of the 128 (or less) entries to either write or read CALENDAR_DATA. CALENDAR_DATA is the PHY address to be serviced during the sequence associated with CALENDAR_ADDR. The length of the calendar is set in the RXPHY Calendar Length register. For the S/UNI-2488, this register should be set to all zeros.

CALENDAR_ADDR[6:0]

The CALENDAR_ADDR register is an indirect address register that is used with CALENDAR_DATA register. The two registers together allow indirect address reads and writes using a small amount of external address space. The CALENDAR_ADDR is used with CONFIG_RWB and BUSY to command reads and writes.

CONFIG_RWB

The CONFIG_RWB register allows the indirect addressing method to specify whether a read or write is being performed. A value of '1' means that a read is to be performed on the data at CALENDAR_ADDR and will be placed in the CALENDAR_DATA register. A value of '0' means that a write of the information in CALENDAR_DATA will be performed at address CALENDAR_ADDR.

BUSY

The BUSY bit is used in indirect addressing to indicate the operation of read or write is currently being executed. A value of '1' means the operation is currently in progress and the microprocessor should wait. A value of '0' means the operation is finished and the microprocessor may proceed with further access.

Register 0786H: RXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	POS_FIELD[7]	0
Bit 14	R/W	POS_FIELD[6]	0
Bit 13	R/W	POS_FIELD[5]	0
Bit 12	R/W	POS_FIELD[4]	0
Bit 11	R/W	POS_FIELD[3]	0
Bit 10	R/W	POS_FIELD[2]	0
Bit 9	R/W	POS_FIELD[1]	0
Bit 8	R/W	POS_FIELD[0]	1
Bit 7	R/W	ATM_FIELD[7]	0
Bit 6	R/W	ATM_FIELD[6]	0
Bit 5	R/W	ATM_FIELD[5]	0
Bit 4	R/W	ATM_FIELD[4]	0
Bit 3	R/W	ATM_FIELD[3]	0
Bit 2	R/W	ATM_FIELD[2]	0
Bit 1	R/W	ATM_FIELD[1]	0
Bit 0	R/W	ATM_FIELD[0]	0

The RXPHY Data Type Field register is used in POS-PHY L3 mode of operation only and identifies the type of traffic, ATM or packet, being sent over the POS-PHY L3 interface. ATM or packet PHYs are selected using the POS_SEL bits in the RXSDQ FIFO Indirect Configuration register.

ATM_FIELD[7:0]

The ATM_FIELD register is provided to identify ATM cell transfers over the POS-PHY L3 interface. When the outgoing data is an ATM cell, the ATM_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (i.e. when RSX is logic 1).

POS_FIELD[7:0]

The POS_FIELD register is provided to identify packet data transfers over the POS-PHY L3 interface. When the outgoing data is packet data, the POS_FIELD[7:0] is inserted in RDAT[31:24] at the cycle in which the in-band address is inserted in RDAT[5:0] (i.e. when RSX is logic 1).

Register 0788H: TXPHY Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	TPAHOLD	0
Bit 6	R/W	Reserved0	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PARERREN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ODDPARITY	0
Bit 0	R/W	TXPRST	1

All Reserved bits must be set to their default values for proper operation.

TXPRST

The TXPRST bit is used to reset the TXPHY circuitry. When TXPRST is set to logic zero, the TXPHY operates normally. When TXPRST is set to logic one, the TXPHY ignores all pin inputs but the registers may be accessed for initialization. The TXPHY deasserts all outputs until a logic zero is written to TXPRST.

ODDPARITY

The ODDPARITY bit is used to set the type of parity that is checked by the TXPHY. When set to logic 1, odd parity is expected. When set to logic 0, even parity is expected.

PARERREN

When set to logic 1, PARERREN will enable the TXPHY to pass an error signal to the TXSDQ upon detection of a parity error. This will cause the packet to be aborted by the packet processor. This bit has no effect on ATM cells with parity errors. This bit must be set while TXPRST is logic one.

Reserved0

This bit must be set to logic 0 for proper operation.

TPAHOLD

TPAHOLD can be used for systems where the PL3 is burst-based. Because it's burst based, between every burst, TENB must be logic 1. This is just a cycle that separates bursts.

With TPAHOLD = 1, the DTPA signal will respond (-> 0) with the minimum 1 cycle delay. With TPAHOLD =0, the response is 5 cycles.

TPAHOLD = 1 will allow the user to more fully utilize the entire FIFO when the buffer threshold is set to 2*burst size.

See Section 13.12 for more information. This bit cannot be changed during operation and can only be changed when TXPRST is logic 1.

Register 0789H: TXPHY Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	Reserved	X
Bit 1	R	TPARERRI	X
Bit 0	R	RUNTCELLI	X

RUNTCELLI

The RUNTCELLI bit indicates that TENB was detected as being deasserted before the end of the cell transfer when operating in UTOPIA Level 3™ mode. This will result in a partial cell transfer and an erroneous cell will be passed to the TXSDQ. Possible causes are incorrect setting in the size of the cell expected by this interface. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

TPARERRI

The TPARERR bit is used to indicate that a Parity Error was observed on the incoming TDAT bus since the last time the interrupt was read. The packet will be marked erroneous and sent on to the TXSDQ. ATM cell transmission is not affected by parity errors. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 078AH: TXPHY Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	TPARERRE	0
Bit 0	R/W	RUNTCELLE	0

RUNTCELLE

The RUNTCELLE bit is used to enable the detection of the runt cell condition (RUNTCELLI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

TPARERRE

The TPARERRE bit is used to enable the detection of a parity error (TPARERRI) to assert a hardware interrupt on the INTB pin. When set to logic 0, the hardware interrupt is masked. When set to logic 1, the hardware interrupt is enabled.

Reserved

This Reserved bit must be set to logic 0 for proper operation.

Register 078BH: TXPHY Data Type Field

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

These Reserved bits should be left in their default state for proper operation.

Register 0790H: SIRP Configuration Timeslot

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TS1_FORCE_LCD	0
Bit 4	R/W	TS1_RDI20F	0
Bit 3	R/W	TS1_ERDI	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	TS1_PROV	0

All Reserved bits must be set to their default values for proper operation.

TS1_PROV

TS1_PROV suppresses the flow of data through the SIRP. For proper operation of the S/UNI 2488, the TS1_PROV must be set to 1 except when TPAIS_EN (bit 3 register 0002H) is asserted. TS1_PROV should be set to logic 0 only when transmit path AIS is to be generated.

TS1_ERDI

The TS1_ERDI bit selects between normal and extended RDI encoding. When TS1_ERDI is set high, extended RDI is selected. When TS1_ERDI is set low, normal RDI is selected. These selections are summarized in Table 15. Table 15 SIRP RDI Settings

Table 15 SIRP RDI Settings

	ERDI Code	ERDI Interpretation
TS1_ERDI = 1	001	No RDI-P defect
	010	ERDI-P payload defect
	101	ERDI-P server defect
	110	ERDI-P connectivity defect
TS1_ERDI = 0	000	No RDI-P defect
	000	No RDI-P defect

TS1_ERDI = 0	100	RDI-P defect
	100	RDI-P defect

TS1_RDI20F

The TS1_RDI20F bits specify the configuration of RDI maintenance duration. The standard required duration is 10 frames. The GR-253 objective duration is 20 frames. The two options are specified by the TS1_RDI20F bit are selected as shown in Table 16.

Table 16 SIRP RDI Maintenance

TS1_RDI20F	Configuration
0	A particular RDI value for will be maintained for the required 10 frames before changing to a lower priority RDI code.
1	A particular RDI value for will be maintained for the GR-253 objective 20 frames before changing to a lower priority RDI code.

TS1_FORCE_LCD

The TS1_FORCE_LCD bit is used to force a Loss of ATM Cell Delineation (LCD) event. A logic OR operation is performed on the LCD indication and the TS1_FORCE_LCD bit. When TS1_FORCE_LCD is set high, an LCD event is assumed and RDI[1:0] is sourced entirely from a specified 2 bit RDI code (LCD[1:0]). The TS1_FORCE_LCD bit is ignored when TS1_RMODE[1:0] = b'01.

Register 079CH: SIRP Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RDIPRIHI[1]	0
Bit 4	R/W	RDIPRIHI[0]	0
Bit 3	R/W	RDIPRIMID[1]	0
Bit 2	R/W	RDIPRIMID[0]	0
Bit 1	R/W	LCD[1]	1
Bit 0	R/W	LCD[0]	0

LCD[1:0]

The LCD[1:0] bits represent the top two bits of the RDI code generated when a Loss of ATM Cell Delineation (LCD) event is detected. The third bit (LSB) is the inverse of the second (LCD[0]). **To conform to Bellcore and ITU SONET/SDH standards, this register field must be set to 01 (note the default is 10).**

RDIPRIMID[1:0]

The RDIPRIMID[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the second highest priority code. These bits combined with the RDIPRIHI bits determine the priority scheme. The bits are interpreted as shown in RDIPRIHI[1:0]. **To comply with Bellcore and ITU SONET/SDH standards this register field must be set to 11**.

RDIPRIHI[1:0]

The RDIPRIHI[1:0] bits specify which two-bit alarm code point (RDI) will be treated as the highest priority code. High priority codes will replace low priority codes at the next transmit G1 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed. **To comply with Bellcore and ITU SONET/SDH standards this register field must be set to 10**.

Table 17 SIRP RDI Priority Schemes

RDIPRIHI[1:0]	RDIPRIMID[1:0]	Priority of Codes (3 = Highest)	
		Code	Priority
11	01	110	3
		010	2
		101	1
		001	0
11	10	110	3
		101	2
		010	1
		001	0
10	11	101	3
		110	2
		010	1
		001	0
10	01	101	3
		010	2
		110	1
		001	0
01	11	010	3
		110	2
		101	1
		001	0
01	10	010	3
		101	2
		110	1
		001	0
00	00	110	1
		101	1
		010	1
		001	0
Other codes	other codes	Reserved	

Notes:

1. When RDIPRIHI[1:0] and RDIPRIMID[1:0] are both equal to b'00, all RDI codes have equal priority except RDI[1:0] = b'00 which always has lowest priority.
2. The above table only affects the relationship between the configured LCD value and whatever in-band RDI is provided by the SARC/RHPP in the Protect device. For example, the priority of any Server Defect cannot be made lower than a Connectivity Defect by changing these register values.

Register 0800H: PRGM Indirect Address
Register 0810H: PRGM Aux 2 Indirect Address
Register 0820H: PRGM Aux 3 Indirect Address
Register 0830H: PRGM Aux 4 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. For the S/UNI-2488, PATH[3:0] is normally set to 1H except when accessing the monitor error counter registers.

IADDR[3:0]

The internal address bits select which internal register is accessed by the current indirect transfer. Six registers are defined for the monitor while four pages are defined for the generator.

IADDR[3:0]	Register
0000	Monitor – Timeslot Configuration page
0001	Monitor – PRBS[22:7] page
0010	Monitor – PRBS[6:0] page
0011	Reserved
0100	Monitor – Monitor error count page
0101	Reserved
1000	Generator – Timeslot Configuration page
1001	Generator – PRBS[22:7] page

1010	Generator – PRBS[6:0] page
1011	Reserved

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal register. When RWB is set to logic 1, an indirect read access to the register is initiated. The data from the addressed location in the internal register will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the register is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal register. Do not write to indirect registers 04H to 07H.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal register has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 0801H: PRGM Indirect Data
Register 0811H: PRGM Aux 2 Indirect Data
Register 0821H: PRGM Aux 3 Indirect Data
Register 0831H: PRGM Aux 4 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from an internal register during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal register will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal register. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which internal register is being accessed.

Register 0802H: PRGM Generator Payload Configuration
Register 0812H: PRGM Aux 2 Generator Payload Configuration
Register 0822H: PRGM Aux 3 Generator Payload Configuration
Register 0832H: PRGM Aux 4 Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

All Reserved bits must be set to their default values for proper operation.

GEN_MSSLEN[2:0], GEN_STS12C, GEN_STS12CSL

These bits control the operating mode of the PRGM generators. The bits should be set according to the table below.

PRGM	GEN_STS12C	GEN_STS12CSL	GEN_MSSLEN[2:0]
Master	1	0	011
Aux2 Aux3 Aux4	1	1	011

Register 0803H: PRGM Monitor Payload Configuration Register
Register 0813H: PRGM Aux2 Monitor Payload Configuration
Register 0823H: PRGM Aux3 Monitor Payload Configuration
Register 0833H: PRGM Aux2 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

All Reserved bits must be set to their default values for proper operation.

MON_MSSLEN[2:0], MON_STS12C, MON_STS12CSL

These bits control the operating mode of the PRGM monitors. The bits should be set according to the table below.

PRGM	MON_STS12C	MON_STS12CSL	MON_MSSLEN[2:0]
Master	1	0	011
Aux2 Aux3 Aux4	1	1	011

Register 0804H: PRGM Monitor Byte Error Interrupt Status
Register 0814H: PRGM Aux 2 Monitor Byte Error Interrupt Status
Register 0824H: PRGM Aux 3 Monitor Byte Error Interrupt Status
Register 0834H: PRGM Aux 4 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_ERRI	X
Bit 10	R	MON[N+11]_ERRI	X
Bit 9	R	MON[N+10]_ERRI	X
Bit 8	R	MON[N+9]_ERRI	X
Bit 7	R	MON[N+8]_ERRI	X
Bit 6	R	MON[N+7]_ERRI	X
Bit 5	R	MON[N+6]_ERRI	X
Bit 4	R	MON[N+5]_ERRI	X
Bit 3	R	MON[N+4]_ERRI	X
Bit 2	R	MON[N+3]_ERRI	X
Bit 1	R	MON[N+2]_ERRI	X
Bit 0	R	MON[N+1]_ERRI	X

MON**x**_ERRI

The Monitor Byte Error Interrupt Status registers contain the status of the interrupt generated by each of the 48 STS-1 paths when an error has been detected.

PRGM Monitor Byte Error Interrupt Status register, N = 0.
PRGM Aux2 Monitor Byte Error Interrupt Status register, N = 1.
PRGM Aux3 Monitor Byte Error Interrupt Status register, N = 2.
PRGM Aux4 Monitor Byte Error Interrupt Status register, N = 3.

The MON**x**_ERRI bit is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE, and is cleared after it has been read. MONx_ERRI is cleared to logic 0 when this register is read if WCIMODE is set to logic 0. MONx_ERRI is cleared only when it is written to logic 1 if WCIMODE is set to logic 1.

Register 0805H: PRGM Monitor Byte Error Interrupt Enable
Register 0815H: PRGM Aux 2 Monitor Byte Error Interrupt Enable
Register 0825H: PRGM Aux 3 Monitor Byte Error Interrupt Enable
Register 0835H: PRGM Aux 4 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON[N+12]_ERRE	0
Bit 10	R/W	MON[N+11]_ERRE	0
Bit 9	R/W	MON[N+10]_ERRE	0
Bit 8	R/W	MON[N+9]_ERRE	0
Bit 7	R/W	MON[N+8]_ERRE	0
Bit 6	R/W	MON[N+7]_ERRE	0
Bit 5	R/W	MON[N+6]_ERRE	0
Bit 4	R/W	MON[N+5]_ERRE	0
Bit 3	R/W	MON[N+4]_ERRE	0
Bit 2	R/W	MON[N+3]_ERRE	0
Bit 1	R/W	MON[N+2]_ERRE	0
Bit 0	R/W	MON[N+1]_ERRE	0

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable registers enable the interrupt for each of the 48 STS-1 paths.

PRGM Monitor Byte Error Interrupt Enable register, N = 0.
PRGM Aux2 Monitor Byte Error Interrupt Enable register, N = 1.
PRGM Aux3 Monitor Byte Error Interrupt Enable register, N = 2.
PRGM Aux4 Monitor Byte Error Interrupt Enable register, N = 3.

When MON**x**_ERRE is set high, the Byte Error Interrupt is allowed to generate an interrupt on INTB.

Register 0809H: PRGM Monitor Synchronization Interrupt Status
Register 0819H: PRGM Aux 2 Monitor Synchronization Interrupt Status
Register 0829H: PRGM Aux 3 Monitor Synchronization Interrupt Status
Register 0839H: PRGM Aux 4 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_SYNCI	X
Bit 10	R	MON[N+11]_SYNCI	X
Bit 9	R	MON[N+10]_SYNCI	X
Bit 8	R	MON[N+9]_SYNCI	X
Bit 7	R	MON[N+8]_SYNCI	X
Bit 6	R	MON[N+7]_SYNCI	X
Bit 5	R	MON[N+6]_SYNCI	X
Bit 4	R	MON[N+5]_SYNCI	X
Bit 3	R	MON[N+4]_SYNCI	X
Bit 2	R	MON[N+3]_SYNCI	X
Bit 1	R	MON[N+2]_SYNCI	X
Bit 0	R	MON[N+1]_SYNCI	X

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status registers indicate synchronization interrupts for each of the 48 STS-1 paths.

PRGM Monitor Synchronization Interrupt Status register, N = 0.
PRGM Aux2 Monitor Synchronization Interrupt Status register, N = 1.
PRGM Aux3 Monitor Synchronization Interrupt Status register, N = 2.
PRGM Aux4 Monitor Synchronization Interrupt Status register, N = 3.

The Monitor Synchronization Interrupt Status Interrupt (MON**x**_SYNCI) bit is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in this PRBS monitor will set MONx_SYNCI high. This bit is independent of MONx_SYNCE. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Note that the PRGM will synchronize on an all zeroes or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register 080AH: PRGM Monitor Synchronization Interrupt Enable
Register 081AH: PRGM Aux 2 Monitor Synchronization Interrupt Enable
Register 082AH: PRGM Aux 3 Monitor Synchronization Interrupt Enable
Register 083AH: PRGM Aux 4 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON[N+12]_SYNCE	0
Bit 10	R/W	MON[N+11]_SYNCE	0
Bit 9	R/W	MON[N+10]_SYNCE	0
Bit 8	R/W	MON[N+9]_SYNCE	0
Bit 7	R/W	MON[N+8]_SYNCE	0
Bit 6	R/W	MON[N+7]_SYNCE	0
Bit 5	R/W	MON[N+6]_SYNCE	0
Bit 4	R/W	MON[N+5]_SYNCE	0
Bit 3	R/W	MON[N+4]_SYNCE	0
Bit 2	R/W	MON[N+3]_SYNCE	0
Bit 1	R/W	MON[N+2]_SYNCE	0
Bit 0	R/W	MON[N+1]_SYNCE	0

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable registers enables the synchronization interrupts for each of the 48 STS-1 paths.

PRGM Monitor Synchronization Interrupt Enable register, N = 0.
PRGM Aux2 Monitor Synchronization Interrupt Enable register, N = 1.
PRGM Aux3 Monitor Synchronization Interrupt Enable register, N = 2.
PRGM Aux4 Monitor Synchronization Interrupt Enable register, N = 3.

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INTB. When MON**x**_SYNCE is set high, a change in the synchronization state of the monitor in STS-1 path **x** generates an interrupt on INTB.

Register 080BH: PRGM Monitor Synchronization Status
Register 081BH: PRGM Aux 2 Monitor Synchronization Status
Register 082BH: PRGM Aux 3 Monitor Synchronization Status
Register 083BH: PRGM Aux 4 Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON[N+12]_SYNCV	X
Bit 10	R	MON[N+11]_SYNCV	X
Bit 9	R	MON[N+10]_SYNCV	X
Bit 8	R	MON[N+9]_SYNCV	X
Bit 7	R	MON[N+8]_SYNCV	X
Bit 6	R	MON[N+7]_SYNCV	X
Bit 5	R	MON[N+6]_SYNCV	X
Bit 4	R	MON[N+5]_SYNCV	X
Bit 3	R	MON[N+4]_SYNCV	X
Bit 2	R	MON[N+3]_SYNCV	X
Bit 1	R	MON[N+2]_SYNCV	X
Bit 0	R	MON[N+1]_SYNCV	X

MON**x**_SYNCV

The Monitor Synchronization Status registers reflects the synchronization state of each STS-1 path.

PRGM Monitor Synchronization Status register, N = 0.
PRGM Aux2 Monitor Synchronization Status register, N = 1.
PRGM Aux3 Monitor Synchronization Status register, N = 2.
PRGM Aux4 Monitor Synchronization Status register, N = 3.

The Monitor Synchronization Status registers reflect the state of the monitor's state machine. When MON**x**_SYNCV is set high, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low, the monitor is out of sync for the STS-1 Path **x**. The Synchronization Status is only valid when the corresponding monitor is enabled.

Note that the PRGM will synchronize on an all zeroes or all ones pattern. To verify that a valid PRBS pattern is the signal the PRGM is locked to, check the PRBS[22:0] bits in the PRGM Monitor PRBS Accumulator Page. If the bits are not all zeroes or all ones, then the synchronization is due to locking on a valid PRBS pattern.

Register 080CH: PRGM Performance Counters Transfer Trigger
Register 081CH: PRGM Aux 2 Performance Counters Transfer Trigger
Register 082CH: PRGM Aux 3 Performance Counters Transfer Trigger
Register 083CH: PRGM Aux 4 Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	TIP	

A write in this register will trigger the transfer of the error counters for that slice to holding registers from which they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low. A write to register 0x0000, the S/UNI-2488 Identity and Global Performance Monitor Update register, will also trigger the transfer of the error counters for all PRGM monitors.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred to the holding register yet. When TIP is low, the value of the error counters are available to be read in the holding registers. This bit can be polled after an error counters transfer request to determine if the counters are ready to be read.

Indirect Register 00H: PRGM Monitor Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

All Reserved bits must be set to their default values for proper operation.

MON_ENA

The Monitor Enable register bit enables the PRBS monitors for the PRGM blocks (all 48). If MON_ENA is set high, a PRBS sequence is generated and compared to the incoming PRBS sequence inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the input monitor data is ignored.

INV_PRBS

INV_PRBS sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted. When set low, the PRBS bytes will be compared unmodified.

RESYNC

RESYNCH sets the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machines will be forced in the Out Of Sync state and will automatically try to resynchronize to the incoming stream. To force another resynchronization, the bit needs to be set low again before it is set high.

SEQ_PRBSB

SEQ_PRBSB enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload is expected to contain PRBS bytes. When high, the payload is expected to contain a sequential pattern.

Indirect Register 01H: PRGM Monitor PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 02H: PRGM Monitor PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7		Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]

The PRBS[22:0] register contains the state of the LFSR monitor. It is possible to write to this register to change the initial state of the monitor.

Indirect Register 04H: PRGM Monitor Error Count Page

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

ERR_CNT[15:0]

The ERR_CNT[15:0] register is the number of errors in the PRBS bytes detected during monitoring. Errors are generally accumulated only when the monitor is in the synchronized state. Even if there are multiple errors within one PRBS byte, only one error is counted. The transfer of the error counter to this holding register is triggered by an indirect write to the PRGM Performance Counters Transfer Trigger register for the particular STS-12 slice (register 080CH, 081CH, 082CH or 083CH respectively) or by writing to register 0000H for a global performance monitor update. Do not write to this register. The error counter will not wrap around after reaching FFFFH. It will saturate to this value.

Note that the 3 errors which cause the PRGM to lose synchronization may be counted as 3, 4, or 5 errors.

Indirect Register 08H: PRGM Generator Timeslot Configuration Page

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	PRBS_ENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	S[1]	0
Bit 6	R/W	S[0]	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

All Reserved bits must be set to their default values for proper operation.

INV_PRBS

INV_PRBS sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted. When set low, the PRBS bytes will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register will clear itself when the operation is complete. A read operation will always result in a logic '0'.

SEQ_PRBSB

SEQ_PRBSB enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes. When high, a sequential pattern is inserted.

S[1:0]

The S[1:0] bits contain the value inserted in the S[1:0] bit positions in the payload pointer.

PRBS_ENA

This bit specifies if PRBS overwriting is enabled. If PRBS_ENA is high, PRBS patterns are generated and are used to overwrite the data stream. If PRBS_ENA is low, no pattern is generated and the data stream is not overwritten.

Indirect Register 09H : PRGM Generator PRBS[22:7] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	PRBS[22:7]	0000

Indirect Register 0AH: PRGM Generator PRBS[6:0] Accumulator Page

Bit	Type	Function	Default
Bit 15 to Bit 7		Unused	00
Bit 6 to Bit 0	R/W	PRBS[6:0]	00

PRBS[22:0]

The PRBS[22:0] register contains the state of the LFSR generator. It is possible to write in this register to change the initial state of the monitor.

Register 0840H: R8TD APS1 Control and Status
Register 0848H: R8TD APS2 Control and Status
Register 0850H: R8TD APS3 Control and Status
Register 0858H: R8TD APS4 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	SETLCV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

All Reserved bits must be set to their default values for proper operation.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment circuit on a serial link. A transition from logic zero to logic one in this bit forces the receiver to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment circuit. A transition from logic zero to logic one in this bit forces the receiver to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment circuit. OCAV is set high when the receiver is in the out-of-character-alignment state. OCAV is set low when the receiver is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment circuit. OFAV is set high when the receiver is in the out-of-frame-alignment state. OFAV is set low when the receiver is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment circuit changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is set low.

SETLCV

The SETLCV bit is used to introduce line code violations in the receive data stream. When logic 1, SETLCV will induce a large number of LCVs on the data stream. When logic 0, SETLCV will not alter the incoming data stream. This feature can be used to cause excessive LCVs which in turn will force the R8TD to search for a new character alignment.

Reserved

The Reserved bits must be set to their default value for proper operation.

Register 0841H: R8TD APS1 Interrupt Status
Register 0849H: R8TD APS2 Interrupt Status
Register 0851H: R8TD APS3 Interrupt Status
Register 0859H: R8TD APS4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit, the OCAI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs. When the interrupt is masked by the OFAE bit, the OFAI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit, the LCVI remains valid and may be polled to detect change of frame alignment events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit, the FUOI remains valid and may be polled to detect underrun/overrun events. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0842H: R8TD APS1 Line Code Violation Count
Register 084AH: R8TD APS2 Line Code Violation Count
Register 0852H: R8TD APS3 Line Code Violation Count
Register 085AH: R8TD APS4 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

LCV[15:0]

The LCV[15:0] bits report the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0000H, the S/UNI-2488 Identity and Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers within 6 TCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0843H: R8TD APS1 Analog Control 1
Register 084BH: R8TD APS2 Analog Control 1
Register 0853H: R8TD APS3 Analog Control 1
Register 085BH: R8TD APS4 Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DRU_CTRL[3]	0
Bit 4	R/W	DRU_CTRL[2]	0
Bit 3	R/W	DRU_CTRL[1]	0
Bit 2	R/W	DRU_CTRL[0]	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls internal analog functions. This register should be written to 0xcc34 for normal operation.

Reserved

The Reserved bits, must be set to the indicated default value for correct operation.

Reserved1

The Reserved1 bit must be set to logic 1 for proper operation.

DRU_CTRL[3:0]

The DRU_CTRL[3:0] bits control the DRU CTRL[3:0] inputs. **The DRU_CTRL[3:0] bits need to be set to 'b1101 following a reset for correct operation of the S/UNI-2488**.

A_RSTB

The A_RSTB bit is a soft-reset for the Data Recovery Unit Analog block. Setting A_RSTB to logic 0 will reset the block. A_RSTB should be set to logic 0 to conserve power consumption for applications not using the APS port.

RX_ENB

The RXLV enable bit (RX_ENB) bit controls the operation of RXLV block #X. Setting RX_ENB to logic 0 enables the block. Setting RX_ENB to logic 1 disables the block. RX_ENB should be set to logic 1 to conserve power consumption for applications not using the APS port.

DRU_ENB

The TXLV enable bit (DRU_ENB) bit controls the operation of Data Recovery Unit Analog block #X. Setting DRU_ENB to logic 0 enables the block. Setting DRU_ENB to logic 1 disables the block. DRU_ENB should be set to logic 1 to conserve power consumption for applications not using the APS port.

Register 0844H: R8TD APS1 Analog Control 2
Register 084CH: R8TD APS2 Analog Control 2
Register 0854H: R8TD APS3 Analog Control 2
Register 085CH: R8TD APS4 Analog Control 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal analog functions. This register should not be used and should be left in its default state.

Register 0845H: R8TD APS1 Analog Control 3
Register 084DH: R8TD APS2 Analog Control 3
Register 0855H: R8TD APS3 Analog Control 3
Register 085DH: R8TD APS4 Analog Control 3

Bit	Type	Function	Default
Bit 15	R/W	Reserved	X
Bit 14	R/W	Reserved	X
Bit 13	R/W	Reserved	X
Bit 12	R/W	Reserved	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register controls internal analog functions. This register should not be used and should be left in its default state.

Register 0860H: T8TE APS1 Control and Status
Register 0868H: T8TE APS2 Control and Status
Register 0870H: T8TE APS3 Control and Status
Register 0878H: T8TE APS4 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	LLBEN	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

The Reserved bit must be set to its default value for proper operation.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the APS outgoing serial data. When DLCV is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that Serial-TelecomBus control characters are not affected by the DLCV bit and are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

The FIFO should be CENTERed whenever any of the following actions are taken: (1) the chip is reset/powered on, (2) CSU is reset, (3) APS is reset or (4) the position of APSIFP changes.

For proper operation in a CHESS system, the T8TEs' CENTER bit must be set to logic 1 after the APS CSU is locked. This is the only way to guarantee that all transmit FIFO depths are within 1 or 2 clock cycles of each other. This is required for J0 alignment at the far end.

LLBEN

The line loopback enable bit (LLBEN) controls line loopback operation. LLBEN routes the raw 8b10b encoded receive stream from the LVDS receiver to the LVDS transmitter. There it is serialized and transmitted without further processing. When LLBEN is set high, serial line loopback is enabled. When LLBEN is set low, line loopback is disabled.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) controls the FIFO overrun interrupt event. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

Reserved

Reserved should be kept at its default value.

Register 0861H: T8TE APS1 Interrupt Status
Register 0869H: T8TE APS2 Interrupt Status
Register 0871H: T8TE APS3 Interrupt Status
Register 0879H: T8TE APS4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when the T8TE Interrupt status register is read. This bit does not cause a hardware interrupt on INTB unless the FIFOERRE bit is set high. If WCIMODE is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0, then a read of this register automatically clears the bit.

Register 0862H: T8TE APS1 TelecomBus Mode #1
Register 086AH: T8TE APS2 TelecomBus Mode #1
Register 0872H: T8TE APS3 TelecomBus Mode #1
Register 087AH: T8TE APS4 TelecomBus Mode #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE7[1]	0
Bit 14	R/W	TMODE7[0]	0
Bit 13	R/W	TMODE6[1]	0
Bit 12	R/W	TMODE6[0]	0
Bit 11	R/W	TMODE5[1]	0
Bit 10	R/W	TMODE5[0]	0
Bit 9	R/W	TMODE4[1]	0
Bit 8	R/W	TMODE4[0]	0
Bit 7	R/W	TMODE3[1]	0
Bit 6	R/W	TMODE3[0]	0
Bit 5	R/W	TMODE2[1]	0
Bit 4	R/W	TMODE2[0]	0
Bit 3	R/W	TMODE1[1]	0
Bit 2	R/W	TMODE1[0]	0
Bit 1	R/W	TMODE0[1]	0
Bit 0	R/W	TMODE0[0]	0

Register 0863H: T8TE APS1 TelecomBus Mode #2
Register 086BH: T8TE APS2 TelecomBus Mode #2
Register 0873H: T8TE APS3 TelecomBus Mode #2
Register 087BH: T8TE APS4 TelecomBus Mode #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE11[1]	0
Bit 6	R/W	TMODE11[0]	0
Bit 5	R/W	TMODE10[1]	0
Bit 4	R/W	TMODE10[0]	0
Bit 3	R/W	TMODE9[1]	0
Bit 2	R/W	TMODE9[0]	0
Bit 1	R/W	TMODE8[1]	0
Bit 0	R/W	TMODE8[0]	0

TMODE0[1:0]-TMODE11[1:0]

The TelecomBus mode registers (TMODE0[1:0]-TMODE11[1:0]) contain TelecomBus mode settings for each STS-1 timeslot in the STS-12 stream. **All STS-1 timeslots in all streams must work in the same mode**.

A S/UNI-2488 configured to be an APS protect device **must** have HPT mode enabled.

A S/UNI-2488 configured to be in cross-connect mode must be in MST mode so it can pass the SONET/SDH overhead transparently.

The setting stored in TMODE**x**[1:0] (**x** can be 0-11) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters (see Section 13.1.12). Table 18 defines the values for setting each mode.

Table 18 TelecomBus Mode

TMODEx[1:0]	Functional Description
00	MST Mode
01	HPT Mode
10, 11	Reserved

Register 0864H: T8TE APS1 Test Pattern
Register 086CH: T8TE APS2 Test Pattern
Register 0874H: T8TE APS3 Test Pattern
Register 087CH: T8TE APS4 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

TP[9:0]

The Test Pattern registers (TP[9:0]) contain the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

Register 0865H: T8TE APS1 Analog Control
Register 086DH: T8TE APS2 Analog Control
Register 0875H: T8TE APS3 Analog Control
Register 087DH: T8TE APS4 Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IDDQ	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	APISO_ENB	0
Bit 6	R/W	ATIN[3]	0
Bit 5	R/W	ATIN[2]	0
Bit 4	R/W	ATIN[1]	0
Bit 3	R/W	ATIN[0]	0
Bit 2	R/W	TXLV_ATMSB	1
Bit 1	R/W	APISO_ATMSB	1
Bit 0	R/W	ARSTB	1

All Reserved bits must be set to their default values for proper operation.

ARSTB

The analog reset bit (ARSTB) controls the TXLV and APISO operation. When ARSTB is set low, the TXLV and APISO are reset. This bit must be set to logic 1 for normal operation. ARSTB should be set to logic 0 to conserve power consumption for applications not using the APS port.

APISO_ATMSB

The APISO analog test mode select bit (APISO_ATMSB) controls the APISO test operation. APISO_ATMSB drives the output APISO_ATMSB pin low to enable test mode in the APISO. This bit must be set to logic 1 for normal operation.

TXLV_ATMSB

The TXLV analog test mode select bit (TXLV_ATMSB) controls the TXLV test operation. TXLV_ATMSB drives the output TXLV_ATMSB pin low to enable test mode in the TXLV block. This bit must be set to logic 1 for normal operation.

ATIN[3:0]

The analog test control inputs (ATIN[3:0]) control the APISO and TXLV test circuitry. These bits are not used for normal operation.

APISO_ENB

The APISO enable bit (APISO_ENB) controls the APISO operation. When set to logic 1, APISO_ENB disables the APISO. When set to logic 0, APISO_ENB enables the APISO. APISO_ENB should be set to logic 1 to conserve power consumption for applications not using the APS port.

TXLV_ENB

The TXLV enable bit (TXLV_ENB) controls the TXLV operation. When set to logic 1, TXLV_ENB disables the TXLV. When set to logic 0, TXLV_ENB enables the TXLV. TXLV_ENB should be set to logic 1 to conserve power consumption for applications not using the APS port.

IDDQ

The IDDQ controls the APISO operation. When IDDQ is set high, IDDQ test of the APISO is enabled. For normal operation, IDDQ should be set low.

Register 0866H: T8TE APS1 DTB Bus
Register 086EH: T8TE APS2 DTB Bus
Register 0876H: T8TE APS3 DTB Bus
Register 087EH: T8TE APS4 DTB Bus

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	
Bit 7	R/W	DTBO[0]	0
Bit 6	R/W	DTBO[0]	0
Bit 5	R/W	DTBO[0]	0
Bit 4	R/W	DTBO[0]	0
Bit 3	R	DTBI[3]	X
Bit 2	R	DTBI[2]	X
Bit 1	R	DTBI[1]	X
Bit 0	R	DTBI[0]	X

DTBO[3:0]

The analog wrapper digital test bus output bits (DTB_OUT[3:0]) are used to drive values on the digital test bus (DTB[3:0]). These bits are not used in normal operation.

DTBI[3:0]

The analog wrapper digital test bus input bits (DTB_IN[3:0]) are used to read values from the digital test bus (DTB[3:0]). These bits are not used in normal operation.

Register 0880H: RXDLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Reserved	0
Bit 4	R/W	OVERRIDE	0
Bit 3		Unused	
Bit 2	R/W	ERRORE	X
Bit 1	R/W	VERN_EN	0
Bit 0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL.
It is not necessary to setup this register for normal operation.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the RFCLK and the feedback clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the RFCLK and the feedback clock for the first time.

This bit must be set to logic 0 for normal operation.

VERN_EN

The vernier enable register (VERN_EN) forces the DLL to ignore the phase detector and use the tap number specified by the VERNIER[7:0] register bits. When VERN_EN is set to logic zero, the DLL operates normally adjusting the phase offset based on the phase detector. When VERN_EN is set to logic one, the delay line uses the tap specified by the VERNIER[7:0] register bits. This bit must be set to logic 0 for normal operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

OVERRIDE

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DLL generates the DLLCLK by delaying the RFCLK until the rising edge of the feedback clock occurs at the same time as the rising edge of RFCLK. When OVERRIDE is set high, the DLLCLK output is a buffered version of the RFCLK input. This bit must be set to logic 0 for normal operation.

Register 0881H: RXDLL Vernier Control

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	VERNIER[7]	0
Bit 6	R/W	VERNIER[6]	0
Bit 5	R/W	VERNIER[5]	0
Bit 4	R/W	VERNIER[4]	0
Bit 3	R/W	VERNIER[3]	0
Bit 2	R/W	VERNIER[2]	0
Bit 1	R/W	VERNIER[1]	0
Bit 0	R/W	VERNIER[0]	0

The Vernier Control Register provides the delay line tap control when using the vernier option.

VERNIER[7:0]

The vernier tap register bits (VERNIER[7:0]) specifies the phase delay through the DLL when using the vernier feature. When VERN_EN is set high, the VERNIER[7:0] registers specify the delay tap used. When VERN_EN is set low, the VERNIER[7:0] register is ignored.
A VERNIER[7:0] value of all zeros specifies the delay tap with the minimum delay through the delay line. A VERNIER[7:0] value of 255 specifies the delay tap with the maximum delay through the delay line.

This bit must be set to logic 0 for normal operation.

Register 0882H: RXDLL Delay Tap Status/DLL Reset

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	TAP[7]	X
Bit 6	R	TAP[6]	X
Bit 5	R	TAP[5]	X
Bit 4	R	TAP[4]	X
Bit 3	R	TAP[3]	X
Bit 2	R	TAP[2]	X
Bit 1	R	TAP[1]	X
Bit 0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 RFCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0 and back to a lock position.

TAP[7:0]

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate the outgoing clock DLLCLK.

When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay. TAP[7:0] is invalid when vernier enable VERN_EN is set to one.

These bits are not used in normal operation.

Register 0883H: RXDLL Control Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	RFCLKI	X
Bit 6	R	FBCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the feedback clock and the rising edge of RFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or a software reset (via register bits in register 2). RUN is forced high when the OVERRIDE register is set high or when the VERN_EN register is set high.

CHANGE

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight RFCLK cycles when the DLL moves to a new delay line tap.

This bit is not used in normal operation.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLCLK phase which causes the rising edge of the feedback clock to be aligned to the rising edge of RFCLK. ERROR is set low, when the DLL captures lock again.

ERROR is forced low when the OVERRIDE register is set high or when the VERN_EN register is set high.

CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one.

When WCIMODE is low, the CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the CHANGEI register bit is cleared immediately after a logic one is written to the CHANGEI register, thus acknowledging the event has been recorded.

This bit is not used in normal operation.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

FBCLKI

The feedback clock event register bit FBCLKI provides a method to monitor activity on the feedback clock. When the feedback clock primary input changes from a logic zero to a logic one, the FBCLKI register bit is set to logic one.

When WCIMODE is low, the FBCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the FBCLKI register bit is cleared immediately after a logic one is written to the FBCLKI register, thus acknowledging the event has been recorded.

This bit is not used in normal operation.

RFCLKI

The system clock event register bit RFLCKI provides a method to monitor activity on the system clock. When the RFCLK primary input changes from a logic zero to a logic one, the RFCLKI register bit is set to logic one. The RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

When WCIMODE is low, the RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the RFCLKI register bit is cleared immediately after a logic one is written to the RFCLKI register, thus acknowledging the event has been recorded.

Register 0884H: TXDLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Reserved	0
Bit 4	R/W	OVERRIDE	0
Bit 3		Unused	
Bit 2	R/W	ERRORE	X
Bit 1	R/W	VERN_EN	0
Bit 0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL. It is not necessary to setup this register for normal operation.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the TFCLK and the feedback clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the TFCLK and the feedback clock for the first time.

This bit must be set to logic 0 for normal operation.

VERN_EN

The vernier enable register (VERN_EN) forces the DLL to ignore the phase detector and use the tap number specified by the VERNIER[7:0] register bits. When VERN_EN is set to logic zero, the DLL operates normally adjusting the phase offset based on the phase detector. When VERN_EN is set to logic one, the delay line uses the tap specified by the VERNIER[7:0] register bits.

This bit must be set to logic 0 for normal operation.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

OVERRIDE

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DLL generates the DLLCLK by delaying the TFCLK until the rising edge of the feedback clock occurs at the same time as the rising edge of TFCLK. When OVERRIDE is set high, the DLLCLK output is a buffered version of the TFCLK input. This feature provides a back-up strategy in case the DLL does not operate correctly.

This bit must be set to logic 0 for normal operation.

Register 0885H: TXDLL Vernier Control

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	VERNIER[7]	0
Bit 6	R/W	VERNIER[6]	0
Bit 5	R/W	VERNIER[5]	0
Bit 4	R/W	VERNIER[4]	0
Bit 3	R/W	VERNIER[3]	0
Bit 2	R/W	VERNIER[2]	0
Bit 1	R/W	VERNIER[1]	0
Bit 0	R/W	VERNIER[0]	0

The Vernier Control Register provides the delay line tap control when using the vernier option.

VERNIER[7:0]

The vernier tap register bits (VERNIER[7:0]) specifies the phase delay through the DLL when using the vernier feature. When VERN_EN is set high, the VERNIER[7:0] registers specify the delay tap used. When VERN_EN is set low, the VERNIER[7:0] register is ignored.

A VERNIER[7:0] value of all zeros specifies the delay tap with the minimum delay through the delay line. A VERNIER[7:0] value of 255 specifies the delay tap with the maximum delay through the delay line.

This bit must be set to logic 0 for normal operation.

Register 0886H: TXDLL Delay Tap Status/DLL Reset

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	TAP[7]	X
Bit 6	R	TAP[6]	X
Bit 5	R	TAP[5]	X
Bit 4	R	TAP[4]	X
Bit 3	R	TAP[3]	X
Bit 2	R	TAP[2]	X
Bit 1	R	TAP[1]	X
Bit 0	R	TAP[0]	X

The DLL Delay Tap Status Register indicates the delay tap used by the DLL to generate the outgoing clock.

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 TFCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0 and back to a lock position.

TAP[7:0]

The tap status register bits (TAP[7:0]) specifies the delay line tap the DLL is using to generate the outgoing clock DLLCLK.

When TAP[7:0] is logic zero, the DLL is using the delay line tap with minimum phase delay. When TAP[7:0] is equal to 255, the DLL is using the delay line tap with maximum phase delay. TAP[7:0] is invalid when vernier enable VERN_EN is set to one.

These bits are not used in normal operation.

Register 0887H: TXDLL Control Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	TFCLKI	X
Bit 6	R	FBCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the feedback clock and the rising edge of TFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or a software reset (via register 2). RUN is forced high when the OVERRIDE register is set high or when the VERN_EN register is set high.

CHANGE

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight TFCLK cycles when the DLL moves to a new delay line tap.

This bit is not used in normal operation.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLCLK phase which causes the rising edge of the feedback clock to be aligned to the rising edge of TFCLK. ERROR is set low, when the DLL captures lock again.

ERROR is forced low when the OVERRIDE register is set high or when the VERN_EN register is set high.

CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one.

When WCIMODE is low, the CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the CHANGEI register bit is cleared immediately after a logic one is written to the CHANGEI register, thus acknowledging the event has been recorded.

This bit is not used in normal operation.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

FBCLKI

The feedback clock event register bit FBCLKI provides a method to monitor activity on the feedback clock. When the FBCLK primary input changes from a logic zero to a logic one, the FBCLKI register bit is set to logic one.

When WCIMODE is low, the FBCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the FBCLKI register bit is cleared immediately after a logic one is written to the FBCLKI register, thus acknowledging the event has been recorded.

This bit is not used in normal operation.

TFCLKI

The system clock event register bit TFLCKI provides a method to monitor activity on the system clock. When the TFCLK primary input changes from a logic zero to a logic one, the TFCLKI register bit is set to logic one. The TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

When WCIMODE is low, the TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the TFCLKI register bit is cleared immediately after a logic one is written to the TFCLKI register, thus acknowledging the event has been recorded.

Register 0888H: CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	Reserved	1

Except for the CSU_ENB register bit, the other register bits are used for manufacturing test purposes only. They are not required for normal operations.

The Reserved bits should be set to their default values for normal operation.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the APS CSU into a reset. It should be set to logic 0 to conserve power consumption for applications not using the APS port.

CSU_ENB

The active low APS CSU enable control signal (CSU_ENB) bit forces the APS CSU into low power configuration. The APS CSU is disabled when CSU_ENB is logic 1. The APS CSU is enabled when CSU_ENB is logic 0. This bit must be set to logic 0 for normal operation using the APS port. It should be set to logic 1 to conserve power consumption for applications not using the APS port.

Register 0889H: CSTR Interrupt Enable and APS CSU Lock Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1	R	CSU_LOCKV	X
Bit 0	R/W	CSU_LOCKE	0

CSU_LOCKE

The APS CSU lock interrupt enable bit (CSU_LOCKE) enables the assertion of a hardware interrupt on INTB when the APS CSU lock status changes. When CSU_LOCKE is logic 1, the hardware interrupt is enabled. When CSU_LOCKE is logic 0, the hardware interrupt is disabled.

CSU_LOCKV

The APS CSU lock status (CSU_LOCKV) indicates the current state of the APS CSU. When CSU_LOCKV is logic 1, the APS CSU has locked on to the APSIFPCLK reference and is operating normally. When CSU_LOCKV is logic 0, the CSU has not locked onto the APSIFPCLK reference and is not in normal operating mode.

Register 088AH: CSTR APS CSU Lock Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1		Unused	X
Bit 0	R	CSU_LOCKI	X

CSU_LOCKI

The APS CSU lock interrupt indication bit (CSU_LOCKI) reports changes in the APS CSU lock status. CSU_LOCKI is logic 1 when the APS CSU transitions into or out of lock state. CSU_LOCKI is cleared when this register is read when WCIMODE is set to logic 0. When WCIMODE is set to logic 1, CSU_LOCKI is cleared when the bit is written to logic 1.

Register 0900H: Rx APS J0 FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15	R/W	NOJ04E	0
Bit 14	R/W	NOJ03E	0
Bit 13	R/W	NOJ02E	0
Bit 12	R/W	NOJ01E	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	EXJ04E	0
Bit 8	R/W	EXJ03E	0
Bit 7	R/W	EXJ02E	0
Bit 6	R/W	EXJ01E	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	OKJ04E	0
Bit 1	R/W	OKJ03E	0
Bit 1	R/W	OKJ02E	0
Bit 0	R/W	OKJ01E	0

OKJ0*x*E:

The APS correct J0 indication interrupt enable bit (OKJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is detected at the expected time. When OKJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When OKJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

EXJ0*x*E

The APS extra J0 indication interrupt enable bit (EXJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is detected at an unexpected time. When EXJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When EXJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

NOJ0*x*E

The APS J0 absent indication interrupt enable bit (NOJ0*x*E) for APS link number *x* enables the assertion of a hardware interrupt on INTB when the corresponding APS link's J0 character is not detected at an unexpected time. When NOJ0*x*E is logic 1, the hardware interrupt is enabled for APS link number *x*. When NOJ0*x*E is logic 0, the hardware interrupt is disabled for APS link number *x*.

Reserved

The Reserved bits must be set to their default state for proper operation.

Register 0901H: Rx APS J0 FIFO Interrupt Status

Bit	Type	Function	Default
Bit 15	R	NOJ04I	X
Bit 14	R	NOJ03I	X
Bit 13	R	NOJ02I	X
Bit 12	R	NOJ01I	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	EXJ04I	X
Bit 8	R	EXJ03I	X
Bit 7	R	EXJ02I	X
Bit 6	R	EXJ01I	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	OKJ04I	X
Bit 1	R	OKJ03I	X
Bit 1	R	OKJ02I	X
Bit 0	R	OKJ01I	X

OKJ0*x*I

The APS correct J0 indication interrupt indication bit (OKJ0*x*I) for APS link number *x* shows when the corresponding APS link's J0 character is detected at the expected time. When a correct J0 is detected, OKJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

EXJ0*x*I

The APS extra J0 indication interrupt indication bit (EXJ0*x*I) for APS link number *x* shows when an unexpected J0 character is detected on the corresponding APS link. When an unexpected J0 is detected, EXJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

NOJ0*x*I

The APS absent J0 indication interrupt indication bit (NOJ0*x*I) for APS link number *x* shows when the corresponding APS link's J0 character is not detected at the expected time. When the expected J0 is not detected, NOJ0*x*I is set to logic 1. When WCIMODE is set to logic 1, this bit is cleared when a logic 1 is written to it. When WCIMODE is set to logic 0, this bit is cleared when this register is read.

Register 0902H: S/UNI-2488 Miscellaneous Defect Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	TLREIINS	1
Bit 13	R/W	RXAPS_LINK_PAIS	1
Bit 12	R/W	RXAPS_PAIS_EN	1
Bit 11	R/W	RXAPS_NDF_EN	1
Bit 10	R/W	LOS_DEFECT_EN	1
Bit 9	R/W	SD_DEFECT_EN	1
Bit 8	R/W	RPAISINS_EN	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RPAISINS_EN

The RPAISINS_EN bit is used to enable the RHPP's AIS and LOP indications to be propagated to the SVCA output on a per-timeslot basis. Thus, when an AIS-L, AIS-P, or LOP are detected, the SVCA will generate a proper AIS-P on its output**. This bit and the RLAISINSEN, PAISPTREN, PLOPTREN registers bit in the SARC Path RPAISINS Enable indirect register (0x072A) for all 12 available SARC timeslots (see Section 13.17.3) must be set to logic 1 for proper operation.**

SD_DEFECT_EN

The SD_DEFECT_EN bit is used to force an AIS-L on the internal datapath immediately when SD is deasserted. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver.

LOS_DEFECT_EN

The LOS_DEFECT_EN bit is used to force an AIS-L on the internal datapath immediately when an LOS is detected. This will prevent the internal framer's (RRMP) descrambler from producing a scrambled all 0's pattern which, when passed through a transmitter's scrambler will generate the all 0's pattern again. An extended all 0's pattern at the transmitter could potentially cause a loss of lock a the downstream receiver.

RXAPS_NDF_EN

The RXAPS_NDF_EN bit is used to enable generation of an NDF frame when the AIS declaration described in the RXAPS_PAIS_EN bit description clears. When RXAPS_NDF_EN is logic 1, an NDF frame is generated when the AIS condition is cleared. When RXAPS_NDF_EN is logic 0, no NDF frame is generated when the AIS condition is cleared.

RXAPS_PAIS_EN

The RXAPS_PAIS_EN bit is used to enable the AIS generation when the receive APS J0 character is decoded as all 1's, the 8B/10B encoded PAIS signal is detected, or when loss of J0 alignment, or loss of character alignment is declared by the APS receiver (R8TD), When RXAPS_PAIS_EN is logic 1, the feature is enabled. When RXAPS_PAIS_EN is logic 0, the feature is disabled.

Note that the assertion of AIS for this feature is based on the J0 character being decoded as all 1's. This occurs through the detection of the 8B/10B AIS character, by normal decode of the 8B/10B encoded character for 0xFF, or the assertion of loss-of-character alignment or loss-of-J0 alignment by the APS receiver R8TD. Once the J0 character is not decoded as all 1's, then AIS is deasserted.

RXAPS_LINK_PAIS

The RXAPS_LINK_PAIS is used to configure the four Rx APS link AIS indications as 4 separate STS-12/STM-4 channel or as one STS-48/STM-16 channel. When RXAPS_LINK_PAIS is set to logic 1, the 4 APS links are treated as one STS-48/STM-16 channel. If any one of the APS links loses J0 alignment, character alignment, or detects AIS, then data from all four links will be forced to AIS state. When RXAPS_LINK_PAIS is set to logic 0, the 4 APS links are treated separately.

TLREIINS

The TLREIINS register bit controls the insertion of the line remote error indication into the data stream. When TLREIINS is set to logic 1, the remote errors detected by the RRMP are inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 4. When TLREIINS is set to logic 0, the REI in the M1 byte is set to 0.

Reserved

The Reserved bit must be set to logic 0 for proper operation.

Register 0903H – 090D: S/UNI-2488 Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved register bits must be left at their default value for proper operation. They do not perform any normal mode functions at this time.

Register 090EH – 090F: S/UNI-2488 Reserved

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	Reserved	X
Bit 11	R	Reserved	X
Bit 10	R	Reserved	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 1	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Reserved

The Reserved register bits are read only. They do not perform any normal mode functions at this time.

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-2488. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-2488 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-2488 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 19 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000	Master Test Register
2001	Test Mode Address Force Enable
2002	Test Mode Address Force Value
2003	Reserved
2004-3FFF	Reserved For Test

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 2000H: S/UNI-2488 Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	W	PMCATST_2488	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	Reserved	0
Bit 2	W	Reserved	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-2488 test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the S/UNI-2488 using the RSTB input. PMCTST, PMCATST, and BYPASS are reset when CSB is logic 1. PMCTST, and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for OC48 line side analog test.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-2488 . While the HIZIO bit is a logic one, all output pins of the S/UNI-2488 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

PMCTST

The PMCTST bit is used to configure the S/UNI-2488 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-2488 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors, and all analog blocks are forced into IDDQ mode. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the S/UNI-2488 for PMC's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for OC48 line side analog test. Only PMCATST needs to be set high for APS analog test.

PMCATST_2488

The PMCATST_2488 bit is used to configure the 2488 Mbit/s analog portion of the S/UNI-2488 for PMC's manufacturing tests. The PMCATST_2488 can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCATST_2488 (bit 5 and 6) in this register must be set to high for OC48 line side analog test.

Register 2001H: S/UNI-2488 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TM_A_EN[12]	X
Bit 10	R/W	TM_A_EN[11]	X
Bit 9	R/W	TM_A_EN[10]	X
Bit 8	R/W	TM_A_EN[9]	X
Bit 7	R/W	TM_A_EN[8]	X
Bit 6	R/W	TM_A_EN[7]	X
Bit 5	R/W	TM_A_EN[6]	X
Bit 4	R/W	TM_A_EN[5]	X
Bit 3	R/W	TM_A_EN[4]	X
Bit 1	R/W	TM_A_EN[3]	X
Bit 1	R/W	TM_A_EN[2]	X
Bit 0	R/W	TM_A_EN[1]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A_EN[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN[12:2] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2002H: S/UNI-2488Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	TM_A[12]	X
Bit 10	R/W	TM_A[11]	X
Bit 9	R/W	TM_A[10]	X
Bit 8	R/W	TM_A[9]	X
Bit 7	R/W	TM_A[8]	X
Bit 6	R/W	TM_A[7]	X
Bit 5	R/W	TM_A[6]	X
Bit 4	R/W	TM_A[5]	X
Bit 3	R/W	TM_A[4]	X
Bit 1	R/W	TM_A[3]	X
Bit 1	R/W	TM_A[2]	X
Bit 0	R/W	TM_A[1]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] bit replaces the input pin A[X]. The TM_A[X] bits are not cleared on reset.

Register 2003H: S/UNI-2488 Reserved Test Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	Reserved	X

Reserved

The reserved bits should be set to logic 0 for normal tests. They have no affect on the operation of the device when PMCTST is logic 0.

12.2 JTAG Test Port

The S/UNI-2488 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 20 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110

Instructions	Selected Register	Instruction Codes, IR[2:0]
BYPASS	Bypass	111

Table 21 Identification Register

Length	32 bits
Version Number	3H (for revision D)
Part Number	5381H
Manufacturer's Identification Code	0CDH
Device Identification	353810CDH (for revision D)

Table 22 Boundary Scan Register

Name	Register Bit	Cell Type	Device ID
RFCLK	218	IN_CELL	L
OEB_RDAT[31]	217	OUT_CELL	L
RDAT[31]	216	OUT_CELL	H
OEB_RDAT[30]	215	OUT_CELL	H
RDAT[30]	214	OUT_CELL	L
OEB_RDAT[29]	213	OUT_CELL	H
RDAT[29]	212	OUT_CELL	L
OEB_RDAT[28]	211	OUT_CELL	H
RDAT[28]	210	OUT_CELL	L
OEB_RDAT[27]	209	OUT_CELL	L
RDAT[27]	208	OUT_CELL	H
OEB_RDAT[26]	207	OUT_CELL	H
RDAT[26]	206	OUT_CELL	H
OEB_RDAT[25]	205	OUT_CELL	L
RDAT[25]	204	OUT_CELL	L
OEB_RDAT[24]	203	OUT_CELL	L
RDAT[24]	202	OUT_CELL	L
OEB_RDAT[23]	201	OUT_CELL	L
RDAT[23]	200	OUT_CELL	L
OEB_RDAT[22]	199	OUT_CELL	H
RDAT[22]	198	OUT_CELL	L
OEB_RDAT[21]	197	OUT_CELL	L
RDAT[21]	196	OUT_CELL	L
OEB_RDAT[20]	195	OUT_CELL	L
RDAT[20]	194	OUT_CELL	H
OEB_RDAT[19]	193	OUT_CELL	H
RDAT[19]	192	OUT_CELL	L
OEB_RDAT[18]	191	OUT_CELL	L
RDAT[18]	190	OUT_CELL	H

Name	Register Bit	Cell Type	Device ID
OEB_RDAT[17]	189	OUT_CELL	H
RDAT[17]	188	OUT_CELL	L
OEB_RDAT[16]	187	OUT_CELL	H
RDAT[16]	186	OUT_CELL	-
OEB_RDAT[15]	185	OUT_CELL	-
RDAT[15]	184	OUT_CELL	-
OEB_RDAT[14]	183	OUT_CELL	-
RDAT[14]	182	OUT_CELL	-
OEB_RDAT[13]	181	OUT_CELL	-
RDAT[13]	180	OUT_CELL	-
OEB_RDAT[12]	179	OUT_CELL	-
RDAT[12]	178	OUT_CELL	-
OEB_RDAT[11]	177	OUT_CELL	-
RDAT[11]	176	OUT_CELL	-
OEB_RDAT[10]	175	OUT_CELL	-
RDAT[10]	174	OUT_CELL	-
OEB_RDAT[9]	173	OUT_CELL	-
RDAT[9]	172	OUT_CELL	-
OEB_RDAT[8]	171	OUT_CELL	-
RDAT[8]	170	OUT_CELL	-
OEB_RDAT[7]	169	OUT_CELL	-
RDAT[7]	168	OUT_CELL	-
OEB_RDAT[6]	167	OUT_CELL	-
RDAT[6]	166	OUT_CELL	-
OEB_RDAT[5]	165	OUT_CELL	-
RDAT[5]	164	OUT_CELL	-
OEB_RDAT[4]	163	OUT_CELL	-
RDAT[4]	162	OUT_CELL	-
OEB_RDAT[3]	161	OUT_CELL	-
RDAT[3]	160	OUT_CELL	-
OEB_RDAT[2]	159	OUT_CELL	-
RDAT[2]	158	OUT_CELL	-
OEB_RDAT[1]	157	OUT_CELL	-
RDAT[1]	156	OUT_CELL	-
OEB_RDAT[0]	155	OUT_CELL	-
RDAT[0]	154	OUT_CELL	-
OEB_RPRTY	153	OUT_CELL	-
RPRTY	152	OUT_CELL	-
OEB_REOP	151	OUT_CELL	-
REOP	150	OUT_CELL	-

Name	Register Bit	Cell Type	Device ID
OEB_RSOC_RSOP	149	OUT_CELL	-
RSOC_RSOP	148	OUT_CELL	-
OEB_RSX	147	OUT_CELL	-
RSX	146	OUT_CELL	-
OEB_RERR	145	OUT_CELL	-
RERR	144	OUT_CELL	-
OEB_RMOD[1]	143	OUT_CELL	-
RMOD[1]	142	OUT_CELL	-
OEB_RMOD[0]	141	OUT_CELL	-
RMOD[0]	140	OUT_CELL	-
OEB_RCA_RVAL	139	OUT_CELL	-
RCA_RVAL	138	OUT_CELL	-
RENB	137	IN_CELL	-
OEB_ROHCLK	136	OUT_CELL	-
ROHCLK	135	OUT_CELL	-
OEB_ROHFP	134	OUT_CELL	-
ROHFP	133	OUT_CELL	-
OEB_RTOH	132	OUT_CELL	-
RTOH	131	OUT_CELL	-
OEB_RPOHEN	130	OUT_CELL	-
RPOHEN	129	OUT_CELL	-
OEB_B3E	128	OUT_CELL	-
B3E	127	OUT_CELL	-
OEB_RPOH	126	OUT_CELL	-
RPOH	125	OUT_CELL	-
OEB_OOF	124	OUT_CELL	-
OOF	123	OUT_CELL	-
OEB_SALM	122	OUT_CELL	-
SALM	121	OUT_CELL	-
OEB_RALM	120	OUT_CELL	-
RALM	119	OUT_CELL	-
OEB_TOHCLK	118	OUT_CELL	-
TOHCLK	117	OUT_CELL	-
OEB_TOHFP	116	OUT_CELL	-
TOHFP	115	OUT_CELL	-
TTOH	114	IN_CELL	-
TTOHEN	113	IN_CELL	-
TPOH	112	IN_CELL	-
TPOHEN	111	IN_CELL	-
OEB_TPOHRDY	110	OUT_CELL	-

Name	Register Bit	Cell Type	Device ID
TPOHRDY	109	OUT_CELL	-
SD	108	IN_CELL	-
OEB_RCLK	107	OUT_CELL	-
RCLK	106	OUT_CELL	-
OEB_PGMRCLK	105	OUT_CELL	-
PGMRCLK	104	OUT_CELL	-
OEB_TCLK	103	OUT_CELL	-
TCLK	102	OUT_CELL	-
OEB_PGMTCLK	101	OUT_CELL	-
PGMTCLK	100	OUT_CELL	-
OEB_APSOFP	99	OUT_CELL	-
APSOFP	98	OUT_CELL	-
APSIFP	97	IN_CELL	-
APSIFPCLK	96	IN_CELL	-
OEB_D[15]	95	OUT_CELL	-
D[15]	94	IO_CELL	-
OEB_D[14]	93	OUT_CELL	-
D[14]	92	IO_CELL	-
OEB_D[13]	91	OUT_CELL	-
D[13]	90	IO_CELL	-
OEB_D[12]	89	OUT_CELL	-
D[12]	88	IO_CELL	-
OEB_D[11]	87	OUT_CELL	-
D[11]	86	IO_CELL	-
OEB_D[10]	85	OUT_CELL	-
D[10]	84	IO_CELL	-
OEB_D[9]	83	OUT_CELL	-
D[9]	82	IO_CELL	-
OEB_D[8]	81	OUT_CELL	-
D[8]	80	IO_CELL	-
OEB_D[7]	79	OUT_CELL	-
D[7]	78	IO_CELL	-
OEB_D[6]	77	OUT_CELL	-
D[6]	76	IO_CELL	-
OEB_D[5]	75	OUT_CELL	-
D[5]	74	IO_CELL	-
OEB_D[4]	73	OUT_CELL	-
D[4]	72	IO_CELL	-
OEB_D[3]	71	OUT_CELL	-
D[3]	70	IO_CELL	-

Name	Register Bit	Cell Type	Device ID
OEB_D[2]	69	OUT_CELL	-
D[2]	68	IO_CELL	-
OEB_D[1]	67	OUT_CELL	-
D[1]	66	IO_CELL	-
OEB_D[0]	65	OUT_CELL	-
D[0]	64	IO_CELL	-
A[13]	63	IN_CELL	-
A[12]	62	IN_CELL	-
A[11]	61	IN_CELL	-
A[10]	60	IN_CELL	-
A[9]	59	IN_CELL	-
A[8]	58	IN_CELL	-
A[7]	57	IN_CELL	-
A[6]	56	IN_CELL	-
A[5]	55	IN_CELL	-
A[4]	54	IN_CELL	-
A[3]	53	IN_CELL	-
A[2]	52	IN_CELL	-
A[1]	51	IN_CELL	-
A[0]	50	IN_CELL	-
CSB	49	IN_CELL	-
ALE	48	IN_CELL	-
RDB	47	IN_CELL	-
WRB	46	IN_CELL	-
RSTB	45	IN_CELL	-
OEB_INTB	44	OUT_CELL	-
INTB	43	OUT_CELL	-
TDAT[31]	42	IN_CELL	-
TDAT[30]	41	IN_CELL	-
TDAT[29]	40	IN_CELL	-
TDAT[28]	39	IN_CELL	-
TDAT[27]	38	IN_CELL	-
TDAT[26]	37	IN_CELL	-
TDAT[25]	36	IN_CELL	-
TDAT[24]	35	IN_CELL	-
TDAT[23]	34	IN_CELL	-
TDAT[22]	33	IN_CELL	-
TDAT[21]	32	IN_CELL	-
TDAT[20]	31	IN_CELL	-
TDAT[19]	30	IN_CELL	-

Name	Register Bit	Cell Type	Device ID
TDAT[18]	29	IN_CELL	-
TDAT[17]	28	IN_CELL	-
TDAT[16]	27	IN_CELL	-
TDAT[15]	26	IN_CELL	-
TDAT[14]	25	IN_CELL	-
TDAT[13]	24	IN_CELL	-
TDAT[12]	23	IN_CELL	-
TDAT[11]	22	IN_CELL	-
TDAT[10]	21	IN_CELL	-
TDAT[9]	20	IN_CELL	-
TDAT[8]	19	IN_CELL	-
TDAT[7]	18	IN_CELL	-
TDAT[6]	17	IN_CELL	-
TDAT[5]	16	IN_CELL	-
TDAT[4]	15	IN_CELL	-
TDAT[3]	14	IN_CELL	-
TDAT[2]	13	IN_CELL	-
TDAT[1]	12	IN_CELL	-
TDAT[0]	11	IN_CELL	-
TPRTY	10	IN_CELL	-
TEOP	9	IN_CELL	-
TSOC_TSOP	8	IN_CELL	-
TERR	7	IN_CELL	-
TMOD[1]	6	IN_CELL	-
TMOD[0]	5	IN_CELL	-
OEB_TCA_DTPA	4	OUT_CELL	-
TCA_DTPA	3	OUT_CELL	-
TFCLK	2	IN_CELL	-
TENB	1	IN_CELL	-
POSL3_UL3B	0	IN_CELL	-

Note 1: When set high, INTB will be set to high impedance.

Note 2: Each output cell has its own output enable (OEB_*)

Note 3: POSL3_UL3B is the first bit in the boundary scan chain, and RFCLK is the first bit out of the boundary scan chain.

12.3 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 20 Input Observation Cell (IN_CELL)

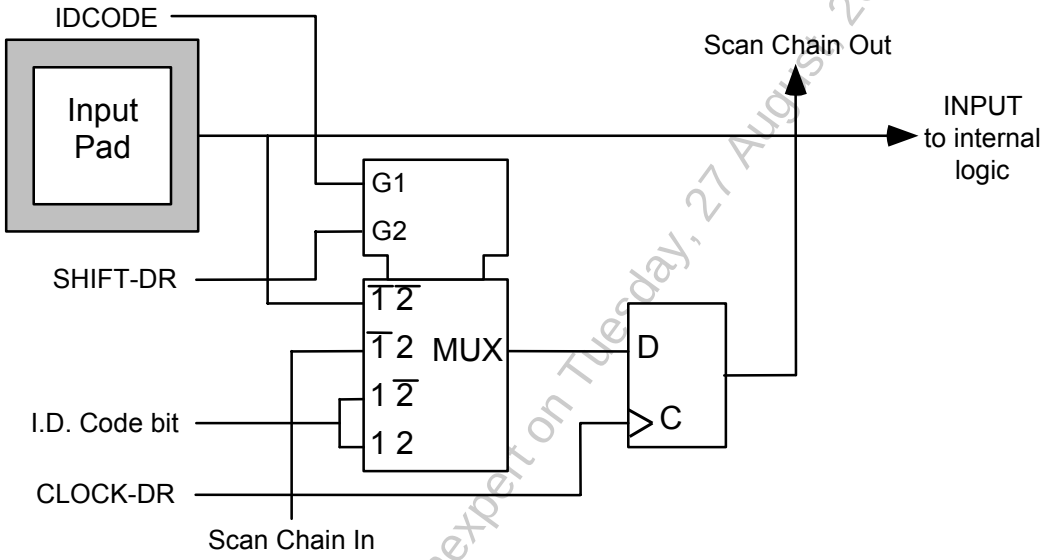


Figure 21 Output Cell (OUT_CELL)

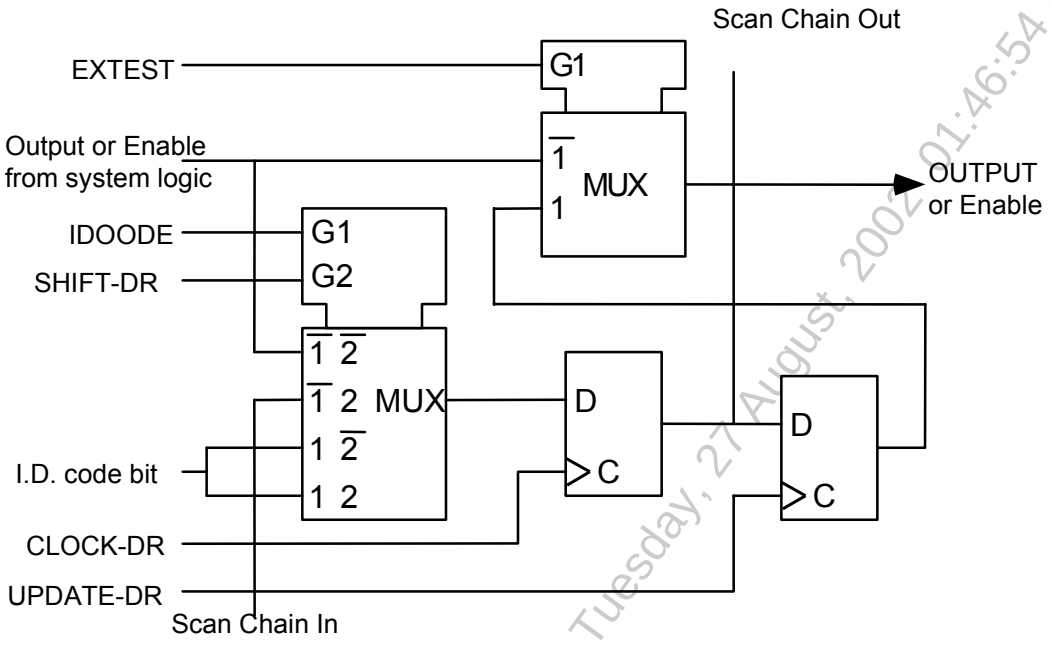


Figure 22 Bidirectional Cell (IO_CELL)

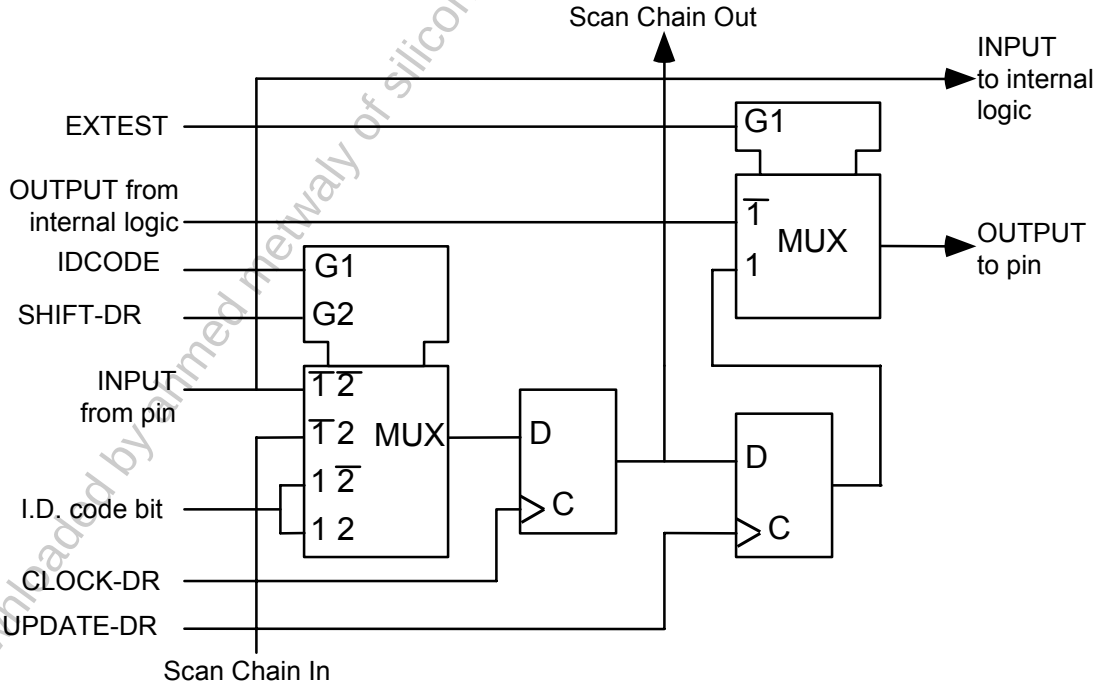
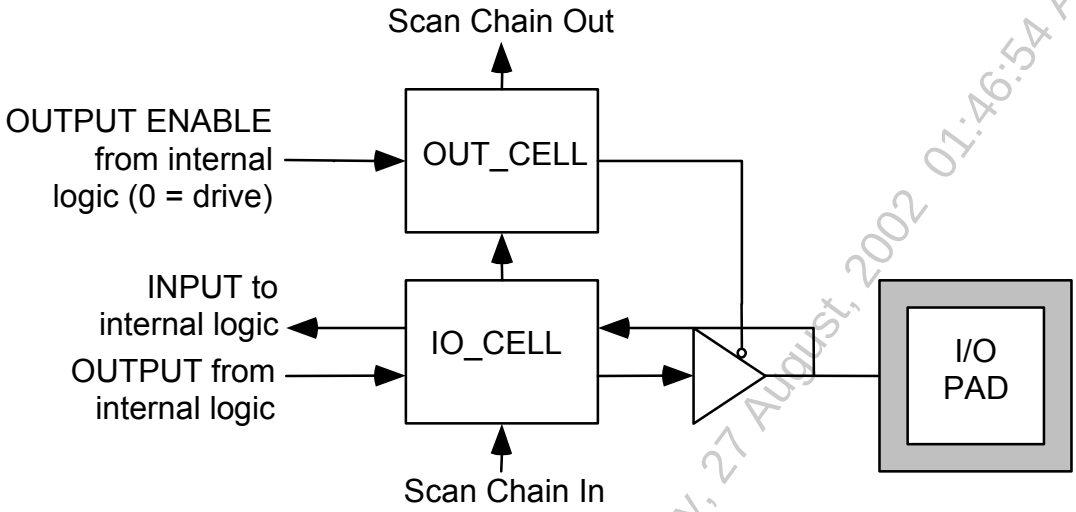


Figure 23 Layout of Output Enable and Bidirectional Cells



13 Operation

13.1 APS Serial TelecomBus (LVDS) Operation

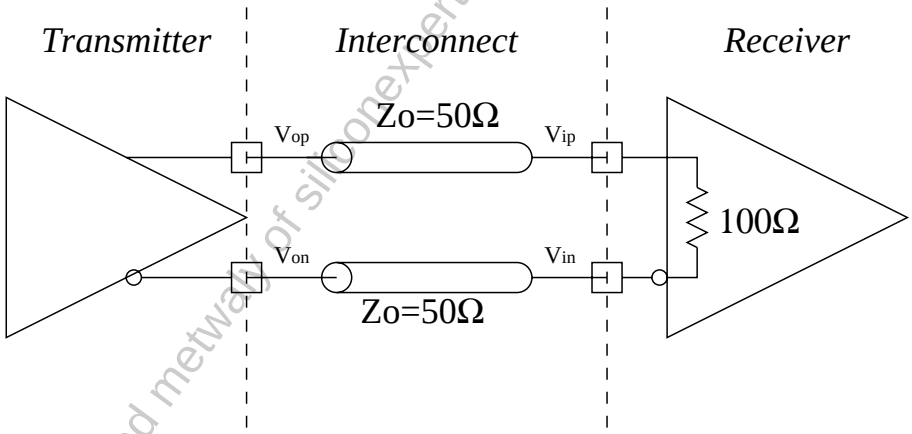
13.1.1 LVDS Overview

The LVDS APS Port implements the 777.6 Mb/s LVDS links. Four 777.6 Mb/s LVDS form a high-speed serial TelecomBus interface for passing an STS-48 aggregate data stream.

A reference clock of 77.76MHz is required via the APSIFPCLK pin. This clock must be an exact divide-by-two of the REFCLK being provided to the chip. Do not use the TCLK or RCLK outputs of the S/UNI-2488 as they are not reliable enough to provide this reference and are not intended for this purpose.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 24 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz APSIFPCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from a divided version of REFCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). It is expected that the clock source of the transmitter is the same as the clock source of the receiver to ensure the data throughput at both ends of the link are identical.

Data must contain sufficient transition density to allow reliable operation of the data recovery units. 8B/10B block coding and decoding is provided by the T8TE and R8TD blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors and up to 1m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350mV.

The LVDS system is comprised of the LVDS Receiver (RXLV), Data Recovery Unit (DRU), Receive 8B/10B TelecomBus Decoder (R8TD), Transmit 8B/10B TelecomBus Encoder (T8TE), APS Parallel to Serial converter (APISO), LVDS Transmitter (TXLV) and Transmitter LVDS Reference (TXLVREF), and Clock Synthesis Unit (CSU) blocks.

13.1.2 LVDS Receiver (RXLV)

The RXLV ABC is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLV ABC is the receiver accepts up to 777.6 Mb/s LVDS signals from the transmitter, amplifies them, converts them to digital signals and passes them to a data recovery unit (DRU). As per to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100mV, and includes at least 25mV of hysteresis.

13.1.3 Data Recovery Unit (DRU)

The DRU is a fully integrated data recovery and serial to parallel converter which is used for 777.6 Mb/s NRZ data. An 8B/10B block code is used to guarantee transition density for optimal performance. The DRU recovers data and outputs a 10-bit word synchronized with a line rate divided by 10 gated clock to allow frequency deviations between the data source and the local oscillator. The DRU accumulates 10 data bits and outputs them on the next clock edge.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

13.1.4 Receive 8B/10B TelecomBus Decoder (R8TD)

The R8TD works in conjunction with the upstream DRU that packs consecutive bits from an incoming 8B/10B serial link into a 10-bit wide stream with arbitrary alignment to the 8B/10B character boundaries.

The R8TD character alignment block uses the K28.5 control character (Comma control / transport frame alignment) to determine 8B/10B character alignment in the incoming stream. When the R8TD character alignment state machine is in the out-of-character-alignment state, it searches for the K28.5 character in all positions of the incoming stream. Upon detecting the K28.5 character, the R8TD will align its internal character boundary, the character alignment state machine will transition to the in-character-alignment state and cease searching for subsequent K28.5 characters. The character alignment block also monitors for line-code violations (LCV) which are accumulated in an internal register. If 5 or more LCVs are detected within a window of 15 characters, the R8TD will enter the out-of-character-alignment state and begin searching for the K28.5 character afresh.

When operating in FIFO mode, aligned characters are written into a 24-character FIFO that isolates the incoming timing domain from the outgoing timing domain and provides a means of synchronizing multiple R8TDs outputs. Otherwise, the FIFO is bypassed.

In order to allow synchronization with other R8TDs that may have slightly different frame alignment and to allow for frame re-alignment, the R8TD frame alignment block monitors the character aligned data stream for the K28.5. An internal frame counter is maintained based on this character. If the K28.5 is found out of place three times, then the frame alignment moves to the out-of-frame-alignment state. When in the out-of-frame-alignment state, the first K28.5 will be written to the 0 position of the FIFO. The read pointer is then set by the APSIFP signal to synchronize the output of the K28.5 characters which ensures that signals leaving the multiple R8TDs will have the same alignment.

The R8TD decodes 8B/10B control characters associated with specific SONET/SDH byte positions in an extended TelecomBus stream. In order to identify more SONET/SDH bytes than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K38.7, K23.7, K27.7, K29.7 and K30.7) are treated specially, where the positive and negative disparity codes are each associated with a different SONET/SDH byte. The reception of these line-codes will not be considered LCVs due to a mismatch with the running disparity.

The R8TD provides a diagnostic loopback port where the outgoing stream from an associated Transmit 8B/10B Encoder block (T8TE) can be processed in place of the incoming stream.

13.1.5 Transmit 8B/10B TelecomBus Encoder (T8TE)

The T8TE encodes a TelecomBus data stream and encodes it into an extended 8B/10B format for transmission on the serial LVDS links. The T8TE encodes TelecomBus control signals such as transport frame and payload boundaries, pointer justification events and alarm conditions into three levels of extended set of 8B/10B characters as well as performing the IEEE mode conversion on data. In order to identify more TelecomBus bytes and events than the 12 control characters available in the standard set, those control characters with balanced line codes for both positive and negative running disparity (K28.0, K28.4, K28.5, k28.6, k28.7, K23.7, K27.7, K29.7 and K30.7) are treated specially. The positive and negative disparity codes are each associated of a different SONET/SDH byte or event.

13.1.6 APS Parallel to Serial Converter (APISO)

The APISO is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mb/s.

13.1.7 LVDS Transmitter (TXLV)

The TXLV is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification. The TXLV accepts 777.6 Mbit/s differential data from the APSIO circuit and transmits the data off-chip as a low voltage differential signal. The TXLV uses the reference current and voltage from the TXLVREF to control the output differential voltage amplitude and the output common-mode voltage.

13.1.8 Character Alignment

The character alignment sub-block locates character boundaries in the incoming Serial TelecomBus 8B/10B data stream. The framer logic may be in one of two states, SYNC state and HUNT state. It uses the 8B/10B control character (K28.5) which encodes the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. It monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in IEEE std. 802.3. Excessive LCVs are used to transition the framer logic to the HUNT state.

Normal operation occurs when the character alignment sub-block is in the SYNC state. 8B/10B characters are extracted from the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If 5 or more LCVs are detected in a window of 15 characters, the character alignment sub-block transitions to the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. In the mean time, the original character alignment is maintained until a K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block transitions to the SYNC state.

13.1.9 Frame Alignment

The frame alignment sub-block monitors the data read from the FIFO buffer sub-block for the J0 byte. When the frame counter sub-block indicates the J0 byte position, a J0 character is expected to be read from the FIFO. If a J0 byte is read out of the FIFO at other byte positions, a J0 byte error counter is incremented. When the counter reaches a count of 3, the frame alignment sub-block transitions to HUNT state. The next time a J0 character is read from the FIFO, the associated read address is latched and the sub-block transitions back to the SYNC state. The J0 byte error counter is cleared when a J0 byte is read from the FIFO at the expected position.

13.1.10 Character Decode

The following tables show the extended 8B/10B maps used by the S/UNI-2488. The extended character set allows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into two sections, one for each software configurable mode of operation.

Table 23 Serial TelecomBus 8B/10B Control Character Decoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	Transport frame alignment
K.28.4-	001111 0010	-	High-order path AIS
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	High-order path H3 byte, no negative justification event
K28.0+	-	110000 1011	High-order path PSI byte, positive justification event
K28.6	001111 0110	110000 1001	High-order path frame alignment. The K28.6 character which signals the J1 byte position is decoded as 0x00 by the R8TD.

13.1.11 Character Encode

The T8TE block encodes the TelecomBus control characters into an extended set of 8B/10B TelecomBus control signals. The table is divided into two sections, one for each mode of operation in the 8B/10B encoder in an external device upstream of the S/UNI-2488.

Table 24 Serial TelecomBus 8B/10B Control Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	Transport frame alignment
K.28.4-	001111 0010	-	High-order path alarm
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	High-order path H3 byte, no negative justification event
K28.0+	-	110000 1011	High-order path PSO byte, positive justification event
K28.6	001111 0110	110000 1001	High-order path frame alignment. The K28.6 character which signals the J1 byte position is decoded as 0x00 by the R8TD.

13.1.12 Serial TelecomBus MST and HPT Modes

The S/UNI-2488 can be made to operate in either Multiplex Section Termination (MST) or High Order Path Termination (HPT) mode.

MST mode is used for systems where each payload terminating device has J1 pointer interpretors so only the J0 frame indicator is required. MST mode **MUST** be used if the LVDS ports are used in a cross-connect application and may be used if the S/UNI-2488 is the APS working device in an APS application (see Figure 6).

HPT mode is used for systems which have devices that do not have J1 pointer interpretors so J1 indications are required on the TelecomBus interfaces. The S/UNI-2488 **MUST** be configured for HPT mode when the S/UNI-2488 is being used as the APS protect device in an APS application (see Figure 7).

The serial TelecomBus needs to be configured for MST or HPT modes. In MST mode, the J1 character is not overwritten by special 8B/10B characters. In HPT mode, it is specially marked to indicate the J1 location.

On the S/UNI-2488 APSO interface, MST mode is activated for timeslot ***x*** by setting the TMODE***x***[1:0] bits to logic 'b00 in the T8TE TelecomBus Mode #1 and T8TE TelecomBus Mode #2 registers. HPT mode is activated by setting TMODE***x***[1:0] to logic 'b01. Note that regardless of the MST/HPT setting in the transmit direction, valid H1/H2 bytes (J1 Pointer) are always output on the TelecomBus, so a downstream device may operate in MST mode.

13.2 Cross Connect Mode of Operation

The processing of an STS-48c frame is the normal mode of operation of the S/UNI-2488, however, the device can also be configured to process any mixture of STS-12c, STS-3c or STS-1 payloads within an STS-48 frame. This mode of operation is supported to allow for use in cross connect applications where multiple S/UNI-2488s are connected to a cross connect fabric (such as the PM5372 TSE) through the S/UNI-2488's APS ports.

The XCONNECTMODE register bit of register 0001H (S/UNI Master Reset, Configuration and Loopback register) controls the cross connect mode of operation. When this bit is set to logic 1, the four RHPP and SVCA blocks of the S/UNI-2488 operate as independent STS-12 masters (normally, these blocks are configured as one master and three slaves in order to process an STS-48c payload). The RHPP and SVCA registers must then be programmed for their payload types.

Each RHPP processes the path overhead of any legal mix of STS-1/3c/12c (VC-3/4/4-4c) payloads. The STS (VC) payloads are independently floating inside the transport frame and the RHPP interprets each of the STS-1/3c/12c (AU3/4/4-4c) pointers in order to locate the boundaries of the payloads i.e. the path trace bytes (J1). Once the STS (VC) payloads are located, the RHPP extracts the path overhead bytes, the fixed stuff bytes and the entire synchronous payload envelope (SPE) bytes.

The pointer interpreter state machines detect path loss of pointer (LOP-P) and path alarm indication signal (AIS-P) defects on the STS (AU) pointers and report the status on two separate ports PLOP and PAIS. The concatenation pointer interpreter state machines detect path loss of pointer concatenation (LOPC-P) and path concatenation alarm indication signal (AISC-L) defects on the STS (AU) concatenated pointers and report the status on two separate ports LOPC and PAISC.

The RHPP accumulates path bit interleaved parity (BIP-8) errors and path remote error indication (REI-P) errors for each of the STS (VC) payloads. The path BIP-8 errors are serially output on a low speed serial port (note, for the S/UNI-2488, only RHPP#1 can serially output BIP-8 errors). Microprocessor readable registers are provided to allow accumulated path BIP-8 errors and path REI errors to be read out at intervals of up to 1 second. Optionally, the RHPP can be configured to accumulate block BIP-8 errors and to extract block REI errors.

The RHPP extracts the path payload signal label byte (PSL-P) from the C2 byte of the STS (VC) payloads. Two algorithms are defined to detect path payload label unstable (PLU-P), path payload label mismatch (PLM-P), path unequipped defect (UNEQ-P) and path payload defect indication (PDI-P) defects on the PSL. The first algorithm is compliant to BELLCORE specifications and the second algorithm is compliant to ITU specifications.

The RHPP detects path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects on the G1 byte of the STS (VC) payloads and indicates their status on two separate ports PRDI and PERDI. The accepted path ERDI value is stored in a microprocessor readable register.

The RHPP supports path REI and path ERDI inband error reporting by optionally regenerating the G1 byte with updated path REI and path RDI values that must be returned to the far end.

The receive path overhead (RPOH) port serially outputs the path overhead (POH) bytes of the STS (VC) payloads of the first STS-12. A 20.736 MHz clock is generated to provide timing for the RPOH port.

The RHPP provides an interrupt output to indicate any change in the status of pointer justifications (NJE, PJE), path loss of pointer (LOP-P, LOPC-P), path alarm indication signal (AIS-P, AISC-P), path payload signal label (PSL-P), path payload label unstable (PLU-P), path payload label mismatch (PLM-P), path unequipped (UNEQ-P), path payload defect indication (PDI-P), path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) or any path BIP-8 errors and path remote error indication (REI-P) errors. An internal register can be read to identify the interrupt source. Each interrupt source is individually maskable.

Note that while the RHPP will perform path-level processing on the receive data stream, the S/UNI-2488 does not perform consequential action of asserting RDI-P for path level alarms.

Each SVCA aligns the transport overhead of an STS-12 stream to a new reference signal (APSIFP). The alignment is accomplished by recalculating the STS payload pointer value based on the offset between the transport overhead of the incoming and outgoing streams

The SVCA can be used to process higher concatenated payloads (STS-48c/VC4). An STS-48c/VC-4-16c is processed by four SVCAs. The first SVCA is master and the three others are slaves.

Frequency offsets (e.g., due to plesiochronous network boundaries or the loss of a primary reference-timing source) and phase differences (due to normal network operation) between the incoming and the outgoing streams are accommodated by outgoing pointer adjustments. Outgoing pointer justification events are indicated on two separate outputs. A slave SVCA uses one of these outputs to perform the required justification when a concatenated STS-48c/STM-16c is processed. The other set of outputs can be used for performance monitoring. Excessive pointer justification events may indicate network synchronisation failure. Finally, the SVCA provides pointer justification performance counters for each path.

The SVCA aligns the synchronous payload of any legal mix of STS-1/3c/12c (VC-3/4/4c). The STS (VC) payloads are independently floating inside the STS-12 (STM-4) transport frame. The SVCA aligns each one independently. The output pointer justification events are multiplexed among all the output streams.

Each SVCA provides an interrupt output to indicate any changes in the status of output pointer justification (NJE, PJE) and FIFO overflows or underflows. Each interrupt source is independently maskable.

The SVCA modifies the transport overhead as follows (Table 25 shows the STS-1 configuration):

Table 25 SVCA STS-1 Transport Overhead Modification

Section Overhead	A1	A2	00	
	00	00	00	
	00	00	00	
Pointers	H1	H2	H3 : Negative Opportunity	P0 : Positive Opportunity
Line Overhead	00h	00h	00h	
	00h	00h	00h	
	00h	00h	00h	
	00h	00h	00h	
	00h	00h	00h	

In the cross connect mode of operation, the APSMUX_RCFP and APSMUX_T8TE register bits must be set to logic 1 so that data are output on the APSO_P/ APSO_N[4:1] port as well as received on the APSI_P/ APSI_N[4:1] port in the correct manner. Please see the S/UNI-2488 Master Reset, Configuration and Loopback register (register 0001H) for a complete description.

For proper operation in a CHESS system, the T8TEs' CENTER bit must be set to logic 1 after the APS CSU is locked. This is the only way to guarantee that all transmit FIFO depths are within 1 or 2 clock cycles of each other. This is required for J0 alignment at the far end.

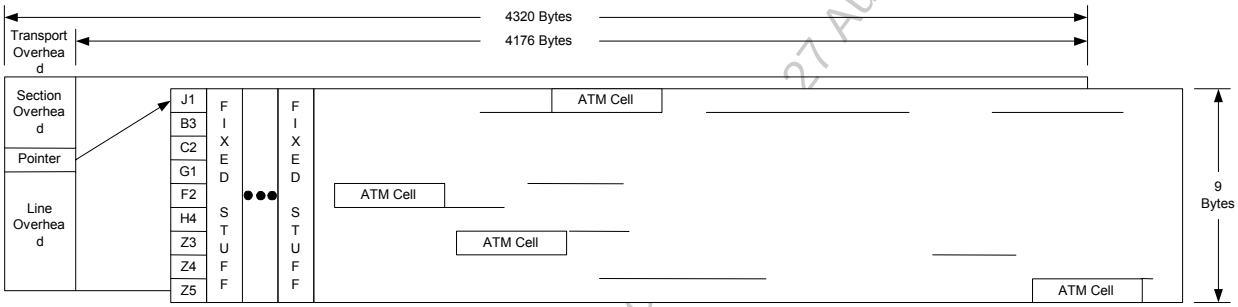
When XCONNECTMODE is a logic 1, the behavior of the POS-PHY Level 3 / UTOPIA Level 3™ port is undefined, since that port is only configured to operate as a single port device.

13.3 SONET/SDH Frame Mappings and Overhead Byte Usage

13.3.1 ATM Mapping

The S/UNI-2488 processes the ATM cell mapping for STS-48c (STM-16c) as shown below in Figure 25. The S/UNI-2488 processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-2488 provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 25, the STS-48c (STM-16c) mapping is shown. In this mapping, fifteen stuff columns are included in the SPE. No other options are provided.

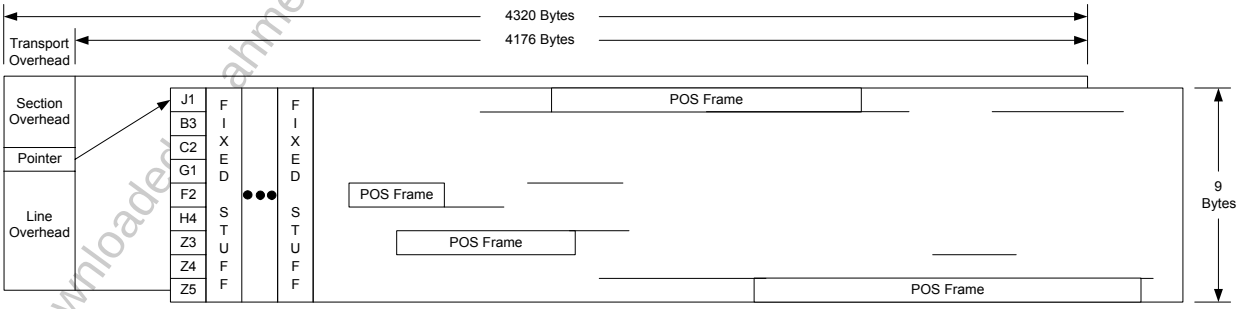
Figure 25 ATM Mapping



13.3.2 Packet Over SONET Mapping

The S/UNI-2488 processes the Packet Over SONET mapping for STS-48c (STM-16c) as shown below in Figure 26. The S/UNI-2488 processes the transport and path overhead required to support Packet Over SONET applications. In addition, the S/UNI-2488 provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. Figure 26, the STS-48c (STM-16c) mapping is shown. In this mapping, the SPE is used for POS Frames. Again, there is one path overhead and 15 fixed stuff columns.

Figure 26 Packet Over SONET Mapping



13.3.3 Transport and Path Overhead Bytes

Transport Overhead Bytes

The Transport Overhead Bytes (TOH) consist of the Section Overhead (SOH) and Line Overhead (LOH) bytes. The S/UNI-2488 has the ability to extract these bytes from the received SONET/SDH frame and also to insert overhead into the transmit stream. This can be done via the RTOH and TTOH ports. See also Section 14.5 in the functional timing chapter for more information on these ports. Note that only the first STS-12 is accessible in this manner.

Section and Line overhead can also be inserted by the TRMP as illustrated in Table 4 in Section 10.12: Transmit Regenerator Multiplexer Processor (TRMP). The TOH should always be configured either via the TTOH port or by the insertion registers within the TRMP.

The TOH consists of the following bytes:

- **A1, A2:** The frame alignment bytes (A1, A2) locate the SONET frame in the STS-48c (STM-16c) serial stream.
- **J0:** The J0 byte is currently defined as the STS-48c (STM-16c) section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.
- **Z0:** The Z0 bytes are currently defined as the STS-48c (STM-16c) section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.
- **B1:** The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the S/UNI-2488 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

- **D1 - D3:** The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.
- **H1, H2:** The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the S/UNI-2488 inserts a fixed pointer value, with a normal new data flag indication in the first H1-H2 pair. The concatenation indication is inserted in the remaining H1-H2 pairs (STS-48c (STM-16c)). Pointer movements can be induced using the THPP registers.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

- **H3:** The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

- **B2:** The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-2488 calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

- **K1, K2:** The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the S/UNI-2488 provides register control for the K1 and K2 bytes.

In the receive direction, the S/UNI-2488 provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

- **D4 - D12:** The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.
- **S1:** The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of STS-48c (STM-16c) signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the S/UNI-2488 provides register control for the synchronization status byte.

In the receive direction, the S/UNI-2488 provides register access to the synchronization status byte.

- **Z1:** The Z1 bytes are located in the second and third STS-1's locations of an STS-48c (STM-16c) and are allocated for future growth.
- **M1:** The M1 byte is located in the third STS-1 location of a STS-48c (STM-16c) and provides a line far end block error function for remote performance monitoring.
- **Z2:** The Z2 bytes are located in the first and second STS-1's locations of a STS-12c (STM-4c) and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

Path Overhead Bytes

The Path Overhead (POH) contains each of the bytes mentioned in this section. POH can be extracted and inserted via the RPOH and TPOH ports respectively. Note that only the first STS-12 can be accessed in this manner. This is wholly sufficient for OC-48c as there is only one POH and it occurs in the first STS-1. Some POH bytes cannot be extracted for some configurations in cross-connect mode. No POH can be inserted in cross-connect mode. See also the description of POH Insertion and Extraction in the Functional Timing section of this document.

POH can also be inserted by the THPP via register writes. See the THPP description in the Functional Description chapter. The POH should always be configured either via the TPOH port or by the insertion registers within the THPP.

The POH consists of the following bytes:

- **J1:** The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TTTP Path Trace register. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

- **B3:** The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI-2488 calculates the B3 bytes. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-2488 calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

- **C2:** The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13. For Packet over SONET (including $X^{43}+1$ payload scrambling), the identification code is 0x16.
- **G1:** The path status byte provides a path RDI function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI-2488 provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path RDI, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path RDI code has 9 legal values, namely 0 to 8 errors.

In the receive direction, a legal path RDI value is accumulated in the path RDI event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

- **H4:** The multi-frame indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.
- **Z3 - Z5:** The path growth bytes provide three unused bytes for future use.

In the transmit direction, the growth bytes may be inserted from the three THPP Path Growth byte registers.

13.4 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-2488 using a 52 byte cell structure on a 32-bit UTOPIA level 3 compliant interface.

Figure 27 shows the ATM cell format for the S/UNI-2488 at the UTOPIA Level 3 interface. It is the 13x32-bit word structure with no HCS or UDF bytes.

Bit 31 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first four header octets).

Figure 27 A 52 Byte ATM Data Structure

	Bit 31 Bit 16		Bit 15 Bit 0	
Word 1	H1	H2	H3	H4
Word 2	Payload 1	Payload 2	Payload 3	Payload 4
Word 3	Payload 5	Payload 6	Payload 7	Payload 8
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Word 12	Payload 41	Payload 42	Payload 43	Payload 44
Word 13	Payload 45	Payload 46	Payload 47	Payload 48

13.5 POS/HDLC Data Structure

Packets may be passed to/from the S/UNI-2488 using a 32-bit POS-PHY Level 3 compliant interface.

The 32-bit POS-PHY Level 3 data structure is shown in Figure 28. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET line. All words are composed of four octets, except the last word of a packet which can have one, two, three, or four octets. If the Transmit Packet Processor (TCFP) is configured to not insert the FCS field, then these bytes should be included with the packet passed through the POS-PHY L3 interface. Similarly, if the Receive Packet Processor (RCFP) is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 28 A 63 Byte Packet Data Structure

	Bit 31	Bit 16	Bit 15	Bit 0
Word 1	Byte 1/SOP	Byte 2	Byte 3	Byte 4
Word 2	Byte 5	Byte 6	Byte 7	Byte 8
Word 3	Byte 9	Byte 10	Byte 11	Byte 12
. . .	. . .	. . .	. . .	. . .
Word 15	Byte 57	Byte 58	Byte 59	Byte 60
Word 16	Byte 61	Byte 62	Byte 63/EOP	Unused

Both the start of the packet and the end of the packet must be identified by the TSOP/RSOP and TEOP/REOP signals. When the first section of a packet is transferred over the interface, the TSOP/RSOP signals will be high for Byte 1 of the packet only. The TMOD[1:0] pins will indicate how many bytes of the final word are valid. Bits 31 to 24 form the first transmitted byte and bit 31 is the bit which is transmitted first.

13.5.1 Limitation When Using Externally Generated FCS In STS-48c Mode

When the S/UNI-2488 is set up in STS-48c POS mode and FCS bytes are passed through the transmit POS-PHY L3 interface, the overall throughput is reduced. The maximum bandwidth throughput will be reduced by a maximum of 2 bytes per packet. The overall effect will depend on the length of the packets + FCS bytes being transferred through the POS-PHY L3 interface. If the packet + FCS length is evenly divisible by 4 bytes, no bandwidth is lost for that packet.

13.5.2 Limitations From Small Packets

The S/UNI-2488 cannot handle packet payloads (excluding FCS) which are smaller than 4 bytes.

In the receive direction, the RCFP should be programmed such that the minimum packet size is at least 4 bytes + FCS. Packet payloads of size 3 bytes or less are tagged by the RCFP packet processor and marked as minimum length violations. For the case where the FCS is passed through the PL3 bus, the min size (packet + FCS) must be at least 5 bytes.

In the transmit direction, the minimum packet payload size permitted is 4 bytes. The exception to this is when the packet is aborted by use of the TERR pin. Aborted packets can be less than the 4 byte minimum. The S/UNI-2488 will extend these packets to 4 bytes before tagging with the appropriate abort sequence.

13.6 TXSDQ and RXSDQ "Block" Sub-Units

The TXSDQ and RXSDQ FIFOs each have a maximum capacity of 3072 bytes. However, the FIFO is divided up into 192 sub-units called blocks. Each block is 16 bytes in size and is the smallest resolution discernable by the TXSDQ and RXSDQ. This means that a packet fragment smaller than 16-bytes and ending with an EOP will use up an entire block. For example, a 17-byte packet will use up two blocks even though the 2nd block is only 1/16th occupied. The remaining 15/16th cannot be used by another packet and is wasted. A 32-byte packet will also use up two blocks, but this time, none of the FIFO capacity is wasted. A 72-byte packet will use up five blocks. The first four blocks will each be fully utilized. The remaining 8 bytes will fill half of the remaining block. The other half of that block is wasted.

13.7 TXSDQ Buffer Available Operation

For the FIFO configured in the TXSDQ, a Buffer Available (BA) bit indicates whether on not the FIFO can accept more data. The BA status is given (BA = 1) when the TXSDQ can accommodate at least another injection of BT[4:0] + 1 blocks (block = 16 bytes) into its FIFO. When the number of blocks available in the FIFO is less than (BT[4:0] + 1), then BA is deasserted (BA = 0). At this point, no more new data can be accepted, but the current transaction completes (if BT is not set at the maximum for the FIFO). Eventually, when some of the data in the FIFO is drained by the read interface, the available FIFO space will equal or exceed BT[4:0] + 1. BA is asserted when this condition is reached. The BA state is reflected by the TCA and DTPA output signals on the Utopia L3 and POS-PHY L3 interfaces when the PHY is selected and/or polled.

In setting the TXSDQ buffer available threshold BT[4:0], the maximum data burst size from the upstream device must be taken into account. Section 13.12 describes how to program BT[4:0] to keep the upstream device from overflowing the TXSDQ FIFO. In general, the following formula applies:

$(BT[4:0] + 1) \geq$ max burst size from upstream device + system application margin

The values of BT[4:0] and DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

$(DT[7:0] + 1) + (BT[4:0] + 1) \leq$ FIFO size

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and DT[7:0] is the TXSDQ is set in the TXSDQ Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP block does not have enough data to initiate a transfer.

For UL3 ATM FIFOs, BT[4:0] and DT[7:0] must be set equal to the value 3. This sets the threshold to be 4 blocks which is the space occupied by an ATM cell.

For PL3 FIFOs, BT[4:0] should be set according to the rules specified in 13.12. For ATM FIFOs, this value should be at least 3 and the upstream device should set its maximum burst size to be equal to one ATM cell.

13.8 RXSDQ and TXSDQ Data Available and Burst-Size Operation

In the RXSDQ and TXSDQ blocks, the FIFO indicates whether or not data is available for reading by asserting the Data Available line (DA). The DA line is asserted by the RXSDQ or TXSDQ under two conditions:

- If the queue depth of the FIFO is greater than a user configured Data Available Threshold (DT), i.e. if there is more data than specified by the threshold.
- If at least one EOP is stored in the FIFO, i.e. the tail end of at least one packet is available in the threshold.

The DA line gets de-asserted when the data in the FIFO falls below the threshold and there are no EOPs in the FIFO. For the RXSDQ, the DA state is reflected by the RCA output signal on the Utopia L3 interface. When using the POS-PHY L3 interface, the RXPHY polls the DA signals using its Calendar Sequence to determine if there is any data in the PHY to output.

For the RXSDQ, the BURST_SIZE[3:0] setting in the RXPHY Indirect Burst Size register is closely tied to the DT[7:0] setting in the RXSDQ FIFO Indirect Data Available Threshold register. BURST_SIZE[3:0] must be set to a value less than or equal to (DT[7:0]). This will prevent the RXPHY from initiating a burst until there is sufficient data in the RXSDQ.

For transfer of ATM cells, the BURST_SIZE[3:0] and DT[7:0] must both be set to the value 3. This makes the threshold equal to 4 blocks which will contain one ATM cell.

It is also important to note that larger burst sizes may cause the FIFO in the RXSDQ to reach higher fill levels because more time is needed for the PHY to complete a burst. Also, since a burst is terminated when an EOP signal is detected, small packets will cause the PHY to be penalized in net throughput across the POS-PHY L3 interface. To maximize fairness, it is recommended to keep the burst size fairly small – on the order of 4 blocks (BURST_SIZE[3:0] = 0x3).

In the TXSDQ, once the DA signal indicates that enough data is in the TXSDQ to begin a cell or packet transfer, the downstream TCFP block will begin pulling data from the FIFO. It will continue pulling regardless of the DA state until the cell or packet is complete. At this time, it will start the next cell or packet transfer from the TXSDQ only after the DA signal is again asserted.

The value of DT[7:0] in the TXSDQ Indirect Data and Buffer Available Thresholds register must be set so that:

$$(DT[7:0] + 1) + (BT[4:0] + 1) \leq \text{FIFO size}$$

The FIFO size is set using the FIFO_BS[1:0] register bits in the TXSDQ FIFO Indirect Configuration register and BT[4:0] is set in the TXSDQ FIFO Indirect Data and Buffer Available Thresholds register. This constraint keeps the FIFO from entering a state where the TXSDQ cannot sustain a new burst from the upstream device and the downstream TCFP block does not have enough data to initiate a transfer.

For packet data streams, it is recommended that DT[7:0] be set to a value close to half or 2/3 of the size of the FIFO. For ATM cell streams, DT[7:0] must be set to the value 0x3.

13.9 Setting ATM Mode of Operation over Utopia L3 or POS-PHY L3

ATM is the default operation mode for the S/UNI-2488. The following sequence of operation should be used to prepare an ATM channel.

1. Input pin POSL3/UL3B must be tied to logic 1 to enable mixed-ATM/POS operation or to logic 0 for pure ATM operation with Utopia Level 3 interface. The POS-PHY L3 interface must be used for dual-mode operation. This must be set at power-up.

2. Unprovision (disable) the TCFP, RCFP, RXSDQ, and TXSDQ blocks. The FIFO of the channel will be reset and emptied when unprovisioned.

3. Leave the TXSDQ and RXSDQ BT[4:0] and DT[7:0] values equal to their default values of 3 respectively. See Sections 13.7 and 13.8 for details.

4. Set the POS_SEL register bits in the TCFP, RCFP, RXSDQ, and TXSDQ blocks to logic 0.

5. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI-2488 Identity and Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.10 Setting Packet Mode of Operation Over POS-PHY L3

The following sequence of operation should be used to prepare a channel for Packet operation without affecting other channels.

1. Input pin POSL3/UL3B must be tied to logic 1 to enable the POS-PHY L3 system interface at power-up.

2. Unprovision (disable) the TCFP, RCFP, RXSDQ, and TXSDQ blocks. The FIFO will be reset and emptied when unprovisioned.

3. Set the POS_SEL register bits in the TCFP, RCFP, RXSDQ, and TXSDQ blocks to logic 1.

4. Set the RXSDQ Data Available threshold (DT[7:0]) values to the desired values. See Section 13.8 for details.

5. Enter the RXPHY BURST_SIZE[3:0]. See Section 13.8 for details.

6. Enter the TXSDQ Buffer Available Threshold (BT[4:0]). See Section 13.7 for details.

7. Enter the TXSDQ Data Available Threshold (DT[7:0]). See Section 13.8 for details.

8. Optionally, reset the performance monitoring counters in all blocks by writing to the S/UNI-2488 Identity and Global Performance Monitor Update register. TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.11 Setting Transparent Mode of Operation Over POS-PHY L3

To send transparent data from the POS-PHY L3 bus, configure the S/UNI-2488 for Packet Over SONET mode as in Section 13.10 with the following amendments:

1. Set the DELINDIS bits and clear the CRC_SEL bits of the TCFP and RCFP.

2. Make sure that the FIFO on the transmit side will never underrun. A FIFO underrun in Transparent mode would result in data corruption.

3. Data should be transferred over the POS-PHY Level3 bus broken up into 64 byte packets

13.12 Transmit PL3 DTPA Behavior

The DTPA signal gives the status of the FIFO which is being filled by the transmit PL3 interface.

When DTPA is logic 1, it indicates that the FIFO has enough room to absorb a pre-determined number of data transfers. Once the FIFO threshold has been exceeded, meaning that the FIFO can no longer absorb the pre-determined number of data transfers, then DTPA will transition to logic 0.

The following diagrams show the behavior of DTPA when the FIFO threshold is reached. It is critical that the upstream device respond properly in order to avoid any FIFO overflows in the TXSDQ.

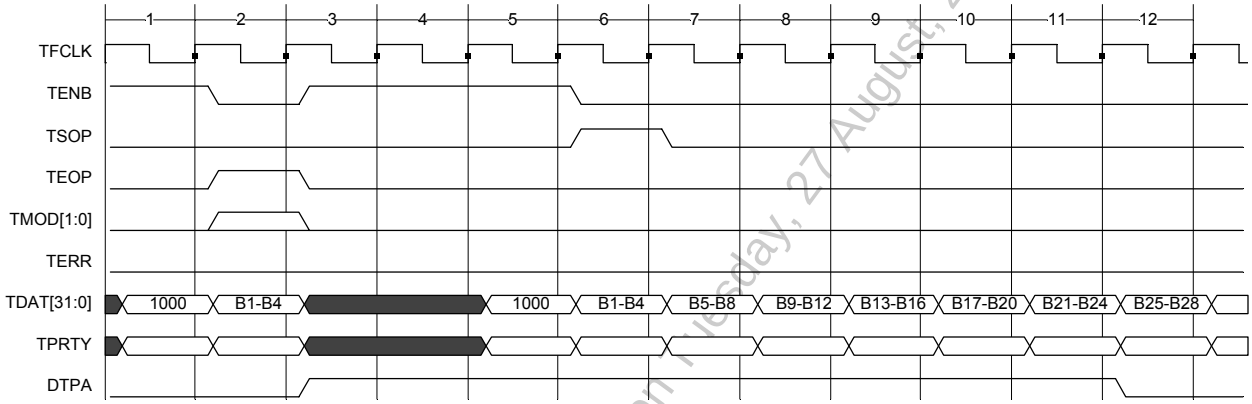
There are two basic methods of transferring data across the PL3 interface: burst-transfer mode, and word-transfer mode. Burst-transfer mode is similar to the UL3 interface. Where the UL3 interface will transfer one cell at a time, the PL3 interface will transfer a maximum number of bytes or end at an end-of-packet indication in one burst, whichever comes first. Setting TPAHOLD (register 788H TXPHY Configuration) to logic 1 will configure the S/UNI-2488 to burst-transfer mode.

Word-transfer mode has no such limitations. The upstream device is expected to watch the DTPA signal to find when it can begin a transfer. Once the transfer is started, it must observe the DTPA signal and pause when required to prevent overflowing the FIFO. Setting TPAHOLD to logic 0 will configure the S/UNI-2488 to word-transfer mode or hybrid word/burst-transfer mode.

13.12.1 TPAHOLD = 0

Figure 29 shows the behavior of DTPA when the TPAHOLD register bit (in register 788H TXPHY Configuration) is set to logic 0. This is the default operating mode. In this example, the write to the FIFO which occurs at the start of cycle 7 crosses the TXSDQ's BT[4:0] threshold. DTPA responds on cycle 12. There is a 5 clock cycle delay between the write and the response on DTPA.

Figure 29 TPAHOLD Set To 0



This 5 cycle delay can be dealt with in 2 ways. First, the upstream device can be programmed to wait for the response before sampling the new DTPA status. For small transfers, this may affect the net throughput possible on the PL3 bus. For this case, the TXSDQ buffer threshold can be set equal or greater than the PL3 burst-size of the upstream device.

BT[4:0] ≥ burst-size – 1

Where burst-size is in units of blocks (1 block = 16 bytes).

Second, if the upstream device cannot account for the DTPA delay or maximum throughput is desired on the PL3 bus, the TXSDQ's buffer threshold must be set to guarantee that any transfers which occur during the 5 cycle delay do not cause any overflows. To do this, the value of the TXSDQ's buffer threshold may need to be increased. It can be calculated by using the following equation:

$$BT[4:0] \geq 1 + (num\_min\_pack * min\_pack\_size\_in\_blocks) + remainder - 1$$

Where:

Let m = minimum packet size
Let s = upstream device's response time to DTPA (# of clocks after DTPA for transfer to stop)

Let ovrhd_cycles = number of non-packet payload cycles per transfer
(each guaranteed null cycle introduced by the
upstream device counts as 1)

num_min_pack = downround ((5 + s - 1) / (m + ovrhd_cycles))

min_pack_size_in_blocks = upround (m / 4)

remainder = upround (((5 + s - 1) mod m) / 4)

Explanation:

The DTPA is late by five clocks and the link layer device takes s number of clocks after DTPA to stop transfer, resulting in 5 + s words that can be written after the threshold gets exceeded.

- the '1' is to deal with the worst case where the threshold gets exceeded during the write of the final word of a packet whose size is one block greater than a multiple of 4 (eg. the EOP word of a 13 word packet, as this word wastes a whole block by itself).
- num_min_pack is the number of full minimum-sized packets that can be written during the 5 + s - 1 clocks. (The subtraction of 1 refers to the EOP word corresponding to point i)

  eg. if s = 2, m = 5, ovrhd_cycles = 0,

  num_min_pack = downround((5+2-1) / (5+0)) = 1.

  That is, in those 6 clocks, there could be one full min-size packet that can be written
- min_pack_size_in_blocks is the number of blocks occupied by a minimum-sized packet. eg. if m = 5 clocks cycles, then min_pack_size_in_blocks is 2.
- remainder refers to how many blocks of a partial packet gets written after the minimum-sized packets had been written. (5 + s – 1)mod m is a calculation of how many words are contained in the final partial packet. The number of blocks occupied is simply that value divided by 4 rounded up.
- the '-1' at the end of the equation refers to the fact that BT in the TXSDQ is one less than what's required.

Examples:

- s = 2 (7 clock latency for response to DTPA)

  m = 1 (min 4-byte packet)
  ovrhd_cycles = 0 (4 byte packet, no null cycles guaranteed between each

  packet/burst)

  num_min_pack = downround ((5+2-1)/(1+0)) = 6

  min_pack_size_in_blocks = upround(1/4) = 1

  remainder = upround (((5+2-1)mod1)/4) = 0

  BT[4:0] ≥ 1 + (6*1) + 0 – 1 = 6

- s = 2 (7 clock latency for response to DTPA)

  m = 1 (min 4-byte packet)

  ovrhd_cycles = 1 (4 byte packet, 1 null cycle guaranteed between each packet/burst)

  num_min_pack = downround ((5+2-1)/(1+1)) = 3

  min_pack_size_in_blocks = upround(1/4) = 1

  remainder = upround (((5+2-1)mod1)/4) = 0

  BT[4:0] ≥ 1 + (3*1) + 0 – 1 = 3

- s= 2 (7 clock latency for response to DTPA)

  m = 13 (atm cell)

  ovrhd_cycles = 0 (no null cycles)

  num_min_pack = downround ((5+2-1)/(13+0)) = 0

  min_pack_size_in_blocks = upround(13/4) = 4

  remainder = upround (((5+2-1)mod13)/4) = 2

  BT[4:0] ≥ 1 + (0*4) + 2 – 1 = 2

  For the optional PL3 mode where each burst is not terminated by a TENB transition to logic 1, TPAHOLD must be set to logic 0.

13.12.2 TPAHOLD = 1

Figure 30 shows the behavior of DTPA when the TPAHOLD register bit (in register 788H TXPHY Configuration) is set to logic 1. This is the optional operating mode which decreases the DTPA response delay from 5 cycles to 1 cycle. This optional mode is only usable when each burst is terminated by a TENB transition to logic 1. Once a burst has been allowed by polling DTPA at logic 1, then one full burst is allowed. DTPA must be polled at logic 1 again before another burst can be started.

In this example, the write to the FIFO which occurs at the start of cycle 7 crosses the TXSDQ's BT[4:0] threshold. DTPA responds on cycle 8. There is a 1 clock cycle delay between the write and the response on DTPA.

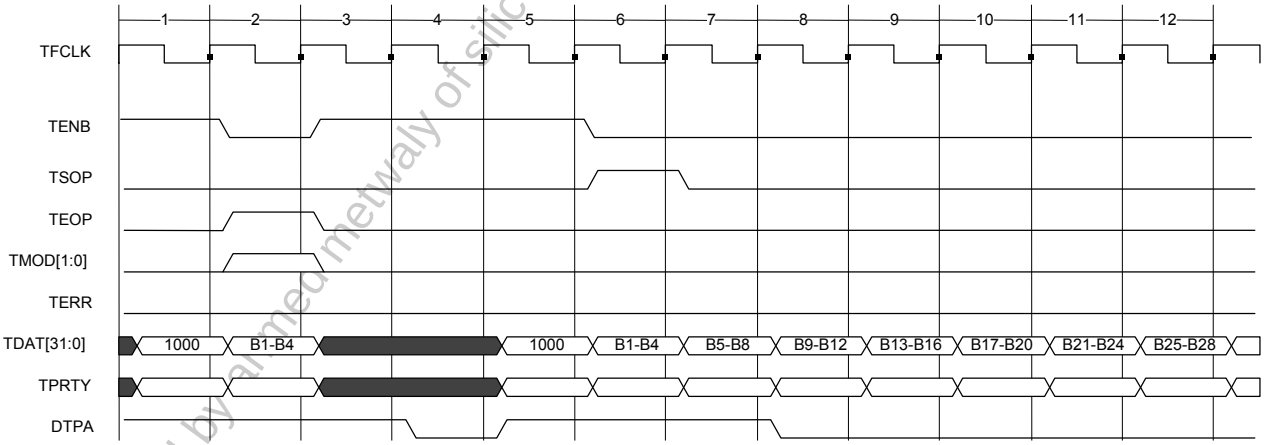
The TXSDQs FIFO threshold must be set-up differently. For this mode to operate correctly:

- BT[4:0] = 2*burst-size – 1
  Where burst-size is in units of blocks (1 block = 16 bytes).

While the TXSDQ's FIFO threshold is set so it transitions when less than 2 bursts remain available, the TPAHOLD feature will hold DTPA high until there is less than 1 burst available. Thus, the user can still fully utilize the entire FIFO.

Because we usually want the TXSDQ's data threshold (DT[7:0]) to be a fairly large value to prevent FIFO underruns, the burst-size must be set to a reasonable value (see Section 13.7 for restrictions on the relationship between TXSDQ's DT[7:0] and BT[4:0]).

Figure 30 TPAHOLD Set To 1



13.13 System Interface Error Recovery

13.13.1 Utopia Level 3 Transmit Interface Misalignment Recovery

On the Transmit UL3 interface, cell alignment is done on logic 1-to-0 transition of TENB. That is, TSOC is expected on the same cycle where TENB has just transitioned to logic 0. Thus, if the upstream device has misalignment between its TENB and TSOC, the S/UNI-2488 will align its cells to the TENB and may give error indications on its RUNTCELLI (TXPHY Interrupt Status register, 789H) and/or SOPI interrupt (TXSDQ SOP Error Port and Interrupt Indication, 775H). Once the upstream device has realigned its signals, the S/UNI-2488 will realign on the next 1-to-0 transition of TENB.

13.13.2 Utopia Level 3 Receive Interface Misalignment Recovery

On the Receive UL3 interface, cell transfer is aligned to the RENB signal. Once asserted to logic 0, RENB must not deassert until cycle P11 of a cell. The S/UNI-2488 will not respond to early deassertions of RENB and will continue transfer of the cell in progress.

To realign the S/UNI-2488 to the downstream device, the RENB must remain deasserted for more than 13 clock cycles. This will guarantee that the S/UNI-2488 has completed transfer of any cell and the next cell will be aligned to RENB.

This means that RENB cannot be tied low with the downstream device expecting to align using the RSOC output of the S/UNI-2488.

The alternate method to realign cells is to unprovision the RCFP and then unprovision and flush the RXSDQ. When the RXSDQ and RCFP are restarted, the cells will be properly aligned to RENB.

13.13.3 Utopia Level 3 Transmit Clock (TFCLK) Error Recovery

When the TFCLK is taken away and restored or is corrupted by a glitch in UL3 mode, the TxDLL will indicate an error by asserting the ERRORI register bit in the TxDLL Control Status register. The SUNI 2488 may also generate continuous SOPI interrupts in the TXSDQ block or RUNTCELLI interrupts in the TXPHY block which indicate a misalignment state.

When this condition is detected, the following recovery procedure should be used:

1. Detect TxDLL ERRORI interrupt
2. Reset the TxDLL by writing to the TxDLL Delay Tap Status register (0886H)
3. Unprovision and flush the TXSDQ to stop the upstream device from transmitting (indirect register 0779H, bit 15 and indirect register 0778H, bit 13)
4. Reset the TXPHY
5. Clear the reset on the TXPHY

6. Clear the flush bit and provision the TXSDQ

13.13.4 Utopia Level 3 Receive Clock (RFCLK) Error Recover

When the RFCLK is taken away and restored or is corrupted by a glitch in UL3 mode, the SUNI-2488's RxDLL will indicate an ERRORI interrupt. The system-side link-layer device may get continuous RSOC errors and the RXPHY block may give continuous RUNTCELLI interrupts.

When this condition is detected, the following recovery procedure should be used:

1. Detect RxDLL ERRORI interrupt
2. Reset the RFCLK_DLL by writing to the RxDLL Delay Tap Status register (0882H)
3. Unprovision the RCFP cell/packet processors (register 0740H bit 0)
4. Unprovision and flush the RXSDQ (indirect register 0769H, bit 15 and indirect register 0768H, bit 13)
5. Reset the RXPHY
6. Clear the reset on the RXPHY
7. Clear the flush bit and provision the RXSDQ
8. Provision the RCFP

13.13.5 POS-PHY Level 3 Transmit (TFCLK) Error Recovery

When the TFCLK is taken away and restored or corrupted by a glitch in PL3 mode, the TxDLL will indicate an ERRORI interrupt. In some cases the SUNI-2488 TXSDQ also asserts SOPI, and EOPI interrupts.

When this condition is detected, the following recovery procedure should be used:

1. Detect ERRORI interrupt in TXDLL Control Status Register (register 0887H)
2. Reset the TxDLL (write to register 0886H)
3. Disable the TXSDQ FIFO (indirect register 0779H, bit 15)
4. Flush the TXSDQ FIFO (indirect register 0778H, bit 13)
5. Reset the TXPHY
6. Clear the reset on the TXPHY
7. Enable the TXSDQ (indirect register 0779H, bit 15)

13.13.6 POS-PHY Level 3 Receive (RFCLK) Error Recovery

When the RFCLK is taken away and restored or corrupted by a glitch in PL3 mode, the system side link-layer device may get continuous RSOP errors. The SUNI's RxDLL indicates a ERRORI interrupt.

When this condition is detected, the following recovery procedure should be used:

1. Detect RxDLL ERRORI bit asserted [register 0883H, bit 5].
   Note: upstream device may get continuous RSOP errors.
2. Reset the RxDLL [write to register 0882H]
3. Unprovision the upstream cell/packet processor (RCFP) [register 0740H, bit 0]
4. Disable the RXSDQ FIFO [indirect register 0769H, bit 15]
5. Flush the RXSDQ FIFO [indirect register 0768H, bit 13]
6. Reset the RXPHY
7. Clear the reset on the RXPHY
8. Clear the flush bit and enable the RXSDQ FIFO [indirect register 0769H, bit 15]
9. Provision the RCFP [register 0740H bit 0]

13.14 Using the SONET/SDH Inband Error Report Processor (SIRP)

The remote alarm port RDI and REI values are sourced from an upstream module in the S/UNI-2488. The SIRP allows these alarm indications to be transmitted back to the remote end.

Register Controlled Mode (TS1_RMODE[1:0] =b'00)

In this mode, REI[3:0] and RDI[1:0] are both sourced from internal registers TS1_REI[3:0] and TS1_RDI[1:0] respectively. The remote alarm port is ignored as well as the RCFP's loss-of-cell-delineation LCD alarms (which is mapped to a programmable RDI code).

Remote Alarm Input Only Mode (TS1_RMODE[1:0] =b'01)

In this mode, the REI and RDI values transmitted are sourced entirely from the remote alarm port.

Remote Alarm Input With Loss Of ATM Cell Delineation Input Mode (TS1_RMODE[1:0] =b'10)

In this mode, the REI values are sourced from the remote alarm port and the RDI indication is generated by the receive cell processor's loss-of-cell delineation assertion state (which is mapped to a programmable RDI code).

Normal Error Reporting Mode (TS1_RMODE[1:0] =b'11)

In this mode, the REI and RDI values are sourced from the remote alarm port. If the extended RDI mode is enabled, the receive cell processor's loss-of-cell delineation state, which is mapped to a programmable RDI code if asserted, is compared with the remote port's RDI code. The higher priority RDI will take precedence.

13.15 Using the PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. It cannot be inserted into the ATM cell or packet payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope.

13.15.1 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

In master/slave configuration of the monitor (STS-48c/VC-4-16c concatenated payloads) more bytes are needed to recover the LFSR state, because the slaves needs a few bytes to be synchronized with the J1 byte indicator.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

An Out of Synchronization and Synchronized State is defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 bytes with errors. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization.

It is important to note that the monitor can falsely synchronize to an all zero pattern or, if the incoming pattern is inverted, an all ones pattern. It is recommended that users poll the PRGM Monitor's LFSR value after synchronization has been declared to confirm that the value is neither all 1's or all 0's.

Upon detecting 3 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erroneous PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

13.15.2 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of erroneous bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh, ie it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. An indirect read to that register will initiate a transfer of the error counter into the registers for reading. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. All 48 STS-1 error counts belonging to the concatenated stream must be read. The error counts in each associated register must be summed by software.

Bit errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming high the RESYNC register bit, or once it detects 3 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated. However, it should be noted that when the PRGM goes out of synchronization, 1 or 2 extra errors may be counted. In other words, the 3 errors which cause the PRGM to lose synch may in fact be counted as 3, 4, or 5 errors.

13.16 Using the SONET/SDH Bit Error Rate Alarm Monitor (SBER)

Refer to PMC's application note PMC-1950820 "SONET/SDH Bit error Threshold Monitoring" for further details on SONET/SDH bit-error threshold requirements. Table 26 and Table 27 show the set-up configuration to meet the SONET and SDH bit-error rate monitor thresholds.

Table 26 BERM Configuration for SDH STM-16c

BER	Evaluation Period	CMODE	Accumulation Period	Detection Threshold	Clear Threshold
1.0e-3	0.01	0	00000A	2AF8	A28
1.0e-4	0.1	0	000064	2AF8	A28
1.0e-5	1	0	0003E8	2AF8	A28
1.0e-6	10	0	002710	2AF8	A28
1.0e-7	100	0	0186A0	2AF8	A28
1.0e-8	1000	0	0F4240	2AF8	A28

1.0e-9	10000	0	989680	2AF8	A28

Table 27 BERM Configuration for SONET STS-48c

BER	Evaluation Period	CMODE	Accumulation Period	Detection Threshold	Clear Threshold
1.0e-3	0.0025	0	000003	B97	25F
1.0e-4	0.008	0	000008	6BB	0D8
1.0e-5	0.008	0	000008	0A2	01B
1.0e-6	0.0625	1	00003F	07C	08E
1.0e-7	0.625	1	000271	07C	08E
1.0e-8	5.2	1	001450	065	078
1.0e-9	42	1	00A410	04F	062

13.17 Using the SONET/SDH Alarm Reporting Controller (SARC)

The SARC block is used to process STS-48c alarms. All its features, save for one, are dedicated solely for STS-48c payloads. The one feature where sub-STS-48c channels need to be configured for the SARC is for AIS-P generation to the APS links when working in x-connect mode. This is described in Section 13.17.3.

13.17.1 SARC Indirect Register Access

The procedure used to access the SARC's indirect registers is different from that used in the other functional blocks of the S/UNI-2488 (as defined in Section 13.19). For STS-48c modes, the user must write the value 0x0001 to register 0x0720 first. Then, all the other registers (0x0722 to 0x0735) can be written and read as normal registers. For the one configuration where non-STS-48c channel access is required, the user must write the value of the master timeslot of the STS-Nc channel to register 0x0720, then program the configurations for that channel to the other registers (0x0722 to 0x0735). After this is done, then the next STS-Nc channel master timeslot can be configured. Examples of the configuration are given in the following sections.

13.17.2 STS-48c Operation

In STS-48c mode, one SARC is sufficient to process all the defect consequential actions. To enable the defect consequential actions, the PATH_REG_EN[0] register bit in register 0x0720 must be set to logic 1. Then, the bits in registers 0x0722 to 0x0731 and 0x0734 must be configured to enable the desired consequential actions.

Note that conditions to enable AIS-L will make a difference in internal functions only. The RLAISINSEN bit in register 0x072A should be enabled to allow AIS-L to propagate to AIS-P. This will allow transmission of an AIS-P signal to the transmit APS links (in x-connect mode) and to the RCFP cell/packet processor.

13.17.3 Sub-STS-48c Operation

Sub-STS-48c functions in the SARC are required for just one function: AIS-P generation to the APS links when operating in x-connect mode. There is only one SARC in the S/UNI-2488 and it resides on the first STS-12 timeslots. In this position, it can only process the alarms for an STS-48c, the first STS-12c, any channels residing in the first 4 STS-3c timeslots, or any channels residing in the first 12 STS-1 timeslots. It does not do any alarm processing for the remaining 36 timeslots.

When working in the x-connect mode, the channels contained in the STS-48 may consist of anything from STS-1s to an STS-48c. For each of these channels residing in the first 12 timeslots, the SARC must be configured properly in order for the S/UNI-2488 to generate proper AIS-P at the SVCA's output which is connected to the transmit APS port in x-connect mode. For the remaining 36 timeslots which are not serviced by a SARC, AIS-P generation is accounted for by the RPAISINS_EN bit in register 0x0902.

The following example shows how proper AIS-P generation is configured for the following channel set-up:

STS-3c channels in timeslots #1,3, and 4. STS-1 channels in timeslots 2, 6, and 10. Various channels in timeslots 13 to 48.

- Set up STS-3c channel in timeslot #1:

  1. Write 0x0001 to register 0x0720

  2. Write the value 0x040F to register 0x0724 to enable line AIS assertion for all the possible defect conditions. Only these defects, which will cause the RHPP to declare AIS-P, can be enabled.

  3. Set the PAISPTREN, PLOPTREN, and RLAISINSEN register bits in register 0x0072A to enable AIS-P generation upon detection of a path AIS pointer defect, a Loss of Pointer defect, or a receive line AIS (generated by the conditions specified in point#2 above).

Repeat steps 1 to 3 by writing the values 0x0003 and 0x0004 into register 0x0720 in step 1 to configure STS-3c channels residing in master timeslots 3 and 4 respectively. Note that only the master timeslot of each STS-Nc channel should be configured.

- Set up STS-1 channel in timeslot #2:

  Write 0x0002 to register 0x0720

  Write the value 0x040F to register 0x0724 to enable line AIS assertion for all the major defect conditions. Only these defects, which will cause the RHPP to declare AIS-P, can be enabled.

  Set the PAISPTREN, PLOPTREN, and RLAISINSEN register bits in register 0x0072A to enable AIS-P generation upon detection of a path AIS pointer defect, a Loss of Pointer defect, or a receive line AIS defect (generated by the conditions specified in point#5 above).

Repeat steps 4 to 6 by writing the values 0x0006 and 0x000A into register 0x0720 to configure the remaining STS-1 channels residing in timeslots 6 and 10 respectively.

Set RPAISINS_EN register bit to 1 in register 0x0902.

Note that an STS-12c channel residing in the first STS-12 position can also be configured using the exact steps 1 to 3.

Note that the other features of the SARC such as Section TLRDIINS Enable, Path Configuration, Path RALM Enable, LOP Pointer Status, LOP Pointer Interrupt Enable, LOP Pointer Interrupt Status, AIS Pointer Status, AIS Pointer Interrupt Enable, and AIS Pointer Interrupt Status should not be used for non-STS-48c modes.

Also note that PAIS will not be generated as a consequential action to Loss of Pointer LOP, Loss of Concatenated Pointer LOPC, or Concatenated AIS detection PAISC.

13.18 Interrupt Service Routine

The S/UNI-2488 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the S/UNI-2488 Master Interrupt Status #1-#7 registers (0004H – 000AH). The bits point to the functional block(s) which caused the hardware interrupt. For instance, if the RXSDQ block caused the interrupt, the RXSDQI bit will be logic 1 in register 0008H. These bits get cleared when the interrupt is cleared.

2. Find the register address of the corresponding block which caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from steps 1 and 2 are cleared once these register has been read and the interrupt(s) identified.

3. Service the interrupt(s).

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.19 Accessing Indirect Registers

Indirect registers are used to conserve address space in the S/UNI-2488. Indirect registers are accessed by writing the indirect address register. The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data register(s).

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data register(s) to find the state of the register bits for the selected channel number.

Note that the TXSDQ and RXSDQ are handled a little bit differently than most TSB's with indirect registers. It has several Indirect Data Registers – though only one Indirect Address register that controls them all. See the TXSDQ and RXSDQ register description for more information.

The SARC's indirect registers are also programmed in a slightly different manner. See Section 13.17.1.

A particular idiosyncracy should be noted for the SVCA's indirect registers. When configured for concatenated payloads, the value written to SVCA indirect register 2 (diagnostics reg) of a master timeslot gets propagated to (overwrites) the indirect register 2 values of all slave timeslots associated to the master timeslot (within the SVCA where the indirect write was performed). Similarly, when the payload is changed to a higher concat level (eg 12xSTS-1 to STS-12c), the value previously present in the master timeslot is propagated to (overwrites) the values in the slave timeslots without any indirect write actions being performed.

When the payload is changed back to a lower concatenation level, the new SVCA indirect register 2 values remain and the old ones are lost.

The same behaviour is observed when writing to indirect register 2 of timeslot 1 (the de-facto master) of an SVCA configured as a STS-12 slave of an STS-48c payload.

13.20 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. The TCFP, RCFP, R8TD, RXSDQ, TXSDQ, RHPP, RRMP, and PRGM all contain performance monitor registers. The counters have been sized to not saturate if polled every second.

Each block's counters can be accumulated independently if one of the registers which contain the latched counter values is written to. A device update of all the counters can be done by writing to the S/UNI-2488 Global Performance Monitor Update register (register 0000H). After this register is written to, the TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

13.21 Loopback Operation

There are 3 loopback modes available in the S/UNI-2488. They are shown in Figure 5.

Parallel diagnostic Loopback enables a digital loopback from the transmit line to the receive line before the 2.488Gbps analog circuitry. It is enabled by setting the PDLE bit in register 0x0001.

Serial Diagnostic Loopback enables a loopback from the transmit 2.488Gbps serial line to the receive 2.488Gbps serial line. It is enabled by setting the SDLE bit in register 0x0012.

Line Loopback enables a loopback from the receive 2.488Gbps serial line to the transmit 2.488Gbps serial line. It is enabled by setting LINE_LOOP_BACK bit in register 0x0013 and the SLLE register bit in register 0x0020 to logic 1. The CSU_MODE[7] bit in register 0x0021 must be set to logic 0.

13.22 Required Reset Sequence

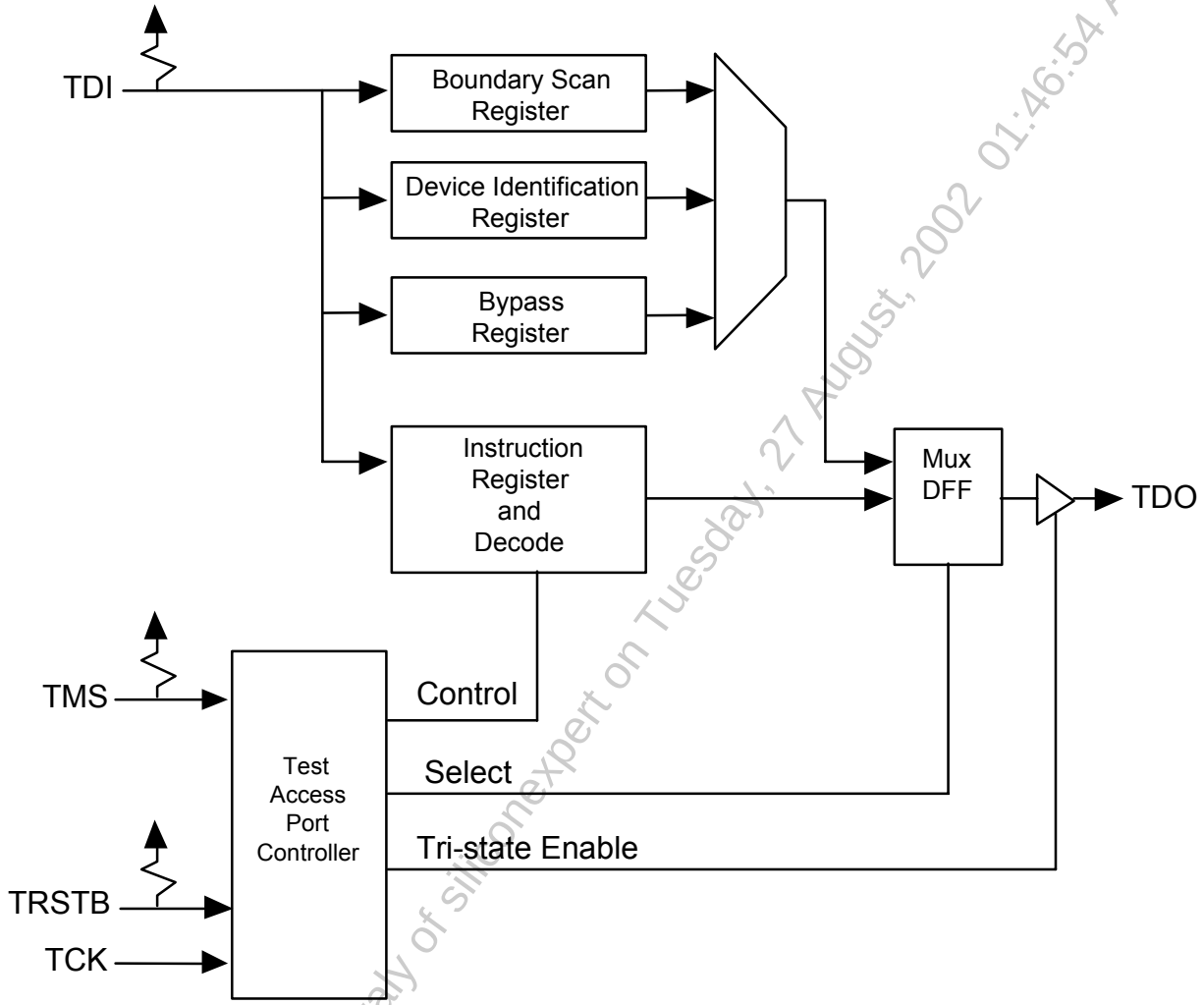
After digital reset, and before starting any software routines to capture performance monitor count values, a write to register 0x0000 should be executed to initiate a global performance monitor count update. Then, the TIP bit in register 0x0000 should be monitored after 32 REFCLK clock periods (approx 102.8ns). If it is logic 1, a software reset (done by setting and then clearing DRESET in register 0x0001) should be done to clear a TIP lock-up condition. Repeat this sequence until TIP is read to be logic 0.

If this reset routine is not followed, there is a minute chance that the RHPP's, the TXSDQ's, or the RXSDQ's performance monitor counters, and the TIP register bit will start up in a lock-up condition and not operate properly.

13.23 JTAG Support

The S/UNI-2488 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TRSTB should be tied to RSTB if the JTAG interface is not used. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 31 Boundary Scan Architecture



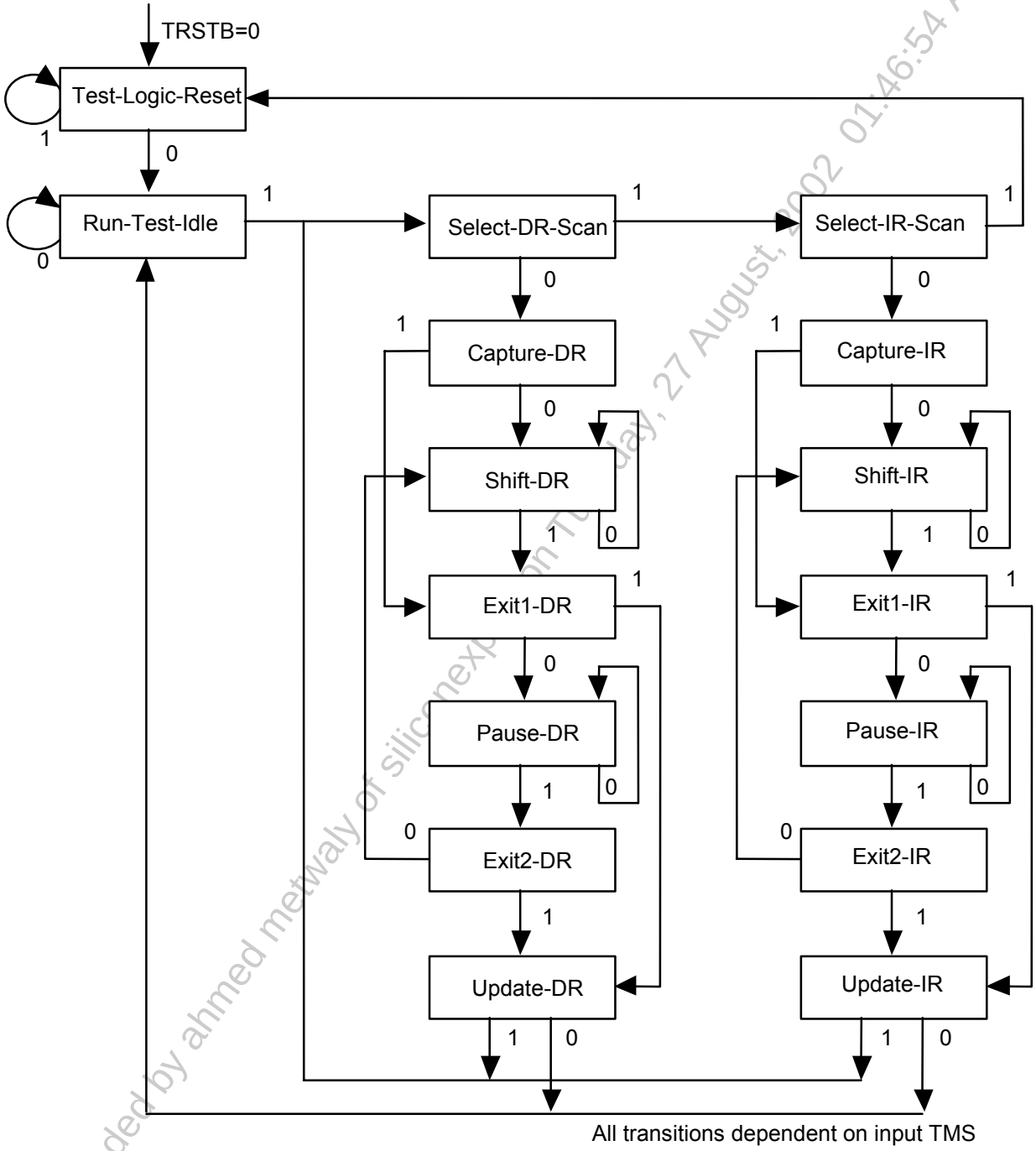
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.23.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 32 TAP Controller Finite State Machine



13.23.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.23.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

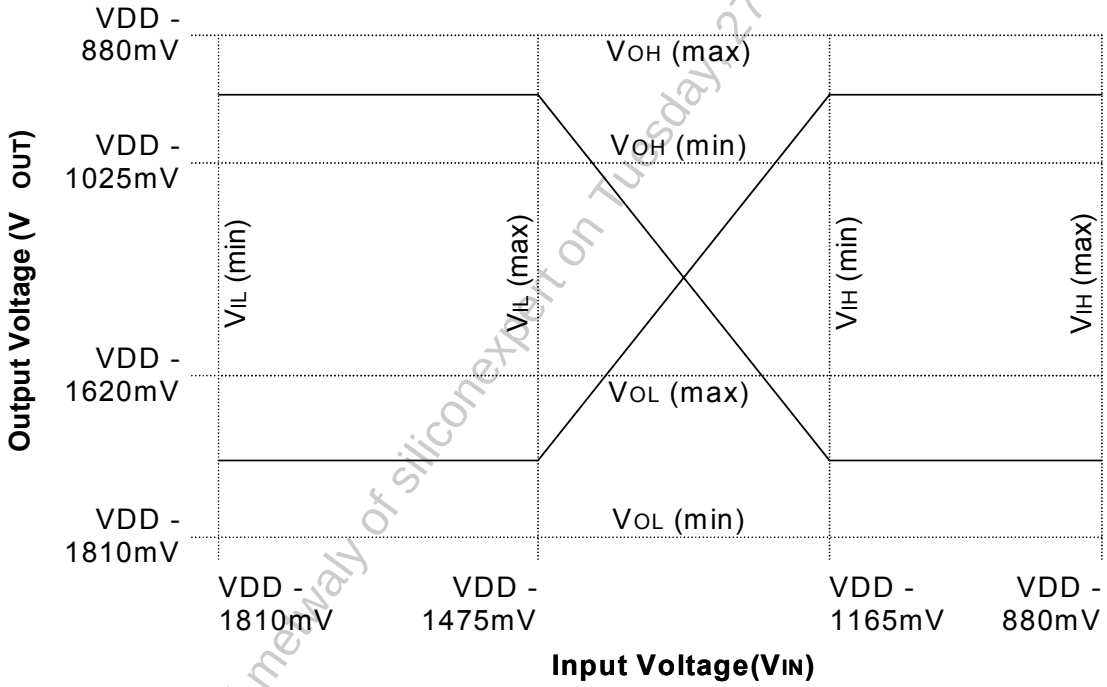
The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.24 Interfacing to ECL or PECL Devices

13.25 Output Levels

The S/UNI-2488 is targeting for CML compatible input and output level characteristics. The S/UNI-2488 generates outputs which are approximately 2/3 100k ECL/PECL swing levels, but are compatible with the requirements of most Optical Modules as shown in Table 28. Figure 33 shows DC ECL/PECL output levels and their limits. We see that output levels are referenced to a positive power supply, VDD (VDD=0V for ECL and is typically 2.5V, 3.3V or 5V for PECL). Therefore, regardless of the value of VDD, the typical value of VOH is required to be 952.5 mV below VDD and the typical value of VOL is required to be an additional 762.5 mV below that.

Figure 33 PECL Levels (100K Characteristics)



There are no hard specifications for CML, but the signal swing is typically about half that of the ECL/PECL levels (≈800mVppd[2] - the signal swing and common mode depend on the resistor size, amount of current and the positive voltage supply). The lower pulse amplitudes lead to lower crosstalk, EMI and noise transients. Thus each device that claims CML compatibly must be looked at carefully to insure interoperability with other devices.

[2] Vppd: Peak-to-peak differential voltage (typically equals 2 x single-ended peak-to-peak).

Table 28 compares the S/UNI-2488 Rx and Tx signal levels to a few ODLs (note ODL Rx's connect to S/UNI-2488 Rx's and ODL Tx's connect to S/UNI-2488 Tx's).

Table 28 S/UNI-2488 and ODL PECL Amplitude Specifications

Device	Min	Typ.	Max
Standard ECL/PECL levels	1190mVppd	1525mVppd	1806mVppd
Typical CML levels		800mVppd	
S/UNI-2488 Tx (standard output amplitude) [1]	900mVppd	1000mVppd	1100mVppd
S/UNI-2488 Tx (low output amplitude) [2]	465mVppd	533mVppd	600mVppd
S/UNI-2488 Rx	400mVppd[3]		2Vppd
Lucent Tx (1417K4A)	300mVppd	-	1.6Vppd
Lucent Rx (1417K4A)	600mVppd	-	1Vppd
Sumitomo Tx SDM-7128-XC	900mVppd	-	2.4Vppd
Sumitomo Rx SDM-7128-XC	400mVppd	-	2.3Vppd
Sumitomo Tx SCM-6028-GL	0.8Vppd	-	2Vppd
Sumitomo Rx SCM-6028-GL	400mVppd	-	2.3Vppd
HP HFCT-Tx HFCT-5404D	400mVppd	-	1.8Vppd
HP HFCT-Rx HFCT-5404D	600mVppd	-	No Spec
Hitachi Tx HTR6540	300mVppd		1.2Vppd
Hitachi Rx HTR6540	640mVppd	800mVppd	1Vppd

Notes:
[1] Register 0020H, Bit 6 = '0' (default)
[2] Register 0020H, Bit 6 = '1'
[3] The S/UNI-2488 Rx does work below this value (measured to work down to 100mVppd), but the jitter goes up, which will degrade the jitter tolerance of the device. Thus going below this limit is not recommended

As can be seen, the S/UNI-2488 Tx must be correctly programmed (in general the reduced Tx output amplitude should be used) to be able to inter-operate with the ODLs. Some ODLs claim to be able to tolerate Tx PECL levels, but this will limit their Rx optical range, thus for best operation care must be taken to insure the correct levels are sent to the ODL.

13.26 Termination Scheme

The S/UNI-2488 is to be AC coupled and double terminated, see Figure 34 to Figure 36 below for several connects. Note that while the S/UNI-2488 could be DC coupled to a 3.3V CML ODL on the Tx side, **it has not been tested, thus is NOT recommended.** Another note is that the external termination in practice might be integrated in ODL transceiver.

Figure 34 S/UNI-2488 Tx Termination Scheme #1

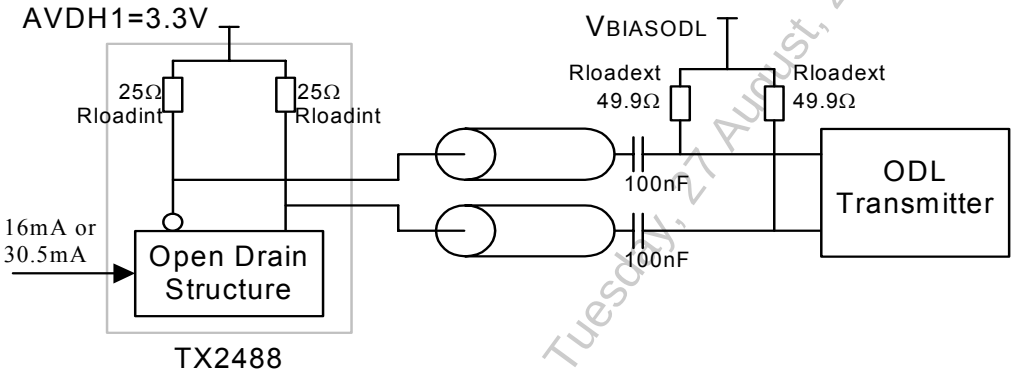


Figure 35 S/UNI-2488 Tx Termination Scheme #2

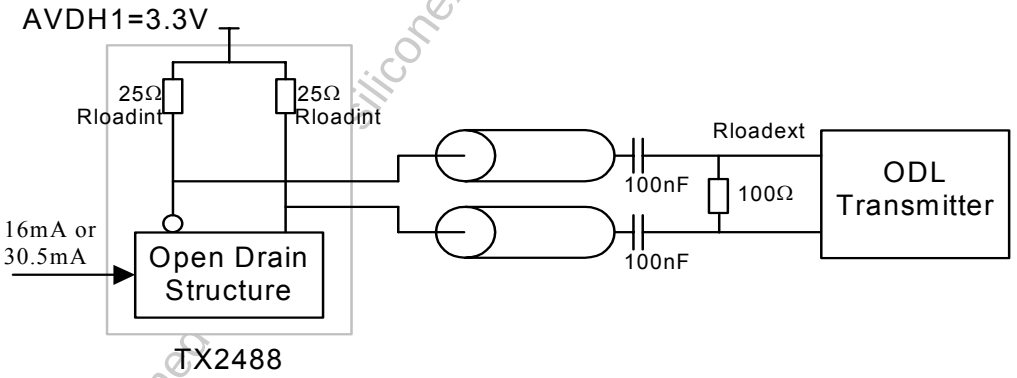
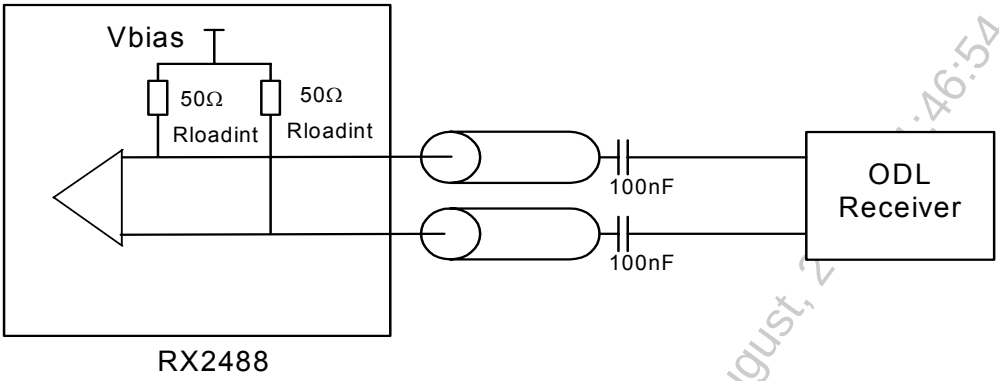


Figure 36 S/UNI-2488 Rx Termination Scheme

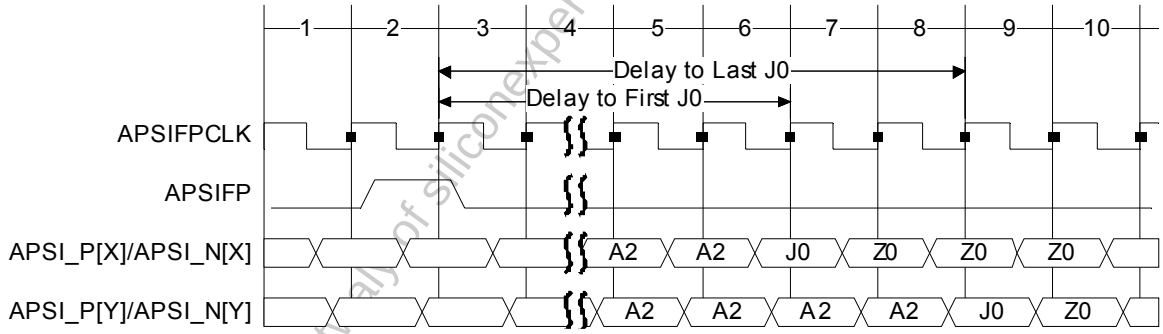


14 Functional Timing

14.1 Incoming APS Serial TelecomBus

Figure 37 shows the relative timing of the incoming APS serial TelecomBus LVDS links. Links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the APS Input Frame Pulse signal (APSIFP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other but are frequency locked. The delay from APSIFP being sampled high to the first and last J0 character is shown in Figure 37. In this example, the first J0 is delivered by one of the four APSI links (APSI+/APSI-). The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, one of the links (APSI+[Y]/APSI-[Y]) is shown to be the slowest. The minimum value for the internal programmable delay (AIJ0DLY[13:0]) is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 31. Consequently, the external system must ensure that the relative delays between all the APSI LVDS links be less than 16 characters (approximately 205ns). The relative phases of the links in Figure 37 are shown for illustrative purposes only.

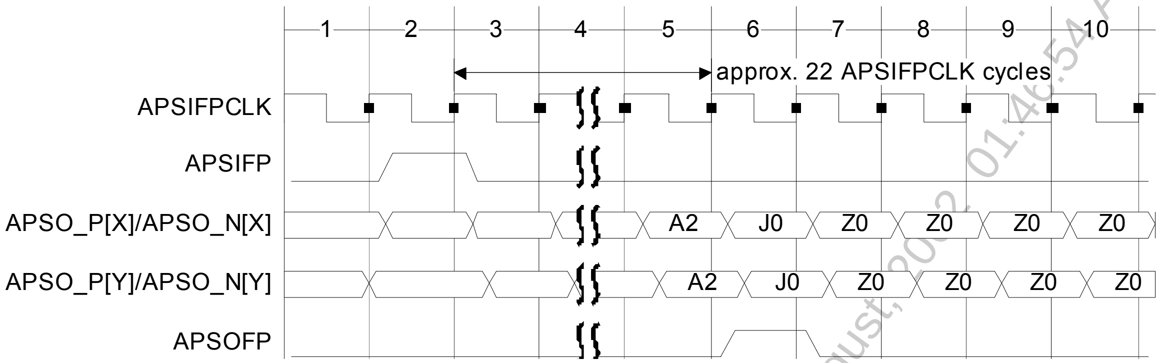
Figure 37 Incoming APS Serial TelecomBus Timing



14.2 Outgoing APS Serial TelecomBus

Figure 38 shows the timing relationships around the APSIFP signal. The Outgoing APS J0 Frame Pulse (APSOFP) signal indicates the approximate time at which the J0 byte is available on the output APS LVDS links. Note the time between APSIFP and APSOFP is approximately 22 APSIFPCLK cycles.

Figure 38 Outgoing APS Serial TelecomBus Timing



14.3 ATM UTOPIA Level 3™ System Interface

The ATM UTOPIA Level 3 System Interface is compatible with the UTOPIA Level 3 specification. The S/UNI-2488 only supports the 32-bit mode of operation.

14.3.1 Transmit UL3 Interface

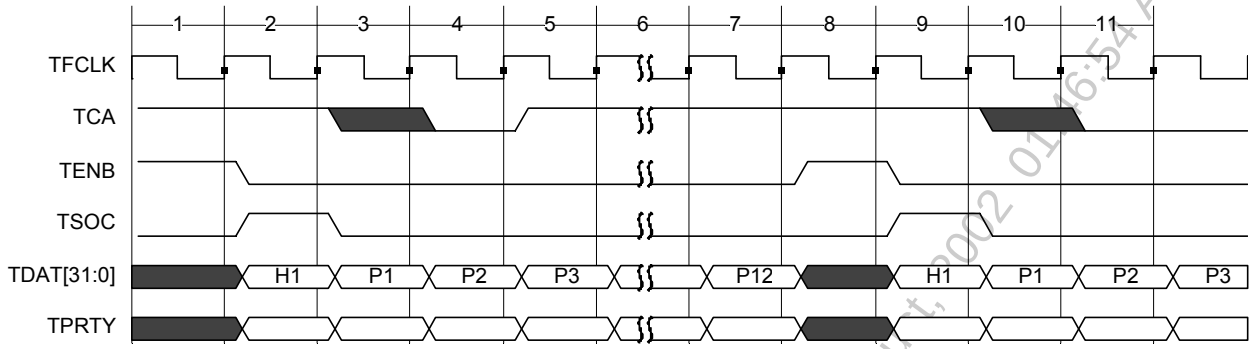
The Transmit UTOPIA Level 3 System Interface Timing diagram (Figure 39) illustrates the operation of the system side transmit UL3 interface. The single PHY case shown in Figure 39 illustrates the behavior of the TCA signal. At the start of cycle 4, there is only enough FIFO buffer space for the cell being transferred so TCA is deasserted. The deassertion occurs on the TFCLK edge **after** TSOC of the cell (cell#1) being written to the FIFO is sampled. This cell will take the last remaining cell buffer space in the FIFO. This TCA behavior is consistent with the Utopia L3 specification which states that TCA is invalid on the TFCLK edge that initiates the transition of TSOC to logic 1.

On cycle 5, a cell has been read out of the FIFO to the S/UNI-2488 core so it now has room to accommodate the cell currently being transferred (cell#1) plus one additional cell (cell#2). At the start of cycle 8, the transfer of cell#1 is completed. TCA remains high because there is still buffer space for one more cell. At the start of cycle 10, transfer of cell#2 starts. TCA is deasserted at cycle 11 because besides the space for holding cell#2, there is no FIFO space for any more cells.

If TENB is held low, back-to-back cell transfers can be performed without a dead cycle.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the H1 byte. If TSOC is asserted at the wrong time (not at proper cell boundaries), a corrupted (but complete) cell will be transmitted from the S/UNI-2488. This corrupted cell will contain the bytes from the runt cell transferred through the UL3 interface plus some random bytes to fill the remainder of the ATM cell.

Figure 39 Transmit UTOPIA Level 3 System Interface Timing for Single PHY



14.3.2 Receive UL3 Interface

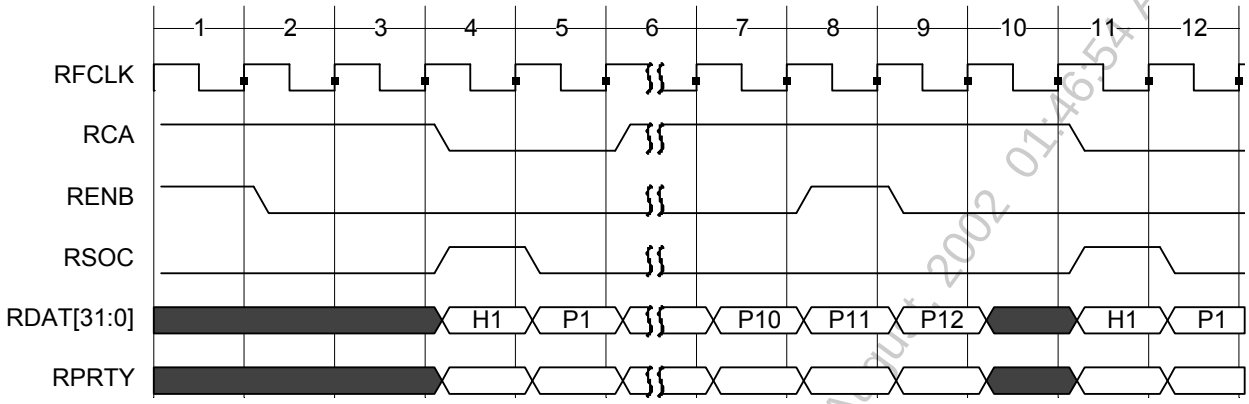
The Receive UTOPIA Level 3 System Interface Timing diagrams (Figure 40) illustrate the operation of the system side receive interface.

The single PHY case shown in Figure 40 illustrates the behavior of the RCA signal. At the start of cycle 3, RENB is sampled low which initiates a cell transfer from the S/UNI-2488. The transfer begins at cycle 4. The response to RENB always occurs on the rising RFCLK edge following the RFCLK edge which samples RENB. Also note that RENB must remain asserted during a cell transfer as specified by the Utopia L3 standard. In Figure 40, this occurs on the rising edge of RFCLK at the start of cycle 9.

RCA is deasserted in cycle 4 and 11 coincident with the RSOC assertion indicating that the cell transfer which has just started contains the last cell in the FIFO at this time. RCA may be asserted at any time due to the insertion of a complete cell into the FIFO.

Back-to-back cells from the same PHY can be handled by holding RENB asserted at logic 0 during cycle 8. In this case, cycle 10 for RSOC, RDAT[31:0], and RPRTY will be eliminated and the following cycles will be advanced.

Figure 40 Receive UTOPIA Level 3 System Interface Timing for Single PHY



14.4 Packet over SONET (POS-PHY) Level 3 System Interface

The Packet over SONET (POS-PHY) Level 3 System Interface is compatible with the OIF-SPI3 specification. The S/UNI-2488 only supports the 32-bit mode of operation.

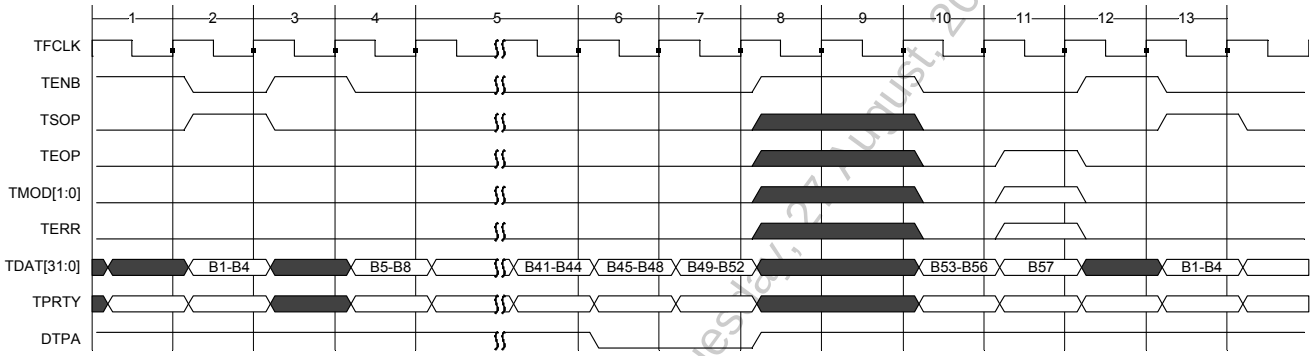
14.4.1 Transmit PL3 Interface

The Transmit POS-PHY Level 3 System Interface Timing diagram (Figure 41) illustrates the operation of the system side transmit FIFO interface. TENB is asserted in cycle 2 to start the transfer. DTPA shows that there is room in the FIFO (the FIFO fill threshold is user programmable) for PHY address 0. The packet data is transferred on TDAT[31:0] starting at the rising TFCLK edge at the start of cycle 3. TSOP is also asserted at this cycle to indicate the data on TDAT[31:24] contains the start-of-packet byte. TENB is deasserted in cycle 3 by the upstream device to pause the transfer. Data transfer continues in cycle 4. In cycle 6, DTPA is deasserted indicating that the FIFO for PHY address 0 has fallen below the data available threshold (TXSDQ's BT[4:0] register bits). In the example shown here, the upstream device responds by stopping its transfer immediately at cycle 8 by deasserting TENB. With many set-up configurations, the upstream device does not need to stop immediately. It can complete the transfer of one more burst before stopping. See Section 13.12 for details on the behaviour of DTPA.

Because DTPA is asserted again on cycle 8, transfers can be conducted again. TENB is asserted again before cycle 11 to continue the transfer. In cycle 11, TEOP is asserted to indicate that TDAT[31:0] contains one byte which is the end of the packet. TMOD[1:0] is valid at the same time to indicate which bytes in TDAT[31:0] contain valid data and thus the last byte of the packet can be inferred. TERR is also valid during this cycle to indicate whether or not this packet should be aborted because of an upstream error. If TERR is logic 1, the packet will be aborted by the S/UNI-2488's packet processor. In cycle 12, TENB is deasserted again.

TSOP must be high during transfers which contain the first byte of a packet. TEOP must be high during transfers which contain the last byte of a packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when TDAT[31:0] contain both the SOP and EOP. When TSOP is asserted and the previous transfer was not marked with TEOP, the system interface realigns itself to the new timing, and both the previous packet and the current packet may be corrupted and aborted.

Figure 41 Transmit POS-PHY Level 3 System Interface Timing



14.4.2 Receive PL3 Interface

The Receive POS-PHY Level 3 System Interface Timing diagram (Figure 42) illustrates the operation of the system side receive interface. The SUNI-2488 performs the polling operation internally and pushes data to the downstream reader when it is available.

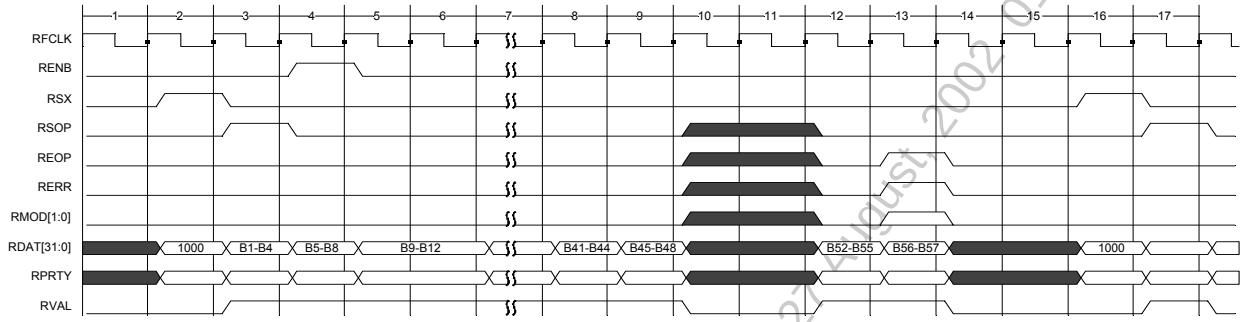
When data is available, the RVAL signal is asserted. RSX is also asserted in cycle 2 to indicate that the PHY address (always equal to 0x00 for the S/UNI-2488) for which data is being transferred is present on RDAT[7:0]. RDAT[31:24] holds the Data Type Field (see register 786H). At cycle 3, RSOP is asserted to indicate that the RDAT[31:24] contains the first byte of a packet. RENB is deasserted in cycle 4 because the downstream device wants to pause the data transfer.

Data transfer continues until cycle 10 when RVAL is deasserted. At cycle 12 and 13, the last two transfers for the packet are performed. In cycle 13, REOP signals the last byte of the packet is contained in RDAT[31:0] and the value of RMOD[1:0] indicates which bytes in RDAT[31:0] contain valid data. RERR is asserted along with REOP if errors were detected in this packet (aborted, length violation, FIFO overrun, FCS errors) so the downstream device may discard the packet. In cycle 16, the setup for a new transfer is initiated by reasserting RSX and the PHY address and data type on RDAT[7:0] and RDAT[31:24] respectively. In cycle 17 the new transfer begins.

The burst length of any transfer can be limited by setting the RXPHY's BURST_SIZE[7:0] register bits.

The FIFO threshold at which data transfer begins is set by the RXSDQ's DT[7:0] register bits. ATM cells can be transferred through the PL3 interface as fixed length packets. The DT[7:0] value should be set so that only complete ATM cells are transferred.

Figure 42 Receive POS-PHY Level 3 System Interface Timing



14.5 Overhead Extraction and Insertion

14.5.1 Transport Overhead Extraction

Figure 43 shows the receive transport overhead (RTOH) functional timings. Transport overhead insertion is available for STS-1 #1 to 12. ROHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are output on RTOH between two ROHFP assertions.

Figure 43 RTOH Output Timing

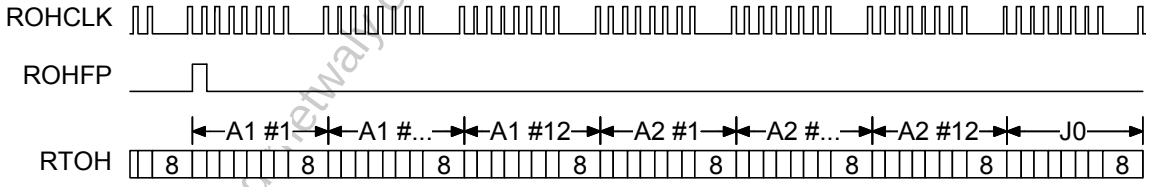
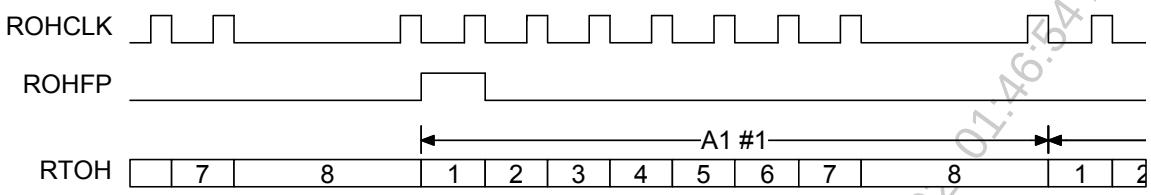


Figure 44 shows that RTOH and ROHFP are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RTOH and ROHFP. Sampling ROHFP high identifies the MSB of the first A1 byte on RTOH.

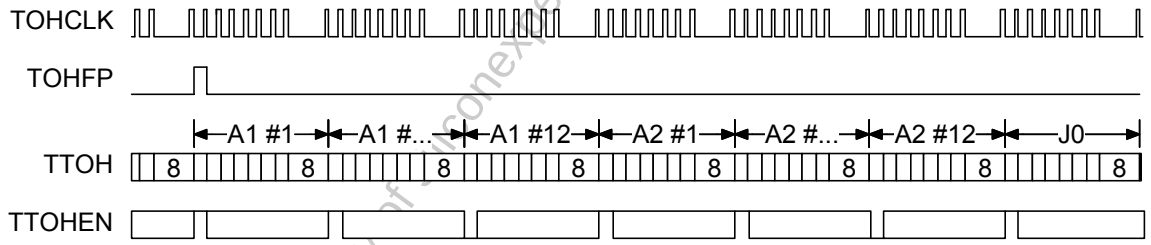
Figure 44 RTOH and ROHFP Output Timing



14.5.2 Transport Overhead Insertion

Figure 45 shows the transmit transport overhead (TTOH) functional timings. TOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are input on TOH between two TOHFP assertions. The 2592 bits is equivalent to the transport overhead of the first STS-12. Transport overhead insertion is available only for STS-1 #1 to 12.

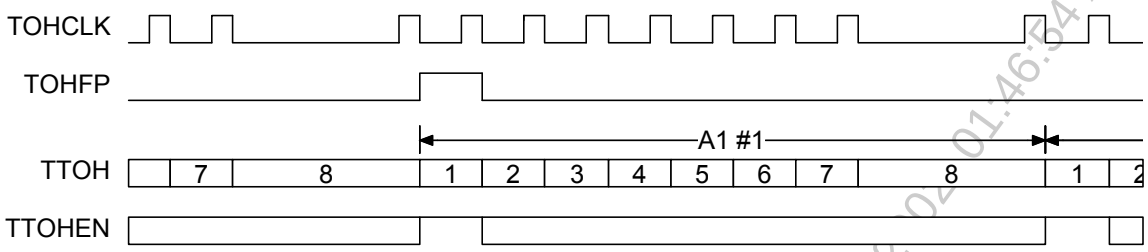
Figure 45 TTOH and TTOHEN Input Timing



TTOHEN is used to validate the insertion of the corresponding byte on TTOH. When TTOHEN is sampled high on the MSB of the byte, the byte will be inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the byte, the byte is not inserted. TTOH and TTOHEN are sampled with the rising edge of TOHCLK. TOHFP is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TOHFP. Sampling TOHFP high identifies the MSB of the first A1 byte on TTOH.

When the Transport Overhead Insertion interface is not being used, the TRMP should be set to use its internal insertion registers (see register description for Register 0081H, 00A1H, 00C1H and 00E1H).

Figure 46 TTOH and TOHFP Input Timing



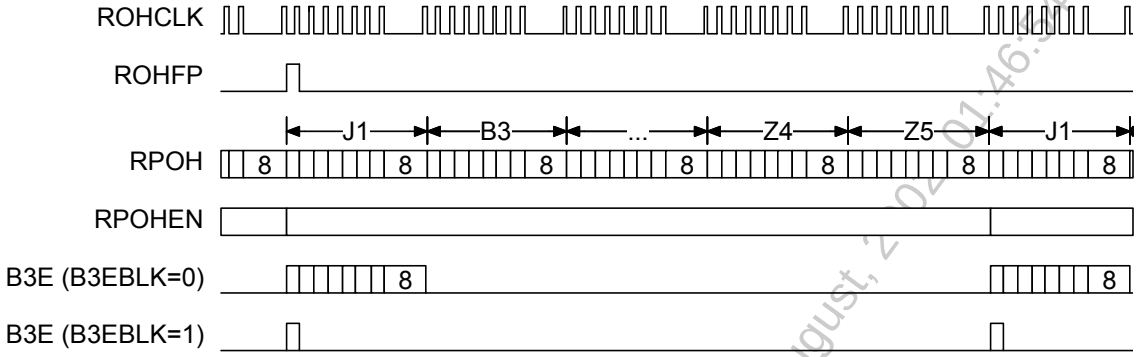
14.5.3 Path Overhead Extraction

Figure 47 shows the receive path overhead (RPOH) functional timings. The RPOH port (RPOH, RPOHEN and B3E) is used to output the POH bytes of the STS (VC) payloads and the path BIP-8 errors. Note that the RPOH is only provided for the first STS-12. In OC-48c mode, all bytes of interest are available. In cross connect mode, path and BIP-8 information from STS-12 #2-4 are unavailable.

The POH bytes are output on RPOH MSB first in the same order that they are received. Since ROHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. RPOHEN is used to indicate new POH bytes on RPOH. RPOHEN is either asserted or de asserted for the nine POH bytes. The path BIP-8 errors are output on B3E at the same time the path trace byte is output on RPOH. Optionally, block BIP-8 errors can be output on B3E.

Figure 47 shows that RPOH and RPOHEN are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RPOH and RPOHEN. Sampling ROHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on RPOH and the first possible path BIP-8 error of STS-1/STM-0 #1 on B3E.

Figure 47 RPOH Output Timing



14.5.4 Path Overhead Insertion

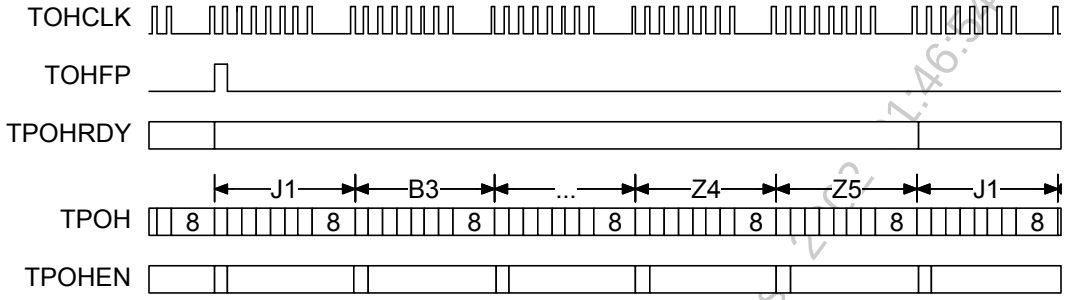
Figure 48 shows the transmit path overhead (TPOH) functional timings. The TPOH port (TPOH, TPOHEN and TPOHRDY) is used to input the POH bytes of the STS (VC) payloads. Note that the TPOH is only provided for the first STS-12. In OC-48c mode, all bytes of interest may be inserted. In cross connect mode, path bytes from STS-12 #2-4 cannot be inserted in this manner.

The POH bytes are input on TPOH - MSB first - in the same order that they are to be transmited. Since TOHFP is synchronized on the transport frame, zero, one or two path overhead can be input per path per frame.

TPOHRDY is asserted to indicate that the S/UNI-2488 is ready to receive POH bytes. TPOHEN is used to validate the insertion of the corresponding byte on TPOH. If TPOHRDY is logic high and TPOHEN is sampled high on the MSB of the byte, the byte will be inserted in the path overhead. When TPOHEN is sampled low on the MSB of the byte, the byte is not inserted in the output stream. If TPOHRDY is logic low and TPOHEN is sample high on the MSB of the byte, the byte will not be inserted in the path overhead and must be represented at the next opportunity.

TPOH and TPOHEN are sampled with the rising edge of TOHCLK. TPOHRDY is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TPOHRDY. Sampling TOHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on TPOH.

Figure 48 TPOH Input Timing

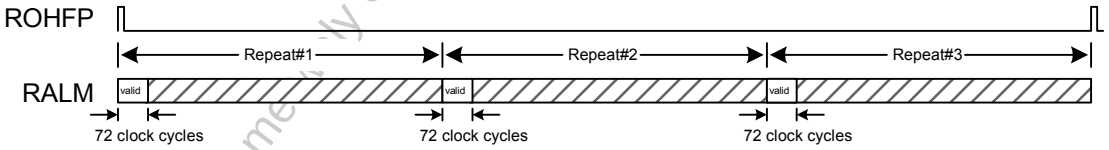


When the Path Overhead Insertion interface is not being used, the THPP should be set to use its internal insertion registers (see register description for THPP Indirect Register 01H, the THPP Source and Pointer Control Register).

14.6 SONET Alarm Indication Signal

Figure 49 shows the receive path alarm functional timings. RALM is used to output the "ORing" of the enabled path defects. RALM is timed off of ROHCLK (a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle)). 2592 clock cycles of ROHCLK are output on RALM between two ROHFP assertions. ROHFP high identifies clock cycle 1 of 2592. Only the first 72 cycles (cycles 1 to 72) contain necessary information. That information is repeated again at clock cycles 865-936 and 1729-1800.

Figure 49 RALM and ROHFP Output Timing



15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 29 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
Supply Voltage for 1.8V	-0.3V to +2.5V
Supply Voltage for 3.3V	-0.3V to +4.6V
Voltage on any PECL Compatible Pin	-0.3V to (AVDH + 0.3V)
Voltage on any LVDS Pin	-0.3V to (AVDH + 0.3V)
Voltage on any Digital Pin except for SD	-0.3V to (VDDO + 0.3V)
Voltage on SD Digital TTL input pin	-0.3V to 5.5V
Static Discharge Voltage	±1000 V
Latch-Up Current except RESK pin	±100 mA
Latch-Up Current on RESK pin	±50 mA
DC Input Current	±20 mA
Lead/Ball Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C
Maximum Overshoot on Output pins *	-2V to (VDDO + 2V) for 10ns, 20mA max
Input pad overshoot tolerance	-2V to (VDDO + 2V) for 10ns, 100mA max

* Most output pins require termination circuitry.

16 Power Information

16.1 Power Requirements

Table 30 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
Cross-connect mode. TFCLK and RFCLK are static	IDDOP (VDDI)	930	—	1350	mA
	IDDOP (VDDO)	37	—	60	mA
	IDDOP (AVDL)	290	—	490	mA
	IDDOP (AVDH)	150	—	180	mA
	Total Power	2.80	3.61	—	W
PL3/UL3 mode. TFCLK and RFCLK at 104MHz. APS analog blocks are held in reset (APS_CSU, TXLV, RXLV, APS_APISO, APS_DRU)	IDDOP (VDDI)	1100	—	1550	mA
	IDDOP (VDDO)	190	—	300	mA
	IDDOP (AVDL)	175	—	310	mA
	IDDOP (AVDH)	80	—	90	mA
	Total Power	3.20	4.08	—	W
PL3 working/protect mode. Same as above but all the APS analog is active.	IDDOP (VDDI)	1150	—	1610	mA
	IDDOP (VDDO)	195	—	300	mA
	IDDOP (AVDL)	290	—	500	mA
	IDDOP (AVDH)	150	—	160	mA
	Total Power	3.75	4.70	—	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system

2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)

3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system

4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

16.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. VDDO power must be supplied either before VDDI or simultaneously with VDDI.

2. AVDH can be applied either before or after VDDO, but must be applied either before or simultaneously with VDDI and AVDL. In operation, the differential voltage measured between AVDH supplies and VDDO_DC must be less than 0.5 volt. The relative power sequencing of the multiple AVDH power supplies is not important.

3. AVDL must be applied after AVDH and VDDO, and either before or after VDDI. Or, AVDL can be applied simultaneously with VDDO, AVDH, and VDDI.

4. I/Os get driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

5. Power down the device in the reverse sequence.

16.3 Power Supply Filtering

1. Use a single plane for both digital and analog grounds.

2. Provide separate analog transmit, analog receive, and digital supplies, but otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

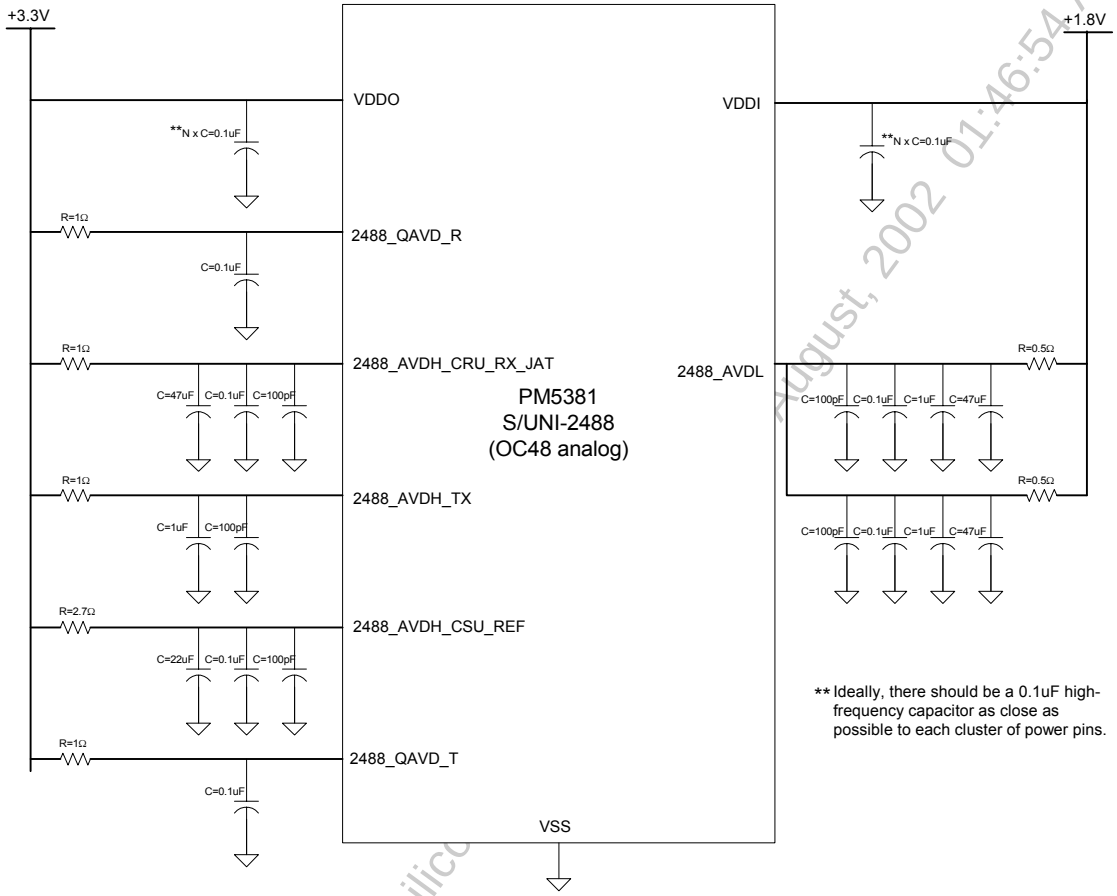
4. The following analog power-supply filtering is recommended:

Table 31 Optimal OC48 Analog Power-Supply Filtering Recommendations

Ball Name	Ball Location	Label in Figure 50	Function	Filtering
AVDH	AB1	AVDH (CSU)	APS CSU power	3.3Ω + [100nF || 10nF]
AVDH	AC4, AF4, AG3, AH2 AJ1, W4, U3, U4	AVDH (TXLV)	APS transmitter power	3.3Ω + [1.0uF || 10nF] (can be paired up - maximum of 2 per filter)

AVDL	AD4, AD3, AF2	AVDL (CSU)	APS CSU power	0.47Ω + [4.7uF || 10nF]
AVDL	AA4	AVDL (analog core)	APS core power (except APS CSU)	0Ω + [100nF || 10nF]
AVDH	AG20, AH20	2488_QAVD_R	3.3V power for receive-side isolation moat	1Ω + 0.1uF
AVDH	AG19, AH19, AJ19, AK19, AG17, AH17, AJ17	2488_AVDH_CRU_RX_JAT	3.3V power for 2.5G CRU, RX & JAT	1.8Ω + [47uf || 0.1uF || 100pF]
AVDH	AG14, AH14, AJ14	2488_AVDH_TX	3.3V power for 2.5Gbps PECL transmitter	1Ω + 1.0uF || 100pF
AVDH	AG10, AH10, AJ10, AG9, AH9, AJ9	2488_AVDH_CSU_REF	3.3V power for 2.5GHz CSU & Ref	2.7Ω + [22uf || 0.1uF || 100pF]
AVDH	AG8, AH8	2488_QAVD_T	3.3V power for transmit-side isolation moat	1Ω + 0.1uF
AVDL	AG5, AG6, AG21, AH5, AH6, AH21, AJ5, AJ6, AJ21, AK5, AK6, AK21	2488_AVDL	1.8V power to all 2.5G line-side analog	0.5Ω + [47uF || 1uf || 0.1uF || 100pF] Have two of the above filter in II. Short them on PCB before going to pins

Figure 50 Optimal OC48 Analog Power Supply Filters



For boards designed with previous revisions of the S/UNI-2488, the follow analog power supply filtering components can be used. The number of components matches the previously recommended filter.

Table 32 Backwards Compatible OC48 Analog Power-Supply Filtering Recommendations

Ball Name	Ball Location	Label in Figure 51	Function	Filtering
AVDH	AB1	AVDH (CSU)	APS CSU power	3.3Ω + [100nF || 10nF]
AVDH	AC4, AF4, AG3, AH2 AJ1, W4, U3, U4	AVDH (TXLV)	APS transmitter power	3.3Ω + [1.0uF || 10nF] (can be paired up - maximum of 2 per filter)
AVDL	AD4, AD3, AF2	AVDL (CSU)	APS CSU power	0.47Ω + [4.7uF || 10nF]
AVDL	AA4	AVDL (analog core)	APS core power (except APS CSU)	0Ω + [100nF || 10nF]
AVDH	AG20, AH20	2488_QAVD_R	3.3V power for	1Ω + 0.1uF

Ball Name	Ball Location	Label in Figure 51	Function	Filtering
			receive-side isolation moat	
AVDH	AG19, AH19, AJ19, AK19	2488_AVDH_ CRU_JAT	3.3V power for 2.5G CRU & JAT	4.7Ω + [22uf || 0.1uF || 100pF]
AVDH	AG17, AH17, AJ17	2488_AVDH_RX	3.3V power for 2.5Gbps PECL receiver	1Ω + [0.1uF || 100pF]
AVDH	AG14, AH14, AJ14	2488_AVDH_TX	3.3V power for 2.5Gbps PECL transmitter	1Ω + 1.0uF || 100pF
AVDH	AG10, AH10, AJ10	2488_AVDH_ CSU	3.3V power for 2.5GHz CSU	2.7Ω + [22uf || 0.1uF || 100pF]
AVDH	AG9, AH9, AJ9	2488_AVDH_RE F	3.3V power for 155MHz PECL reference inputs	1Ω + [0.1uF || 100pF]
AVDH	AG8, AH8	2488_QAVD_T	3.3V power for transmit-side isolation moat	1Ω + 0.1uF
AVDL	AG5, AG6, AG21, AH5, AH6, AH21, AJ5, AJ6, AJ21, AK5, AK6, AK21	2488_AVDL	1.8V power to all 2.5G line-side analog	0.33Ω + [47uF || 1uf || 0.1uF || 100pF]

Figure 51 Backwards Compatible OC48 Analog Power Supply Filters

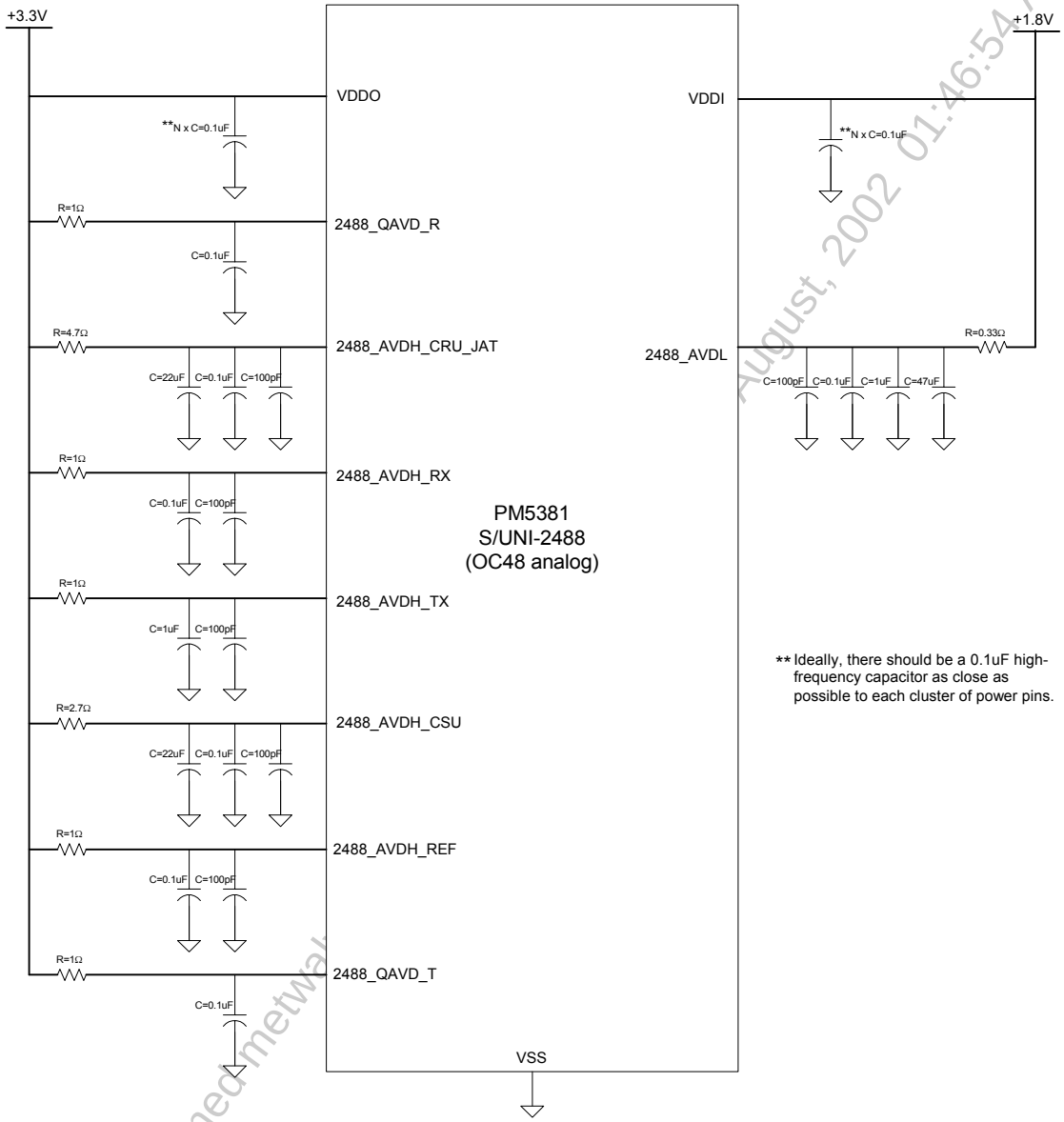
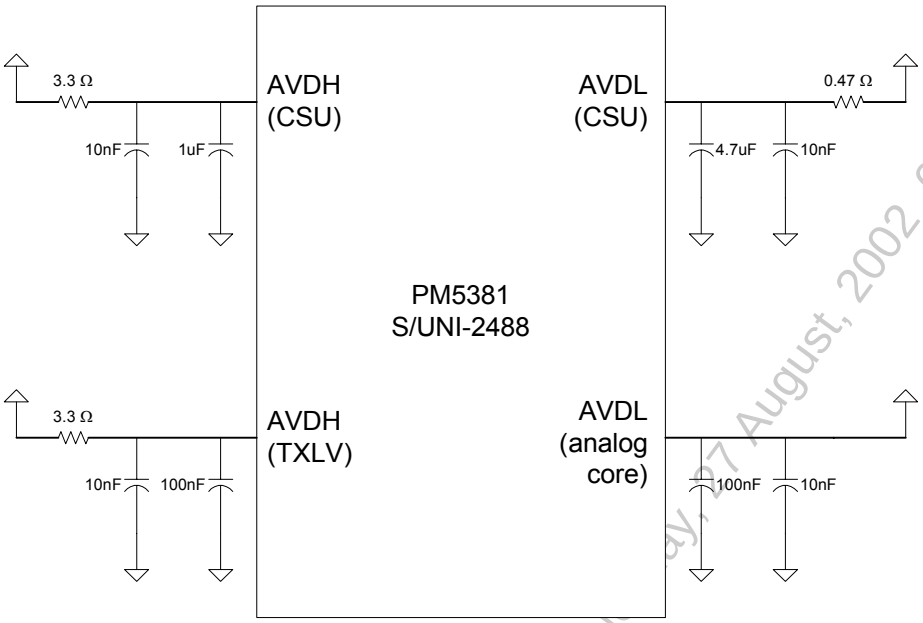


Figure 52 APS Interface LVDS Analog Power Supply Filters



17 D.C. Characteristics

T_a = -40°C to T_j = 125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%, AVDL = $AVDL_{typical}$ ± 5%, AVDH = $AVDH_{typical}$ ± 5%, QAVD = $QAVD_{typical}$ ± 5%

Typical Conditions: T_a = 25°C, VDDI = 1.8V, VDDO = 3.3V, AVDH = 3.3V, AVDL = 1.8V, QAVD = 3.3V

Table 33 D.C Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_{VDDI}	Power Supply	1.71	1.8	1.89	Volts	
V_{VDDO}	Power Supply	3.14	3.3	3.46	Volts	
V_{AVDL}	Power Supply	1.71	1.8	1.89	Volts	
V_{AVDH}	Power Supply	3.14	3.3	3.46	Volts	
V_{QAVD}	Power Supply	3.14	3.3	3.46	Volts	
V_{IL}	Input Low Voltage			0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at VDD=3.14 V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	VDDO – 0.2		Volts	Guaranteed output High voltage at VDD=3.14 V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.2			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	-200	-50	-10	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 2 and 3.
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity	20		100	mV	
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between "0" and "1"			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between "0" and "1"			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
ISPN	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
$V_{OA, PECL}$	PECL Output Amplitude Register 0020H, Bit 6 = '0' (default) Register 0020H, Bit 6 = '1'	 0.900 0.465	 1.000 0.533	 1.100 0.600	 Vppd Vppd	Differential Peak-to-Peak Voltage (Tx) Min: at -40ºC, V_{AVDH}(min), V_{AVDL}(min) Max: at 125ºC, V_{AVDH}(max),V_{AVDL}(max)
$V_{IA, PECL}$	PECL Input Amplitude	0.4		2.0	Vppd	Differential Peak-to-Peak Voltage (Rx)
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

18 A.C. Timing Characteristics

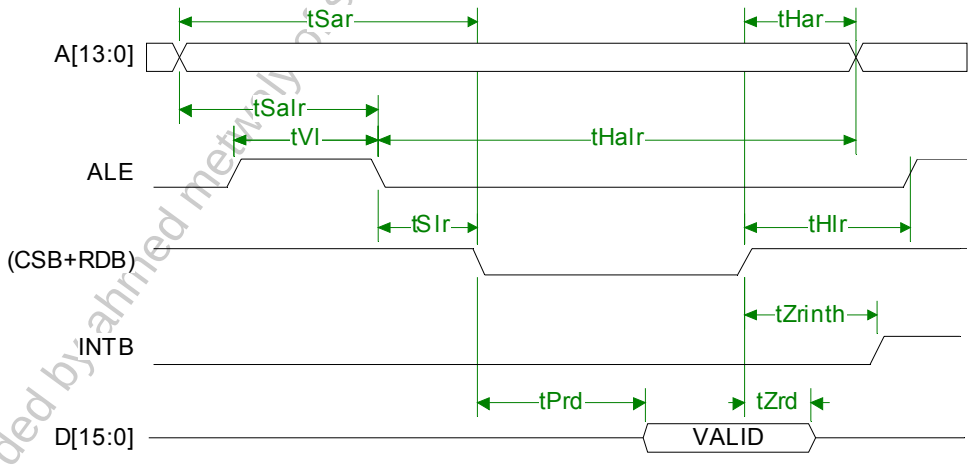
T_a = -40°C to T_j = 125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%, AVDL = $AVDL_{typical}$ ± 5%, AVDH = $AVDH_{typical}$ ± 5%, QAVD = $QAVD_{typical}$ ± 5%

18.1 Microprocessor Interface Timing Characteristics

Table 34 Microprocessor Interface Read Access Timing (Figure 53)

Symbol	Parameter	Min	Max	Units
TS_{ar}	Address to Valid Read Set-up Time	10		ns
TH_{ar}	Address to Valid Read Hold Time	10		ns
TS_{alr}	Address to Latch Set-up Time	10		ns
TH_{alr}	Address to Latch Hold Time	10		ns
TV_{l}	Valid Latch Pulse Width	5		ns
TS_{lr}	Latch to Read Set-up	0		ns
TH_{lr}	Latch to Read Hold	10		ns
TP_{rd}	Valid Read to Valid Data Propagation Delay		70	ns
TZ_{rd}	Valid Read Negated to Output Tri-state		20	ns
TZ_{rinth}	Valid Read Negated to INTB High (WCIMODE = 0)		50	ns

Figure 53 Intel Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

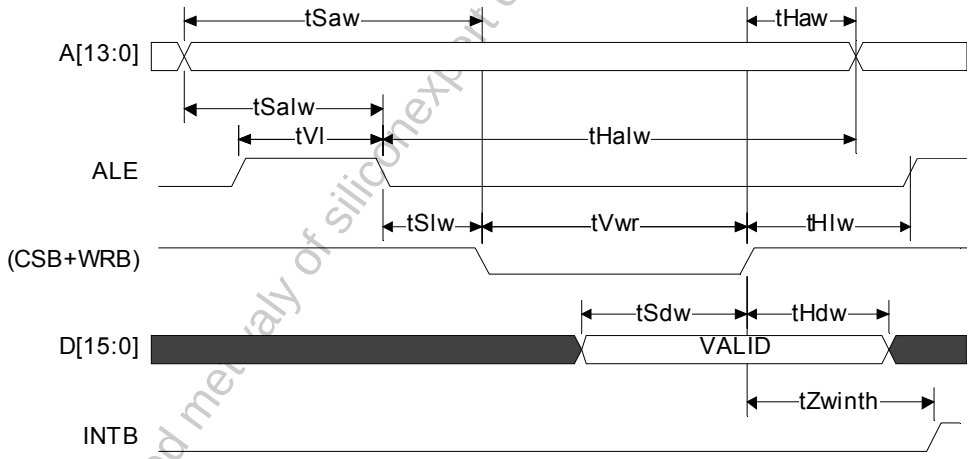
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{alr}, tH_{alr}, tV_{l}, tS_{lr}, and tH_{lr} are not applicable.
5. Parameter tH_{ar} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 35 Microprocessor Interface Write Access Timing (Figure 54)

Symbol	Parameter	Min	Max	Units
tS_{aw}	Address to Valid Write Set-up Time	10		ns
tS_{dw}	Data to Valid Write Set-up Time	20		ns
tS_{alw}	Address to Latch Set-up Time	10		ns
tH_{alw}	Address to Latch Hold Time	10		ns
tV_{l}	Valid Latch Pulse Width	5		ns
tS_{lw}	Latch to Write Set-up	0		ns
tH_{lw}	Latch to Write Hold	10		ns
tH_{dw}	Data to Valid Write Hold Time	5		ns
tH_{aw}	Address to Valid Write Hold Time	10		ns
tV_{wr}	Valid Write Pulse Width	40		ns
TZ_{winth}	Valid Write Negated to INTB High (WCIMODE = 1)		50	ns

Figure 54 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

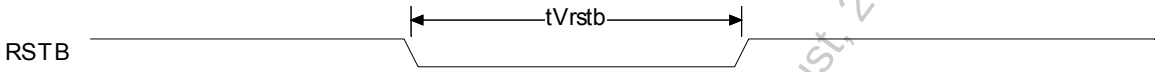
1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{alw}, tH_{alw}, tV_{l}, tS_{lw}, and tH_{lw} are not applicable.
3. Parameter tH_{aw} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt

18.2 Reset Pulse Width Timing Characteristics

Table 36 Reset Pulse Width Timing (Figure 55)

Symbol	Description	Min	Max	Units
tV_{rstb}	RSTB pulse width	2		ms

Figure 55 Reset pulse width

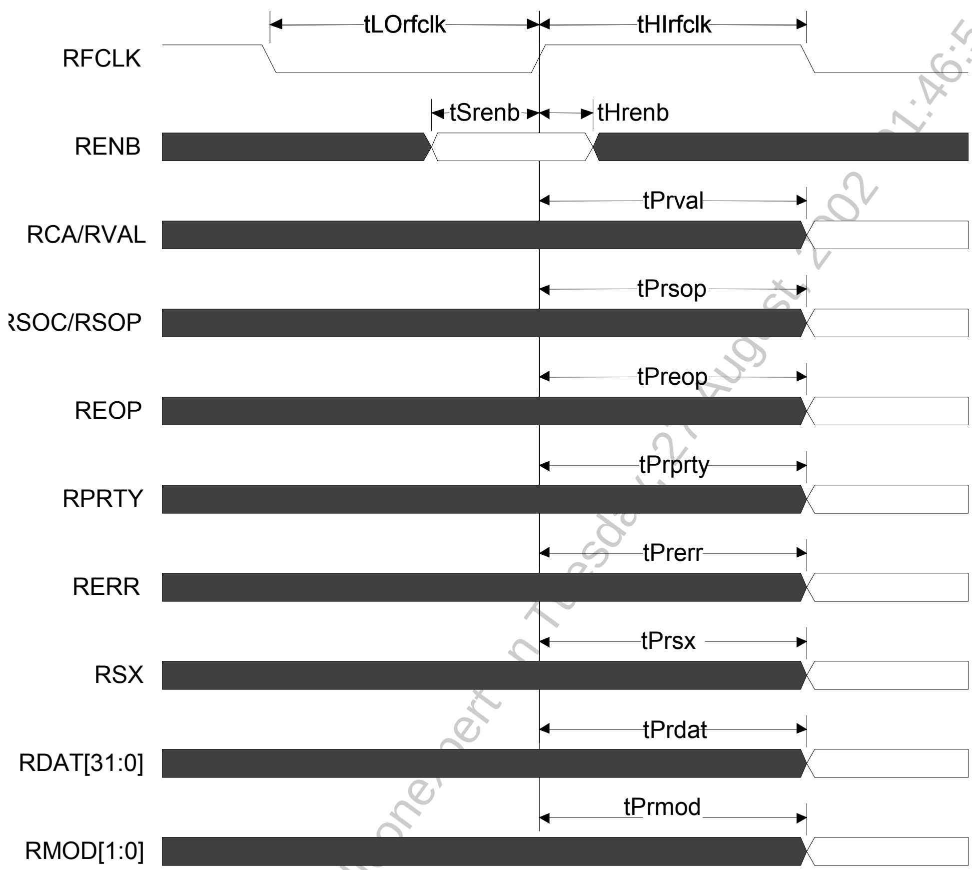


18.3 Receive System Interface Timing Characteristics

Table 37 Receive System Interface Timing (Figure 56)

Symbol	Description	Min	Max	Units
F_{rfclk}	RFCLK Frequency	60	104	MHz
tHI_{rfclk}	RFCLK HI Pulse Width	3.85		ns
tLO_{rfclk}	RFCLK LO Pulse Width	3.85		ns
tS_{renb}	RENB Set-up time to RFCLK	2		ns
tH_{renb}	RENB Hold time to RFCLK	0.5		ns
tP_{rval}	RFCLK High to RCA/RVAL Valid	1.5	6	ns
tP_{rsop}	RFCLK High to RSOC/RSOP Valid	1.5	6	ns
tP_{reop}	RFCLK High to REOP Valid	1.5	6	ns
tP_{rprty}	RFCLK High to RPRTY Valid	1.5	6	ns
tP_{rerr}	RFCLK High to RERR Valid	1.5	6	ns
tP_{rsx}	RFCLK High to RSX Valid	1.5	6	ns
tP_{rdat}	RFCLK High to RDAT[31:0] Valid	1.5	6	ns
tP_{rmod}	RFCLK High to RMOD[1:0] Valid	1.5	6	ns

Figure 56 Receive System Interface Timing Diagram



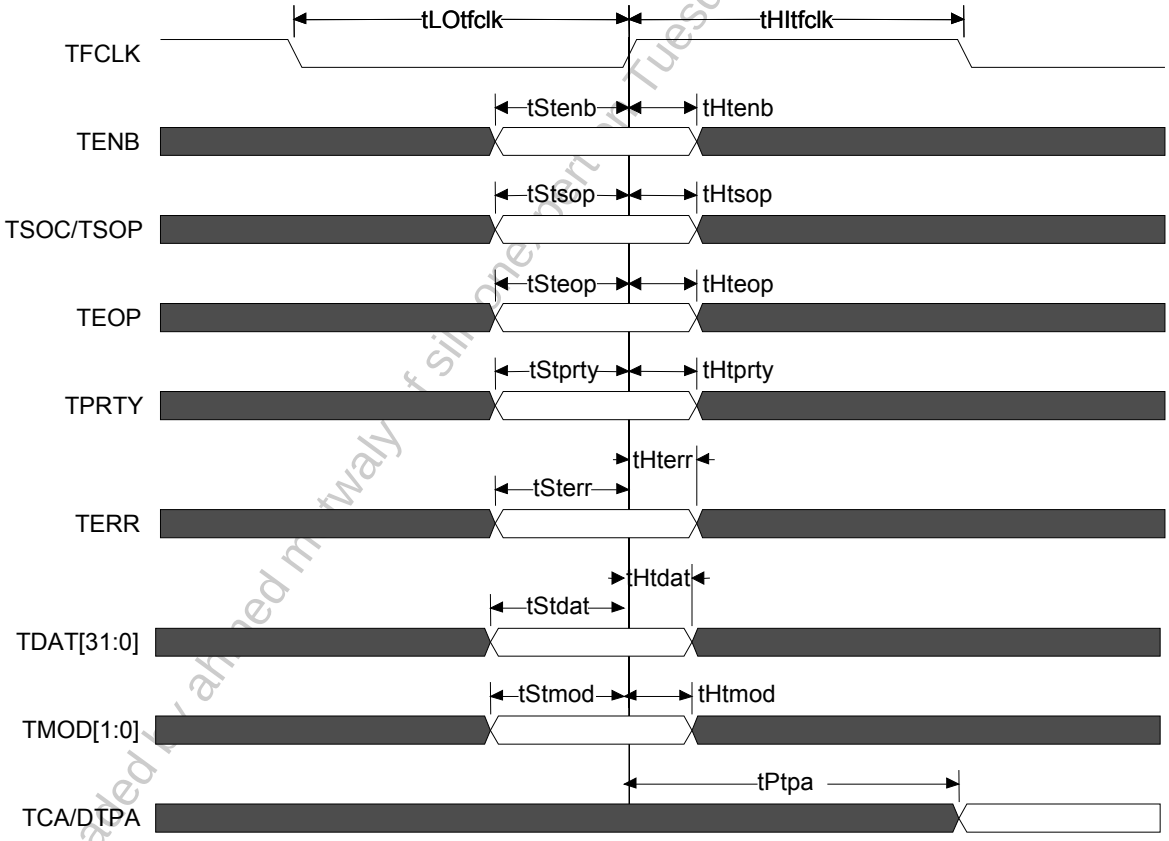
18.4 Transmit System Interface Timing Characteristics

Table 38 Transmit System Interface Timing (Figure 57)

Symbol	Description	Min	Max	Units
F_{tfclk}	TFCLK Frequency	60	104	MHz
tHI_{tfclk}	TFCLK HI Pulse Width	3.85		ns
tLO_{tfclk}	TFCLK LO pulse Width	3.85		ns
tS_{tenb}	TENB Set-up time to TFCLK	2		ns
tH_{tenb}	TENB Hold time to TFCLK	0.5		ns
tS_{tsop}	TSOC/TSOP Set-up time to TFCLK	2		ns
tH_{tsop}	TSOC/TSOP Hold time to TFCLK	0.5		ns
tS_{teop}	TEOP Set-up time to TFCLK	2		ns
tH_{teop}	TEOP Hold time to TFCLK	0.5		ns

Symbol	Description	Min	Max	Units
tS_{tprty}	TPRTY Set-up time to TFCLK	2		ns
tH_{tprty}	TPRTY Hold time to TFCLK	0.5		ns
tS_{terr}	TERR Set-up time to TFCLK	2		ns
tH_{terr}	TERR Hold time to TFCLK	0.5		ns
tS_{tdat}	TDAT[31:0] Set-up time to TFCLK	2		ns
tH_{tdat}	TDAT[31:0] Hold time to TFCLK	0.5		ns
tS_{tmod}	TMOD[1:0] Set-up time to TFCLK	2		ns
tH_{tmod}	TMOD[1:0] Hold time to TFCLK	0.5		ns
tP_{tpa}	TFCLK High to TCA/DTPA Valid	1.5	6	ns

Figure 57 Transmit System Interface Timing



18.5 SONET/SDH Overhead Interface Timing Characteristics

Table 39 SONET/SDH Overhead Interface Timing (Figure 58 and Figure 59)

Symbol	Description	Min	Max	Units
t_{Prohfp}	ROHCLK Low to ROHFP valid	-7	7	ns
t_{Prpoh}	ROHCLK Low to RPOH valid	-7	7	ns
$t_{Prpohen}$	ROHCLK Low to RPOHEN valid	-7	7	ns
t_{Prtoh}	ROHCLK Low to RTOH valid	-7	7	ns
t_{Pralm}	ROHCLK Low to RALM valid	-7	7	ns
t_{Pb3e}	ROHCLK Low to B3E valid	-7	7	ns
t_{Poof}	RCLK High to OOF valid	1	7	ns
t_{Psalm}	RCLK High to SALM valid	1	7	ns
t_{Ptohfp}	TOHCLK Low to TOHFP valid	-7	7	ns
$t_{Ptpohrdy}$	TOHCLK Low to TOHFP valid	-7	7	ns
t_{Stpoh}	TPOH Set-up time to TOHCLK	14		ns
t_{Htpoh}	TPOH Hold time to TOHCLK	0		ns
$t_{Stpohen}$	TPOHEN Set-up time to TOHCLK	14		ns
$t_{Htpohen}$	TPOHEN Hold time to TOHCLK	0		ns
t_{Sttoh}	TTOH Set-up time to TOHCLK	14		ns
t_{Httoh}	TTOH Hold time to TOHCLK	0		ns
$t_{Sttohen}$	TTOHEN Set-up time to TOHCLK	14		ns
$t_{Httohen}$	TTOHEN Hold time to TOHCLK	0		ns

Figure 58 SONET/SDH Receive Overhead Interface Timing

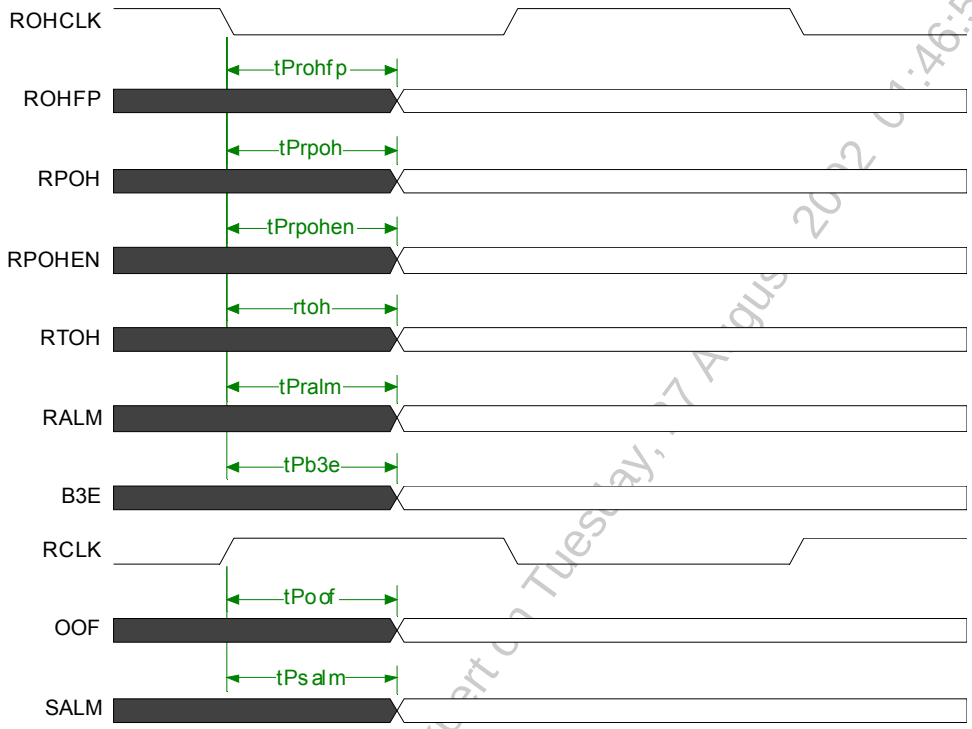
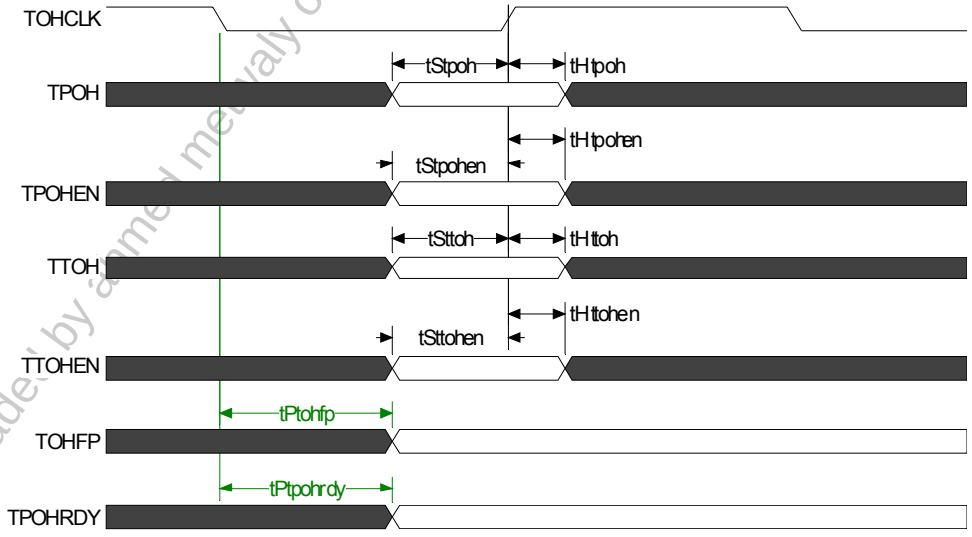


Figure 59 SONET/SDH Transmit Overhead Interface Timing

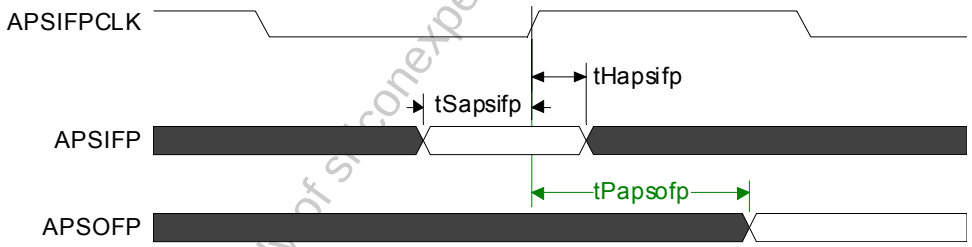


18.6 APS Port Interface Timing Characteristics

Table 40 APS Port Interface Timing (Figure 60)

Symbol	Description	Min	Typical	Max	Units
tSapsifp	APSIFP Set-up time to APSIFPCLK	3			ns
tHapsifp	APSIFP Hold time to APSIFPCLK	0			ns
tPapsofp	APSIFPCLK High to APSOFP valid		10		ns
FRlvds	APSI_P/ APSI_N[4:1], APSO_P/ APSO_N[4:1] Bit Rate	$5f_{APSIFPCLK}$ – 100ppm	$5f_{APSIFPCLK}$	$5f_{APSIFPCLK}$ + 100ppm	Mbit/s
Taps,jitter	Jitter acceptable on APSIFPCLK input			50	ps
Tfall	V_{ODM} fall time, 80%-20%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
Trise	V_{ODM} rise time, 20%-80%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
Tskew	Differential Skew			50	ps

Figure 60 APS Port Interface Timing



18.7 OC-48 Interface Timing Characteristics

Table 41 OC-48 Interface Timing

Symbol	Description	Min	Typical	Max	Units
F_{refclk}	Required frequency for REFCLK_P and REFCLK_N inputs (Bellcore spec for +/-20ppm clock sources); all conditions	155.517	155.52	155.523	MHz
Tref,rise	Rise time for REFCLK_P and REFCLK_N inputs; all conditions	-	-	1	ns
Tref,fall	Fall time for REFCLK_P and REFCLK_N inputs; all conditions	-	-	1	ns
DC_{ref}	Duty Cycle for REFCLK_P and REFCLK_N inputs; all conditions	45	50	55	%
$T_{ref\_rms\_jit}$	RMS Jitter acceptable on REFCLK_P and REFCLK_N inputs (12KHz – 20MHz jitter band); all conditions	-	-	1	ps
$T_{ref\_pk\_jit}$	Peak-to-Peak Jitter acceptable on REFCLK_P and REFCLK_N inputs (12KHz – 20MHz jitter band); all conditions	-	-	10	ps
rb	Bit rate for OC-48 compatible transmit and receive data	-	2.48832 = 16 x F_{refclk}	-	Gb/s
Jrms[1]	Output RMS jitter (12kHz to 20MHz).		0.008	0.01	UI

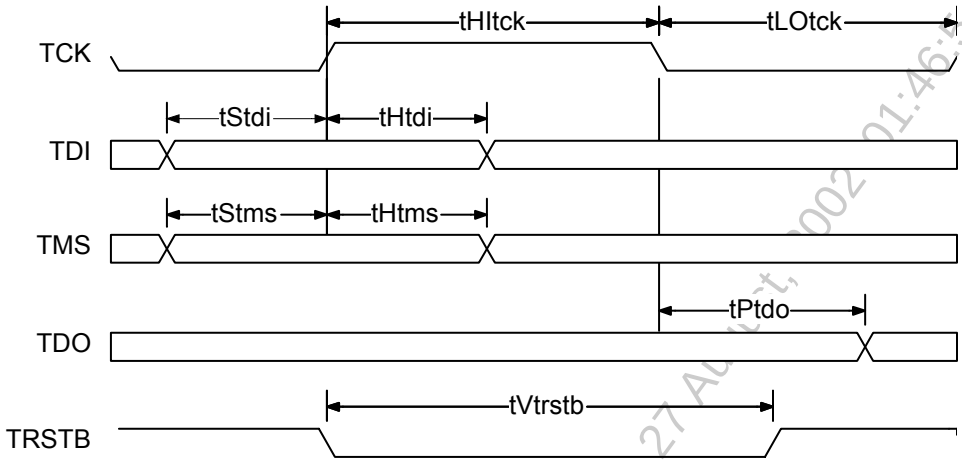
1. Value is based on the nominal STS-48 bit rate. Note that the optical jitter value was characterized with a Finisar FTRJ-1320 Optical Data Link on a PMC validation board.

18.8 JTAG Port Interface Timing Characteristics

Table 42 JTAG Port Interface Timing (Figure 61)

Symbol	Description	Min	Max	Units
f_{tck}	TCK Frequency		4	MHz
tHI_{tck}	TCK HI Pulse Width	100		ns
tHI_{tck}	TCK LO Pulse Width	100		ns
tS_{tms}	TMS Set-up time to TCK	25		ns
tH_{tms}	TMS Hold time to TCK	25		ns
tS_{tdi}	TDI Set-up time to TCK	25		ns
tH_{tdi}	TDI Hold time to TCK	25		ns
tP_{tdo}	TCK Low to TDO Valid	2	25	ns
tV_{trstb}	TRSTB Pulse Width	100		ns

Figure 61 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
4. Maximum and minimum output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified. D[15:0] is with 100pF load.

19 Ordering Information

Table 43 Ordering Information

Part No.	Description
PM5381-BI	416-pin Ultra Ball Grid Array (UBGA)

20 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 44 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105°C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85°C.	125°C
Minimum ambient temperature (T_A)	-40°C

Table 45 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.4°C/W
Junction-to-Board Thermal Resistance, θ_{JB}	6.1°C/W

Table 46 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation

Power depends upon the operating mode. To obtain power information, refer to 'High' power values in Section 16 Power Information.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

The following tables show the thermal resistance vs. air flow if the S/UNI-2488 is not used with a heat sink. In this application, one must be careful to keep the long-term junction temperature at or below 105°C.

Table 47 Thermal Resistance vs. Air Flow[3]

Airflow	Natural Convection	200 LFM	400 LFM
θ_{JA} (°C/W) JEDEC board	12.6	10.2	9.0

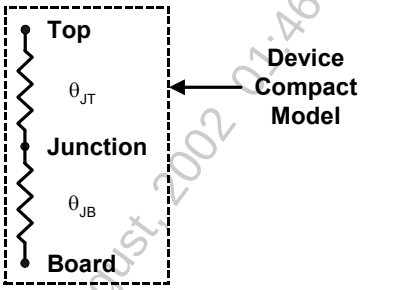


Table 48 Device Compact Model[4]

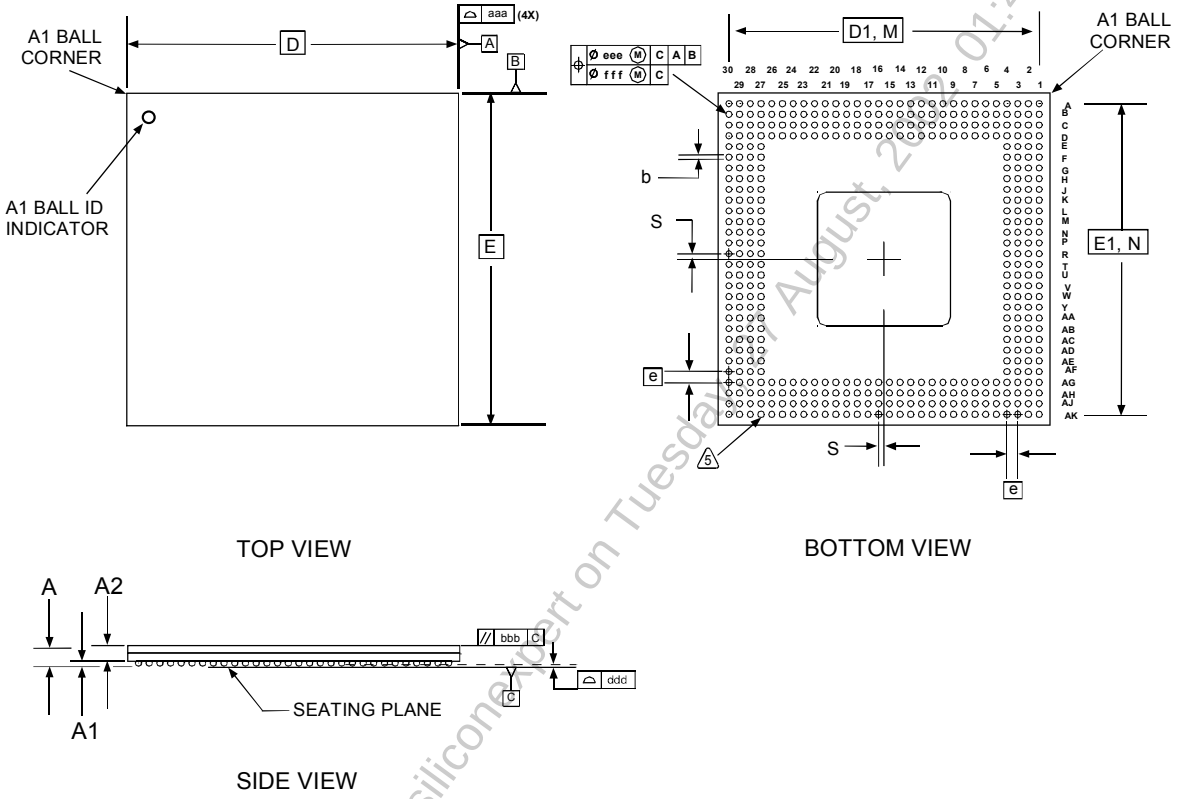
Junction-to-Top Thermal Resistance, θ_{JT}	0.4°C/W
Junction-to-Board Thermal Resistance, θ_{JB}	6.1°C/W

Power depends upon the operating mode. To obtain power information, refer to 'High' power values in Section 16 Power Information.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core
3. θ_{JA}, the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P)
4. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 and θ_{JT}, the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88

21 Mechanical Information



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.45 +/- 0.025 MM (SMD).
6) PACKAGE IS COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192, VARIATION AAN-1 BUT DOES NOT MEET SOLDER BALL POSITIONAL TOLERANCE eee & fff.

PACKAGE TYPE : 416 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 31 x 31 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	1.32	0.40	0.92	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	31.00 BSC	29.00 BSC	31.00 BSC	29.00 BSC	30x30	0.63	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.30	0.10	0.05