PM5361

TUPP

SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR

DATA SHEET

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PUBLIC REVISION HISTORY

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8	July 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R8 data sheet from PMC-920102, issue R10.

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1 FEATURES

- Configurable, multi-channel, payload processor for alignment of SONET virtual tributaries (VTs) or SDH tributary units (TUs). Processes an STS-3 or STM-1 byte serial data stream.
- Transfers all incoming tributaries in the three STS-1 synchronous payload envelopes of an STS-3 byte serial stream to the three STS-1 synchronous payload envelopes of an outgoing STS-3 byte serial stream.
- Transfers all incoming tributaries in the single AU4 or three AU3 administrative units of an STM-1 byte serial stream to the single AU4 or three AU3 administrative units of an outgoing STM-1 byte serial stream.
- Compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11) tributary pointers.
- Provides multiframe synchronization for ring closure at the headend node in a SONET/SDH ring.
- Provides independently configurable AU3/AU4 frame format on incoming and outgoing directions.
- Configurable to process any legal mix of tributaries such as VT1.5, VT2, VT3, VT6, TU11, TU12, TU2, or TU3. Each VT group or TUG2 can be configured to carry one of four tributary types. TUG2s can be multiplexed into VC3s or TUG3s. Each TUG3 can also be configured to carry a TU3.
- Optionally frames to the H4 byte in the path overhead to determine tributary multiframe boundaries. Internally generated H4 bytes with leading logic 1 bits are inserted into the outgoing administrative units.
- Verifies parity on the IC1J1 and ISPE signals and on the incoming data stream and generates parity on the outgoing data stream.
- Detects loss of pointer and re-acquisition for each tributary and optionally generates interrupts. Loss of pointer detection can optionally generate tributary path AIS.

- Allows insertion of all zeros or all ones tributary idle code with unequipped indication and valid pointer into any tributary.
- Allows insertion of tributary path AIS into any tributary.
- Operates in conjunction with the PM5323 TSPP Triple SONET/SDH Payload Processor and the PM5344 SONET/SDH Path Terminating Transceiver to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect.
- Operates from a single 19.44 MHz clock.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, +5 Volt, CMOS technology, TTL compatible inputs and outputs.
- 160 pin plastic quad flat pack (PQFP) package

2 APPLICATIONS

- SONET and SDH Wideband Cross-Connects
- SONET and SDH Add-Drop and Terminal Multiplexers

3 REFERENCES

1. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1988.

2. CCITT Blue Book, Recommendation G.708 - "Network Node Interface For The Synchronous Digital Hierarchy", Volume III, Fascicle III.4, 1988.

3. CCITT Blue Book, Recommendation G.709 - "Synchronous Multiplexing Structure", Volume III, Fascicle III.4, 1988.

4. CCITT Study Group XVIII, Report R 33 - "Recommendations Drafted By Working Party XVIII/7" (Digital Hierarchies) To Be Approved In 1990 Including Revised Draft Recommendations G.708 and G.709", June 1990.

5. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 2, December 1991.

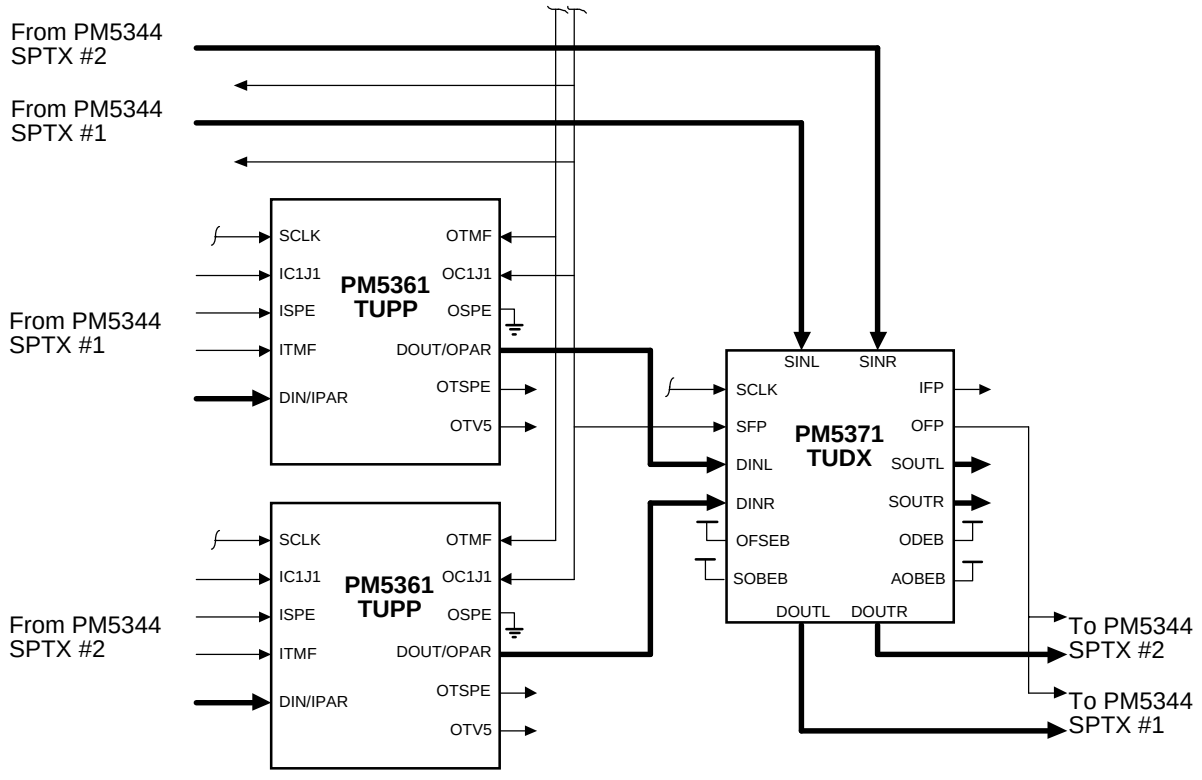
4 APPLICATION EXAMPLE

The PM5361 TUPP is typically used as part of a SONET/SDH tributary cross-connect. TUPPs can be used to transfer the payloads of incoming tributaries into outgoing tributaries that are aligned to facilitate switching. A typical example is shown below.

This example shows the tributaries extracted from an STS-1 or AU3 path terminating device, such as the PM5344 SPTX SONET/SDH Path Terminating Transceiver, being routed through TUPPs so as to be aligned for cross-connection using the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect.

The TUPP (and SPTX) can be bypassed by switching through whole STS-1s or AU3s that are output by the PM5323 TSPP Triple SONET/SDH Payload Processor. Note that in this application example, the TUPPs are operating in locked output mode (i.e. their OJ1EN bits are low) to allow convenient interfacing to the TUDX chip.

Figure 1 - SONET/SDH Tributary Cross-Connect Application



5 BLOCK DIAGRAM

Figure 2 - Overall Device

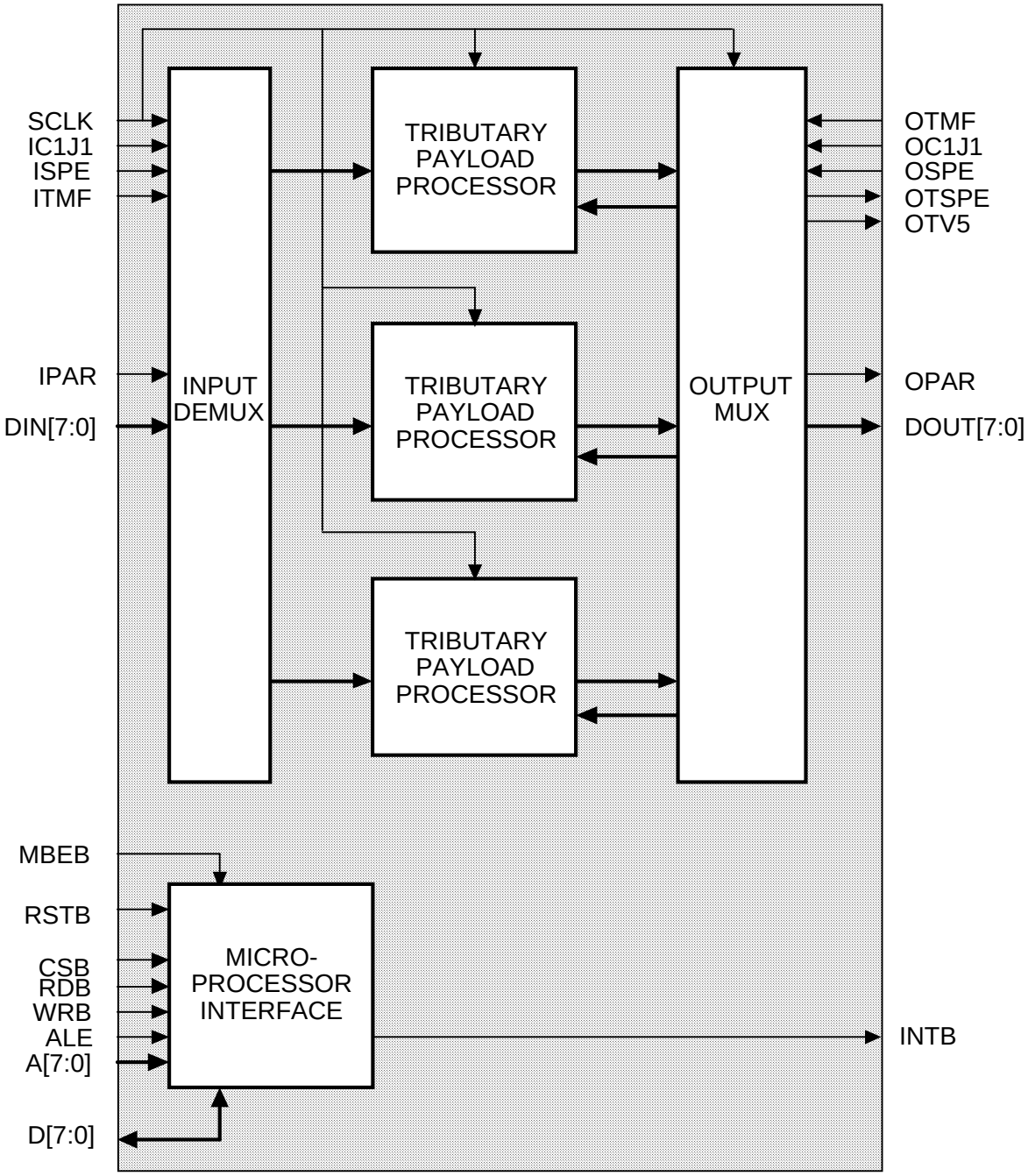
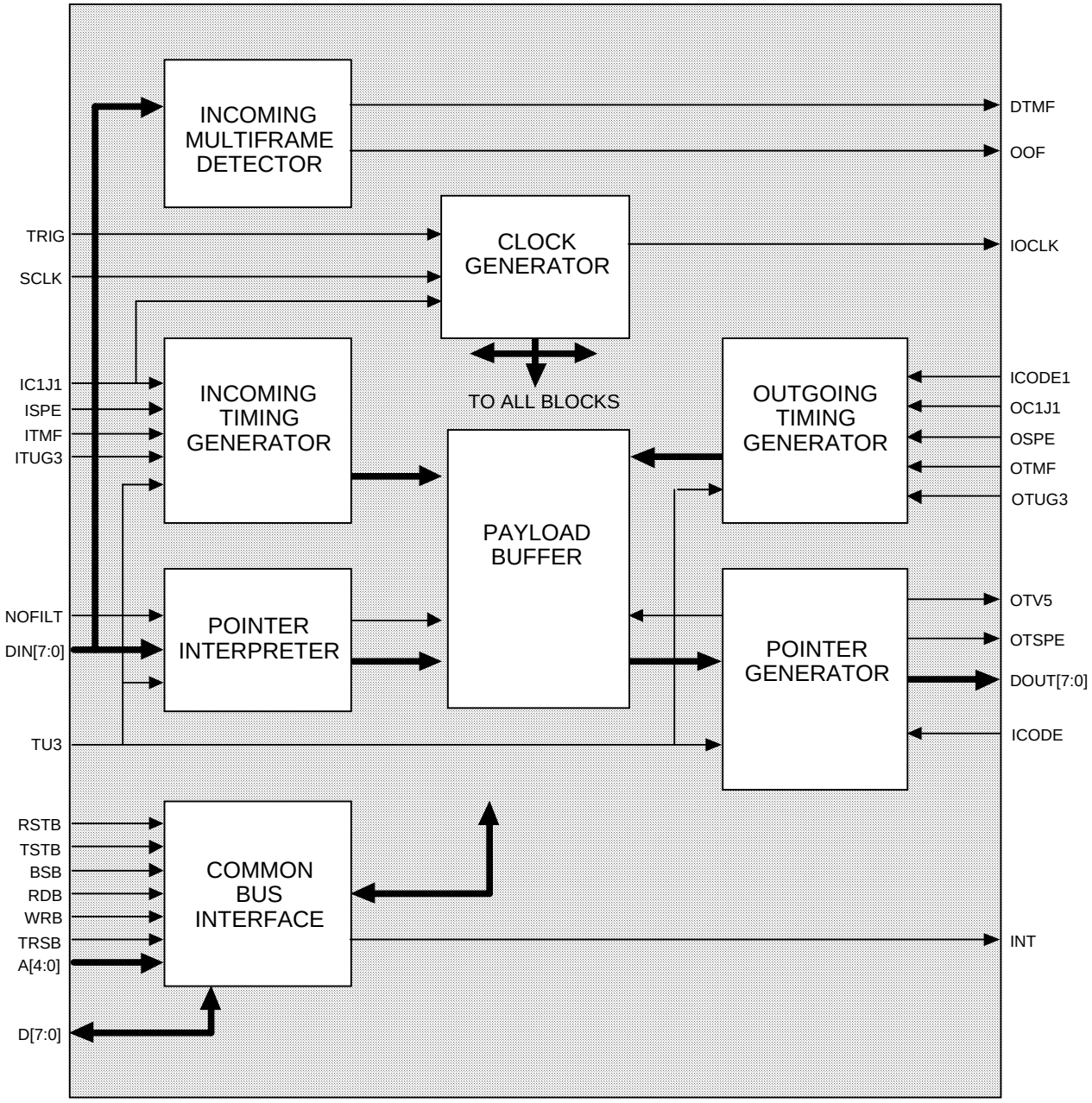


Figure 3 - Each Tributary Payload Processor



6 DESCRIPTION

The PM5361 TUPP SONET/SDH Tributary Unit Payload Processor is a monolithic integrated circuit that implements a configurable, multi-channel, payload processor for alignment of SONET virtual tributaries (VTs) or SDH tributary units (TUs.)

When configured for SONET compatible operation, the TUPP transfers all tributaries in the three STS-1 synchronous payload envelopes of an incoming STS-3 byte serial stream to the three STS-1 synchronous payload envelopes of an outgoing STS-3 byte serial stream. Similarly, when configured for SDH compatible operation, the TUPP transfers all tributaries in the single AU4 or three AU3 administrative units of an incoming STM-1 byte serial stream to a single AU4 or three AU3 administrative units of an outgoing STM-1 byte serial stream. The TUPP compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, TU11) tributary pointers.

The TUPP is configurable to process any legal mix of tributaries. Each VT group can be configured to carry any one of the four tributary types (VT1.5, VT2, VT3, or VT6) and each TUG2 can be configured to carry any one of three tributary types (TU11, TU12, or TU2). TUG2s can be multiplexed into a VC3 or a TUG3. Alternatively, each TUG3 can be configured to carry a TU3.

The TUPP operates in conjunction with the PM5323 TSPP Triple SONET/SDH Payload Processor and the PM5344 SONET/SDH Path Terminating Transceiver to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect.

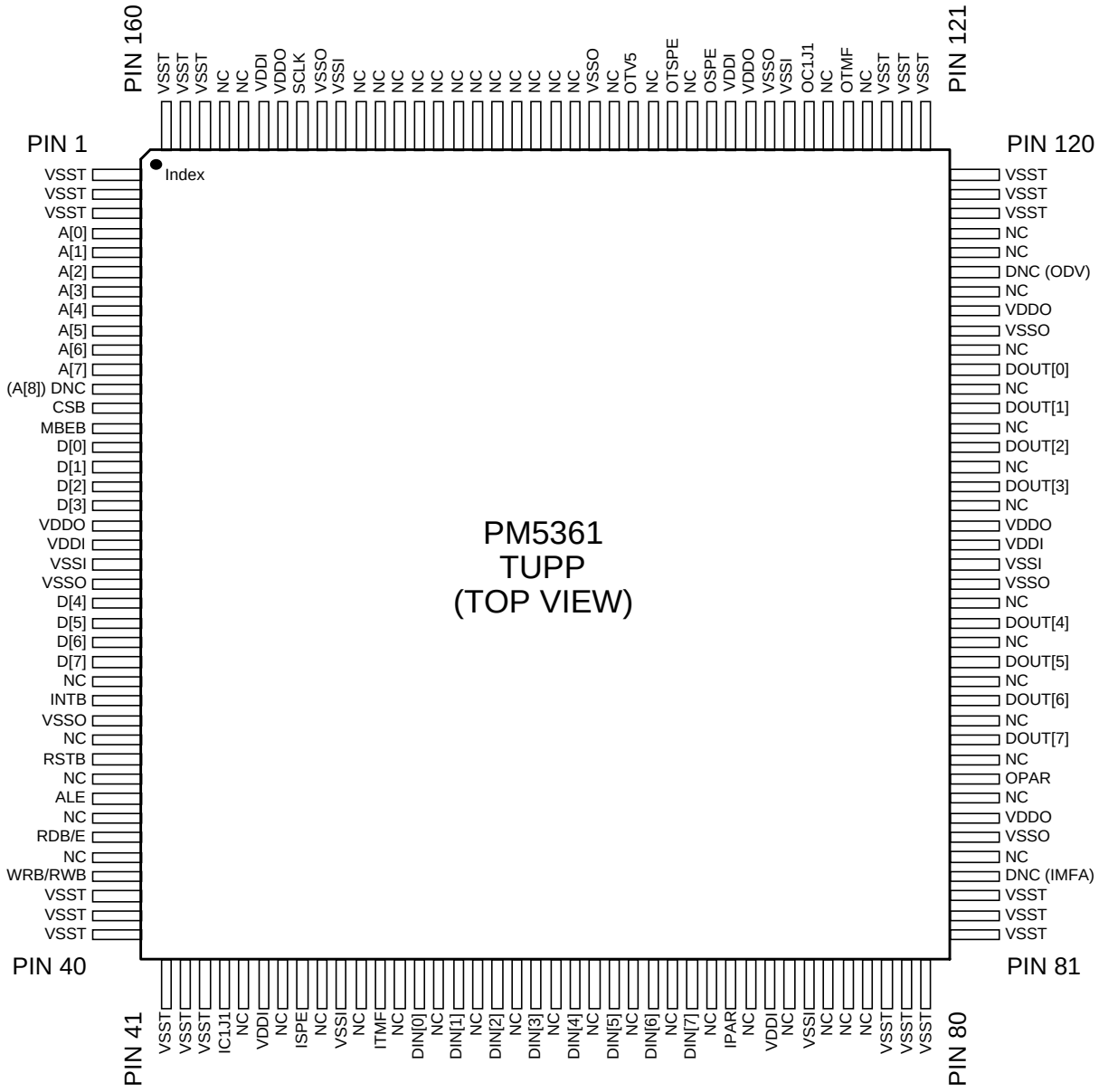
The TUPP provides useful maintenance functions. They include detection of loss of pointer and pointer re-acquisition for each tributary, and optional generation of interrupts. The TUPP also allows insertion of tributary path AIS or tributary idle (unequipped). The TUPP can also insert inverted new data flag fields that can be used to diagnose downstream pointer processing elements.

No auxiliary high speed clocks are required as the TUPP operates from a single 19.44 MHz line rate clock. The TUPP is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The TUPP is implemented in low power, +5 Volt, CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 160 pin PQFP package.

7 PIN DIAGRAM

The TUPP is packaged in an 160 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.65 mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
SCLK VCLK	Input	153	The system clock (SCLK) provides timing for TUPP internal operation. SCLK is a 19.44 MHz, nominally 50% duty cycle clock. The test vector clock (VCLK) signal is used during TUPP production testing to verify internal functionality.
IC1J1	Input	44	The input C1/J1 frame pulse (IC1J1) identifies the transport envelope and synchronous payload envelope frame boundaries on the DIN[7:0] bus. IC1J1 is set high while ISPE is low to mark the first C1 byte of the transport envelope frame on the DIN[7:0] bus. IC1J1 is set high while ISPE is high to mark each of the J1 bytes of the synchronous payload envelope(s) on the DIN[7:0] bus. IC1J1 must be present at every occurrence of the first C1 and all J1 bytes. The TUPP will ignore a pulse on IC1J1 at the byte position of the V1 byte of the first tributary of each TUG3 or VC3. IC1J1 is sampled on the rising edge of SCLK.

Pin Name	Type	Pin No.	Function
ITMF	Input	52	The active high incoming tributary multiframe (ITMF) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit. ITMF is enabled by the setting the ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF is selectable to pulse high during the V1 byte of the first tributary or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking V1 or H4 bytes is controlled by the ITMFH4 register bit. Pulses on ITMF are only effective during the H4 or V1 byte positions, as appropriate. ITMF is ignored at other byte positions. The ITMFEN and ITMFH4 bits are located in the master incoming configuration register. ITMF is sampled on the rising edge of SCLK.
ISPE	Input	48	The active high incoming synchronous payload envelope (ISPE) signal identifies the bytes within the transport envelope frame on the DIN[7:0] bus that carry the AU3 or AU4 virtual containers, and STS-1 synchronous payload envelopes. ISPE must be brought high to mark each such byte. ISPE is sampled on the rising edge of SCLK.

Pin Name	Type	Pin No.	Function
IPAR	Input	70	The incoming stream parity (IPAR) signal carries the parity of the incoming signals. The parity calculation encompasses the IC1J1 signal, the ISPE signal and the DIN[7:0] bus. IC1J1 and ISPE can be included in the parity calculation by setting the INCIC1J1 and INCISPE register bits respectively high. Odd parity is selected by setting the IOP register bit high, and even parity is selected by setting the IOP bit low. The INCIC1J1, INCISPE and IOP bits are located in the master incoming configuration register. IPAR is sampled on the rising edge of SCLK.
OC1J1	Input	127	The outgoing C1/J1 frame pulse (OC1J1) marks the transport envelope and synchronous payload envelope frame boundaries on the DOUT[7:0] bus. When the OJ1EN register bit is set low, OC1J1 pulses high to mark the first C1 byte of the transport envelope frame on the DOUT[7:0] bus. The position of the J1 bytes is implicit and fixed to the bytes immediately following the last C1 byte. When the OJ1EN register bit is set high, the OC1J1 signal pulses high while ISPE is low to mark the first C1 byte of the transport envelope frame on the DOUT[7:0] bus and pulses high while OSPE is high to mark each of the J1 bytes of the synchronous payload envelope(s) on the DOUT[7:0] bus. OC1J1 must be present at every occurrence of the first C1 byte and all J1 bytes. A V1 pulse added to the OC1J1 input will be ignored by the TUPP. The OJ1EN bit is located in the master outgoing configuration register. OC1J1 is sampled on the rising edge of SCLK.

Pin Name	Type	Pin No.	Function
OTMF	Input	125	The active high outgoing tributary multiframe (OTMF) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, and STS-1 synchronous payload envelope. OTMF is selectable to pulse high during the V1 byte of the first tributary or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking V1 or H4 bytes is controlled by the OTMFH4 bit located in the master outgoing configuration register. Pulses on OTMF are only effective during the H4 or V1 byte positions, as appropriate. OTMF is ignored at other byte positions. OTMF is sampled on the rising edge of SCLK.
OSPE	Input	132	The active high outgoing synchronous payload envelope (OSPE) signal identifies the bytes within the transport envelope frame on the DOUT[7:0] bus that carry the AU3 or AU4 virtual container(s), and the STS-1 synchronous payload envelopes. When the OJ1EN register bit is set high, OSPE must be set high to mark each such byte. When the OJ1EN bit is set low, the outgoing virtual container (synchronous payload envelope) is locked with the J1 byte immediately following the C1 byte. OSPE is ignored. DOUT[7:0], OTSPE, and OTV5 contain valid data only for bytes in the AU3 or AU4 virtual container(s), or the STS-1 synchronous payload envelopes. Their contents should be ignored for bytes in the transport overhead. The OJ1EN bit is located in the master outgoing configuration register. OSPE is sampled on the rising edge of SCLK.

Pin Name	Type	Pin No.	Function
DIN[0] DIN[1] DIN[2] DIN[3] DIN[4] DIN[5] DIN[6] DIN[7]	Input	54 56 58 60 62 64 66 68	The data input bus (DIN[7:0]) carries SONET/SDH frame data in byte serial format. DIN[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. DIN[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The DIN[7:0] bus is sampled on the rising edge of SCLK.
DOUT[0] DOUT[1] DOUT[2] DOUT[3] DOUT[4] DOUT[5] DOUT[6] DOUT[7]	Output	110 108 106 104 97 95 93 91	The data output bus (DOUT[7:0]) carries SONET/SDH frame data in byte serial format. DOUT[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first DOUT[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. DOUT[7:0] contains valid data only for bytes in the AU3 or AU4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. The DOUT[7:0] bus is updated on the rising edge of SCLK.
OPAR	Output	89	The outgoing stream parity (OPAR) signal carries the parity of the outgoing data stream. Odd parity is selected by setting the OOP register bit in the master parity configuration register high, and even parity is selected by setting the OOP bit low. OPAR is updated on the rising of SCLK.

Pin Name	Type	Pin No.	Function
OTSPE	Output	134	The outgoing tributary synchronous payload envelope (OTSPE) signal marks the bytes carrying the tributary synchronous payload envelope(s). OTSPE is set high to mark each such byte on the DOUT[7:0] bus. OTSPE, contains valid data only for bytes in the AU3 or AU4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. OTSPE is updated on the rising edge of SCLK.
OTV5	Output	136	The outgoing tributary V5 byte (OTV5) signal marks the various tributary V5 bytes. OTV5 is set high to mark each tributary V5 byte on the DOUT[7:0] bus. When the output tributary is a TU3, OTV5 marks the J1 byte of the TU3. OTV5 contains valid data only for bytes in the AU3 or AU4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. OTV5 is updated on the rising edge of SCLK.
MBEB	Input	14	The active low Motorola bus enable (MBEB) signal configures the TUPP for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the TUPP is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
CSB	Input	13	The active low chip select (CSB) signal is low during TUPP register accesses.

Pin Name	Type	Pin No.	Function
RDB/ E	Input	35	The active low read enable (RDB) signal is low during TUPP register read accesses while in Intel bus mode. The TUPP drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. The active high external access (E) signal is high during TUPP register access while in Motorola bus mode.
WRB/ RWB	Input	37	The active low write strobe (WRB) signal is low during a TUPP register write accesses while in Intel bus mode. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select (RWB) signal selects between TUPP register read and write accesses while in Motorola bus mode. The TUPP drives the D[7:0] bus with the contents of the addressed register while CSB is low and RWB and E are high. The D[7:0] bus contents are clocked into the addressed register on the falling E edge while CSB and RWB are low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	15 16 17 18 23 24 25 26	The bidirectional data bus D[7:0] is used during TUPP register read and write accesses.

Pin Name	Type	Pin No.	Function
A[0] A[1] A[2] A[3] A[4] A[5] A[6]	Input	4 5 6 7 8 9 10	The address bus A[7:0] selects specific registers during TUPP register accesses.
A[7]/TRS		11	The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS has an integral pull down resistor.
RSTB	Input	31	The active low reset (RSTB) signal provides an asynchronous TUPP reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	33	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the TUPP to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	OD Output	28	The active low interrupt (INTB) signal goes low when a TUPP interrupt source is active. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Pin Name	Type	Pin No.	Function
VDDI1 VDDI2 VDDI3 VDDI4 VDDI5 VDDI6	Power	20 46 72 101 131 155	The core power (VDDI1 - VDDI6) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2 VSSI3 VSSI4 VSSI5 VSSI6	Ground	21 50 74 100 128 151	The core ground (VSSI1 - VSSI6) pins should be connected to GND in common with VSSO.
VDDO1 VDDO2 VDDO3 VDDO4 VDDO5 VDDO6	Power	19 87 102 113 130 154	The pad ring power (VDDO1 - VDDO6) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VSSO1 VSSO2 VSSO3 VSSO4 VSSO5 VSSO6 VSSO7 VSSO8	Ground	22 29 86 99 112 129 138 152	The pad ring ground (VSSO1 - VSSO8) pins should be connected to GND in common with VSSI.

Pin Name	Type	Pin No.	Function
VSST1	Ground	1	The thermal ground (VSST1 - VSST24) pins should be connected to GND in common with VSSI and VSSO. They may also be left floating. The VSST pins may be electrically connected together (fused) and connected to the back of the die to improve the thermal characteristics of the package.
VSST2		2	
VSST3		3	
VSST4		38	
VSST5		39	
VSST6		40	
VSST7		41	
VSST8		42	
VSST9		43	
VSST10		78	
VSST11		79	
VSST12		80	
VSST13		81	
VSST14		82	
VSST15		83	
VSST16		118	
VSST17		119	
VSST18		120	
VSST19		121	
VSST20		122	
VSST21		123	
VSST22		158	
VSST23		159	
VSST24		160	

Notes on Pin Description:

1. All TUPP inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

2. All TUPP digital outputs and bidirectionals have 4 mA drive capability.

3. The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the TUPP.

4. The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the TUPP.

9 FUNCTIONAL DESCRIPTION

9.1 Input Bus Demultiplexer

The input bus demultiplexer captures data sampled on the DIN bus and distributes this data to the three tributary payload processors within the TUPP.

The input bus demultiplexer also provides timing signals for the other blocks within the TUPP. The system clock, SCLK, is buffered and distributed to the tributary payload processors and the output bus multiplexer. Frame alignment signals for the incoming data stream, IC1J1, ITMF, and ISPE, are sampled, buffered and distributed to the tributary payload processors (TPPs). In order to have synchronous operation of the TPPs with a single clock, the incoming data and control signals may be delayed by up to two system clock cycles before distribution to the TPP. The delay is used to align the incoming data with the outgoing data at each TPP. The amount of delay is adjusted such that the separation of the incoming STS/AU frame and the outgoing frame at each TPP appears to be in multiples of three SCLK periods.

When configured for AU4 mode, the input bus demultiplexer provides the necessary timing coordination between the three tributary payload processors. The single J1 byte marker input on IC1J1 is retimed and distributed to each of the three tributary payload processors. The tributary multiframe detected by TPP #1 is distributed to the two other TPPs, as TPP #1 is the only one receiving a valid H4 byte.

9.2 Output Bus Multiplexer

The output bus multiplexer gathers data from the three tributary payload processors within the TUPP and multiplexes this data onto the DOUT[7:0] bus. It also multiplexes signals from each tributary payload processor that mark tributary SPEs and tributary V5 bytes onto the shared OTSPE and OTV5 signals.

The output bus multiplexer also provides timing signals for other blocks within the TUPP. Frame alignment signals for the outgoing data stream, OC1J1, OSPE and OTMF, are sampled, buffered and distributed to the tributary payload processors (TPPs). The output bus multiplexer contains a four frame counter that will flywheel in the absence of an active OTMF input, internally generating tributary multiframe timing for the outgoing data stream. When configured for locked output mode, i.e. when OJ1EN is low, the output bus multiplexer will internally

generate J1 and SPE timing for the outgoing data stream that corresponds to the J1 bytes following the C1 bytes and no pointer justifications at the STS-1 (AU3) or AU4 level. This timing drives the outputs of the three tributary payload processors, substituting for the function otherwise provided by the OC1J1 and OSPE inputs.

When configured for AU4 mode, the output bus multiplexer provides the necessary timing coordination between the three tributary payload processors. This consists of deriving VC4 framing from the single J1 byte marker input on OC1J1 and distributing this to each tributary payload processor.

9.3 Tributary Payload Processor

Each tributary payload processor processes the tributaries within an STS-1, AU3, or TUG3. Each TPP can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each TPP ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or all TU11s).

9.3.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary payload processor. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary payload processor.

9.3.2 Incoming Timing Generator

The incoming timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the TPP (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The H4 byte is identified for the incoming multiframe detector so that it can determine the incoming tributary multiframe boundaries. The identification of specific tributaries allows the pointer interpreter to be time-sliced across the mix of tributaries present in the incoming data stream. The identification of the V1-V3 bytes of VTs, or TUs (or H1-H3 bytes in the case of TU3s) allows the pointer interpreter to function.

9.3.3 Incoming Multiframe Detector

The incoming multiframe detector frames to the tributary multiframe encoded into the H4 bytes. It aligns a fly-wheeling multiframe counter to the alignment indicated by the H4 bytes when confidence is achieved in the H4 bytes. A change of incoming tributary multiframe occurs when the H4 bytes cycle error free and in correct sequence for four frames, and the detected alignment is new. The incoming multiframe detector is disabled and the multiframe is indicated by the ITMF input signal, when ITMF is enabled through the ITMFEN register bit.

9.3.4 Pointer Interpreter

The pointer interpreter is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM as directed by the incoming timing generator. The pointer interpreter processes the incoming tributary pointers such that all bytes within the tributary synchronous payload envelope can be identified and written into the unique payload buffer for the tributary in question. A marker that tags the V5 byte (or J1 byte in the case of a TU3) is passed through the payload buffer. The incoming timing generator directs the pointer interpreter to the correct payload buffer for the tributary being processed. Loss of pointer status is captured in microprocessor readable registers for each tributary and interrupts can optionally be generated upon loss of pointer and pointer acquisition. The pointer interpreter detects tributary path AIS and suppresses the loss of pointer indication that would otherwise occur. The pointer interpreter passes this information to the pointer generator triggering path AIS insertion into the corresponding outgoing tributary.

The pointer generator can be configured to insert tributary path AIS into outgoing tributaries if loss of pointer is detected on the associated incoming tributary.

9.3.5 Payload Buffer

The payload buffer is a bank of FIFO buffers. It is synchronous in operation and is based on a time-sliced RAM. The three 19.44 MHz clock cycles in each 6.48 MHz period are shared between the read and write operations. The pointer interpreter writes tributary payload data and the V5 (or TU3 J1) tag into the payload buffer. A 16 byte FIFO buffer is provided for each of the (up to 28) tributaries. Address information is also passed through the payload buffer to allow FIFO fill status to be determined by the pointer generator.

9.3.6 Outgoing Timing Generator

The outgoing timing generator identifies the outgoing tributary byte being processed. Based on the configuration of the TPP , the outgoing timing generator effectively constructs the STS-1 SPE, VC3, or VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and bytes that carry specific tributaries. The identification of specific tributaries allows the pointer generator to be time-sliced across the mix of tributaries to be sourced in the outgoing data stream. The identification of the V1-V3 bytes of VTs, or TUs (H1-H3 bytes of TU3s) allows the pointer generator to function.

The sequence H4 bytes is generated by each tributary payload processor and inserted into the outgoing administrative units. The six most significant bits of H4 are set to logic 1. The sequence of the remaining two H4 bits is determined by the OTMF input when enabled or from the incoming multiframe alignment.

9.3.7 Pointer Generator

The pointer generator is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM at the address associated with the current tributary. The pointer generator fills the outgoing tributary synchronous payload envelopes with bytes read from the associated FIFO in the payload buffer for the current tributary. The pointer generator creates pointers in the V1-V3 bytes (or H1-H3 bytes in the case of TU3s) of the outgoing data stream. The marker that tags the V5 byte (or J1 byte in the case of a TU3) that is passed through the payload buffer is used to align the pointer. The outgoing timing generator directs the pointer generator to the FIFO is the payload buffer associated with the tributary being processed. The pointer generator monitors the fill levels of the payload buffers and inserts outgoing pointer justifications as necessary to avoid FIFO spillage. Normally, the pointer generator has a FIFO dead band of 4 bytes. The dead band can be collapse to one so that any incoming pointer justifications will be reflected by a corresponding outgoing justification with no attenuation. Signals are output by the pointer generator that identify outgoing V5 bytes (or J1 bytes in the case of a TU3) and the tributary synchronous payload envelopes. These facilitate tributary performance monitoring external to the TUPP. On a per tributary basis, tributary path AIS and tributary idle (unequipped) can be inserted as controlled by microprocessor accessible registers. The idle code is selectable globally for the entire VC3 or TUG3 to be all zeros or all ones. It is also possible to force an inverted new data flag on individual tributaries for the purpose of diagnosing downstream pointer processors. Tributary path AIS is automatically inserted into

outgoing tributaries if the pointer interpreter detects tributary path AIS on the corresponding incoming tributary.

9.3.8 Common Bus Interface

The common bus interface allows microprocessor access to the registers within each tributary payload processor. It is used during normal operation and also during production test. It forms part of the overall microprocessor interface of the TUPP.

9.4 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the TUPP. Tributary based normal mode registers are arranged in order of transmission; TU #1 in TUG2 #1 is the first tributary transmitted, while TU #4 in TUG2 #7 is the last. The register set is accessed as follows:

9.5 Register Memory Map

Address	Register
00H	TUPP Master Incoming Configuration
01H	TUPP Master Outgoing Configuration
02H	Input Signal Activity Monitor
03H	TUPP Master Reset and Identity
04H	Tributary Payload Processor #1 Configuration
05H	Tributary Payload Processor #2 Configuration
06H	Tributary Payload Processor #3 Configuration
07H	Tributary Payload Processor and H4 OOF Interrupt Enable
08H	Tributary Payload Processor Interrupt Status and H4 OOF Status
09H	Parity Error and H4 OOF Interrupt
0AH-1FH	Reserved
20H	TPP #1, TU3, or TU #1 in TUG2 #1, Configuration and Status

Address	Register
21H	TPP #1, TU #1 in TUG2 #2, Configuration and Status
22H	TPP #1, TU #1 in TUG2 #3, Configuration and Status
23H	TPP #1, TU #1 in TUG2 #4, Configuration and Status
24H	TPP #1, TU #1 in TUG2 #5, Configuration and Status
25H	TPP #1, TU #1 in TUG2 #6, Configuration and Status
26H	TPP #1, TU #1 in TUG2 #7, Configuration and Status
27H	TPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt
28H	TPP #1, TU #2 in TUG2 #1, Configuration and Status
29H	TPP #1, TU #2 in TUG2 #2, Configuration and Status
2AH	TPP #1, TU #2 in TUG2 #3, Configuration and Status
2BH	TPP #1, TU #2 in TUG2 #4, Configuration and Status
2CH	TPP #1, TU #2 in TUG2 #5, Configuration and Status
2DH	TPP #1, TU #2 in TUG2 #6, Configuration and Status
2EH	TPP #1, TU #2 in TUG2 #7, Configuration and Status
2FH	TPP #1, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt
30H	TPP #1, TU #3 in TUG2 #1, Configuration and Status
31H	TPP #1, TU #3 in TUG2 #2, Configuration and Status
32H	TPP #1, TU #3 in TUG2 #3, Configuration and Status
33H	TPP #1, TU #3 in TUG2 #4, Configuration and Status
34H	TPP #1, TU #3 in TUG2 #5, Configuration and Status
35H	TPP #1, TU #3 in TUG2 #6, Configuration and Status
36H	TPP #1, TU #3 in TUG2 #7, Configuration and Status
37H	TPP #1, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt
38H	TPP #1, TU #4 in TUG2 #1, Configuration and Status
39H	TPP #1, TU #4 in TUG2 #2, Configuration and Status
3AH	TPP #1, TU #4 in TUG2 #3, Configuration and Status
3BH	TPP #1, TU #4 in TUG2 #4, Configuration and Status

Address	Register
3CH	TPP #1, TU #4 in TUG2 #5, Configuration and Status
3DH	TPP #1, TU #4 in TUG2 #6, Configuration and Status
3EH	TPP #1, TU #4 in TUG2 #7, Configuration and Status
3FH	TPP #1, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt
40H-5FH	Tributary Payload Processor #2 Registers
60H-7FH	Tributary Payload Processor #3 Registers
80H	Master Test
81H-FFH	Reserved for Test

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TUPP. Normal mode registers (as opposed to test mode registers) are selected when A[7] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TUPP to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect TUPP operation unless otherwise noted.

Register 00H: Master Incoming Configuration

Bit	Type	Function	Default
Bit 7	R/W	IPE	0
Bit 6	R/W	AUTOAIS	0
Bit 5	R/W	INCISPE	0
Bit 4	R/W	INCIC1J1	0
Bit 3	R/W	IOP	0
Bit 2	R/W	ITMFH4	0
Bit 1	R/W	ITMFEN	0
Bit 0	R/W	ICONCAT	0

This register configures the TUPP functionality that are related to the incoming data stream.

ICONCAT:

When set high, the ICONCAT bit configures the incoming section of the TUPP to operate in AU4 mode. When the ICONCAT bit is set low, the incoming section operates in AU3 mode (or equivalently, STS-1 mode).

ITMFEN:

When set high, the ITMFEN bit enables the TUPP to use the ITMF input signal to locate tributary multiframe boundaries. The H4 bytes in the incoming data stream are ignored. When ITMFEN is set low, the H4 bytes are used to locate the boundaries, and the ITMF signal is ignored.

ITMFH4:

The ITMFH4 bit selects the location of the ITMF in the tributary multiframe. When ITMFH4 is set high, ITMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary multiframe. When ITMFH4 is set low, ITMF marks the V1 byte of the first tributary. ITMFH4 is ignored if ITMF is disabled by setting the ITMFEN bit low.

IOP:

The IOP bit controls the expected parity on the incoming parity signal IPAR. When IOP is set high, the parity of the parity signal set, together with IPAR is

expected to be odd. When IOP is set low, the expected parity is even. Membership of the parity signal set always includes DIN[7:0], and may include input signals IC1J1 and ISPE as controlled by the INCIC1J1 and INCISPE bits, respectively.

INCIC1J1:

The INCIC1J1 bit controls the whether the 1C1J1 input signal participates in the incoming parity calculations. When INCIC1J1 is set high, the parity signal set includes the IC1J1 input. When INCIC1J1 is set low, parity is calculated without regard to the state of IC1J1. Selection of odd or even parity is controlled by the IOP bit.

INCISPE:

The INCISPE bit controls the whether the ISPE input signal participates in the incoming parity calculations. When INCISPE is set high, the parity signal set includes the ISPE input. When INCISPE is set low, parity is calculated without regard to the state of ISPE. Selection of odd or even parity is controlled by the IOP bit.

AUTOAIS:

The AUTOAIS bit is an active high AIS insertion enable. When AUTOAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that exhibit a LOP state. When AUTOAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

IPE:

The IPE bit is an active high interrupt enable. When IPE is set high, the occurrence of a parity error on the incoming parity signal set will cause an interrupt to be asserted on the interrupt (INTB) output. When IPE is set low, incoming parity errors will not cause an interrupt.

Register 01H: Master Outgoing Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	OOP	0
Bit 2	R/W	OTMFH4	0
Bit 1	R/W	OJ1EN	0
Bit 0	R/W	OCONCAT	0

This register configures the TUPP functionality that are related to the outgoing data stream.

OCONCAT:

When set high, the OCONCAT bit configures the outgoing section of the TUPP to operate in AU4 mode. When the OCONCAT bit is set low, the outgoing section operates in AU3 mode (or equivalently, STS-1 mode).

OJ1EN:

When set high, the OJ1EN bit enables the TUPP output bus to operate in floating mode where the OC1J1 signal marks the first C1 byte and the J1 bytes in the outgoing data stream, DOUT[7:0]. The OSPE input is used to distinguish between bytes in the transport overhead and the payload envelope, and consequently C1 and J1. Only one J1 byte, and one VC or concatenated SPE, are expected to be marked when configured for AU4 mode (OCONCAT set high).

When the OJ1EN bit is low, the TUPP output bus operates in locked mode where the OC1J1 signal marks the first C1 byte only in the outgoing data stream, DOUT[7:0]. In this mode, the OSPE input must be logic zero for the C1 byte. The TUPP defaults to fixed output timing where the J1 bytes of the STS-1, AU3 or AU4 synchronous payload envelopes are assumed to immediately follow the C1 bytes.

In either floating or locked mode, the OTMF input is used to establish the transmit tributary multiframe boundaries on the outgoing data stream DOUT[7:0].

OTMFH4:

The OTMFH4 bit selects the location of the OTMF in the tributary multiframe. When OTMFH4 is set high, OTMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary multiframe. When OTMFH4 is set low, OTMF marks the V1 byte of the first tributary.

OOP:

The OOP bit controls the parity placed on the outgoing parity signal OPAR. When OOP is set low, the parity of outgoing data stream DOUT[7:0], together with OPAR is even. When OOP is set high, the parity is odd.

Register 02H: Input Signal Activity Monitor

Bit	Type	Function	Default
Bit 7	R	OTMFA	X
Bit 6	R	OSPEA	X
Bit 5	R	OC1J1A	X
Bit 4	R	DINA	X
Bit 3	R	ITMFA	X
Bit 2	R	ISPEA	X
Bit 1	R	IC1J1A	X
Bit 0	R	SCLKA	X

This register provides activity monitoring on major TUPP inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodically to detect for stuck at conditions.

SCLKA:

The SCLK active (SCLKA) bit monitors for low to high transitions on the SCLK input. SCLKA is set high on a rising edge of SCLK, and is set low when this register is read.

IC1J1A:

The IC1J1 active (IC1J1A) bit monitors for low to high transitions on the IC1J1 input. IC1J1A is set high on a rising edge of IC1J1, and is set low when this register is read.

ISPEA:

The ISPE active (ISPEA) bit monitors for low to high transitions on the ISPE input. ISPEA is set high on a rising edge of ISPE, and is set low when this register is read.

ITMFA:

The ITMF active (ITMFA) bit monitors for low to high transitions on the ITMF input. ITMFA is set high on a rising edge of ITMF, and is set low when this register is read.

DINA:

The DIN bus active (DINA) bit monitors for low to high transitions on the DIN[7:0] inputs. DINA is set high when rising edges have been observed on all the signals on the DIN[7:0] bus, and is set low when this register is read.

OC1J1A:

The OC1J1 active (OC1J1A) bit monitors for low to high transitions on the OC1J1 input. OC1J1A is set high on a rising edge of OC1J1, and is set low when this register is read.

OSPEA:

The OSPE active (OSPEA) bit monitors for low to high transitions on the OSPE input. OSPEA is set high on a rising edge of OSPE, and is set low when this register is read.

OTMFA:

The OTMF active (OTMFA) bit monitors for low to high transitions on the OTMF input. OTMFA is set high on a rising edge of OTMF, and is set low when this register is read.

Register 03H: Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision of the TUPP to be read by software permitting graceful migration to support for newer, feature enhanced versions of the TUPP, should revision of the TUPP occur. It also provides software reset capability.

ID[6:0]:

The ID bits can be read to provide a binary TUPP revision number.

RESET:

The RESET bit allows the TUPP to be reset under software control. If the RESET bit is a logic 1, the entire TUPP is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the TUPP out of reset. Holding the TUPP in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 04H: Tributary Payload Processor #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TPPEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to configure the major operational modes of tributary payload processor #1.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. When the TU3 bit is set high, the ITUG3 and OTUG3 bits should be set low. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 20H and 27H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are

disabled; data written is ignored, data read is invalid. When not in TU3 mode, register 20H reflects status and configuration of TUG2 #1, TU #1 and register 27H reflect LOP interrupt status of TU #1 in all seven TUG #2s.

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Regardless of the idle code selected, a valid pointer and a valid V5 byte that tags the tributary as unequipped is inserted. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

TPPEN:

When set high, the TPPEN bit enables the operation of tributary payload processor #1. When TPPEN is low, TPP #1 is held in a low power, reset state. The data destined for TPP #1 is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details.

Register 05H: Tributary Payload Processor #2 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TPPEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to configure the major operational modes of tributary payload processor #2.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. When the TU3 bit is set high, the ITUG3 and OTUG3 bits should be set low. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 40H and 47H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are

disabled; data written is ignored, and read data is invalid. When not in TU3 mode, register 40H reflects status and configuration of TUG2 #1, TU #1 and register 47H reflect LOP interrupt status of TU #1 in all seven TUG #2s.

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Regardless of the idle code selected, a valid pointer and a valid V5 byte that tags the tributary as unequipped is inserted. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

TPPEN:

When set high, the TPPEN bit enables the operation of tributary payload processor #2. When TPPEN is low, TPP #2 is held in a low power, reset state. The data destined for TPP #2 is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details.

Register 06H: Tributary Payload Processor #3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TPPEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to configure the major operational modes of tributary payload processor #3.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. When the TU3 bit is set high, the ITUG3 and OTUG3 bits should be set low. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 60H and 67H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are

disabled; data written is ignored and read data is invalid. When not in TU3 mode, register 60H reflects status and configuration of TUG2 #1, TU #1 and register 67H reflect LOP interrupt status of TU #1 in all seven TUG #2s.

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Regardless of the idle code selected, a valid pointer and a valid V5 byte that tags the tributary as unequipped is inserted. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

TPPEN:

When set high, the TPPEN bit enables the operation of tributary payload processor #3. When TPPEN is low, TPP #3 is held in a low power, reset state. The data destined for TPP #3 is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details.

Register 07H: TPP and H4 OOF Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	OOF3E	0
Bit 4	R/W	OOF2E	0
Bit 3	R/W	OOF1E	0
Bit 2	R/W	TPP3E	0
Bit 1	R/W	TPP2E	0
Bit 0	R/W	TPP1E	0

This register provides interrupt enable of the three H4 byte framers and of the three tributary payload processors in the TUPP.

TPP1E:

TPP1E is the interrupt enable bit for tributary payload processor #1 in the TUPP. Interrupts enabled at tributary processor #1 but masked by TPP1E will still be reported by the TPP1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #1 will not be reported by the TPP1I bit.

TPP2E:

TPP2E is the interrupt enable bit for tributary processor #2 in the TUPP. Interrupts enabled at tributary payload processor #2 but masked by TPP2E will still be reported by the TPP2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #2 will not be reported by the TPP2I bit.

TPP3E:

TPP3E is the interrupt enable bit for tributary payload processor #3 in the TUPP. Interrupts enabled at tributary processor #3 but masked by TPP3E will still be reported by the TPP3I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #3 will not be reported by the TPP3I bit.

OOF1E:

The OOF1E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #1. When OOF1E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when OOFE is set low.

OOF2E:

The OOF2E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #2. When OOF2E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when OOFE is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

OOF3E:

The OOF3E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #3. When OOF3E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when OOFE is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

Register 08H: TPP Interrupt Status and H4 OOF Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	OOF3V	0
Bit 4	R	OOF2V	0
Bit 3	R	OOF1V	0
Bit 2	R	TPP3I	0
Bit 1	R	TPP2I	0
Bit 0	R	TPP1I	0

This register provides interrupt status of the three H4 byte framers and of the three tributary payload processors in the TUPP.

TPP1I:

TPP1I identifies tributary payload processor #1 as the source of a pending interrupt. It is necessary to read the LOP Interrupt Status registers in tributary processor #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #1 will not be reported by the TPP1I bit.

TPP2I:

TPP2I identifies tributary payload processor #2 as the source of a pending interrupt. It is necessary to read the LOP Interrupt Status registers in tributary processor #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #2 will not be reported by the TPP2I bit.

TPP3I:

TPP1I identifies tributary payload processor #3 as the source of a pending interrupt. It is necessary to read the LOP Interrupt Status registers in tributary processor #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #3 will not be reported by the TPP3I bit.

OOF1V:

The OOF1V bit indicates the status of the H4 byte framer in tributary payload processor #1. OOF1V is set high when the H4 framer goes out of frame and is set low when it re-acquires frame.

OOF2V:

The OOF2V bit indicates the status of the H4 byte framer in tributary payload processor #2. OOF2V is set high when the H4 framer goes out of frame and is set low when it re-acquires frame. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

OOF3V:

The OOF3V bit indicates the status of the H4 byte framer in tributary payload processor #3. OOF3V is set high when the H4 framer goes out of frame and is set low when it re-acquires frame. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

Register 09H: Parity Error and H4 OOF Interrupt

Bit	Type	Function	Default
Bit 7	R	IPI	0
Bit 6		Unused	X
Bit 5	R	OOF3I	0
Bit 4	R	OOF2I	0
Bit 3	RF	OOF1I	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides interrupt status of the H4 byte framers in the three tributary payload processor and of the input parity checker in the TUPP.

OOF1I:

The OOF1I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #1 goes out of frame and when it re-acquires frame. The OOF1I bit is set high when an out of frame event occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The OOFI bit remains valid when interrupts are not enabled (OOF1E set low) and may be polled to detect out of frame events.

OOF2I:

The OOF2I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #2 goes out of frame and when it re-acquires frame. The OOF2I bit is set high when an out of frame event occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The OOF2I bit remains valid when interrupts are not enabled (OOF2E set low) and may be polled to detect out of frame events.

OOF3I:

The OOF3I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #2 goes out

of frame and when it re-acquires frame. The OOF3I bit is set high when an out of frame event occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The OOF3I bit remains valid when interrupts are not enabled (OOF3E set low) and may be polled to detect out of frame events.

IPI:

The incoming parity error interrupt bit (IPI) is set high when a parity error is detected on the incoming parity signal set. If the IPE bit in the master incoming configuration register is set high, the interrupt output (INTB) is activated. When this register is read, IPI (and the corresponding interrupt) is cleared.

Register 20H, 40H, 60H: TU3, or TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

In TU3 mode (TU3 bit in TPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the TPP. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in TUG2 #1 or TU3 depending on whether the TPP is in TU3 mode. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has precedence over the IIDLE and the DLOP bits.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #1 in TUG2 #1 or TU3 depending on whether the TPP is in TU3 mode. Tributary idle is inserted with the idle code in the tributary bytes, except for a valid pointer and a valid V5 byte that tags the tributary as unequipped. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labelled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has no effect when the IPAIS bit is set high.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in TUG2 #1 or TU3 depending on

whether the TPP is in TU3 mode, is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

LOPE:

The LOPE bit enables loss of pointer interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the TPP is in TU3 mode. When LOPE is set high, an interrupt is generated upon loss of pointer and upon re-acquisition. Interrupts due to LOP status change are masked when LOPE is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the TPP is in TU3 mode.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in TUG2 #1 or TU3 depending on whether the TPP is in TU3 mode. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 21H-26H, 41H-46H, 61H-66H: TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has precedence over the IIDLE and the DLOP bits.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #1 in the corresponding TUG2. Tributary idle is inserted with the idle code in the tributary bytes, except for a valid pointer and a valid V5 byte that tags the tributary as unequipped. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has no effect when the IPAIS bit is set high.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with

the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

LOPE:

The LOPE bit enables loss of pointer interrupts for tributary TU #1 in the corresponding TUG2. When LOPE is set high, an interrupt is generated upon loss of pointer and upon re-acquisition. Interrupts due to LOP status changes are masked when LOPE is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the TUG2 tributary group. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 27H, 47H, 67H: TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 TO TUG2 #7. It is also used to identify and acknowledge TU3 loss of pointer interrupts.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. In TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of the TU3 pointer. Out of TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set high when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (LOPE set low) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts

are not enabled (LOPE set low) and may be polled to detect loss of pointer events.

ACCEL:

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Register 28H-2EH, 48H-4EH, 68H-6EH: TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has precedence over the IIDLE and the DLOP bits.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #2 in the corresponding TUG2. Tributary idle is inserted with the idle code in the tributary bytes, except for a valid pointer and a valid V5 byte that tags the tributary as unequipped. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has no effect when the IPAIS bit is set high.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

LOPE:

The LOPE bit enables loss of pointer interrupts for tributary TU #2 in the corresponding TUG2. When LOPE is set high, an interrupt is generated upon loss of pointer and upon re-acquisition. Interrupts due to LOP status change are masked when LOPE is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 2FH, 4FH, 6FH: TU #2 in TUG2 #1 to TUG2 #7

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 TO TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (LOPE set low) and may be polled to detect loss of pointer events.

Register 30H-36H, 50H-56H, 70H-76H: TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has precedence over the IIDLE and the DLOP bits.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #3 in the corresponding TUG2. Tributary idle is inserted with the idle code in the tributary bytes, except for a valid pointer and a valid V5 byte that tags the tributary as unequipped. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has no effect when the IPAIS bit is set high.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

LOPE:

The LOPE bit enables loss of pointer interrupts for tributary TU #3 in the corresponding TUG2. When LOPE is set high, an interrupt is generated upon loss of pointer and upon re-acquisition. Interrupts due to LOP status change are masked when LOPE is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 37H, 57H, 77H: TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 TO TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (LOPE set low) and may be polled to detect loss of pointer events.

Register 38H-3EH, 58H-5EH, 78H-7EH: TU #4 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or, TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has precedence over the IIDLE and the DLOP bits.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #4 in the corresponding TUG2. Tributary idle is inserted with the idle code in the tributary bytes, except for a valid pointer and a valid V5 byte that tags the tributary as unequipped. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. The IIDLE bit has no effect when the IPAIS bit is set high.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is

inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

LOPE:

The LOPE bit enables loss of pointer interrupts for tributary TU #4 in the corresponding TUG2. When LOPE is set high, an interrupt is generated upon loss of pointer and upon re-acquisition. Interrupts due to LOP status changes are masked when LOPE is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 3FH, 5FH, 7FH: TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3, or TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (LOPE set low) and may be polled to detect loss of pointer events.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs when the MBEB input is negated (low), causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TUPP. Test mode registers (as opposed to normal mode registers) are selected when A[7] is high.

Test mode registers may also be used for board testing. When all of the tributary payload processors within the TUPP are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Table 1 - Test Mode Register Memory Map

Address	Register
00H-7FH	Normal Mode Registers
80H	Master Test
81H-9FH	Reserved
A0H	TPP #1 Test Register 0
A1H	TPP #1 Test Register 1
A2H	TPP #1 Test Register 2
A3H	TPP #1 Test Register 3
A4H-BFH	Reserved
C0H	TPP #2 Test Register 0
C1H	TPP #2 Test Register 1
C2H	TPP #2 Test Register 2
C3H	TPP #2 Test Register 3
C4H-DFH	Reserved
E0H	TPP #3 Test Register 0
E1H	TPP #3 Test Register 1

Address	Register
E2H	TPP #3 Test Register 2
E3H	TPP #3 Test Register 3
E4H-FFH	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 80H: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	MOTOTST	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable TUPP test features. All bits, except PMCTST, are reset to zero by a reset of the TUPP.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the TUPP . While the HIZIO bit is a logic 1, all output pins of the TUPP except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the TUPP for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

MOTOTST:

The MOTOTST bit is used to test the decoding of the RDB_E and WRB_RWB control signals when MBEB is logic 0.

PMCTST:

The PMCTST bit is used to configure the TUPP for PMC's manufacturing tests. When PMCTST is set to logic 1, the TUPP microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

11.1 I/O Test Mode

In I/O test mode, the TUPP allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable I/O test mode, the IOTST bit in the Master Test register is set to logic 1.

Reading the following address locations returns the values for the indicated inputs :

Table 2 - I/O Test Mode — Input Read Register Description

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H82	X	X	X	X	X	OTMF	OC1J1	OSPE
H83	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
H84	X	X	X	SCLK	ITMF	ISPE	IC1J1	IPAR

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 3 - I/O Test Mode — Output Write Register Description

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H81	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0
H82	0	0	0	0	INTB	OTV5	OTSPE	OPAR

12 OPERATION

12.1 Configuration Options

The TUPP consists of three tributary payload processors or TPPs. Each TPP deals with a portion of the SONET frame that corresponds to an STS-1 SPE. Equivalently, each TPP deals with a portion of the SDH frame that corresponds to a VC3 together with the 2 columns of fixed stuff that are added when mapping a VC3 into an AU3. By coordinating the operation of the three TPPs, they can process the portion of an SDH frame that corresponds to a VC4. The coordination that may be required between the three TPPs relates to the J1 byte marker and the encoding of the tributary multiframe into the H4 byte. When processing a VC4 that carries three TUG3s, the alignment provided by the J1 byte marker and the H4 byte of the VC4 must be distributed to all TPPs. When processing STS-1 SPEs, or equivalently, VC3s carried within AU3s, each TPP receives its own J1 byte marker and H4 byte. Coordination is accomplished as follows: The tributary multiframe alignment that is detected by TPP #1 is distributed to the two other TPPs as they are not receiving H4 bytes. In addition, the input demultiplexer will stretch the pulse captured on the IC1J1 input that marks the VC4 J1 byte so that it marks the next two bytes. During the demultiplexing process this effectively feeds a "J1" marker to the two "slaved" TPPs.

The modes of operation of the TUPP are summarized as follows:

STS-1 Mode

This is default. Each STS-1 is assumed to carry seven VT groups, each of which can be independently configured to carry VT1.5s, VT2s, VT3s, or VT6s. The IC1J1 input is expected to mark the J1 byte of each STS-1 SPE and each TPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

AU3 Mode

This is also the default, as is corresponds exactly to STS-1 mode, except for nomenclature. Each AU3 is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) The IC1J1 input is expected to mark the J1 byte of each VC3 and each TPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

AU4 Mode

This mode is enabled when the ICONCAT and OCONCAT bits are set high. In AU4 mode, individual TPPs must be configured in either TUG3 mode or TU3 mode. The IC1J1 input is expected to mark the J1 byte of the VC4. This J1 marker is stretched to provide a "J1" marker to each TPP. TPP #2 and TPP#3 are slaved to the tributary multiframe indication provided by TPP #1 as it is the only one that receives a valid H4 byte.

TUG3 Mode

This mode is enabled when the TUG3 bit is set high in a TPP. In addition, the ICONCAT and OCONCAT bits must be set high for the TUPP. The TUG3 processed by the TPP is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) When the TUPP is in AU4 mode, each TPP can be independently configured in TUG3 or TU3 mode.

TU3 Mode

This mode is enabled when the TU3 bit is set high in a TPP. In addition the ICONCAT and OCONCAT bits must be set high for the TUPP. The TUG3 processed by the TPP is assumed to carry a TU3. When the TUPP is in AU4 mode, each TPP can be independently configured in TUG3 or TU3 mode.

For figures in the operation and functional timing sections (Figure 4 to Figure 15), transport overhead and path overhead bytes are shown for notational convenience only. In the incoming direction, except for the H4 byte, DIN[7:0] does not need to contain valid transport and STS/AU path overhead byte values. The H4 byte must be valid only if H4 framing is enabled (ITMFEN=0). Otherwise, it too may be invalid. However, the incoming parity must match the data supplied at all times. In the outgoing direction, TUPP places random data on DOUT[7:0] for transport overhead bytes. It generates all zero bytes for the STS/AU path overhead except for the H4 byte which contains leading ones and an incrementing two bit pattern. The fixed stuff bytes in the tributary mapping to the synchronous payload envelope (virtual container) are also generated as all zero bytes. The outgoing parity reflects the data on DOUT[7:0] at all times.

12.2 STS-1 Mode

An example of the placement of tributaries assumed in STS-1 mode is illustrated in Figure 4. For simplicity, this figure shows the frame on the DOUT[7:0] bus when OJ1EN is low. In this case the outgoing STS-1 SPEs are locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the first frame of the tributary multiframe when the V1 bytes are present. This example illustrates a VT structured STS-1 SPE where all VT groups are configured to carry VT1.5s. The more general case where OJ1EN is high would be similar, except that the STS-1 SPE would be floating within the transport envelope frame.

Figure 4 - SONET STS-3 Carrying VT1.5 Within STS-1

COL / ROW	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	...	265	266	267	268	269	270
1	A1	A1	A1	A2	A2	A2	C1	C1	C1	J1	J1	J1	V1	V1	V1		SPE	SPE	SPE	SPE	SPE	SPE
2	B1	-	-	E1	-	-	F1	-	-	B3	B3	B3	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
3	D1	-	-	D2	-	-	D3	-	-	C2	C2	C2	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
4	H1	H1	H1	H2	H2	H2	H3	H3	H3	G1	G1	G1	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
5	B2	B2	B2	K1	-	-	K2	-	-	F2	F2	F2	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
6	D4	-	-	D5	-	-	D6	-	-	H4	H4	H4	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
7	D7	-	-	D8	-	-	D9	-	-	Z3	Z3	Z3	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
8	D10	-	-	D11	-	-	D12	-	-	Z4	Z4	Z4	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE
9	Z1	-	-	Z2	-	-	E2	-	-	Z5	Z5	Z5	SPE	SPE	SPE		SPE	SPE	SPE	SPE	SPE	SPE

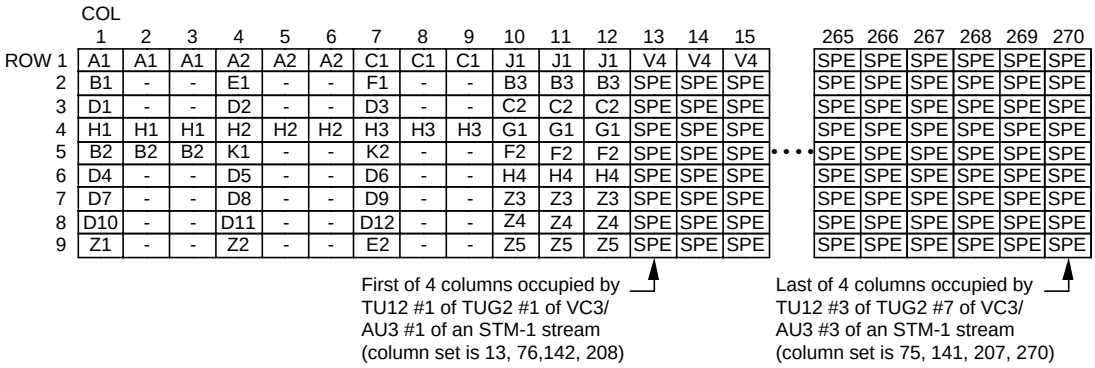
First of 3 columns occupied by VT1.5 #1 of VT group #1 of STS-1 #1 of an STS-3 stream (column set is 13, 100, 187)

Last of 3 columns occupied by VT1.5 #4 of VT group #7 of STS-1 #3 of an STS-3 stream (column set is 96, 183, 270)

12.3 AU3 Mode

An example of the placement of tributaries assumed in AU3 mode is illustrated in Figure 5. For simplicity, this figure shows the frame on the DOUT[7:0] bus when OJ1EN is low. In this case the outgoing VC3s are locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates the case where the VC3s carry TUG2s and all TUG2s are configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC3s would be floating within the transport envelope frame.

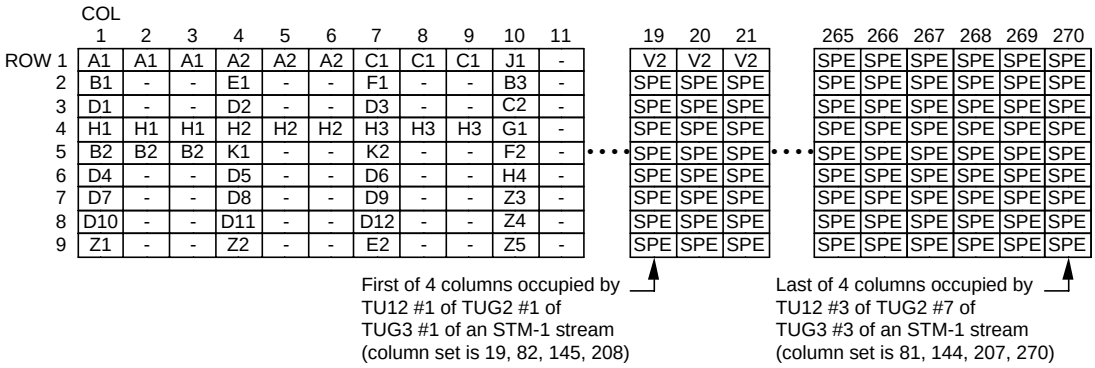
Figure 5 - SDH STM-1 Carrying TU12 Within VC3/AU3



12.4 AU4 Mode

An example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 6. For simplicity, this figure shows the frame on the DOUT[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the second frame of the tributary multiframe when the V2 bytes are present. This example illustrates a case where the VC4 carries TUG3s, all TUG3s carry TUG2s, and all TUG2s are configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

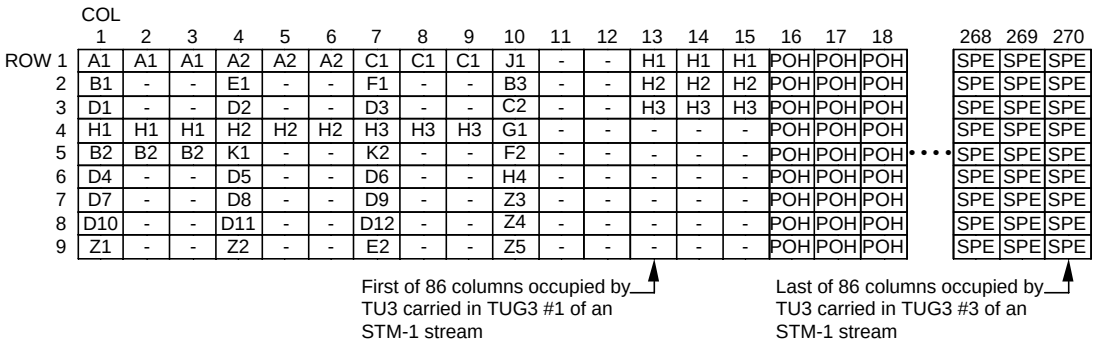
Figure 6 - SDH STM-1 Carrying TU12 Within TUG3/AU4



Another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 7. For simplicity, this figure shows the frame on the

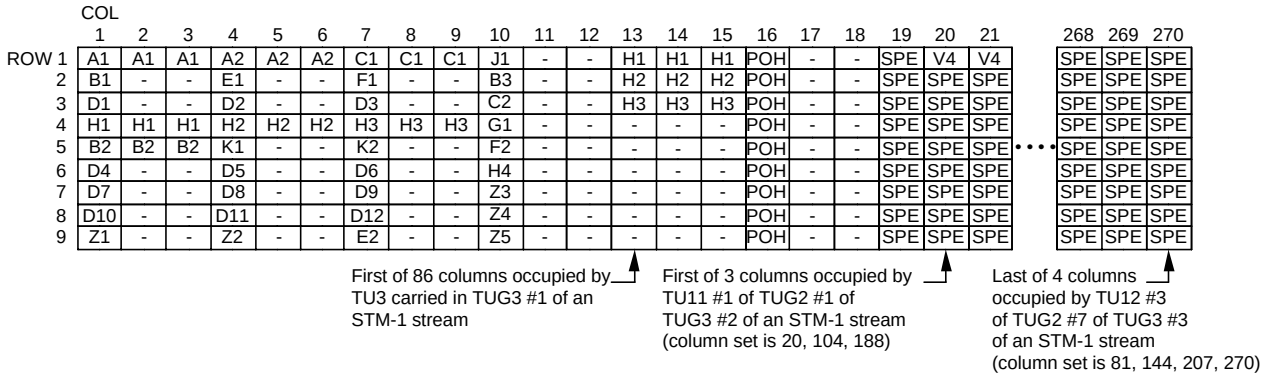
DOUT[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This example illustrates the case where the VC4 carries TUG3s that are all configured to carry TU3s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

Figure 7 - SDH STM-1 Carrying TU3 Within TUG3



Yet another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 8. For simplicity, this figure shows the frame on the DOUT[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates a complex case where the VC4 carries TUG3s and where TUG3 #1 carries a TU3, TUG3 #2 carries TUG2s that are all configured to carry TU11s, and TUG3 #3 carries TUG2s that are all configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

Figure 8 - SDH STM-1 Carrying Mix Of TU11, TU12, TU3 Within TUG3/AU4



In Figure 8 above, the H1 to H3 byte in column 13 form the TU3 offset pointer. The H1 to H3 bytes in columns 14 and 15 are null pointer indications (NPI) for TUG3 #2 and #3.

13 FUNCTIONAL TIMING

The timing of the TUPP input signals is illustrated in Figure 9. This diagram shows a simple STS-3 case that outlines the function of the various input signals. Data on DIN[7:0] is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the ISPE signal being set high. The IC1J1 signal pulses high while ISPE is low to mark the position of the first C1 byte in the STS-3 transport envelope. The IC1J1 signal is set high for three SCLK periods while ISPE is also set high to mark the J1 bytes of each STS-1 SPE. The ITMF signal is selectable to mark the V1 byte of the first tributary in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the last H4 byte of the tributary multiframe in STS-1 #1 and STS-1 #3. The H4 byte in STS-1 #2, as shown, is not last in the tributary multiframe. In this simple example, all STS-1 SPEs are aligned to the STS-3 transport envelope such that the J1 bytes directly follow the C1 bytes and no STS-1 pointer justification events are occurring.

This same diagram applies for the AU3 mode as it is equivalent to the STS-1 mode, except for nomenclature.

Figure 9 - Input Bus Timing - Simple STS-1/AU3 Case

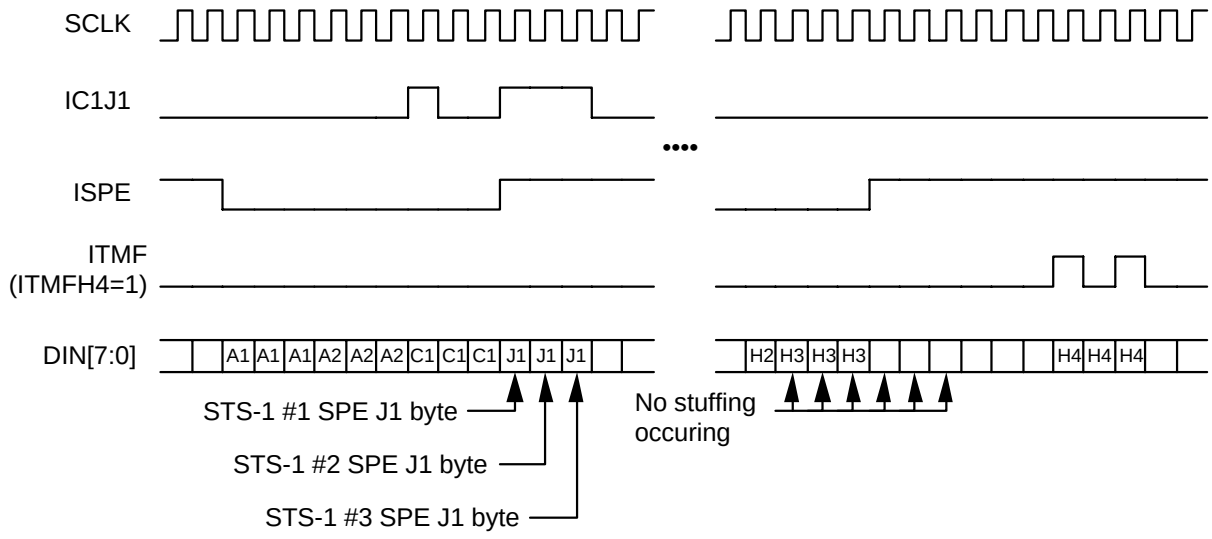


Figure 10 shows a more complex STS-3 case that illustrates the flexibility provided by the various input signals. Data on DIN[7:0] is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the ISPE signal being set high. This example shows a negative stuff event occurring on STS-1 #2 and a positive stuff event occurring on STS-1 #3. The IC1J1 signal pulses high while ISPE is low to mark the position of the C1 byte of STS-1 #1. The IC1J1 signal pulses high again to mark the J1 byte of each of the three STS-1 SPEs. The ITMF signal is selectable to mark the V1 byte of the first tributary in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the V1 byte of the first tributary multiframe in STS-1 #2. The three STS-1 SPEs are shown to have different alignments to the STS-3 transport envelope and the alignment is changing for two of the STS-1 SPEs (STS-1 #2 and #3) due to the pointer justification events shown.

Again, this same diagram would apply for AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

Figure 10 - Input Bus Timing - Complex STS-1 / AU3 Case

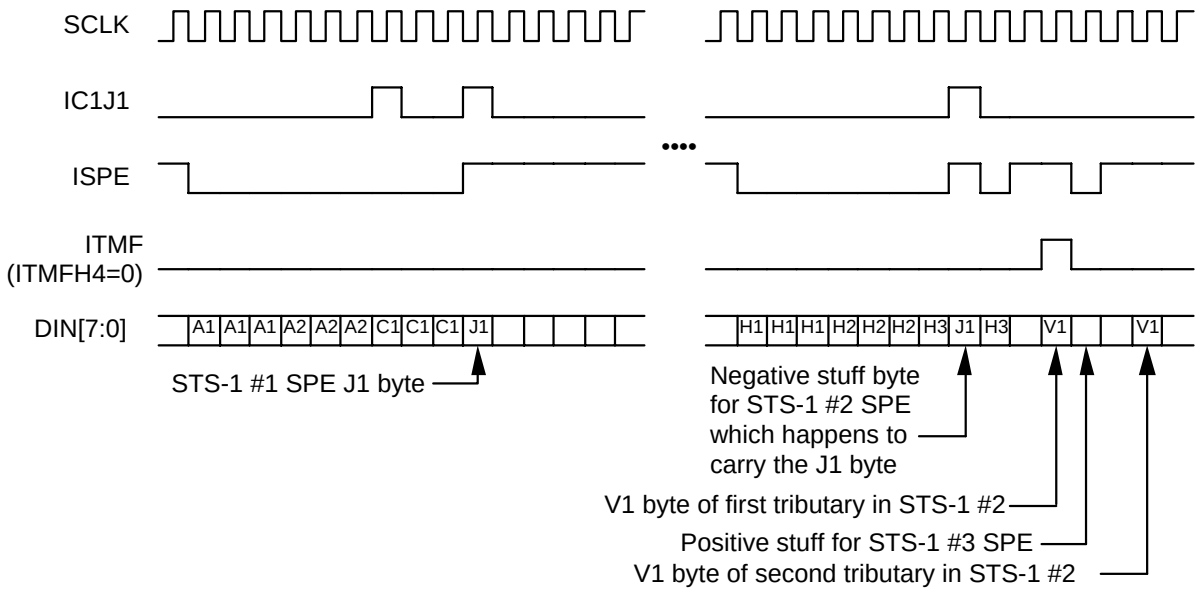
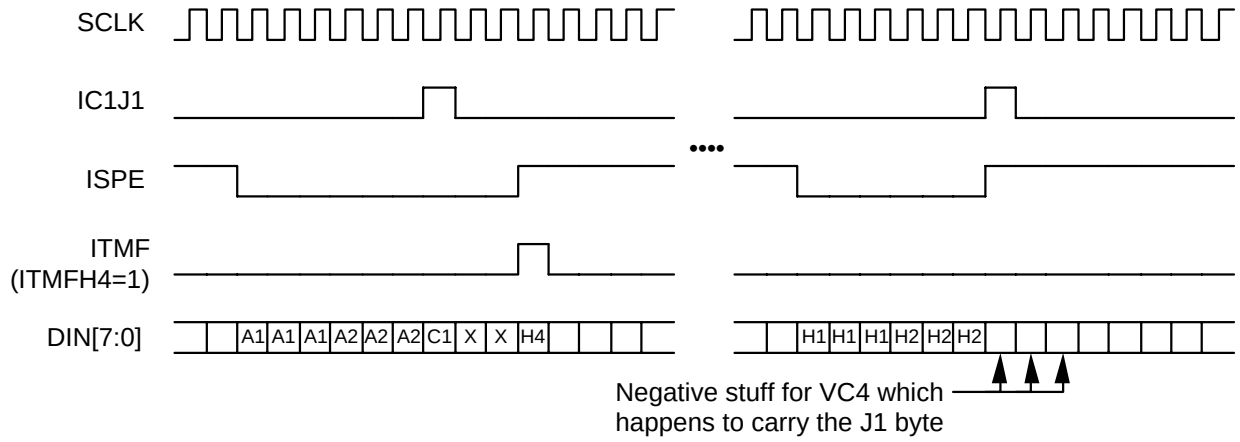


Figure 11 shows timing relationships of the various input signals in the AU4 mode. Data on DIN[7:0] is sampled on the rising edge of SCLK. The bytes forming the AU4 virtual container are identified by the ISPE signal being set high. This example shows a negative stuff occurring for the VC4. The IC1J1 signal

pulses high while ISPE is set low to mark the position of the single C1 byte in the STM-1 transport envelope. The ITMF signal is selectable to mark the V1 byte of the first tributary, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the final H4 byte of the tributary multiframe. The IC1J1 signal pulses high to mark the single J1 byte of the VC4.

This diagram applies when the TUPP is in AU4 mode, regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode.

Figure 11 - Input Bus Timing - AU4 Case



The timing of the TUPP output bus is illustrated in Figure 12. This diagram shows the relationships of the output signals in locked STS-1 mode. Data on DOUT[7:0] is updated on the rising edge of SCLK, and the OSPE input must be logic 0. The OC1J1 signal pulses high to mark the position of the C1 byte of the first STS-1 stream in every frame of the STS-3 transport envelope. In locked STS-1 mode, the position of the J1 bytes and the STS-1 SPEs is implicitly defined by the C1 byte position. All three STS-1 SPEs are defined to be aligned to the STS-3 transport envelope such that the J1 bytes immediately follow the C1 bytes and no STS-1 pointer justification events are possible. The OTMF input marks the frame containing V1 bytes. It is sampled only at the first V1 byte position of the first STS-1 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTSPE signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributary.

This same diagram would apply for AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

Figure 12 - Output Bus Timing - Locked STS-1 SPEs / AU3 VCs Case

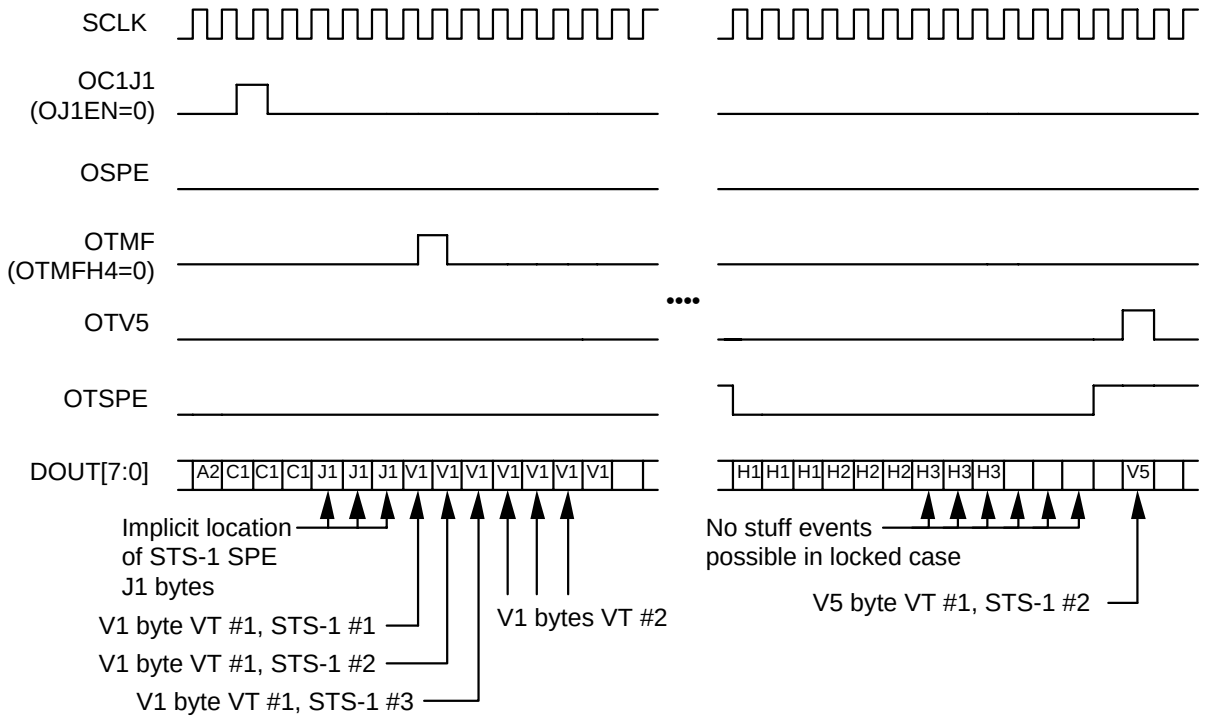
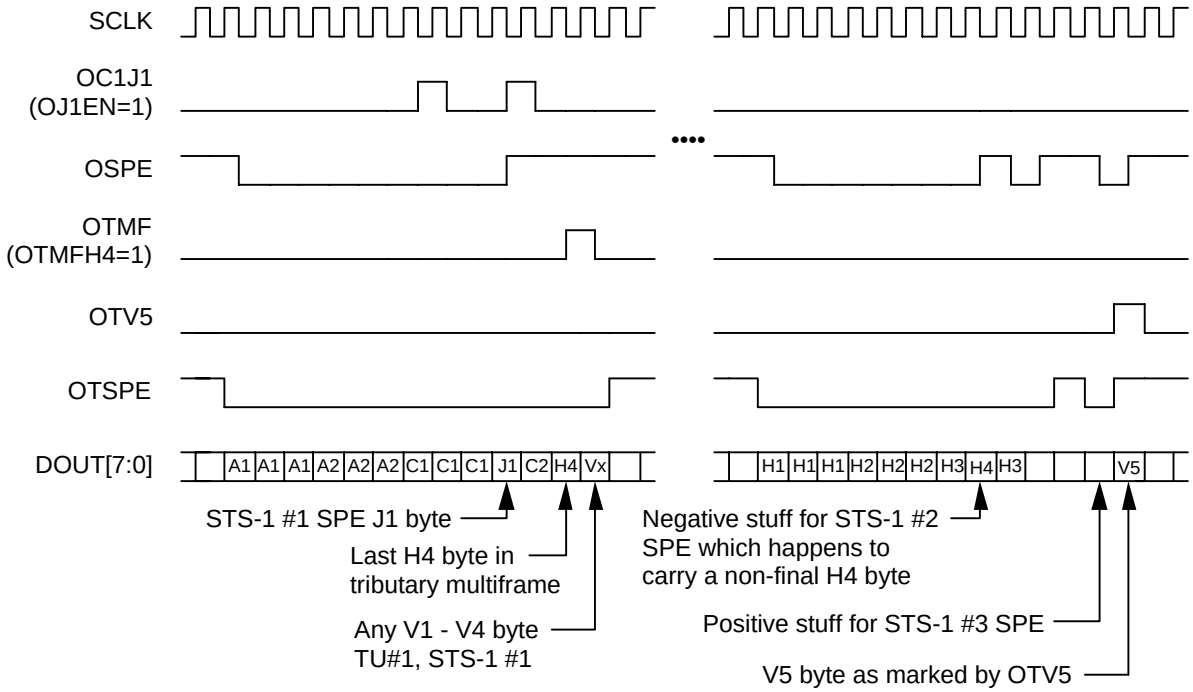


Figure 13 shows the function of the various output signals in floating STS-1 mode. Data on DOUT[7:0] is updated on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the setting the OSPE signal high. In this diagram, a negative stuff event is shown occurring on STS-1 #2 and a positive stuff event on STS-1 #3. The OC1J1 signal pulses high, while OSPE is set low, to mark the C1 byte of the first STS-1 in every frame of the STS-3 transport envelope. The OC1J1 signal is set high to mark every J1 byte of each of the three STS-1 SPEs. The OTMF input is selectable to mark the V1 byte of the first tributary in each STS-1 SPE, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, OTMF is shown to be marking the last H4 byte of the tributary multiframe in STS-1 #1. The bytes forming the various tributary synchronous payload envelopes are identified by the OTSPE signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributaries. The three STS-1 SPEs each have different alignments to the STS-3 transport envelope and the alignment is

changing for two of the STS-1 SPEs (STS-1 #2 and #3) due to the pointer justification events shown.

The same diagram applies for AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

Figure 13 - Output Bus Timing - Floating STS-1 SPEs / AU3 VCs Case



The timing of the TUPP output signals in locked and floating AU4 modes is illustrated in Figure 14 and Figure 15, respectively. The operation of the various signals is analogous to the locked and floating STS-1 modes, except that there is only a single J1 byte and all pointer justification events must involve a group of three stuff bytes. These diagrams apply when the TUPP is in AU4 mode, regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode.

Figure 14 shows the case of the TUPP operating in locked AU4 mode. Data on DOUT[7:0] is updated on the rising edge of SCLK, and the OSPE input must be logic 0. The OC1J1 signal pulses high to mark the position of the single C1 byte in every frame of the AU4 transport envelope. In locked AU4 mode, the position of the single J1 byte and the VC4 is implicitly defined by the C1 byte position.

The VC4 is defined to be aligned to the AU4 transport envelope such that the J1 byte occupies the first available payload byte after the C1 byte, and no pointer justification events are possible. The OTMF input marks the frame containing V1 bytes. It is sampled only at the J1 plus one byte position of the first TUG3 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTSPE signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributary.

Figure 14 - Output Bus Timing - Locked AU4 VC Case

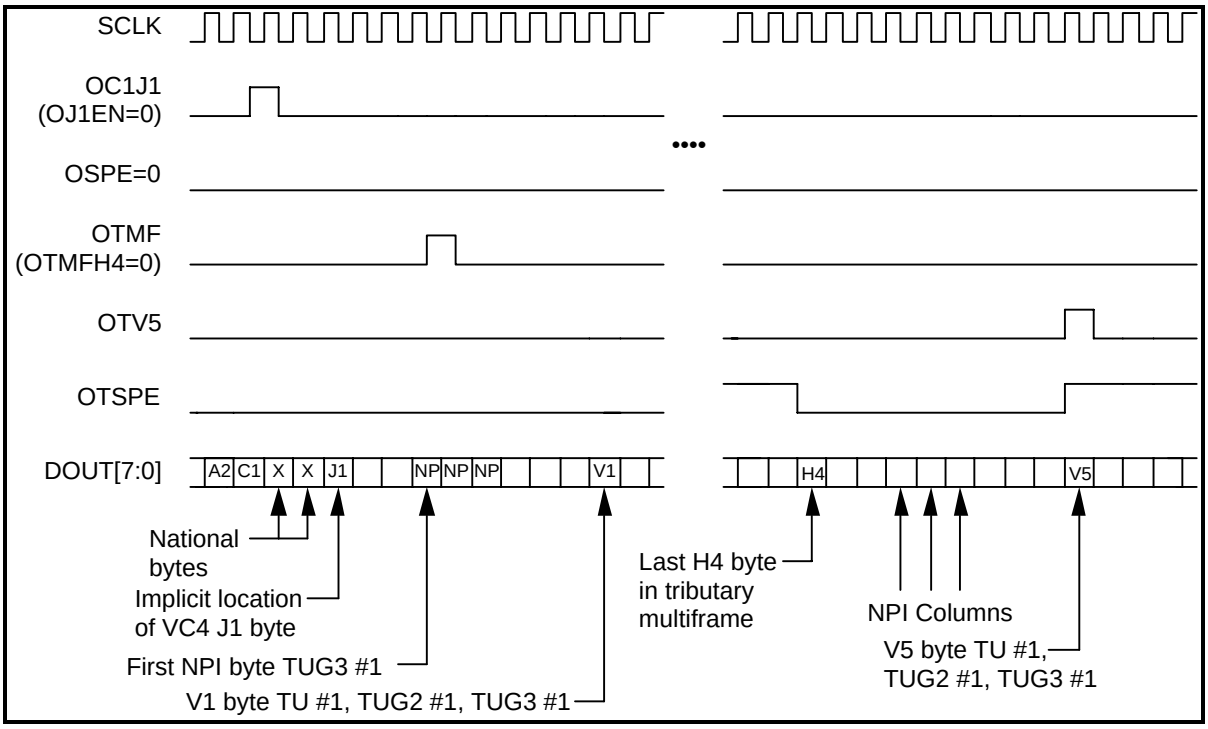
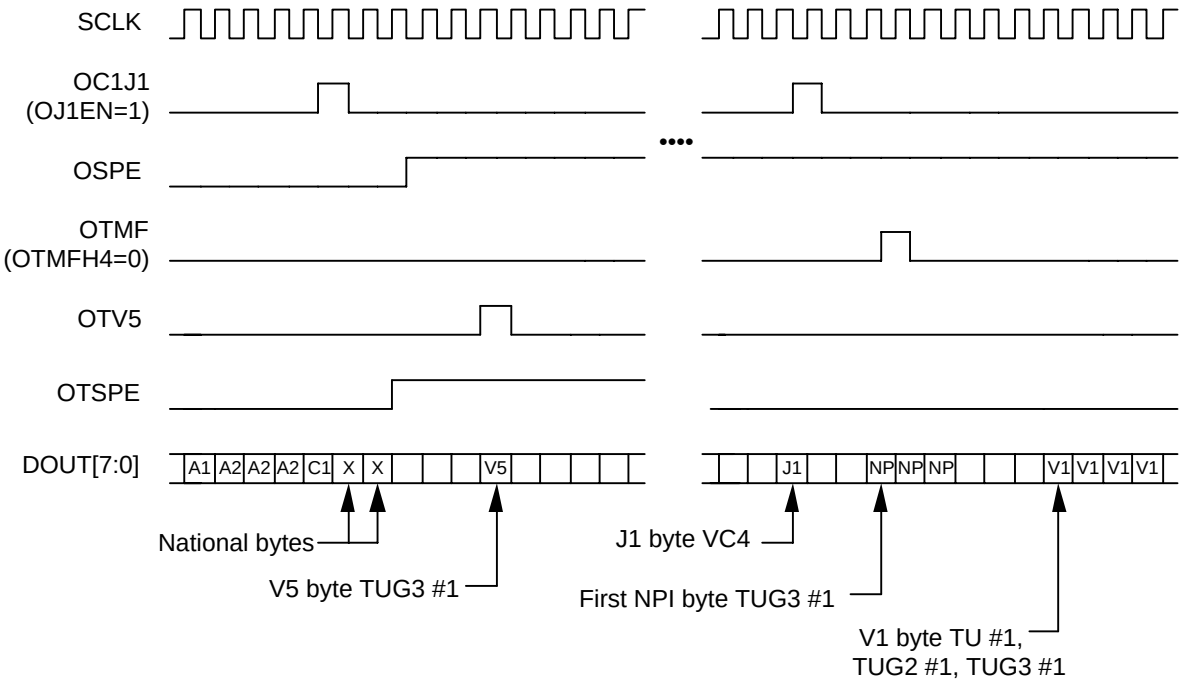


Figure 15 shows the function of the various output signals in floating AU4 mode. Data on DOUT[7:0] is updated on the rising edge of SCLK. The bytes forming the VC4 virtual container are identified by the setting the OSPE signal high. The OC1J1 signal pulses high, while OSPE is set low, to mark the single C1 byte in every frame of the AU4 transport envelope. The OC1J1 signal is set high again with OSPE high to mark the J1 byte of the VC4. The OTMF input is selectable to mark the V1 byte of the first tributary in the VC4, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, OTMF is shown to be marking the first V1 byte. The bytes forming the various tributary synchronous

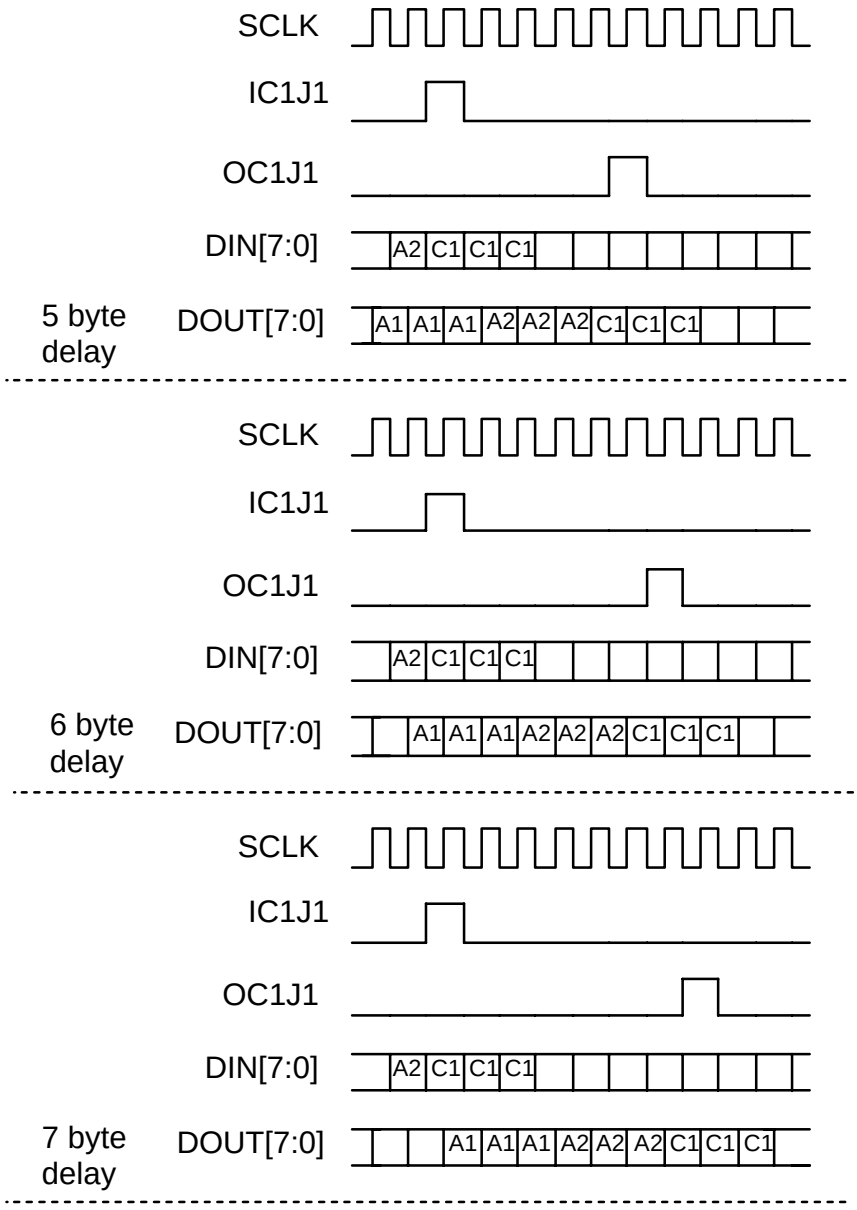
payload envelopes are identified by the OTSPE signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributaries.

Figure 15 - Output Bus Timing - Floating AU4 VC Case



The three tributary payload processor may be individually disabled. Incoming data destined to a disabled processor is re-transmitted unchanged to the outgoing data after some delay. The amount of delay is dependent on the relative phase of the incoming frame pulse (IC1J1) and the outgoing frame pulse (OC1J1). Figure 16 shows the delay for the three possible alignments of IC1J1 in relation to OC1J1. The delay from the rising edge of SCLK where TUPP samples DIN[7:0] to the rising edge of SCLK where a downstream device samples DOUT[7:0] is 5, 6, or 7 cycles.

Figure 16 - By-passed Mode Functional Timing



14 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 4 - D.C. Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OH} = 4 mA, Note 3
V_{T+}	Reset Input High Voltage		3.5	Volts	
V_{T-}	Reset Input Low Voltage	1.0		Volts	
V_{TH}	Reset Input Hysteresis Voltage			Volts	Typically 0.65V
I_{ILPU}	Input Low Current	+20	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	µA	V_{IH} = V_{DD}, Notes 1, 3
I_{ILPD}	Input Low Current	0	+10	µA	V_{IL} = GND, Notes 4, 3
I_{IHPD}	Input High Current	-200	-20	µA	V_{IH} = V_{DD}, Notes 4, 3
I_{IL}	Input Low Current	0	+10	µA	V_{IL} = GND, Notes 2, 3

Symbol	Parameter	Min	Max	Units	Conditions
I_{IH}	Input High Current	-10	0	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5	pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5	pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5	pF	Excluding Package, Package Typically 2 pF
I_{DDOP1}	Operating Current Processing Tributaries		180	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Processing Tributaries
I_{DDOP2}	Operating Current Tributary Processors Bypassed		60	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Tributary Processors Bypassed
I_{DDSB}	Standby Current		100	uA	V_{DD} = 5.5 V, Outputs Unloaded, No Clocks

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.

16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 5 - Microprocessor Interface Read Access (Figure 17, Figure 18)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{RWB}	RWB to Valid Read Set-up Time	25		ns
tH_{RWB}	RWB to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 17 - Microprocessor Interface Read Timing (Intel Mode)

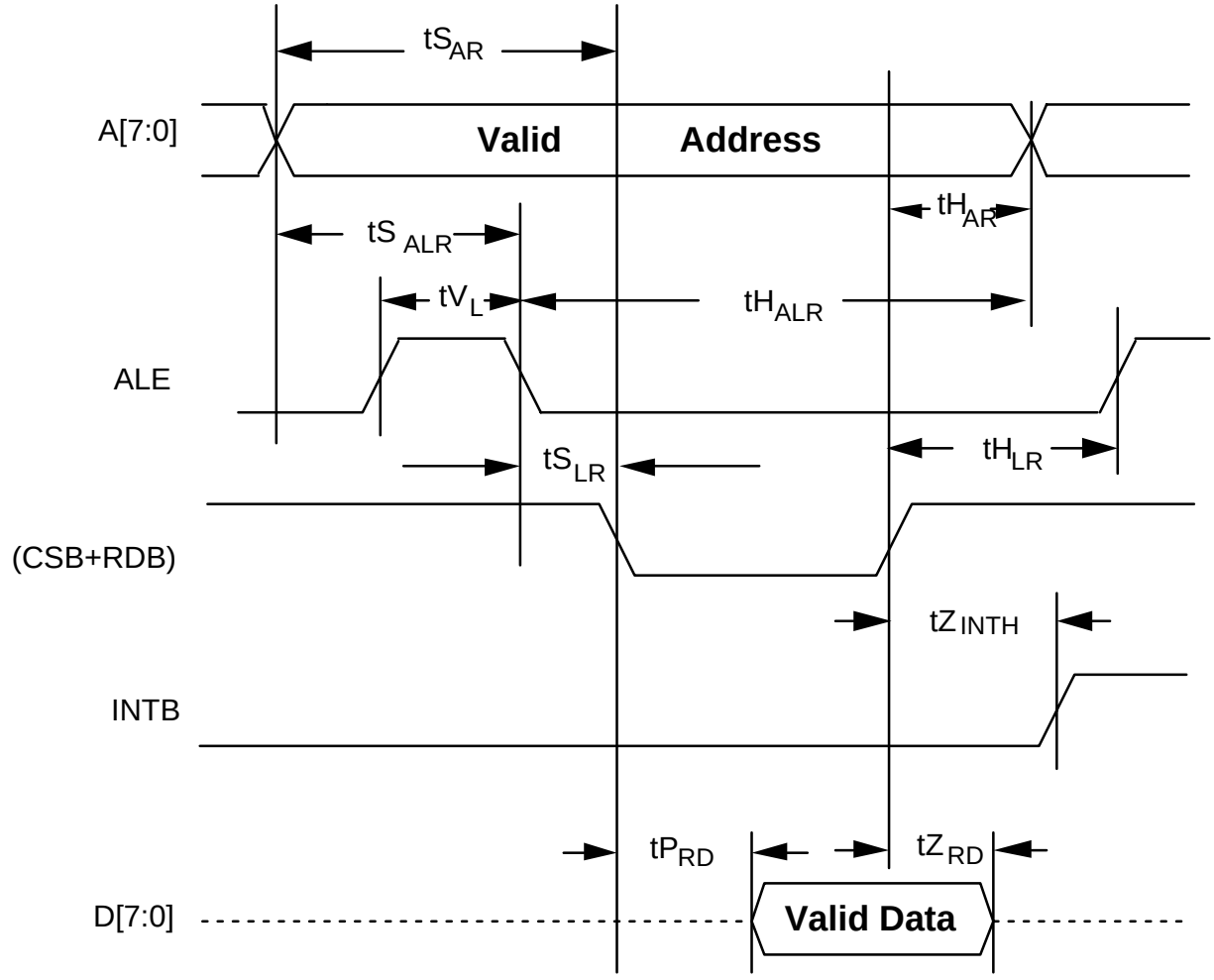
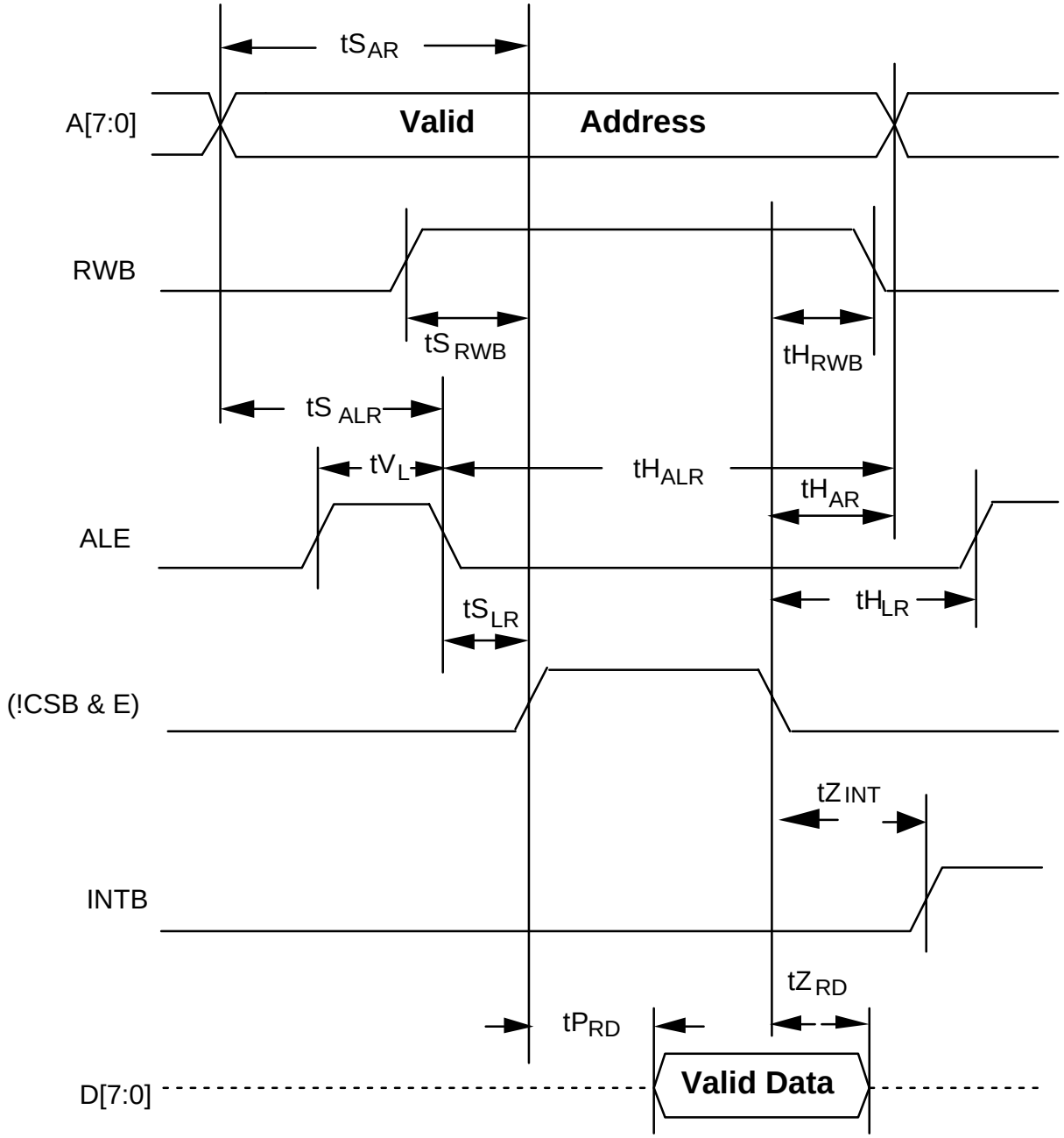


Figure 18 - Microprocessor Interface Read Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. a. In Intel mode, a valid read enable bar is defined as a logical OR of the CSB and the RDB signals.

   b. In Motorola mode, a valid read enable is defined as a logical AND of the E signal, the RWB signal, and the inverted CSB signal.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 6 - Microprocessor Interface Write Access (Figure 19, Figure 20)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_L	Valid Latch Pulse Width	20		ns

Symbol	Parameter	Min	Max	Units
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns
tS_{RWB}	RWB to Write Set-up Time	25		ns
tH_{LW}	RWB to Write Hold Time	20		ns

Figure 19 - Microprocessor Interface Write Timing (Intel Mode)

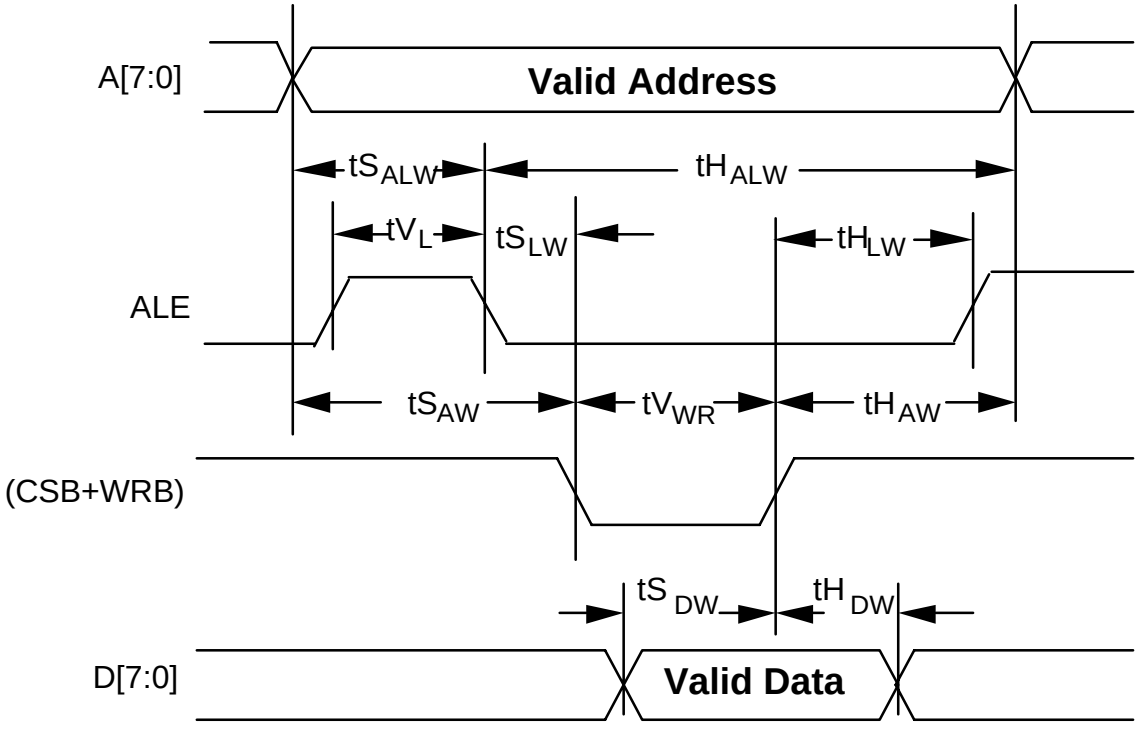
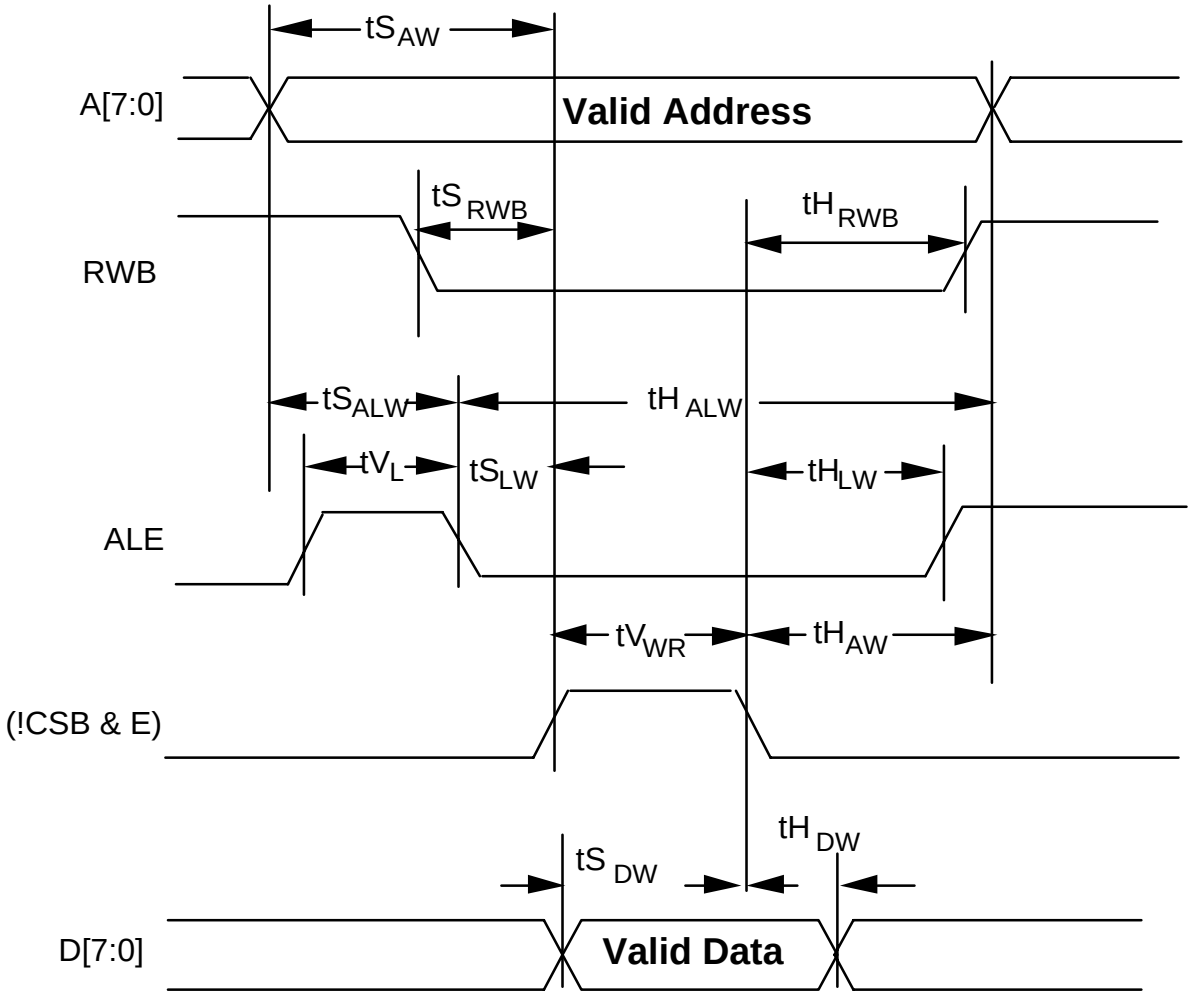


Figure 20 - Microprocessor Interface Write Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. a. In Intel mode, a valid write strobe bar is defined as a logical OR of the CSB and the WRB signals.

   b. In Motorola mode, a valid write strobe is defined as a logical AND of the E signal, the inverted RWB signal, and the inverted CSB signal.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

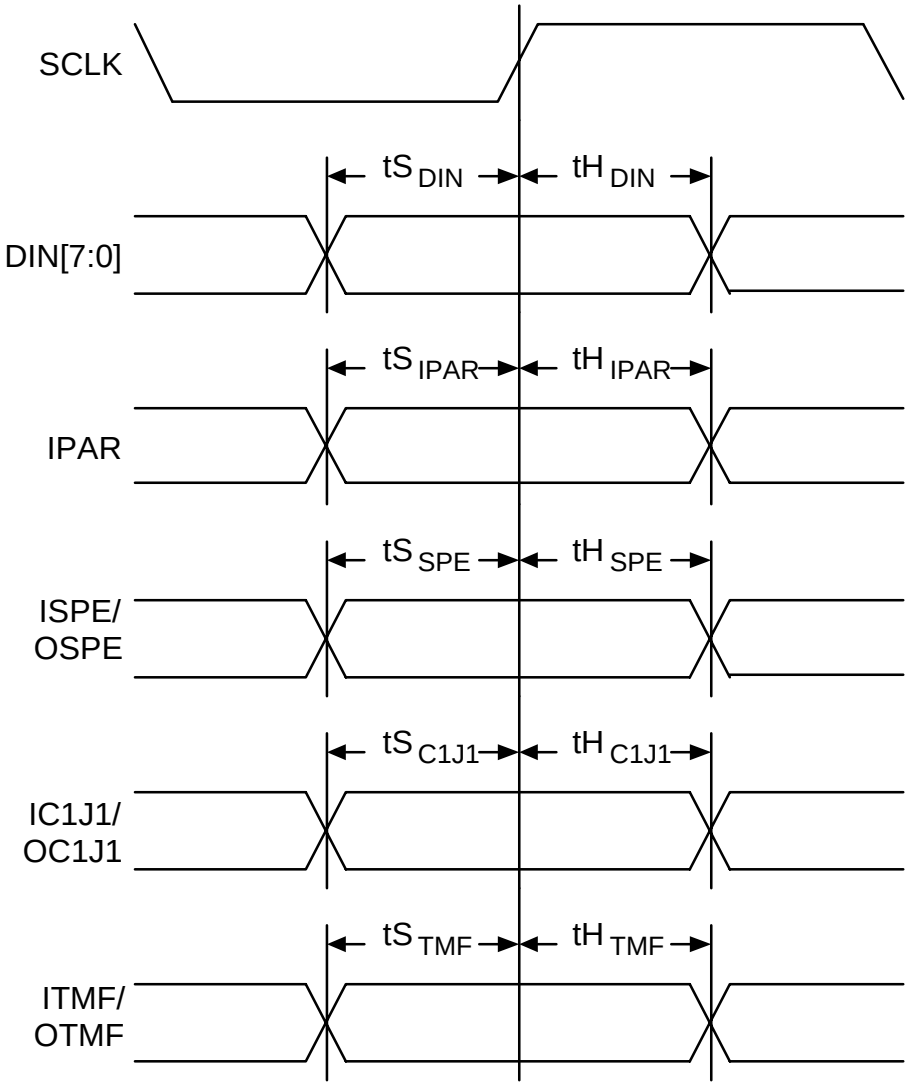
17 TUPP TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 7 - TUPP Input (Figure 21)

Symbol	Description	Min	Max	Units
	SCLK Frequency (nominally 19.44 MHz)		20	MHz
	SCLK Duty Cycle	40	60	%
tS_{DIN}	DIN Set-up Time	5		ns
tH_{DIN}	DIN Hold Time	3		ns
tS_{IPAR}	IPAR Set-up Time	5		ns
tH_{IPAR}	IPAR Hold Time	3		ns
tS_{SPE}	ISPE and OSPE Set-Up Time	5		ns
tH_{SPE}	ISPE and OSPE Hold Time	3		ns
tS_{C1J1}	IC1J1 and OC1J1 Set-Up Time	5		ns
tH_{C1J1}	IC1J1 and OC1J1 Hold Time	3		ns
tS_{TMF}	ITMF and OTMF Set-Up Time	5		ns
tH_{TMF}	ITMF and OTMF Hold Time	3		ns

Figure 21 - Input Timing



Notes on Input Timing:

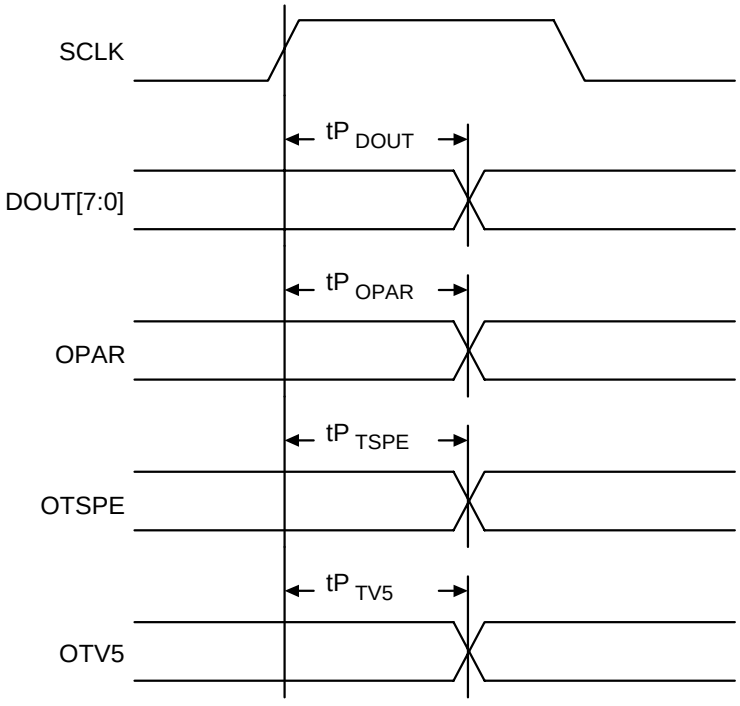
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 8 - TUPP Output (Figure 22)

Symbol	Description	Min	Max	Units
tPDOUT	SCLK High to DOUT Valid Propagation Delay	3	25	ns
tPOPAR	SCLK High to DOUT Valid Propagation Delay	3	25	ns
tPTSPE	SCLK High to OTSPE Valid Propagation Delay	3	25	ns
tPTV5	SCLK High to OTV5 Valid Propagation Delay	3	25	ns

Figure 22 - Output Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

18 ORDERING AND THERMAL INFORMATION

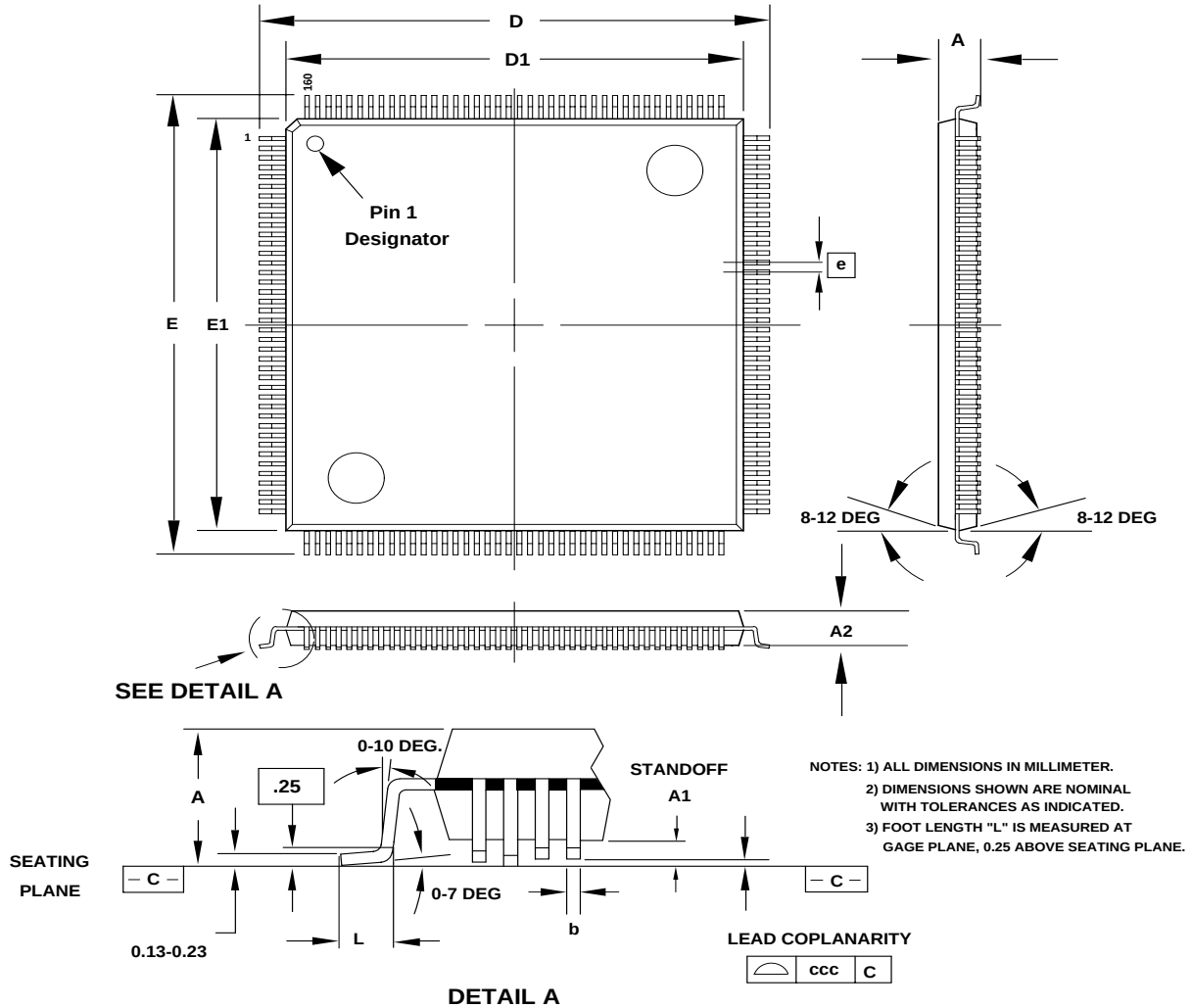
Table 9 - TUPP Ordering Information

PART NO.	DESCRIPTION
PM5361-RI	160 Copper Leadframe Plastic Quad Flat Pack (PQFP)
PM5361-EI	160 Plastic Quad Flat Pack (PQFP) With Fused Corner Pins

Table 10 - TUPP Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5361-RI	-40°C to 85°C	45 °C/W	13 °C/W
PM5361-EI	-40°C to 85°C	31 °C/W	10 °C/W

19 MECHANICAL INFORMATION



PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

NOTES

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