FEATURES

- Monolithic SONET Line Terminating Transceiver for processing the line overhead of a receive and a transmit SONET STS-1, STS-3, STS-9, or STS-12 data stream.
- Operates in one of four modes: STS-1 byte serial mode, STS-3 byte serial mode, STS-9 byte serial mode, or STS-12 byte serial mode.
- Optionally performs byte interleaved multiplexing of lower rate drop side SONET data streams. STS-3 -> STS-1, STS-9 -> STS-3, and STS-12 -> STS-3 multiplexing modes are supported.
- Processes byte serial data at 6.48 Mbyte/s, 6.408 Mbyte/s, 19.44 Mbyte/s, 19.224 Mbyte/s, 58.32 Mbyte/s, 57.672 Mbyte/s, 77.76 Mbyte/s, or 76.896 Mbyte/s depending on the mode selected.
- Compatible with the PM5301 SONET Section Terminating Transceiver, and the PM5323 Triple STS Payload Processor for processing the entire transport overhead of STS-1/3/9/12 streams.
- Calculates the line BIP-8 error detection code for each of the received STS-1 streams, and each of the transmit STS-1 streams.
- Extracts the line BIP-8 error detection codes (B2 bytes) from each of the received STS-1 streams, and optionally inserts the line BIP-8 error detection codes (B2 bytes) into each of the of the transmit STS-1 streams.
- Counts received line BIP-8 errors for performance monitoring purposes.
- Extracts the line order wire channel from STS-1 #1 (E2) of the receive STS-1/3/9/12 stream and serializes it at 64 kbit/s. Optionally inserts the line order wire channel into STS-1 #1 (E2) of the transmit STS-1/3/9/12 stream.
- Extracts the automatic protection switch (APS) channel from STS-1 #1 (K1 and K2) of the receive STS-1/3/9/12 stream and serializes it at 128 kbit/s. Optionally inserts the automatic protection switch (APS) channel into STS-1 #1 (K1 and K2) of the transmit STS-1/3/9/12 stream.
- Detects line far end receive failure (FERF) in the received STS-1/3/9/12 stream.
- Detects line alarm indication signal (AIS) in the received STS-1/3/9/12 stream.
- Optionally inserts line far end receive failure (FERF) in the transmit STS-1/3/9/12 stream.

- Optionally inserts, on a continuous basis, a single bit error in the B2 bytes located in STS-1 #1 to STS-1 #N for diagnostic purposes.
- Low power +5 Volt 1.0 micron CMOS. Device has TTL/CMOS compatible inputs and outputs.
- Standard 144 pin CPGA package, and 160 pin PJQFP (STS-1 and STS-3 operation only).

APPLICATIONS

- OC-N to OC-M multiplexers
- SONET add drop multiplexers
- SONET terminal multiplexers
- SONET test equipment

REFERENCES

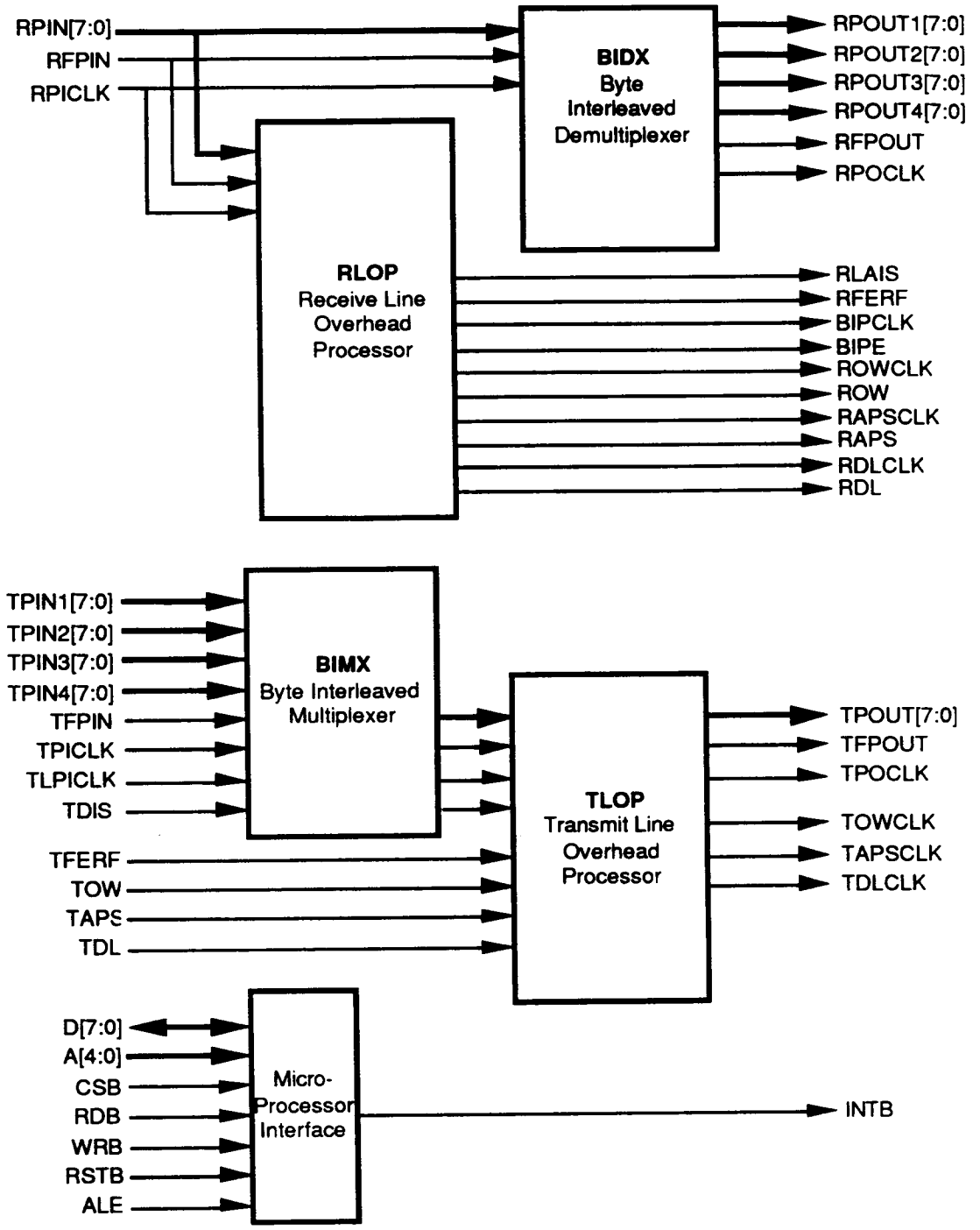
- American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1988.
- Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 1, September, 1989.

DESCRIPTION

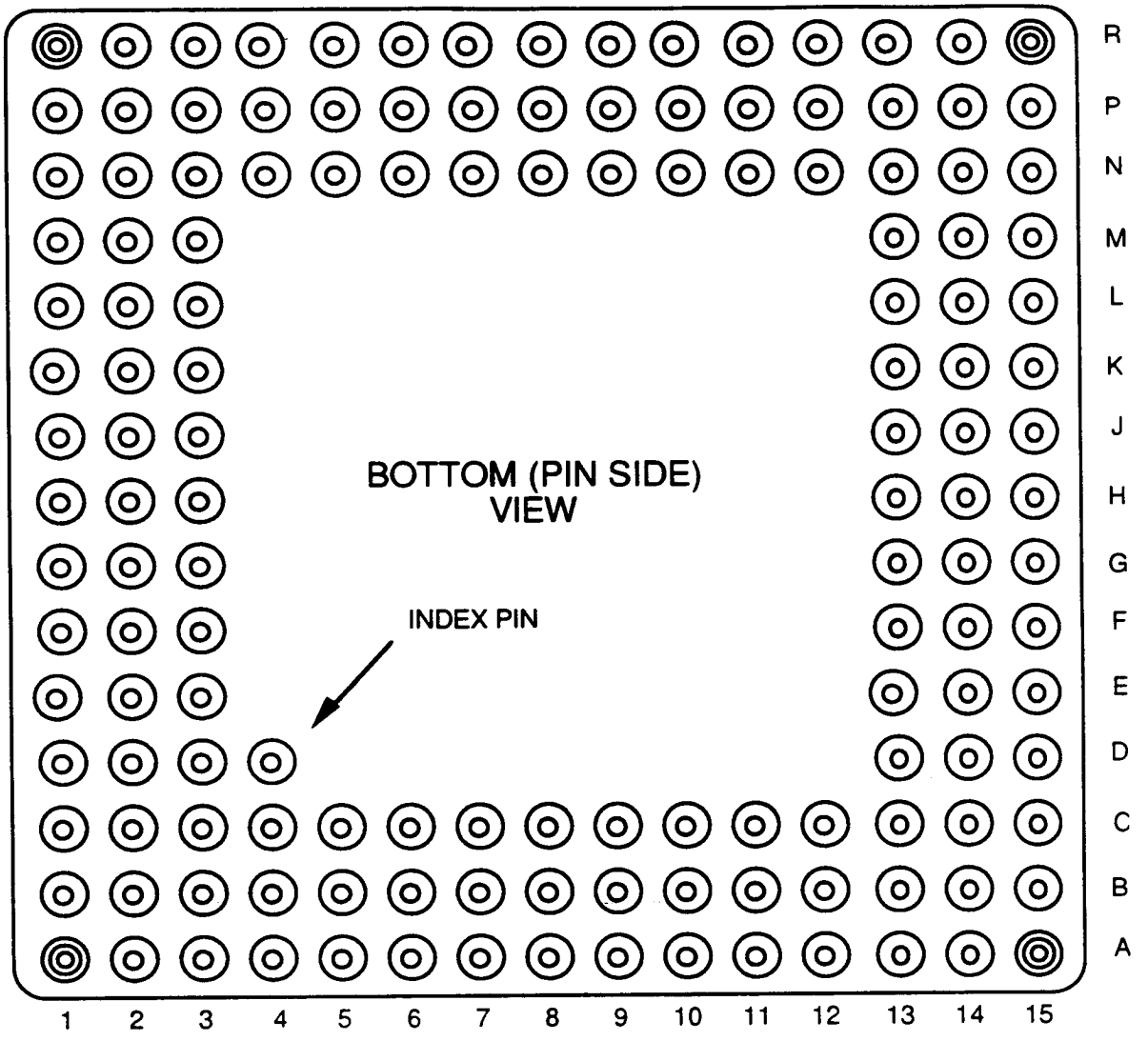
The PM5311 SONET Line Terminating Transceiver (SLTX) is implemented using the PMC SONET Telecom System Block (TSB) Library of ASIC functional blocks. Consequently, the design database of the SLTX standard product is readily customizable to incorporate new features or reduce cost.

The PM5311 SONET Line Terminating Transceiver (SLTX) processes byte serial STS-1/3/9/12 streams, terminating the line overhead. It can operate in conjunction with the PM5301 SONET Section Terminating Transceiver (SSTX) which also processes byte serial STS-1/3/9/12 streams, terminating section overhead, and performing parallel-to-serial and serial-to-parallel conversion for the STS-1 case. The PM5311 may be used with the PM5323 SONET Triple Payload Processor (TSPP), which contains three independent STS payload processors, to provide complete transport overhead processing support.

BLOCK DIAGRAM



PIN DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Type	Pin Coord	Function
RPICLK	Input	C2	The receive parallel input clock (RPICLK) provides timing for sampling the byte serial STS-1/3/9/12 data, RPIN[7:0]. RPICLK is nominally a 6.48 MHz, 6.408 MHz, 19.44 MHz, 19.224 MHz, 58.32 MHz, 57.672 MHz, 77.76 MHz, or 76.896 MHz 45% - 55% duty cycle clock, depending on the operating mode and timing mode selected.
RPIN[7] RPIN[6] RPIN[5] RPIN[4] RPIN[3] RPIN[2] RPIN[1] RPIN[0]	Input Input Input Input Input Input Input Input	F2 F3 D1 E2 C1 E3 D2 B1	The receive parallel input (RPIN[7:0]) bus carries STS-1/3/9/12 stream in byte serial format. RPIN[7:0] is sampled on the rising edge of RPICLK. RPIN7 is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RPIN0 is the least significant bit (corresponding to bit 8 of each serial PCM word).
RFPIN	Input	D3	The active high receive framing position Input (RFPIN) signal indicates the frame alignment for STS-1/3/9/12 streams. RFPIN is high to mark the first byte of the synchronous payload envelope within the transport frame (SPE byte 1 of STS-1 #1). RFPIN does not need to be activated every frame. RFPIN is sampled on the rising edge of RPICLK.
RFERF	Output	B2	The far end receive failure (RFERF) signal is set high when line FERF is detected in the RPIN[7:0] stream. FERF is updated on the falling edge of RPOCLK.
RLAIS	Output	A1	The line alarm indication signal (RLAIS) signal is set high when line AIS is detected in the RPIN[7:0] stream LAIS is updated on the falling edge of RPOCLK.
BIPCLK	Output	C3	The bit interleaved parity error clock (BIPCLK) signal is a 3.24 MHz clock used to update the BIPE output.

BIPE	Output	C4	The bit interleaved parity error (BIPE) signal is high for each line BIP-8 error detected in the RPIN[7:0] stream. BIPE may be asserted for 8N BIPCLK periods per frame (125 µs) in an STS-N stream. BIPE is updated on the falling edge of BIPCLK.
RDLCLK	Output	A2	The receive data link clock (RDLCLK) is a 576 kHz clock used to update the RDL output. RDLCLK is a gapped 2.16 MHz clock.
RDL	Output	B3	The deceive data link (RDL) signal carries the 576 kbit/s line data communication channel extracted from the line overhead of the RPOUT[7:0] stream. RDL is updated on the falling edge of RDLCLK.
ROWCLK	Output	A3	The receive order wire clock (ROWCLK) is a 64 kHz clock used to update the ROW output. ROWCLK is a gapped 72 kHz clock.
ROW	Output	A4	The receive order wire (ROW) signal carries the 64 kbit/s line order wire channel extracted from the line overhead of the RPOUT[7:0] stream. ROW is updated on the falling edge of ROWCLK.
RAPSCLK	Output	B5	The receive automatic protection switch channel Clock (RAPSCLK) is a 128 kHz clock used to update the RAPS output. RUCCLK is a gapped 144 kHz clock.
RAPS	Output	A5	The receive automatic protection switch channel (RAPS) signal carries the 128 kbit/s automatic protection switch channel extracted from the line overhead of the RPOUT[7:0] stream. RAPS is updated on the falling edge of RAPSCLK.
RPOCLK	Output	A12	The receive parallel output clock (RPOCLK) provides timing for updating the demultiplexed byte serial STS-1 or STS-3 outputs, RPOUT1[7:0], RPOUT2[7:0], RPOUT3[7:0], and RPOUT4[7:0]. RPOCLK is nominally a 6.48 MHz, 6.408 MHz, 19.44 MHz, or 19.224 MHz clock, depending on the operating mode and timing mode selected. If demultiplexing is bypassed, RPOCLK is a buffered version of RPICLK, and provides timing for updating the STS-N stream on RPOUT1[7:0].

RPOUT1[7] RPOUT1[6] RPOUT1[5] RPOUT1[4] RPOUT1[3] RPOUT1[2] RPOUT1[1] RPOUT1[0]	Output Output Output Output Output Output Output Output	A10 C9 B9 B11 A13 C11 B12 A14	The receive parallel output #1 bus, (RPOUT1[7:0]), carries demultiplexed STS-1 or STS-3 streams in byte serial format. RPOUT1[7:0] is updated on the falling edge of RPOCLK. RPOUT1[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RPOUT1[0] is the least significant bit (corresponding to bit 8 of each serial PCM word). RPOUT1[7:0] contains the STS-N stream when demultiplexing is bypassed.
RPOUT2[7] RPOUT2[6] RPOUT2[5] RPOUT2[4] RPOUT2[3] RPOUT2[2] RPOUT2[1] RPOUT2[0]	Output Output Output Output Output Output Output Output	D14 C15 D15 E14 E15 F14 G14 F15	The receive parallel output #2 bus, (RPOUT2[7:0]), carries demultiplexed STS-1 or STS-3 streams in byte serial format. RPOUT2[7:0] is updated on the falling edge of RPOCLK. RPOUT2[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RPOUT2[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
RPOUT3[7] RPOUT3[6] RPOUT3[5] RPOUT3[4] RPOUT3[3] RPOUT3[2] RPOUT3[1] RPOUT3[0]	Output Output Output Output Output Output Output Output	B13 C12 A15 B14 C13 D13 B15 C14	The receive parallel output #3 bus, (RPOUT3[7:0]), carries demultiplexed STS-1 or STS-3 streams in byte serial format. RPOUT3[7:0] is updated on the falling edge of RPOCLK. RPOUT3[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RPOUT3[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
RPOUT4[7] RPOUT4[6] RPOUT4[5] RPOUT4[4] RPOUT4[3] RPOUT4[2] RPOUT4[1] RPOUT4[0]	Output Output Output Output Output Output Output Output	C6 B6 B7 A6 A7 A8 B8 A9	The receive parallel output #4 bus, (RPOUT4[7:0]), carries demultiplexed STS-1 or STS-3 streams in byte serial format. RPOUT4[7:0] is updated on the falling edge of RPOCLK. RPOUT4[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). RPOUT4[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
RFPOUT	Output	A11	The active high receive frame position output (RFPOUT) signal is asserted once per frame during the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) in the RPOUT1[7:0], RPOUT2[7:0], RPOUT3[7:0], and RPOUT4[7:0] busses. RFPOUT is updated on the falling edge of RPOCLK.

TPICLK	Input	P2	The transmit parallel input clock (TPICLK) provides timing for multiplexing the byte serial STS-1/3 inputs TPIN1[7:0], TPIN2[7:0], TPIN3[7:0] and TPIN4[7:0], into a higher rate STS-N stream. TPICLK is nominally a 6.48 MHz, 6.408 MHz, 19.44 MHz, 19.224 MHz, 58.32 MHz, 57.672 MHz, 77.76 MHz or 76.896 MHz 45% - 55% duty cycle clock, depending on the operating mode and timing mode selected. If multiplexing is bypassed, TPICLK provides timing for sampling the byte serial STS-N stream on TPIN1[7:0].
TLPICLK	Input	P14	The transmit low speed parallel input clock (TLPICLK) provides timing for sampling the byte serial STS-1/3 streams prior to multiplexing. TLPICLK is synchronous with, but arbitrarily phase aligned to TPICLK. TLPICLK is nominally a 6.48 MHz, 6.408 MHz, 19.44 MHz, or 19.224 MHz clock. TPIN1[7:0], TPIN2[7:0], TPIN3[7:0], TPIN4[7:0], TDIS, TFERF, and TFPIN are sampled on the rising edge of TLPICLK.
VCLK			The vector clock (VCLK) is used during SLTX production test to verify internal functionality.
TPIN1[7] TPIN1[6] TPIN1[5] TPIN1[4] TPIN1[3] TPIN1[2] TPIN1[1] TPIN1[0]	Input	R4 P5 R3 N5 P4 R2 P3 N4	The transmit parallel input bus #1, (TPIN1[7:0]), carries STS-1/3 streams in byte serial format. TPIN1[7:0] is sampled on the rising edge of TPICLK. TPIN1[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TPIN1[0] is the least significant bit (corresponding to bit 8 of each serial PCM word). TPIN1[7:0] contains the STS-N stream when multiplexing is bypassed.
TPIN2[7] TPIN2[6] TPIN2[5] TPIN2[4] TPIN2[3] TPIN2[2] TPIN2[1] TPIN2[0]	Input	P8 R7 R6 N7 P7 R5 P6 N6	The transmit parallel input bus #2, (TPIN2[7:0]), carries STS-1/3 streams in byte serial format. TPIN2[7:0] is sampled on the rising edge of TPICLK. TPIN2[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TPIN2[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).

TPIN3[7] TPIN3[6] TPIN3[5] TPIN3[4] TPIN3[3] TPIN3[2] TPIN3[1] TPIN3[0]	Input	P11 R11 N10 P10 P9 R10 R9 R8	The transmit parallel input bus #3, (TPIN3[7:0]), carries STS-1/3 streams in byte serial format. TPIN3[7:0] is sampled on the rising edge of TPICLK. TPIN3[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TPIN3[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
TPIN4[7] TPIN4[6] TPIN4[5] TPIN4[4] TPIN4[3] TPIN4[2] TPIN4[1] TPIN4[0]	Input	N13 N12 R14 P13 N11 P12 R13 R12	The transmit parallel input bus #4, (TPIN4[7:0]), carries STS-1/3 streams in byte serial format. TPIN4[7:0] is sampled on the rising edge of TPICLK. TPIN4[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TPIN4[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
TFPIN	Input	R1	The active high transmit framing position input (TFPIN) signal indicates the frame alignment for STS-1/3/9/12 streams. TFPIN is sampled on the rising edge of TLPICLK.
TFERF	Input	R15	The active high transmit far end receive failure (TFERF) signal controls the insertion of a far end receive failure indication in the transmitted byte serial output, TPOUT[7:0]. TFERF is sampled on the rising edge of TLPICLK.
TDIS	Input	N3	The active high transmit disable (TDIS) signal selectively disables overwriting each of the STS-1/3 streams with the corresponding line overhead byte. TDIS is sampled on the rising edge of TLPICLK.
TDLCLK	Output	H15	The transmit data link clock (TDLCLK) is a 576 kHz clock used to sample the TDL input. TDLCLK is a gapped 2.16 MHz clock.
TDL	Input	N14	The transmit data link (TDL) signal carries the 576 kbit/s line data communication channel . The channel is inserted in the line overhead of the transmit data stream, TPOUT[7:0]. TDL is sampled on the rising edge of TDLCLK. This pin contains an internal pull up resistor.
TOWCLK	Output	G15	The transmit order wire clock (TOWCLK) is a 64 kHz clock used to sample the TOW input TOWCLK is a gapped 72 kHz clock.

TOW	Input	P15	The transmit order wire (TOW) signal carries the 64 kbit/s line order wire channel. The order wire channel is inserted in the line overhead of the transmit data, TPOUT[7:0]. TOW is sampled on the rising edge of TOWCLK.
TAPSCLK	Output	H14	The transmit automatic protection switch channel Clock (TAPSCLK) is a 128 kHz clock used to sample the TAPS input. TAPSCLK is a gapped 144 kHz clock.
TAPS	Input	M13	The transmit automatic protection switch channel (TAPS) signal carries the 128 kbit/s automatic protection switch channel. The automatic protection switch channel is inserted in the line overhead of the transmit data, TPOUT[7:0]. TAPS is sampled on the rising edge of TAPSCLK.
TPOCLK	Output	M15	The transmit parallel output clock (TPOCLK) provides timing for updating the byte serial STS-1/3/9/12 output, TPOUT[7:0]. TPOCLK is nominally a 6.48 MHz, 6.408 MHz, 19.44 MHz, 19.224 MHz, 58.32 MHz, 57.672 MHz, 77.76 MHz or 76.896 MHz clock. TPOCLK is a buffered version of TPICLK.
TPOUT[7] TPOUT[6] TPOUT[5] TPOUT[4] TPOUT[3] TPOUT[2] TPOUT[1] TPOUT[0]	Output	J15 K15 J13 J14 L14 N15 L13 M14	The transmit parallel output bus, (TPOUT[7:0]), carries data in byte serial format. TPOUT[7:0] is updated on the falling edge of TPOCLK. TPOUT[7] is the most significant bit (corresponding to bit 1 of each serial PCM word, the first bit transmitted). TPOUT[0] is the least significant bit (corresponding to bit 8 of each serial PCM word).
TFPOUT	Output	L15	The active high transmit frame position output (TFPOUT) signal is asserted once per frame during the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) in the TPOUT[7:0] bus. TFPOUT is updated on the falling edge of TPOCLK.
INTB	Output	L2	The active low open-drain interrupt (INTB) signal is asserted when an event is detected on one of the maskable interrupt sources, and that source is unmasked.

A[4] A[3] A[2] A[1] A[0]	Input	M3 P1 N2 L3 M2	The address bus (A[4:0) selects specific registers during accesses.
ALE	Input	N1	The address latch enable (ALE) signal latches the address bus (A[4:0]) when low. This allows the SLTX to be interfaced to a multiplexed address/data bus. The address latches are transparent when ALE is high.
CSB	Input	G3	The active low chip select (CSB) signal is asserted during register accesses.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	L1 K3 K2 K1 J1 H1 G1 F1	The bidirectional data bus, D[7:0], is used during SLTX read and write accesses.
RDB	Input	E1	The active low read enable (RDB) signal is low during an SLTX read access. The SLTX drives the D[7:0] bus with the addressed register's contents while RDB and CSB are low.
WRB	Input	G2	The active low write strobe (WRB) signal is low during an SLTX write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
RSTB	Input	M1	The active low reset (RSTB) signal is low to provide an asynchronous reset to the PM5311. This schmitt triggered pin contains an internal pull up resistor.
VDDI[0] VDDI[1] VDDI[2] VDDI[3]	Power Power Power Power	H3 C7 G13 N8	Core power pins (VDDI[3:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDO[4:0] pins.
VSSI[0] VSSI[1] VSSI[2] VSSI[3]	Gnd Gnd Gnd Gnd	J3 C8 H13 N9	Core ground pins (VSSI[3:0]). These pins must be connected to a common ground together with the VSSO[4:0] pins.

VDDO[0] VDDO[1] VDDO[2] VDDO[3] VDDO[4]	Power Power Power Power Power	H2 C5 B10 E13 K14	Pad ring power pins (VDDO[4:0]). These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDI[3:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins.
VSSO[0] VSSO[1] VSSO[2] VSSO[3] VSSO[4]	Gnd Gnd Gnd Gnd Gnd	J2 B4 C10 F13 K13	Pad ring ground pins (VSSO[4:0]). These pins must be connected to a common ground together with the VSSI[3:0] pins. Care must be taken to avoid coupling noise induced on the VSSO pins into the VSSI pins.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSI are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM5311 between the core and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.
2. Inputs RSTB, TDL, and ALE have internal pull-up resistors.

FUNCTIONAL DESCRIPTION

Receive Line Overhead Processor

The Receive Line Overhead Processor block (RLOP) processes the SONET line overhead of a received SONET data stream. It can be configured to process an STS-1, STS-3, STS-9, or STS-12 data stream that is presented in byte serial format at the STS-N frame rate of 6.48 Mbyte/s, 19.44 Mbyte/s, 58.32 Mbyte/s, or 77.76 Mbyte/s respectively. The RLOP may be configured to process an STS-1, STS-3, STS-9, or STS-12 data stream that is presented in byte serial format at the line overhead frame rate (the line overhead frame rate consists of the line overhead and the synchronous payload envelope) of 6.408 Mbyte/s, 19.224 Mbyte/s, 57.672 Mbyte/s, or 76.896 Mbyte/s. The byte serial input is contained in the RPIN[7:0] bus.

The STS-N transport overhead location is indicated by the RFPIN signal. The RLOP extracts the line data communication channel, line order wire channel and automatic protection switch channel from the line overhead, and provides them as lower rate bit serial outputs (RDL, ROW, RAPS) together with associated clock signals (RDLCLK, ROWCLK, RAPSCLK). Line alarm indication signal, and Line FERF are detected, and indicated using outputs RLAIS and RFERF.

The line level bit-interleaved parity byte is computed, and compared to the received B2 byte for each of the STS-1s in the STS-N stream. Line BIP-8 errors are accumulated in an internal counter. Registers are provided that allow accumulated line BIP-8 errors to be read out at intervals of up to one second duration. A line BIP-8 error output is also provided (BIPE), along with its associated clock (BIPCLK). An interrupt output is provided (INTB) that may be activated by state transitions on the RLAIS, or RFERF outputs, or a single line BIP-8 error event. Each interrupt source is individually maskable.

Byte Interleaved Demultiplexer

The Byte Interleaved Demultiplexer block (BIDX) performs a 1:3 (STS-9 to STS-3, or STS-3 to STS-1), or a 1:4 (STS-12 to STS-3) demultiplexing function on an incoming byte serial STS-3, STS-9, or STS-12 data stream. The demultiplexed streams are available on the four byte wide busses: RPOUT1[7:0], RPOUT2[7:0], RPOUT3[7:0], and RPOUT4[7:0]. The transport overhead of these frame aligned streams is located by the RFPOUT signal. RPOCLK may be used by downstream circuitry to process the synchronous payload envelope(s) contained in the byte serial demultiplexed streams.

The demultiplexer function in this block may be bypassed using a bit in the control register, in which case RPOUT1[7:0] contains data directly from the RPIN[7:0] input bus.

Byte Interleaved Multiplexer

The Byte Interleaved Multiplexer block (BIMX) performs a 3:1 (STS-3 to STS-9, or STS-1 to STS-3), or a 4:1 (STS-3 to STS-12) multiplexing function on an incoming byte serial STS-1, or STS-3 data stream. The multiplexed inputs are contained on the four byte wide busses: TPIN1[7:0], TPIN2[7:0], TPIN3[7:0], and TPIN4[7:0]. The transport overhead of these frame aligned streams is determined by the TFPIN input. The multiplexed byte serial STS-N stream is passed to the transmit line overhead processor block where the line overhead is added to the stream.

The multiplexer function in this block may be bypassed using a bit in the control register, in which case the byte serial TPIN1[7:0] stream is passed directly to the transmit line overhead processor block.

The lower rate STS-1/3 clock (TLPICLK) is synchronous with, but arbitrarily phase aligned to the higher rate STS-3/9/12 clock (TPICLK). A lower rate internal sampling clock is derived by dividing TPICLK by three or four, as appropriate. A phase alignment error is declared when the sampling clock phase, and the TLPICLK clock phase are identical. The sampling clock phase is modified during a phase alignment error to provide a safe phase relationship between the sampling clock, and TLPICLK. An interrupt output is provided (INTB) that may be activated by a phase alignment error event. Each interrupt source is individually maskable.

Transmit Line Overhead Processor

The Transmit Line Overhead Processor block (TLOP) processes the line overhead of a transmit SONET data stream. It can be configured to process an STS-1, STS-3, STS-9, or STS-12 data stream that is presented in byte serial format at the STS-N frame rate of 6.48 Mbyte/s, 19.44 Mbyte/s, 58.32 Mbyte/s, or 77.76 Mbyte/s respectively. The TLOP may be configured to process an STS-1, STS-3, STS-9, or STS-12 data stream that is presented in byte serial format at the line overhead frame rate (the line overhead frame rate consists of the line overhead and the synchronous payload envelope) of 6.408 Mbyte/s, 19.224 Mbyte/s, 57.672 Mbyte/s, or 76.896 Mbyte/s.

The TLOP accepts an STS-N data stream in byte serial format. It optionally inserts the line data communication channel, the line order wire channel, and the automatic protection switch channel into the line overhead of the STS-N data stream. These line overhead channels are separately fed to the TLOP as bit serial inputs (TDL, TOW, TAPS). The PM5103 provides the bit serial clock for each line overhead channel (TDLCLK, TOWCLK, TAPSCLK). Line FERF may be inserted in the STS-1/3/9/12 stream under the control of an external input (TFERF), or a writeable register.

The line BIP-8 error detection codes for each of the constituent STS-1s in the STS-1/3/9/12 stream are calculated by the TLOP and are optionally inserted into the line overhead of each of the STS-1s in the STS-N data stream. Errors may be inserted

in the line BIP-8 codes for diagnostic purposes. A byte serial STS-N stream is output on the TPOUT[7:0] bus. The transport overhead of this stream is located by the TFPOUT signal. TPOCLK may be used by upstream circuitry to insert the section overhead in the byte serial stream.

Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the SLTX to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the SLTX while the test mode registers are used to enhance the testability of the SLTX.

REGISTER DESCRIPTION

Normal Mode Register Memory Map

A[4:0]	Register
00H	Master Configuration
01H	Master Interrupt Enable
02H	Master Interrupt Status
03H	Master Reset and Identity
04H	TLOP Control
05H	TLOP Diagnostic
06H - 07H	Reserved
08H	RLOP Control/Status
09H	RLOP Interrupt
0AH	Line BIP-8 Error Count #1
0BH	Line BIP-8 Error Count #2
0CH	Line BIP-8 Error Count #3
0DH	Reserved
0EH	BIMX Interrupt
0FH	Reserved
10H - 1FH	Reserved for test

Registers are used to configure, and monitor the operation of the SLTX

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. All configuration bits that can be written can also be read back unless otherwise stated. This allows the processor controlling the SLTX to determine the programming state of the block.

3. Writeable register bits are cleared to zero upon reset unless otherwise noted.

4. Writing read-only register bit location does not affect device operation unless otherwise noted.

Address 00H
Master Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	PLE
Bit 4	R/W	DXB
Bit 3	R/W	MXB
Bit 2	R/W	PCS
Bit 1	R/W	MODE[1]
Bit 0	R/W	MODE[0]

The MODE[1:0] bus selects the operating mode of the transmit and receive line overhead processors as follows:

00	selects	STS-1
01	selects	STS-3
10	selects	STS-9
11	selects	STS-12

The BIMX and BIDX blocks are bypassed when STS-1 mode is selected. BIMX and BIDX are configured as a 1:3 and 3:1 multiplexer/demultiplexer pair when STS-3 or STS-9 modes are selected. BIMX and BIDX are configured as a 1:4 and 4:1 multiplexer/demultiplexer pair when STS-12 mode is selected. BIMX and BIDX may also be bypassed while in STS-3, STS-9, or STS-12 mode using the MXB and DXB bits respectively.

The parallel clock select (PCS) bit selects the timing mode for the transmit and receive line overhead processors as follows:

0	selects	STS-N timing
1	selects	line overhead timing

The MXB and DXB bits control the bypassing of the multiplexer and demultiplexer blocks respectively. When MXB is set to a logic 0, the multiplexer block is enabled, and the three or four byte serial input streams are multiplexed to a single byte serial stream before the line overhead is inserted. When MXB is set to a logic 1, the multiplexer block is bypassed, and one byte serial input stream is processed. Similarly, when DXB is set to a logic 0, the demultiplexer block is enabled, and the byte serial input stream is demultiplexed into three or four byte serial output streams. When DXB is set to a logic 1, the demultiplexer block is bypassed, and one byte serial output stream is available.

The payload loopback enable bit (PLE) controls the payload loopback of the SLTX. When PLE is a logic 1, payload loopback is enabled, and the receive byte serial STS-N stream (RPIN[7:0] is passed directly to the Transmit Line Overhead Processor block where new line overhead may be inserted, and the resulting byte serial stream is output on TPOUT[7:0]. When PLE is a logic 0, payload loopback is disabled.

Address 01H
Master Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	BIMXE
Bit 0	R/W	RLOPE

This register provides an interrupt enable bit for each of the blocks in the SLTX. Interrupts may still be masked within each block. Interrupts enabled at the block level, but masked by this register are reported in the Master Interrupt Status Register. Interrupts disabled at the block level are not reported by the Master Interrupt Status Register.

Address 02H
Master Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	BIMXI
Bit 0	R	RLOPI

This register identifies the block that is the source of a pending interrupt. It may be necessary to read the Interrupt Status/Diagnostic register of the interrupting block to determine the event that caused the interrupt. Interrupts disabled at the block level by the Master Interrupt Enable Register are not reported by this register.

Address 03H
Master Reset and Identity

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	ID[6]
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

This register allows software to asynchronously reset the SLTX. The software reset is equivalent to setting the RSTB input pin low. Setting the RESET bit to logic 1 causes the SLTX to be reset. Setting the RESET bit to logic 0 causes reset to be removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

The version identification bits ID[6:0], are set to a fixed value representing the version number of the SLTX. These bits can be read by software to determine the version number.

Address 04H
TLOP Control

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	DGROWTH
Bit 3	R/W	DAPS
Bit 2	R/W	DDL
Bit 1	R/W	DOW
Bit 0	R/W	FERF

The FERF bit controls the insertion of transmit line Far End Receive Failure (FERF). When FERF is set to a logic one, line FERF is inserted into the STS-N stream on TPOUT[7:0]. Line FERF is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in STS-1 #1 of the STS-N stream.

The DGROWTH, DOW, DDL, and DAPS bits control the overwriting of the line growth bytes, the line order wire channel, the line data communication channel, and the automatic protection switch channel. When DGROWTH is set to a logic one the growth byte positions in all STS-1s are not overwritten with zero bytes. When DOW is set to a logic one, the line order wire channel byte position in STS-1 #1 is not overwritten by the data shifted in on input TOW. When DDL is set high, the data communication channel byte positions in STS-1 #1 are not overwritten by the data shifted in on input TDL. When DAPS is set high, the APS byte positions in STS-1 #1 are not overwritten by the APS channel data shifted in on input TAPS.

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Address 05H
TLOP Diagnostic

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R/W	DBIP8

The DBIP8 bit controls the insertion of a single bit error continuously in each of the line BIP-8 bytes (B2 bytes). When DBIP8 is set high, the least significant bit of each of the B2 bytes is inverted.

Address 08H
RLOP Control/Status

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	LAIS
Bit 0	R	FERF

The LAIS, and FERF bits reflect the current state of the RLAIS and RFERF outputs respectively.

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Address 09H
RLOP Interrupt Enable and Status

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	BIPEE
Bit 5	R/W	LAISE
Bit 4	R/W	FERFE
Bit 3		Unused
Bit 2	R	BIPEI
Bit 1	R	LAISI
Bit 0	R	FERFI

The BIPEE, LAISE, and FERFE bits are interrupt enables. When a 1 is written to these locations, the occurrence of the corresponding event will activate the interrupt output, INTB (if the Master Interrupt Enable Register is programmed to enable RLOP interrupts). INTB is removed when the RLOP Interrupt register is read.

The BIPEI, LAISI, and FERFI bits are set high when a transition occurs on the BIPE, TLAIS, or TFERF outputs respectively. These bits are cleared when the RLOP Interrupt register is read.

Address 0AH
RLOP Line BIP-8 Error Count #1

Bit	Type	Function
Bit 7	R	BE7
Bit 6	R	BE6
Bit 5	R	BE5
Bit 4	R	BE4
Bit 3	R	BE3
Bit 2	R	BE2
Bit 1	R	BE1
Bit 0	R	BE0

Address 0BH
RLOP Line BIP-8 Error Count #2

Bit	Type	Function
Bit 7	R	BE15
Bit 6	R	BE14
Bit 5	R	BE13
Bit 4	R	BE12
Bit 3	R	BE11
Bit 2	R	BE10
Bit 1	R	BE9
Bit 0	R	BE8

Address 0CH
RLOP Line BIP-8 Error Count #3

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	BE19
Bit 2	R	BE18
Bit 1	R	BE17
Bit 0	R	BE16

Bits BE0 through BE19 represent the number of line bit-interleaved parity errors that have been detected since the last time the error count was polled. To poll the error count one must write to any of the Line BIP-8 Error Count register addresses. Such a write transfers the the internally accumulated error count to the Error Count registers within 3 BIPECLK cycles (max ~ 1µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation. After the 1µs period has elapsed, the Line BIP-8 Error Count registers may be read.

Address 0EH
BIMX Interrupt Enable and Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	PAEE
Bit 0	R	PAEI

The PAEE bit is an interrupt enable. When a 1 is written to this location, the occurrence of the corresponding event will activate the interrupt output, INTB (if the Master Interrupt Enable Register is programmed to enable BIMX interrupts). INTB is removed when the BIMX Interrupt register is read.

The PAEI bit is set high when a phase alignment error is detected between the low rate multiplex clock (TLPICLK), and an internal sampling signal generated by the high rate multiplex clock (TPICLK) . This bit is cleared when the BIMX Interrupt register is read.

TEST FEATURES DESCRIPTION

Simultaneously asserting the RSTB, CSB, RDB, and WRB inputs causes all output pins, and the data bus to be held in a high-impedance state. This test feature may be used for board or module level testing.

The SLTX provides test features that allow individual testing of its constituent Telecom System Blocks (TSBs). When a particular TSB is under evaluation, most signals associated with the TSB are directly accessible. However, in some cases the individual TSB input/output signals are not directly accessible and specific control signals must be configured to allow indirect access to these signals.

To configure BIDX for individual testing reset the DXB bit in the master control register. To configure RLOP for individual testing set the DXB bit in the master control register. Note that the signals on the RPOUT1[7:0] bus, RFPOUT, and RPOCLK are identical (except for an asynchronous propagation delay) to the input signals RPIN[7:0], RFPIN, and RPICLK respectively.

To configure BIMX for individual testing reset the MXB bit in the master control register, set the input TDIS signal and watch TPOUT[7:0], TFPOUT and TPOCLK for the output signals. To configure TLOP for individual testing set the MXB bit in the master control register and supply input data, clock and frame pulse to TPIN1[7:0], TPICLK and TFPIN respectively.

Test mode registers are used to apply test vectors during production testing of the SLTX. Test mode registers (as opposed to normal mode registers) are selected when A4 is high.

Test mode registers may also be used for board or module level testing. When all of the constituent TSBs within the SLTX are placed in test mode 0, device inputs may be observed, and device outputs may be controlled via the microprocessor interface (refer to the "Test Mode 0" section below for details).

Test Mode Register Memory Map

A[4:0]	Register
00H - 0FH	Reserved for Normal Mode Registers
10H	Master Test
11H	Reserved
12H	BIDX Test Register 0
13H	BIDX Test Register 1
14H	TLOP Test Register 0
15H	TLOP Test Register 1
16H	TLOP Test Register 2
17H	TLOP Test Register 3
18H	RLOP Test Register 0
19H	RLOP Test Register 1
1AH	RLOP Test Register 2
1BH - 1DH	Reserved
1EH	BIMX Test Register 0
1FH	BIMX Test Register 1

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Address 10H
Master Test

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	W	PMCTST
Bit 4	R/W	DBCTRL
Bit 3	R/W	IOTST
Bit 2	W	HIZDATA
Bit 1	W	HIZIO
Bit 0		Unused

The HIZIO and HIZDATA bits control the tri-state modes of the SLTX. While the HIZIO bit is a logic 1, all output pins of the SLTX except the data bus are held in a high impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high impedance state which inhibits microprocessor read cycles. These bits are reset to logic 0 when the RSTB input is asserted, or when the device is reset using the Master Reset and Identity register.

The IOTST bit is used to allow normal microprocessor access to the test registers, and control the test mode in each block in the SLTX. When IOTST is a logic 1, all blocks are held in test mode, and the microprocessor may read and write test registers to control the outputs, and observe the inputs of the SLTX. IOTST is logically ORed with the PMCTST bit to control test mode selection. This bit is reset to logic 0 when the RSTB input is asserted, or when the device is reset using the Master Reset and Identity register.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one, the CSB pin controls the output enable for the data bus; holding CSB high causes the SLTX to drive the data bus, holding CSB low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. This bit is used to test the data bus output drive during production test. This bit is reset to logic 0 when the RSTB input is asserted, or when the device is reset using the Master Reset and Identity register.

The PMCTST bit controls the test mode enabling of the SLTX. When PMCTST is a logic 1, all blocks are held in test mode, and the production test vectors may be applied. PMCTST is reset to a logic 0 when CSB is not asserted (a logic 1). PMCTST is logically ORed with the IOTST bit to control test mode selection.

Test Mode 0

In test mode 0, the SLTX allows the logic levels on the device inputs to be observed through the microprocessor interface, and allows the device outputs to be controlled to either logic level through the microprocessor interface.

Test mode 0 is enabled by resetting the device (using the RSTB input, or the master reset and identity register), and then setting the IOTST bit in the Master Test register. The following addresses must then be written with the value 00H: 13H, 15H, 19H, and 1FH. Applying a rising edge (logic 0 to logic 1 transition) on the VCLK input followed by a read from the following locations returns the value for the indicated pins:

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12H	RPIN[7]	RPIN[6]	RPIN[5]	RPIN[4]	RPIN[3]	RPIN[2]	RPIN[1]	RPIN[0]
13H						RFPIN	RPICLK	
14H		TOW	TDL	TFERF	TAPS			
18H							RFPIN	RPICLK
1AH	RPIN7	RPIN6	RPIN5	RPIN4	RPIN3	RPIN2	RPIN1	RPIN0
1EH						TFPIN	TPICLK	TLPICLK
1EH*	TPIN1[7]	TPIN1[6]	TPIN1[5]	TPIN1[4]	TPIN1[3]	TPIN1[2]	TPIN1[1]	TPIN1[0]
1EH**	TPIN2[7]	TPIN2[6]	TPIN2[5]	TPIN2[4]	TPIN2[3]	TPIN2[2]	TPIN2[1]	TPIN2[0]
1EH***	TPIN3[7]	TPIN3[6]	TPIN3[5]	TPIN3[4]	TPIN3[3]	TPIN3[2]	TPIN3[1]	TPIN3[0]
1EH****	TPIN4[7]	TPIN4[6]	TPIN4[5]	TPIN4[4]	TPIN4[3]	TPIN4[2]	TPIN4[1]	TPIN4[0]

Notes: *The address 1F must be written with the value 01H prior to reading these device inputs.

**The address 1F must be written with the value 02H prior to reading these device inputs.

***The address 1F must be written with the value 03H prior to reading these device inputs.

****The address 1F must be written with the value 04H prior to reading these device inputs.

A write to one of the following locations followed a falling edge (logic 1 to logic 0 transition) on the VCLK input forces each output to the value in the corresponding bit position:

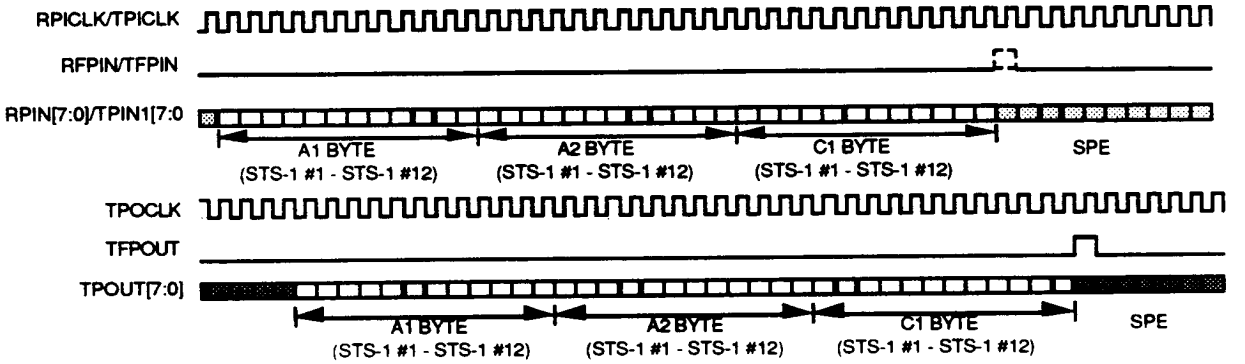
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12H*			RPOUT40	RPOUT30	RPOUT20	RPOUT10	RFPOUT	RPOCLK
14H*			TAPSCLK	TOWCLK	TDLCLK	TFPOUT	TPOUT0	TPOCLK
18H	RAPS	BIPCLK	BIPE	RFERF	RLAIS			
1AH			INTB†	RAPSCLK	RDL	RDLCLK	ROW	ROWCLK
1EH				INTB†				

Notes: †The Master Interrupt Enable register must be written to enable the assertion of the INTB signal.

*The value on outputs TPOUT[N], RPOUT1[N] RPOUT2[N], RPOUT3[N], and RPOUT4[N] are clocked into outputs TPOUT[N+1], RPOUT1[N+1], RPOUT2[N+1], RPOUT3[N+1], and RPOUT4[N+1] ($0 \leq N \leq 6$) respectively by the falling VCLK edge

FUNCTIONAL TIMING

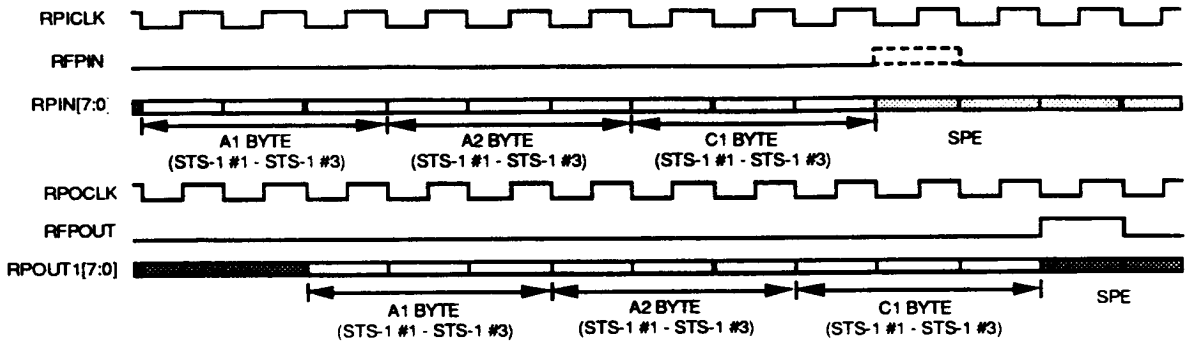
Fig. 1 TLOP STS12 Frame Pulse and Data Alignment



The Transmit Line Overhead Processor (TLOP) frame pulse and data alignment timing diagram (Fig. 1) illustrates the transmit frame pulse input/output alignment within an STS-12 frame for two different SLTX input configurations. First, in the payload loopback configuration (ie. when the PLE bit is set) the receive inputs RPICLK, RFPIN and RPIN[7:0] are connected to the inputs of TLOP. Second, in the BIMX bypass configuration (ie. when the MXB is set and the PLE is reset) the transmit inputs TPICLK, TFPIN and TPIN1[7:0] are connected directly to TLOP. The delay between the incoming streams (on RPIN[7:0]/TPIN[7:0]) and the outgoing

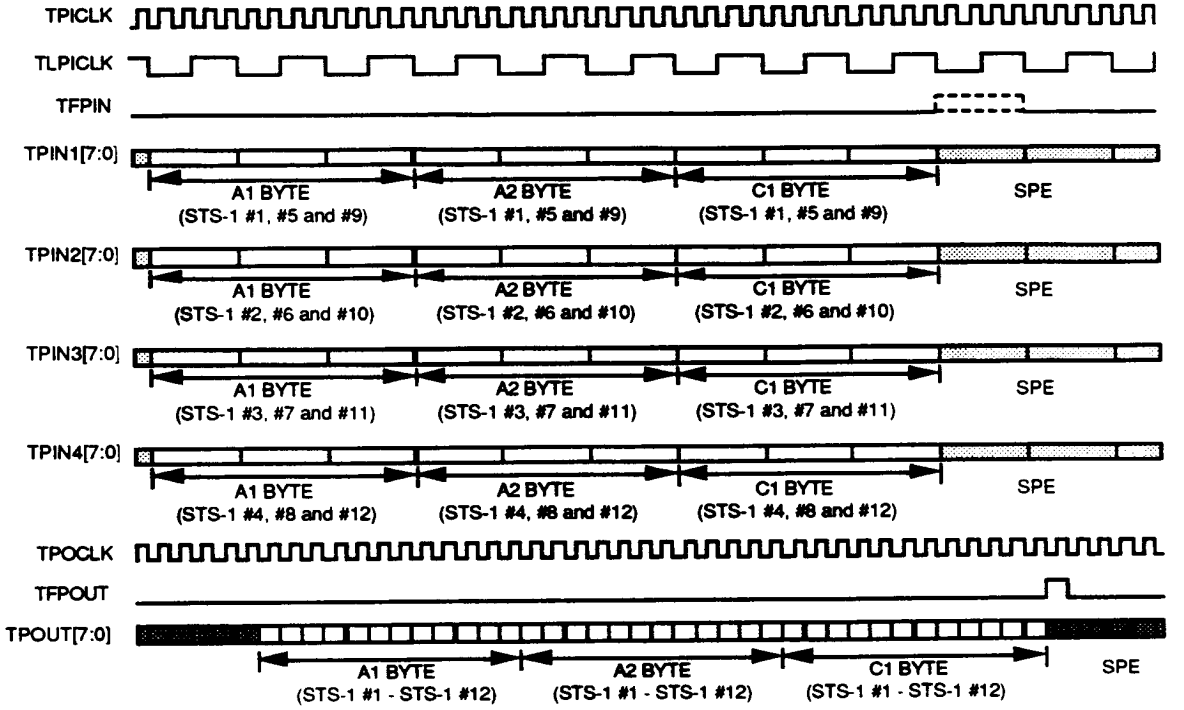
stream TPOUT[1:0] is composed of an asynchronous delay and a logical delay. This delay can range between 36 ns and 56 ns for the STS-12 mode, between 115 ns and 135 ns for the STS-3 mode and between 325 ns and 345 ns for the STS-1 mode. Similar to the diagram above for all other STS rates the frame pulse output, TFPOUT, is aligned to the first byte of the outgoing synchronous payload envelope (SPE). The input frame pulse is aligned to the first byte of the incoming SPE at all rates and it is not always necessary for this pulse to be present.

Fig. 2 RLOP STS3 Frame Pulse and Data Alignment



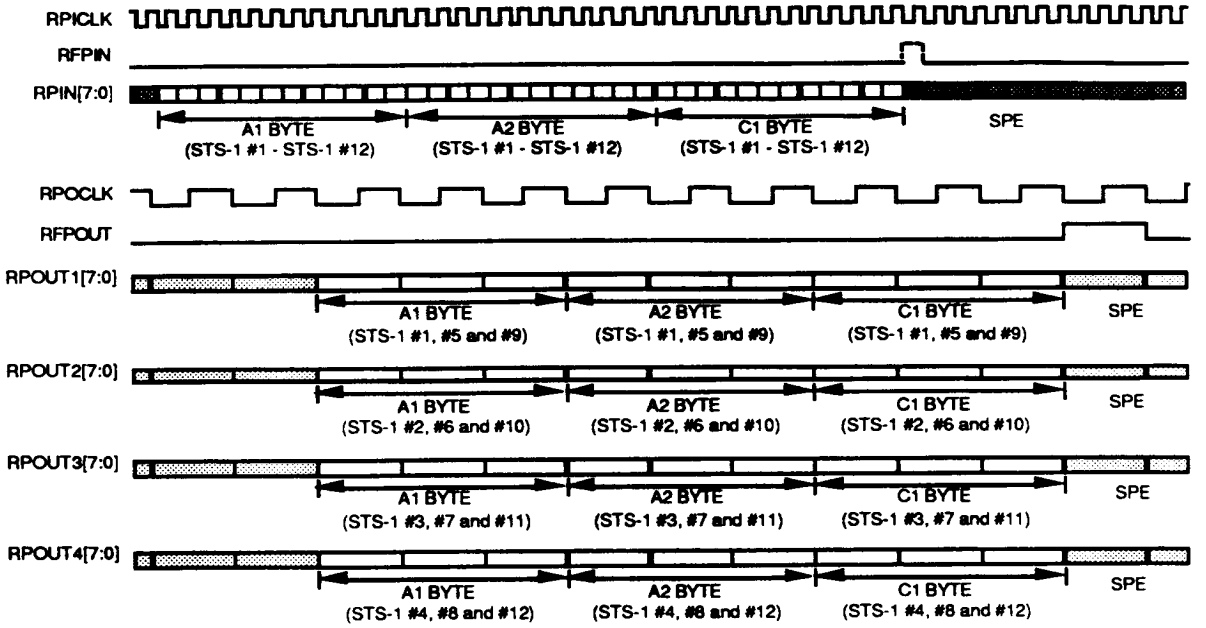
The Receive Line Overhead Processor (RLOP) frame pulse and data alignment timing diagram (Fig. 2) illustrates the receive frame pulse input/output alignment within an STS-3 frame. The SLTX is in the BIDX bypass configuration (ie. when the DXB bit is set) the receive inputs RPICLK, RFPIN and RPIN[7:0] are connected directly to the receive outputs RPOCLK, RFPOUT and RPOUT1[7:0]. Similar to the diagram above for the STS1 rate the frame pulse output, RFPOUT, is aligned to the first byte of the outgoing SPE. The input frame pulse is aligned to the first byte of the incoming SPE at both rates and it is not always necessary for this pulse to be present.

Fig. 3 BIMX-TLOP Frame Pulse and Data Alignment (STS3-to-STS12)



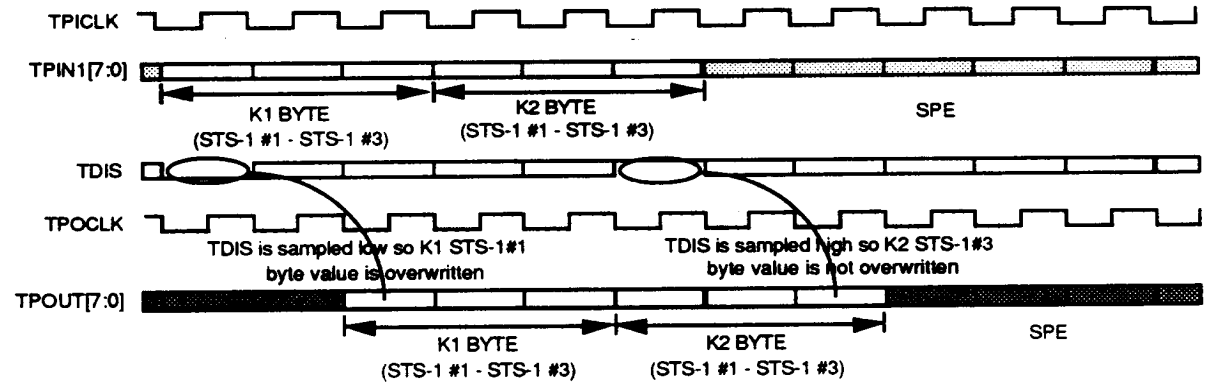
The BIMX-TLOP frame pulse and data alignment timing diagram (Fig. 3) illustrates the transmit frame pulse and data alignment within four incoming STS-3 frames and a single outgoing STS-12 frame. The delay between the incoming streams (on TPIN1[7:0], TPIN2[7:0], TPIN3[7:0] and TPIN4[7:0]) and the outgoing stream TPOUT[1:0] is composed of an asynchronous delay and a logical delay. This delay can range between 93 ns and 167 ns for the STS-3-to-STS-12 mode and between 275 ns and 466 ns for the STS-1-to-STS-3 mode. Similar to the diagram above for all other multiplexing modes the frame pulse output, TFPOUT, is aligned to the first byte of the outgoing SPE. The input frame pulse is aligned to the first byte of the incoming SPE in all multiplexing modes and it is not always necessary for this pulse to be present.

Fig. 4 RLOP-BIDX Frame Pulse and Data Alignment (STS12-to-STS3)



The RLOP-BIDX frame pulse and data alignment timing diagram (Fig. 4) illustrates the receive frame pulse and data alignment within a single incoming STS-12 frame and four outgoing STS-3 frames. Similar to the diagram above for STS3-STS1 and STS9-STS3 the frame pulse output, RFPOUT, is aligned to the first byte of the outgoing SPE. The input frame pulse is aligned to the first byte of the incoming SPE in all multiplexing modes and it is not always necessary for this pulse to be present.

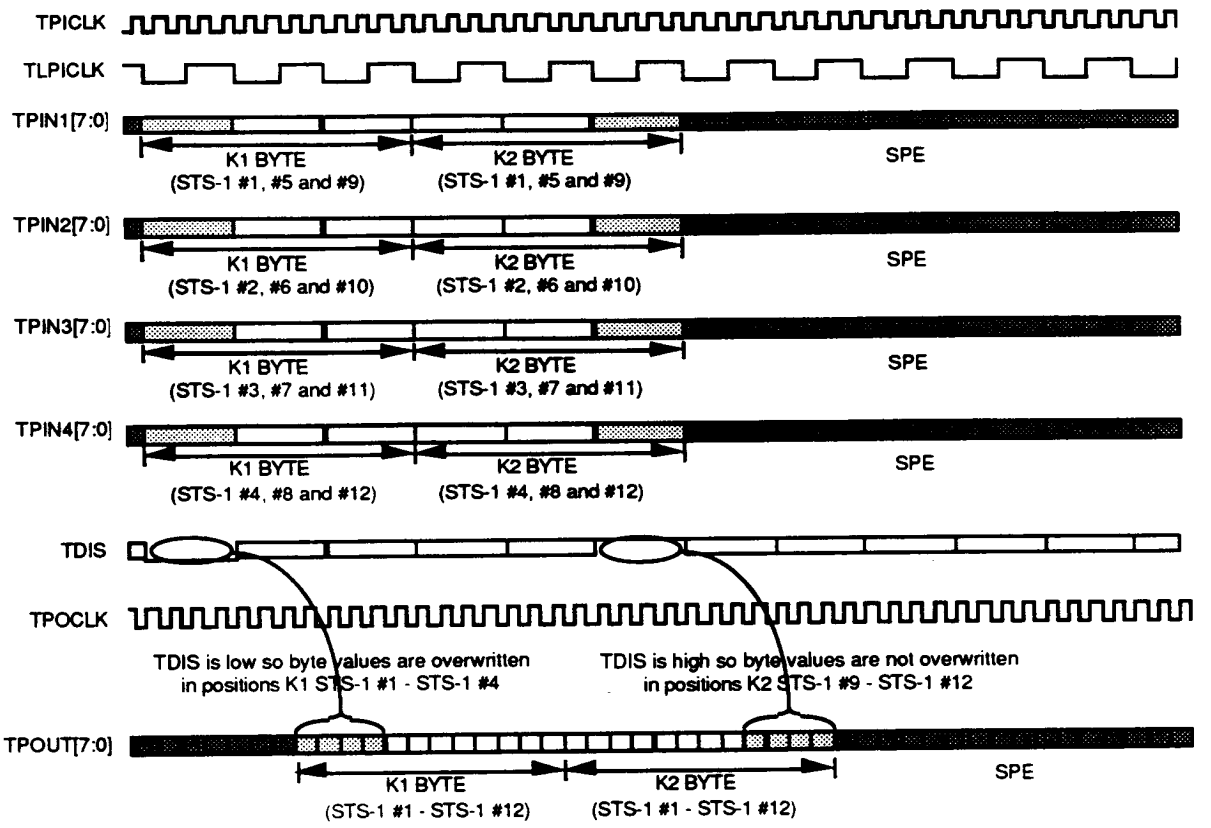
Fig. 5 Line Layer Overwrite Enable and Disable with BIMX bypassed



The line layer overwrite enable and disable timing diagram (Fig. 5) illustrates the operation of the SLTX, in BIMX bypass mode at the STS-3 rate, when the line layer byte overwrite feature is enabled and disabled for the incoming data on TPIN1[7:0].

The diagram shows input TDIS first sampled low during the K1 STS-1 #1 byte and then sampled high during the K2 STS-1 #3 byte. Since TDIS was low the byte value in the K1 STS-1 #1 byte position for the output data TPOUT[7:0] is overwritten with the value shifted in on TAPS. However, the byte value in the K2 STS-1 #3 position for the output data TPOUT[7:0] is not overwritten with an all zero byte because TDIS was sampled high during this byte position on the input data stream. The TDIS input can be used in a similar manner with any byte in the line overhead of an STS-N frame.

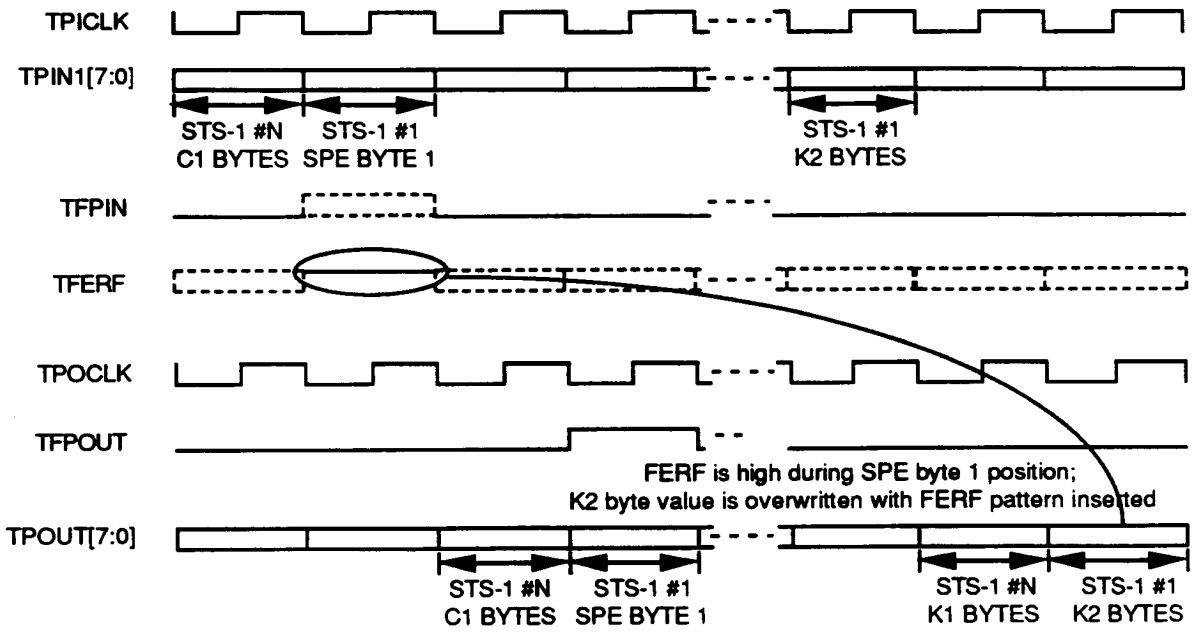
Fig. 6 BIMX-TLOP Line Layer Overwrite Enable and Disable



The BIMX line layer overwrite enable and disable timing diagram (Fig. 6) illustrates the operation of the SLTX, in the STS-3-to-STS-12 configuration, when the line layer byte overwrite feature is enabled and disabled for the incoming data on TPIN1[7:0], TPIN2[7:0], TPIN3[7:0] and TPIN4[7:0]. The diagram shows input TDIS first sampled low during the K1 STS-1 #1 - #4 bytes and then sampled high during the K2 STS-1 #9 - #12 bytes. Since TDIS was low the byte values in the K1 STS-1 #1 - #4 byte positions for the output data TPOUT[7:0] are overwritten. However, the byte values in the K2 STS-1 #9- #12 positions for the output data TPOUT[7:0] are not overwritten because TDIS was sampled high during these byte positions on the

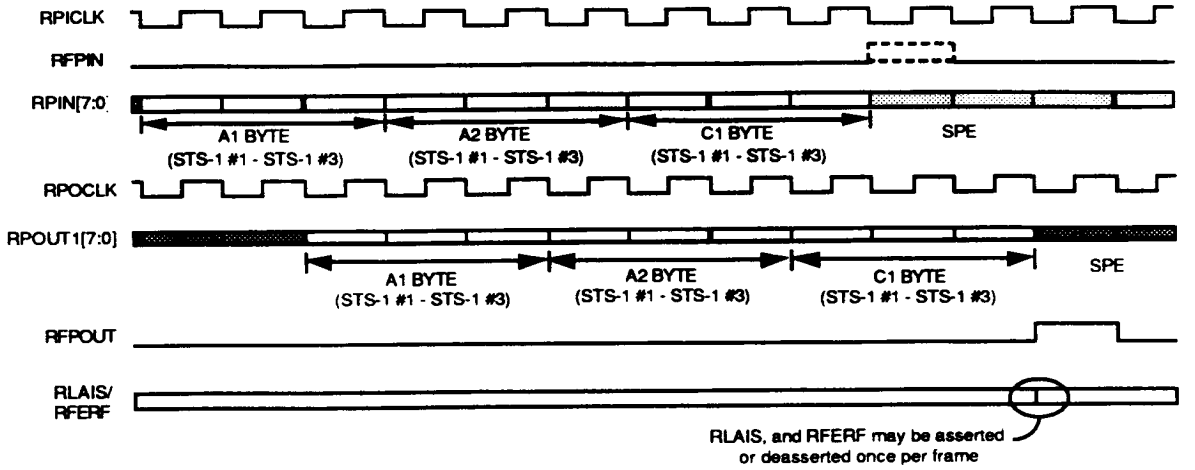
input data streams. The TDIS input can be used in a similar manner with any bytes in the line overhead of an STS-N frame.

Fig. 7 Transmit FERF Insertion



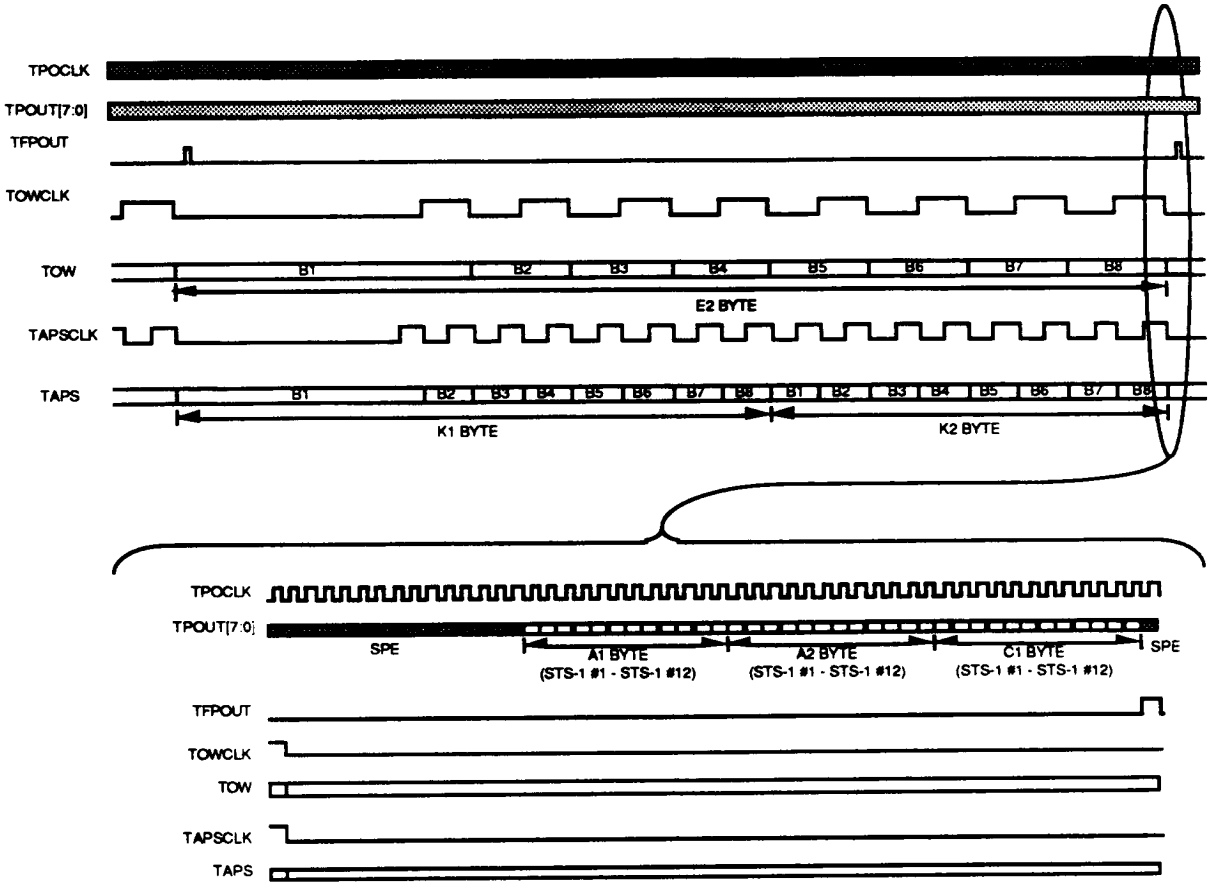
The FERF insertion timing diagram (fig. 7) shows the TFERF input sampled once per frame. Figure illustrates TFERF sampled high during the first byte position. Line FERF is inserted into the STS-1/3/9/12 stream during K2 STS-1 #1. Also illustrated is the location of the framing pulse input, TFPIN, in the STS-1/3/9/12 input stream, TPIN1[7:0]. It is not necessary for TFPIN to be present every frame.

Fig. 8 Receive FERF and LAIS Assertion/Deassertion



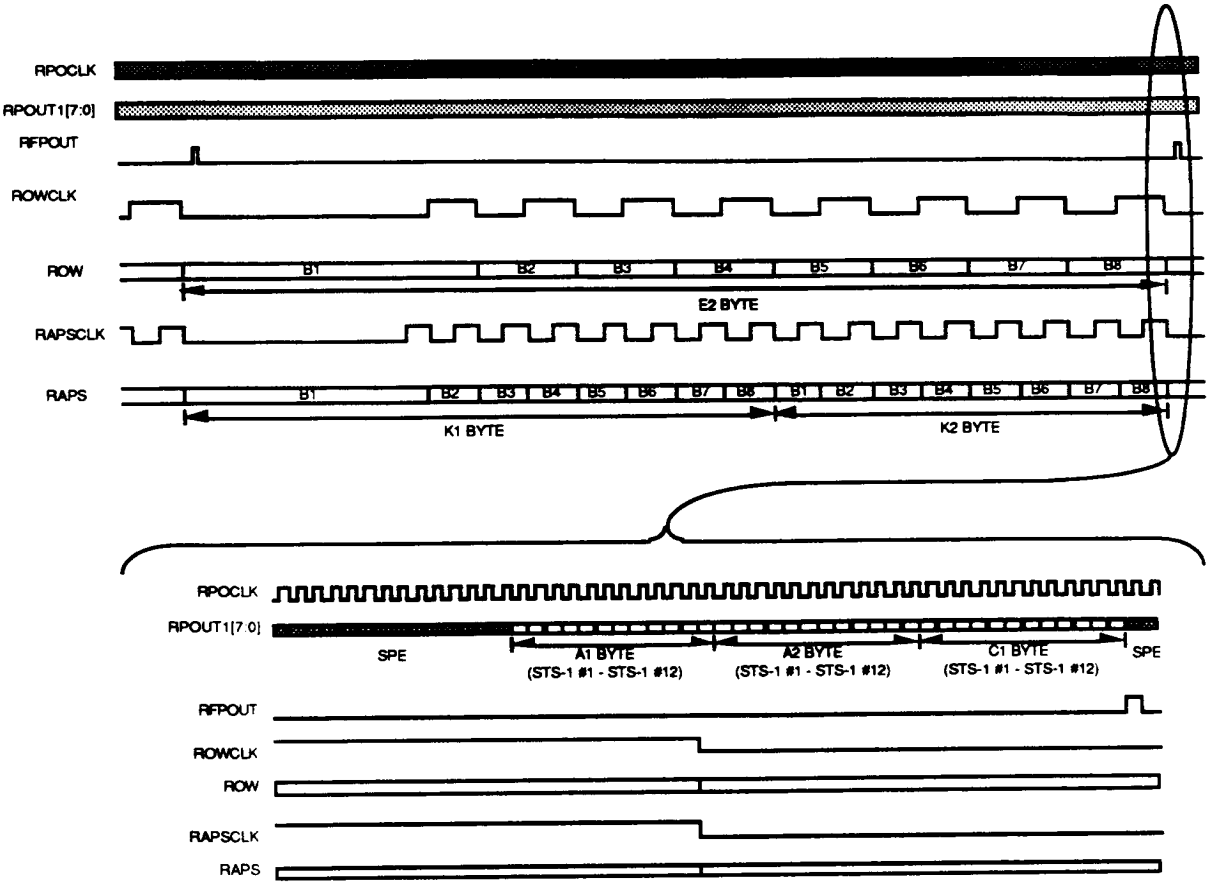
The FERF and LAIS Assertion/Deassertion timing diagram (Fig. 8) shows the assertion and deassertion timing of outputs RFERF and RLAIS for the STS-3 rate. RFERF or RLAIS may be asserted or deasserted once per frame as indicated.

Fig. 9 Transmit OW and APS Clock and Data Alignment



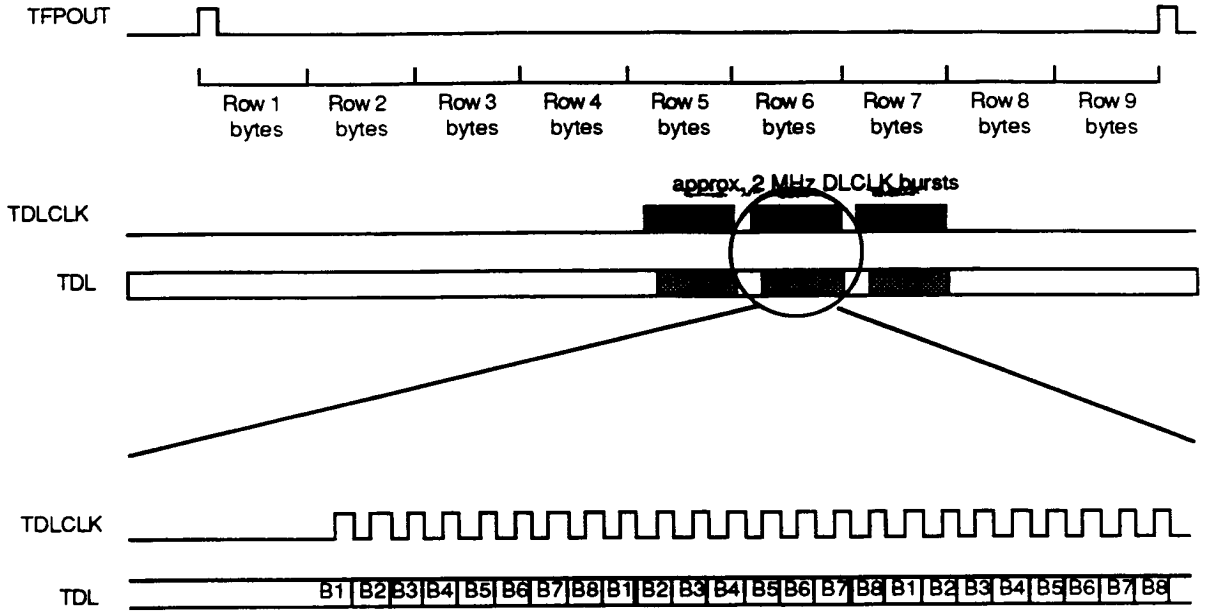
The Transmit OW and APS Clock and Data Alignment timing diagram (Fig. 9) shows the relationship between the TOW and TAPS serial data inputs and their associated clocks, TOWCLK and TAPSCLK respectively. TOWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. TAPSCLK is a 144 kHz 50% duty cycle clock that is gapped to produce a 128 kHz nominal rate and is aligned as shown in the timing diagram. The K1, K2 and E2 bytes shifted into the SLTX on TAPS and TOW in the frame shown are inserted in the corresponding Line Overhead channels in the next frame.

Fig. 10 Receive OW and APS Clock and Data Alignment



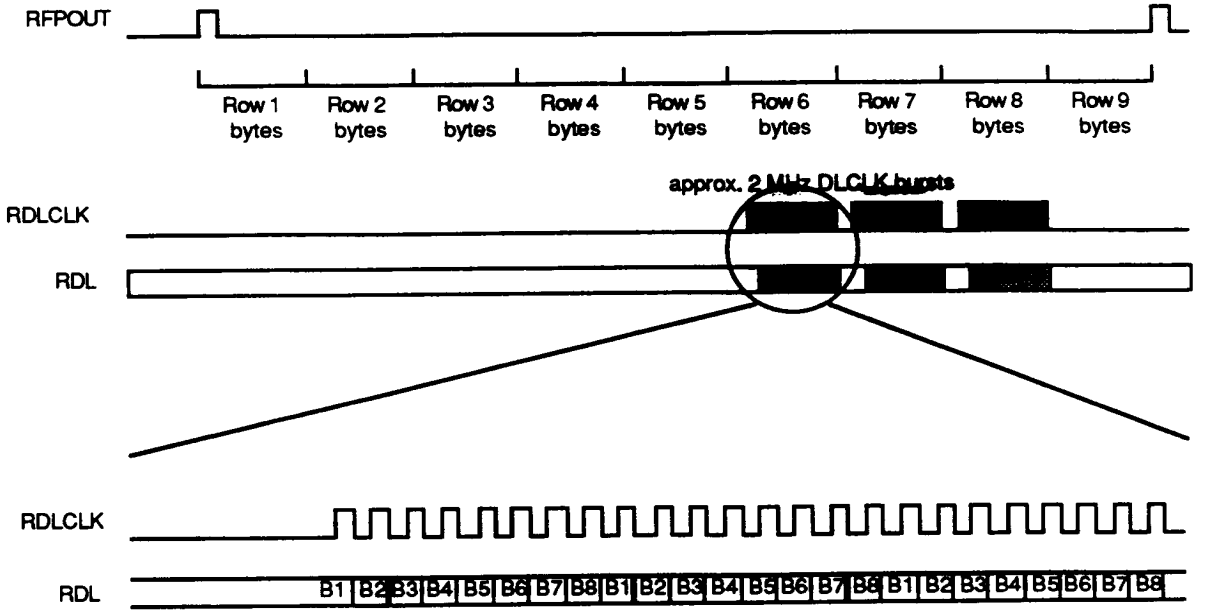
The Receive OW and APS Clock and Data Alignment timing diagram (Fig. 10) shows the relationship between the ROW and RAPS serial data outputs and their associated clocks, ROWCLK and RAPSCLK respectively. ROWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. RAPSCLK is a 144 kHz 50% duty cycle clock that is gapped to produce a 128 kHz nominal rate and is aligned as shown in the timing diagram. The K1, K2 and E2 bytes shifted out of the SLTX on RAPS and ROW in the frame shown are extracted from the corresponding Line Overhead channels in the previous frame.

Fig. 11 Transmit Data Link Clock and Data Alignment



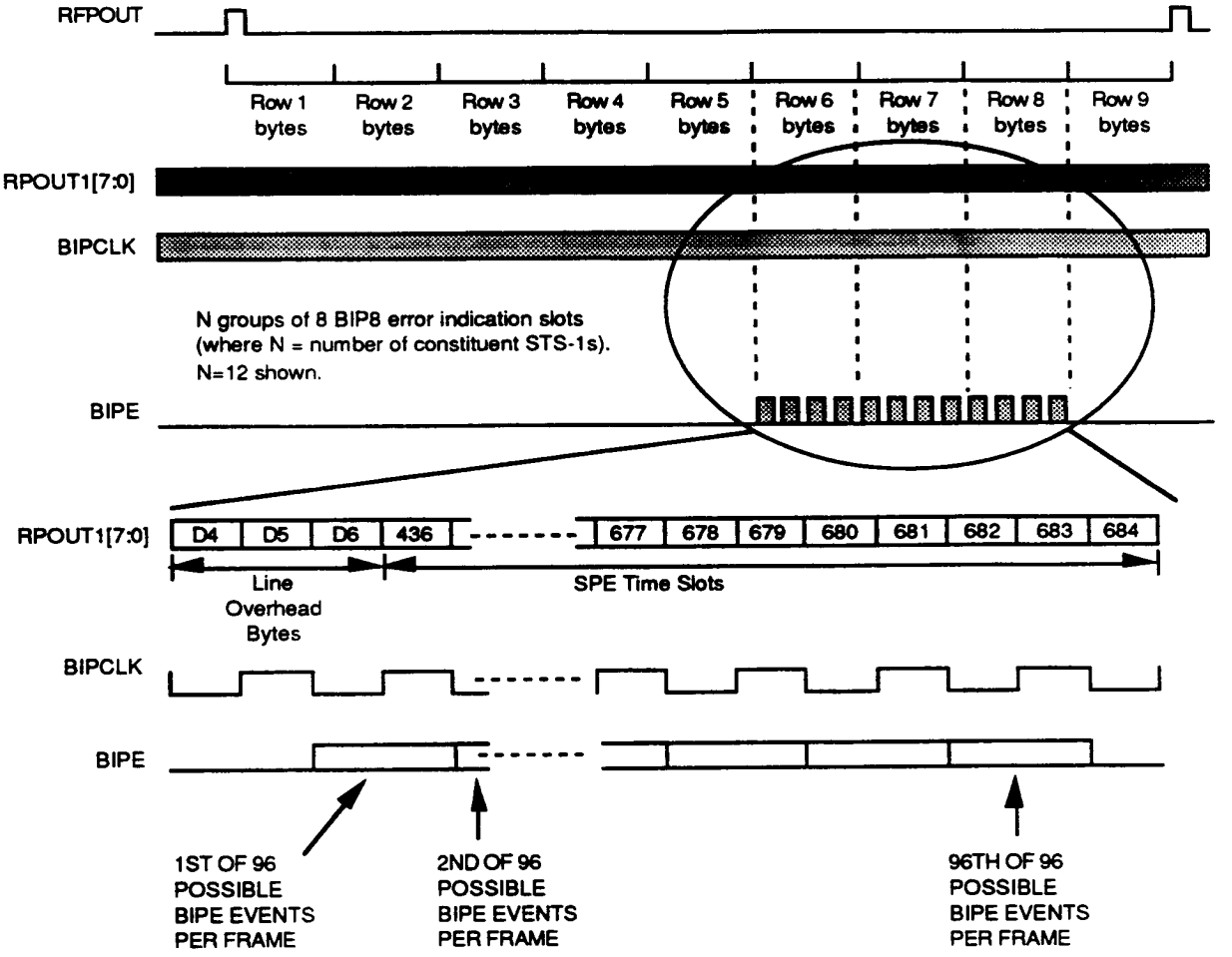
The Transmit Data Link Clock and Data Alignment timing diagram (Fig. 11) shows the relationship between the TDL serial data input, its associated clock, TDLCLK and TFPOUT. TDLCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with TFPOUT as shown in the timing diagram. TDL is sampled on the rising TDLCLK edge. The D4-D12 bytes shifted into the SLTX in the frame shown are inserted in the corresponding transmitted line overhead channels in the following frame.

Fig. 12 Receive Data Link Clock and Data Alignment



The Receive Data Link Clock and Data Alignment timing diagram (Fig. 12) shows the relationship between the RDL serial data output, its associated clock, RDLCLK and RFPOUT. RDLCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with RFPOUT as shown in the timing diagram. RDL is updated on the falling RDLCLK edge. The D4-D12 bytes shifted out of the SLTX in the frame shown are extracted from the corresponding received line overhead channels in the same frame.

Fig. 13 BIP-8 Error Event Occurrence



The BIP-8 Error Event Occurrence timing diagram (Fig. 13) shows the location of BIPE events in the STS-1/3/9/12 frame. Up to 8N (N=1,3,9,12) BIP-8 errors may be detected per frame.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-40°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +7.0V
Voltage on Any Pin	-0.5V to +7.0V
Output Current (all pins driving)	4 mA
Static Discharge Voltage	2000 V
Latch-Up Current (T_A = 0°C to +85°C)	400 mA

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)
COUT	Output Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)
CIO	Bidirectional Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)

D.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	0.3X VDD	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	0.7X VDD	V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_T	Reset Input High Voltage	2.3	2.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage	0.5	1.2	Volts	
I_{ILPU}	Input Low Current	-26	-110	µA	$V_{IL} \leq 1.65$ V, Notes 1, 3
I_{IHPU}	Input High Current	-48	-110	µA	$V_{IH} \geq 3.85$ V, Notes 1, 3
I_{IL}	Input Low Current	-10	0	µA	$V_{IL} \leq 1.65$ V, Notes 2, 3
I_{IH}	Input High Current	-10	0	µA	$V_{IH} \geq 3.85$ V, Notes 2, 3
I_{DDOP}	Operating Current		379	mA	V_{DD} = 5.5 V, Outputs Unloaded, TPICLK = 78 MHz RPICLK = 78 MHz
I_{DDSB}	Standby Current		100	µA	V_{DD} = 5.5 V, Outputs Unloaded,

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

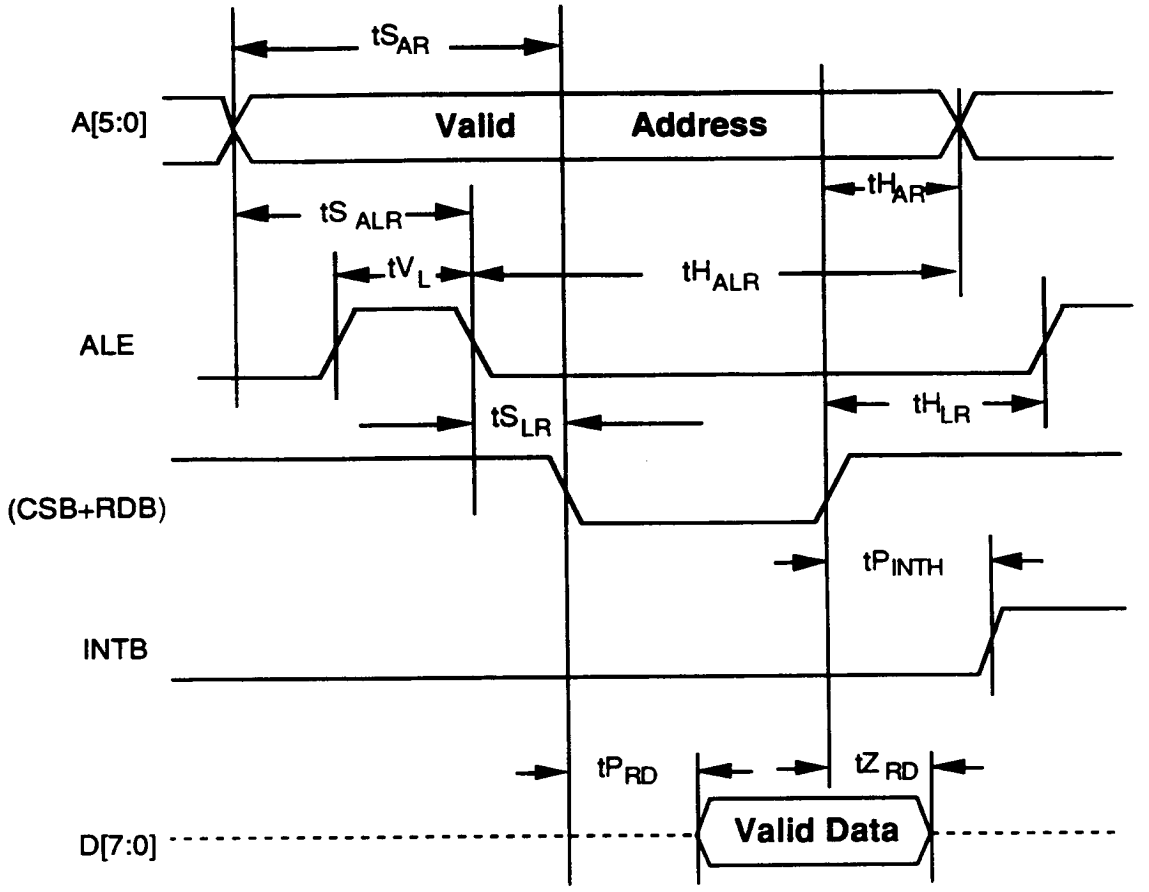
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

Microprocessor Interface Read Access (Fig. 14)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		20	ns
tP_{INTH}	Valid Read Deasserted to INTB High		50	ns

Fig. 14 Microprocessor Interface Read Access Timing



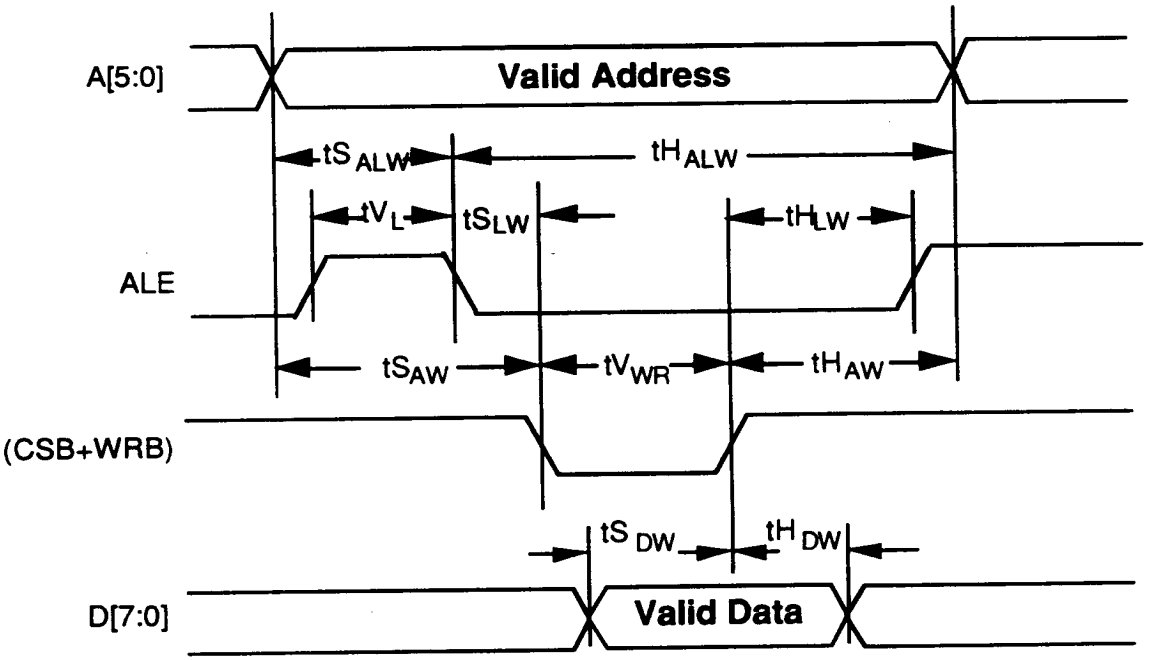
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.
5. In non-multiplexed address/data bus applications, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
6. Parameter tH_{AR} is not applicable is address latching is used.

Microprocessor Interface Write Access (Fig. 15)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 15 Microprocessor Interface Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.
4. Parameter tH_{AW} is not applicable is address latching is used.

SLTX TIMING CHARACTERISTICS

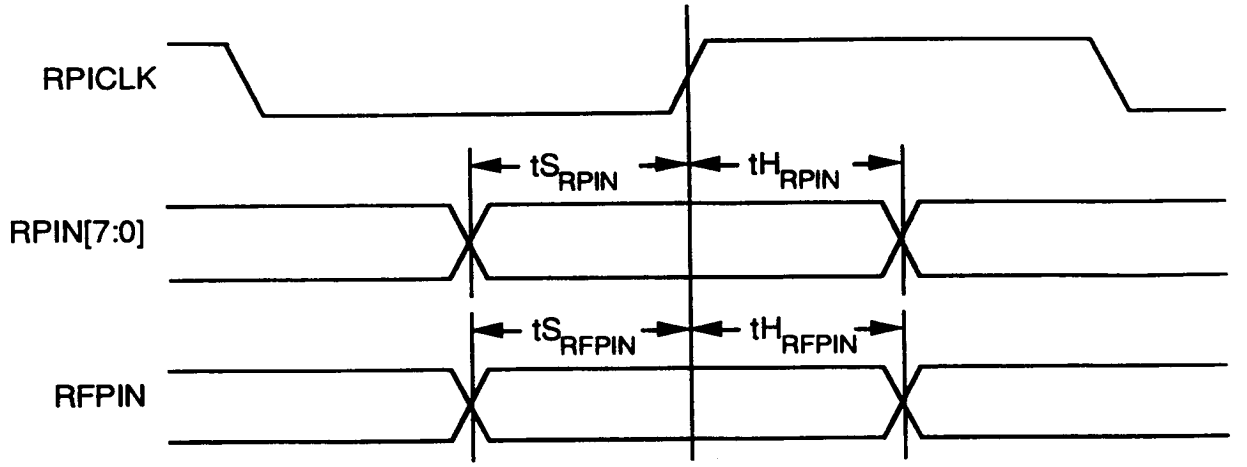
(T_A = 0°C to +70°C, V_{DD} = 5 V ±10%)

INPUT TIMING

Receive Input (Fig. 16)

Symbol	Description	Min	Max	Units
	RPICLK Frequency (nominally 6.48 MHz, 6.408 MHz, 19.224 MHz, 19.44 MHz, 57.672 MHz, 58.32 MHz, 76.896 MHz, or 77.76 MHz)		78	MHz
	RPICLK Duty Cycle	45	55	%
tS_{RPIN}	RPIN[7:0] Set-up Time to RPICLK	1		ns
tH_{RPIN}	RPIN[7:0] Hold Time to RPICLK	6		ns
tS_{RFPIN}	RFPIN Set-Up Time to RPICLK	1		ns
tH_{RFPIN}	RFPIN Hold Time to RPICLK	6		ns

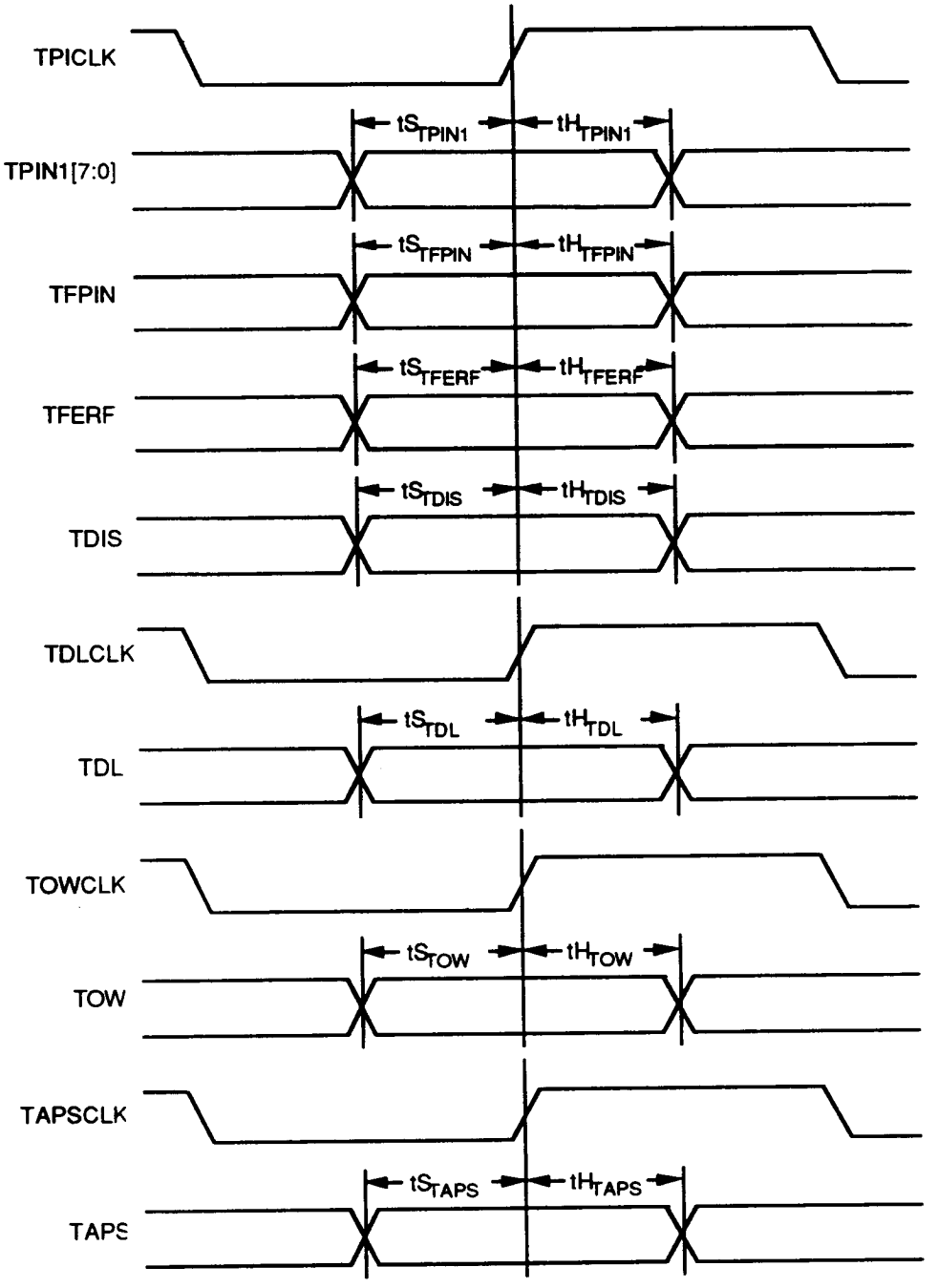
Fig. 16 Receive Input Timing



Transmit Input to TLOP with BIMX Bypassed (Fig. 17)

Symbol	Description	Min	Max	Units
	TPICLK Frequency (nominally 6.48 MHz, 6.408 MHz, 19.224 MHz, 19.44 MHz, 57.672 MHz, 58.32 MHz, 76.896 MHz, or 77.76 MHz)		78	MHz
	TPICLK Duty Cycle	45	55	%
tS_{TPIN1}	TPIN1[7:0] Set-up Time to TPICLK	1		ns
tH_{TPIN1}	TPIN1[7:0] Hold Time to TPICLK	6		ns
tS_{TFPIN}	TFPIN Set-Up Time to TPICLK	1		ns
tH_{TFPIN}	TFPIN Hold Time to TPICLK	6		ns
tS_{TFERF}	TFERF Set-up Time to TPICLK	1		ns
tH_{TFERF}	TFERF Hold Time to TPICLK	6		ns
tS_{TDIS}	TDIS Set-up Time to TPICLK	1		ns
tH_{TDIS}	TDIS Hold Time to TPICLK	6		ns
tS_{TDL}	TDL Set-up Time to TDLCLK	20		ns
tH_{TDL}	TDL Hold Time to TDLCLK	20		ns
tS_{TOW}	TOW Set-up Time to TOWCLK	20		ns
tH_{TOW}	TOW Hold Time to TOWCLK	20		ns
tS_{TAPS}	TAPS Set-up Time to TAPSCLK	20		ns
tH_{TAPS}	TAPS Hold Time to TAPSCLK	20		ns

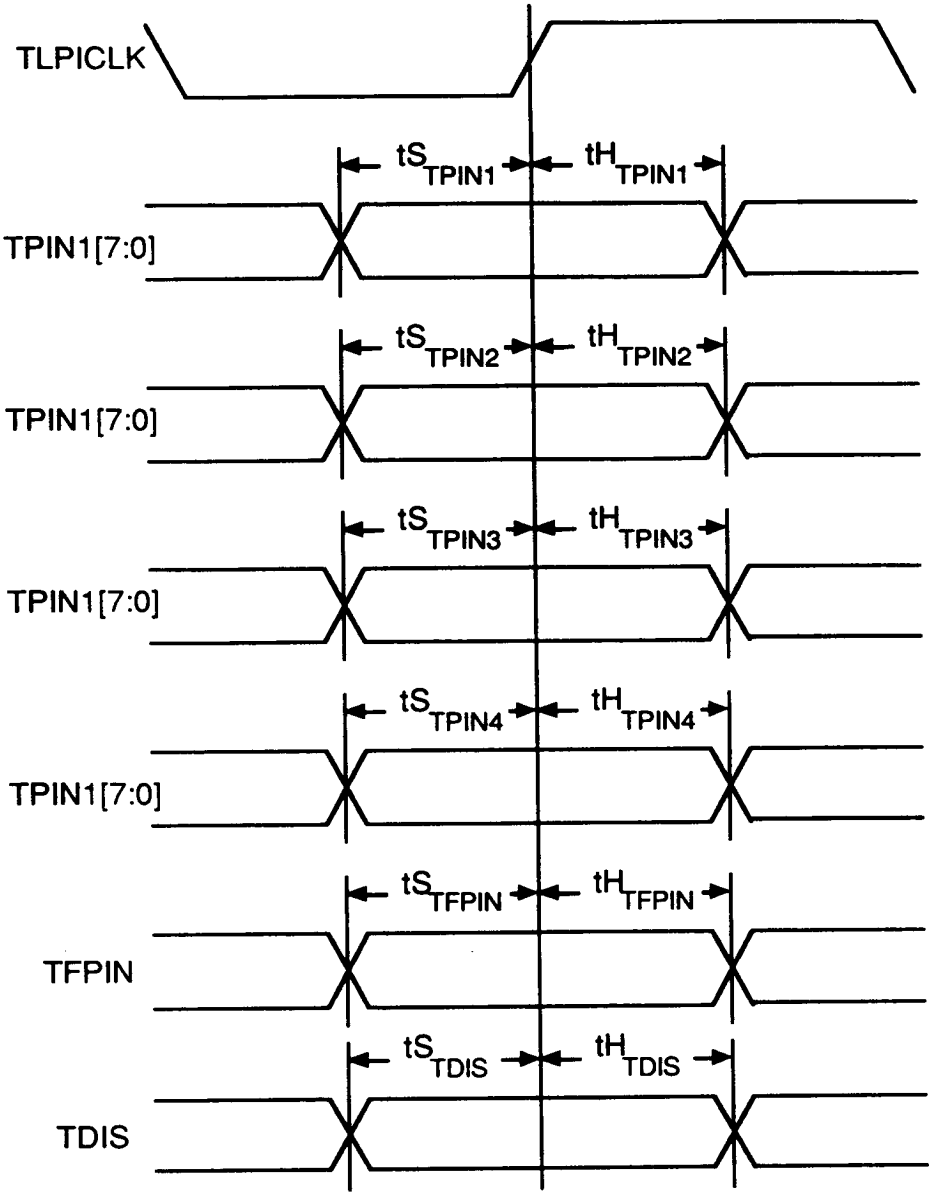
Fig. 17 Transmit Input Timing to TLOP with BIMX Bypassed



Transmit Input to BIMX (Fig. 18)

Symbol	Description	Min	Max	Units
	TPICLK Frequency (nominally 19.44 MHz, 58.32 MHz, or 77.76 MHz)		78	MHz
	TPICLK Duty Cycle	45	55	%
	TLPICLK Frequency (nominally 6.48 MHz or 19.44 MHz)		20	MHz
	TLPICLK Duty Cycle	33	67	%
tS_{TPIN1}	TPIN1[7:0] Set-up Time to TLPICLK	10		ns
tH_{TPIN1}	TPIN1[7:0] Hold Time to TLPICLK	10		ns
tS_{TPIN2}	TPIN2[7:0] Set-up Time to TLPICLK	10		ns
tH_{TPIN2}	TPIN2[7:0] Hold Time to TLPICLK	10		ns
tS_{TPIN3}	TPIN3[7:0] Set-up Time to TLPICLK	10		ns
tH_{TPIN3}	TPIN3[7:0] Hold Time to TLPICLK	10		ns
tS_{TPIN4}	TPIN4[7:0] Set-up Time to TLPICLK	10		ns
tH_{TPIN4}	TPIN4[7:0] Hold Time to TLPICLK	10		ns
tS_{TFPIN}	TFPIN Set-Up Time to TLPICLK	10		ns
tH_{TFPIN}	TFPIN Hold Time to TLPICLK	10		ns
tS_{TDIS}	TDIS Set-up Time to TLPICLK	10		ns
tH_{TDIS}	TDIS Hold Time to TLPICLK	10		ns

Fig. 18 Transmit Input Timing to BIMX

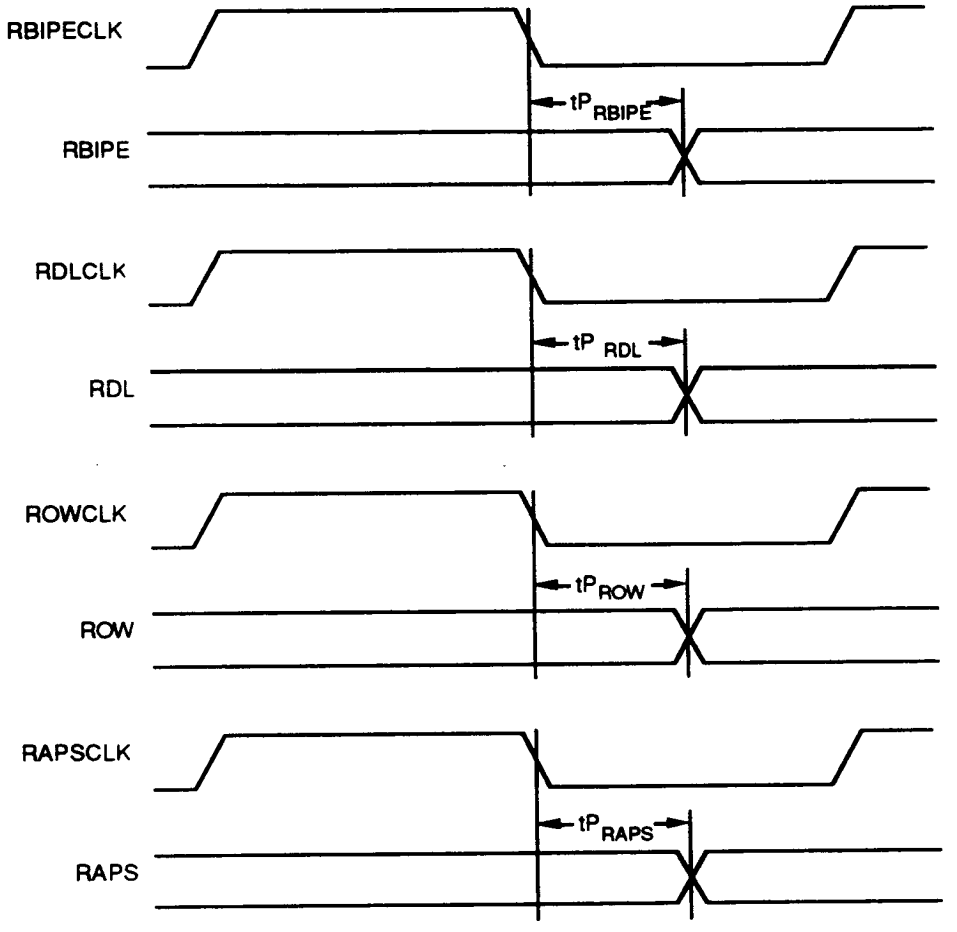


OUTPUT TIMING

Receive Output of RLOP (Fig. 19)

Symbol	Description	Min	Max	Units
tP_{RBIPE}	RBIPECLK Low to RBIPE Valid Prop Delay	2	10	ns
tP_{RDL}	RDLCLK Low to RDL Valid Prop Delay	2	10	ns
tP_{ROW}	ROWCLK Low to ROW Valid Prop Delay	2	10	ns
tP_{RAPS}	RAPSCLK Low to RAPS Valid Prop Delay	2	10	ns

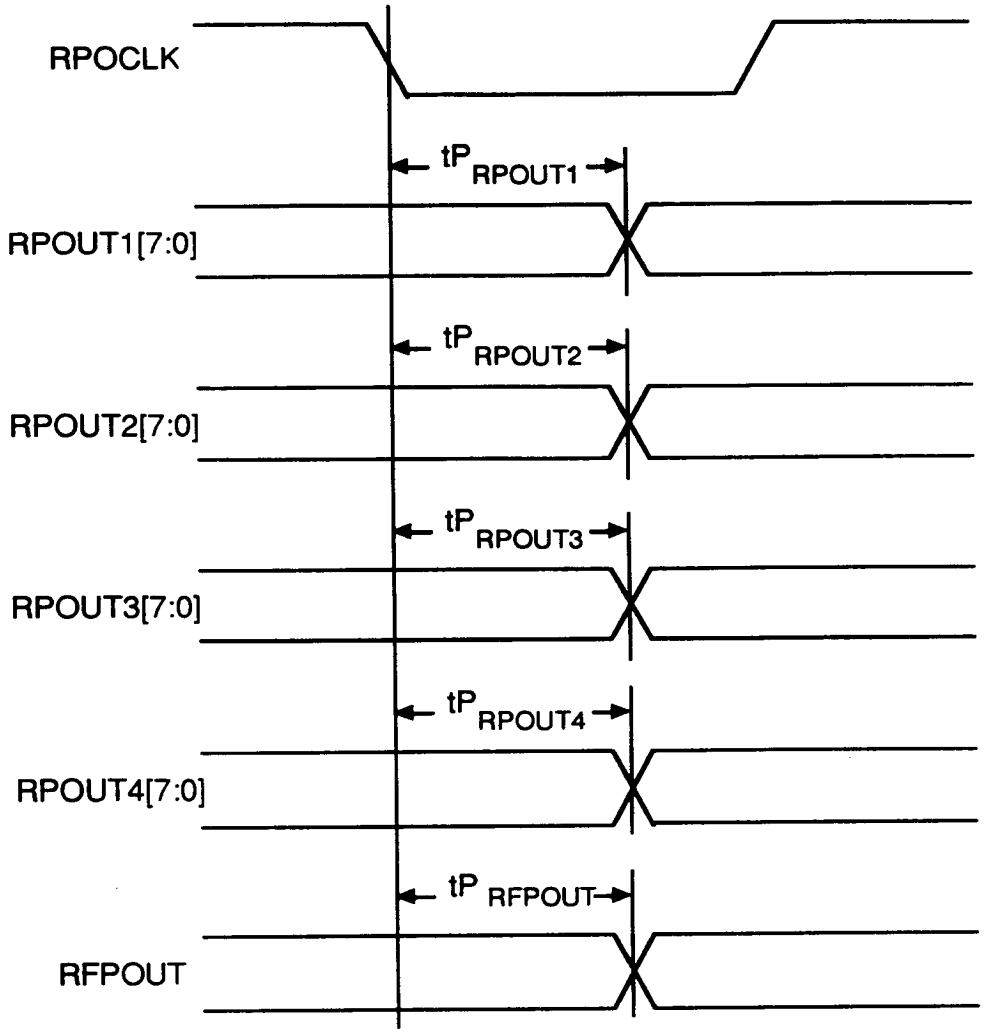
Fig. 19 Receive Output Timing of RLOP



Receive Output of BIDX (Fig. 20)

Symbol	Description	Min	Max	Units
tP_{RPOUT1}	RPOCLK Low to RPOUT1[7:0] Valid Prop Delay	2	10	ns
tP_{RPOUT2}	RPOCLK Low to RPOUT2[7:0] Valid Prop Delay	2	10	ns
tP_{RPOUT3}	RPOCLK Low to RPOUT3[7:0] Valid Prop Delay	2	10	ns
tP_{RPOUT4}	RPOCLK Low to RPOUT4[7:0] Valid Prop Delay	2	10	ns
tP_{RFPOUT}	RPOCLK Low to RFPOUT Valid Prop Delay	2	10	ns

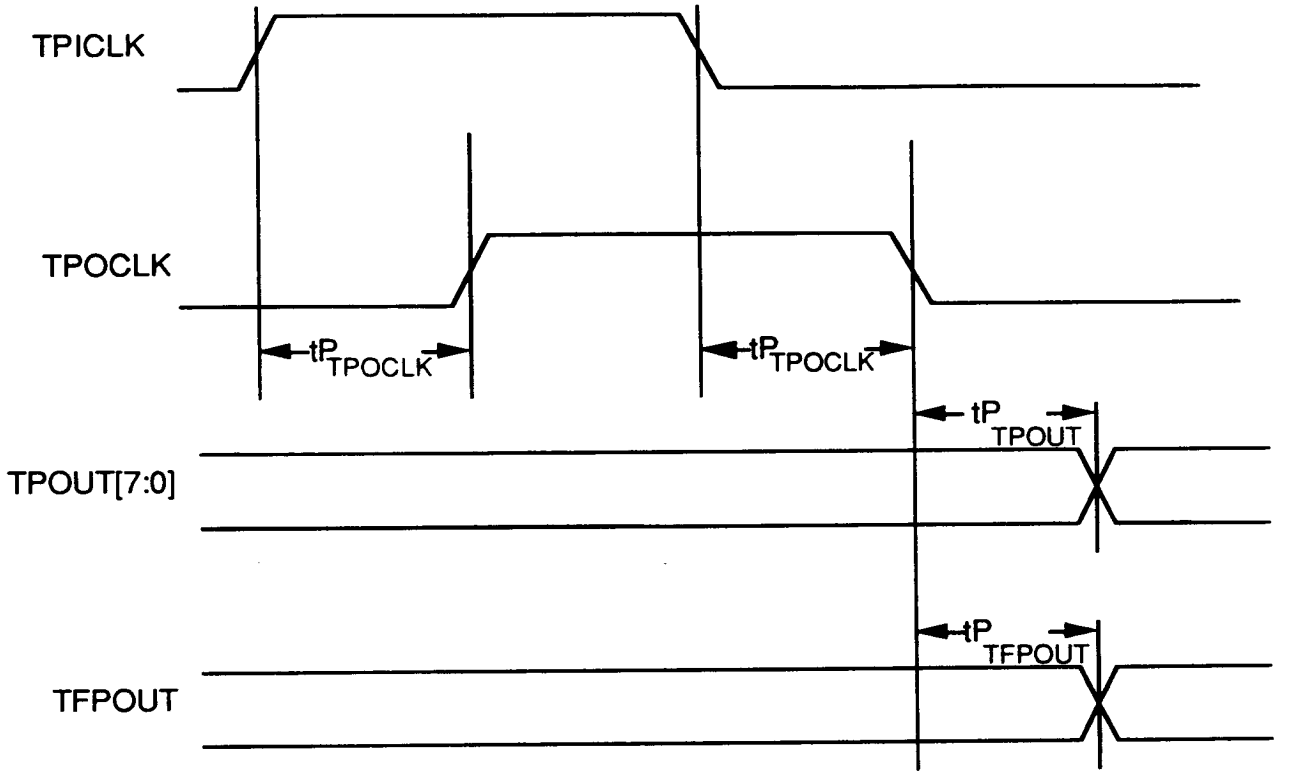
Fig. 20 Receive Output Timing of BIDX



Transmit Output of TLOP (Fig. 21)

Symbol	Description	Min	Max	Units
tP_{TPOCLK}	TPICLK Edge to TPOCLK Edge	14	50	ns
tP_{TPOUT}	TPOCLK Low to TPOUT[7:0] Valid Prop Delay	0	4	ns
tP_{TFPOUT}	TPOCLK Low to TFPOUT Valid Prop Delay	0	4	ns

Fig. 21 Transmit Output Timing of TLOP



NOTES

910420P2 ref 900903P3 Issue date: June, 1991.

Printed in Canada

Pacific Microelectronics Centre 8999 Nelson Way Burnaby, BC Canada V5A 4B5 604 293 5755