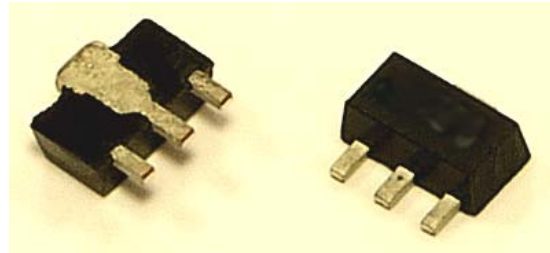


LOW NOISE HIGH LINEARITY PACKAGED PHEMT
FEATURES (1850MHz):

- 29 dBm Output Power (P1dB)
- 14 dB Small-Signal Gain (SSG)
- 1.0 dB Noise Figure
- 44 dBm Output IP3
- 50% Power-Added Efficiency
- FPD2250SOT89E - RoHS compliant


PACKAGE:

GENERAL DESCRIPTION:

The FPD2250SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 μm x 2250 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and i/p power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	28	29		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	12	14		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		50		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS		1.2	1.4	dB
		VDS = 5 V; IDS = 25% IDSS		1.0		
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power		43		dBm
		Matched for best IP3		44		
Saturated Drain-Source Current	IDSS	VDS = 2 V; VGS = 0 V	560	700	825	mA
Maximum Drain-Source Current	IMAX	VDS = 2 V; VGS \approx +1 V		1.1		mA
Transconductance	GM	VDS = 2 V; VGS = 0 V		600		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	10	μA
Pinch-Off Voltage	VP	VDS = 2 V; IDS = 2.25 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	VBDGS	IGS = 2.25 mA	12	18		V
Gate-Drain Breakdown Voltage	VBDGD	IGD = 2.25 mA	12	16		V
Thermal Resistance	R $_{\theta\text{JC}}$			50		$^{\circ}\text{C/W}$

Note: T_{AMBIENT} = 22 $^{\circ}$; RF specification measured at f = 1850 MHz using CW signal (except as noted)

ABSOLUTE MAXIMUM RATING¹:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDss
Gate Current	IG	Forward or reverse current	22mA
RF Input Power ²	PIN	Under any acceptable bias state	525mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	2.5W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits ³		2 or more Max. Limits	

Notes:

¹T_{Ambient} = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device

²Max. RF Input Limit must be further limited if input VSWR > 2.5:1

³Users should avoid exceeding 80% of 2 or more Limits simultaneously

⁴Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power

Total Power Dissipation to be de-rated as follows above 22°C:

$$P_{TOT} = 2.5 - (0.02W/^{\circ}C) \times T_{PACK}$$

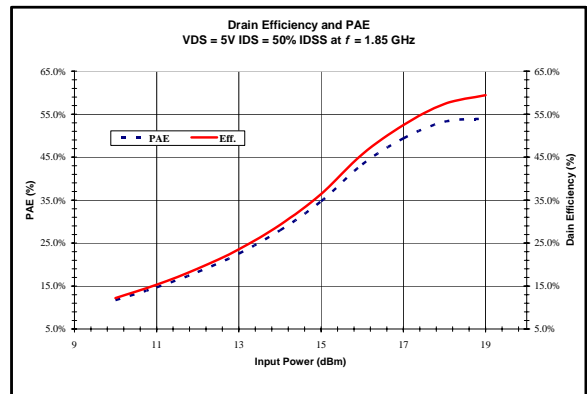
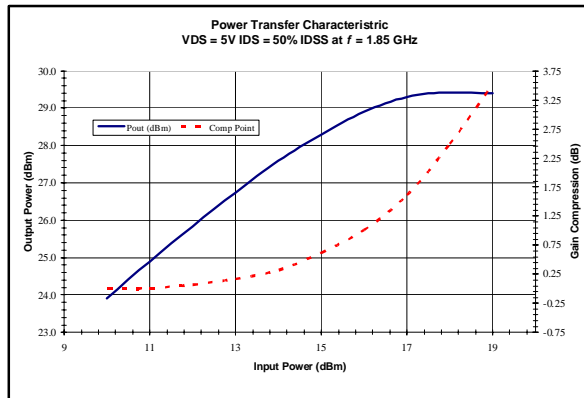
where T_{PACK} = source tab lead temperature above 22°C

(coefficient of de-rating formula is the Thermal Conductivity)

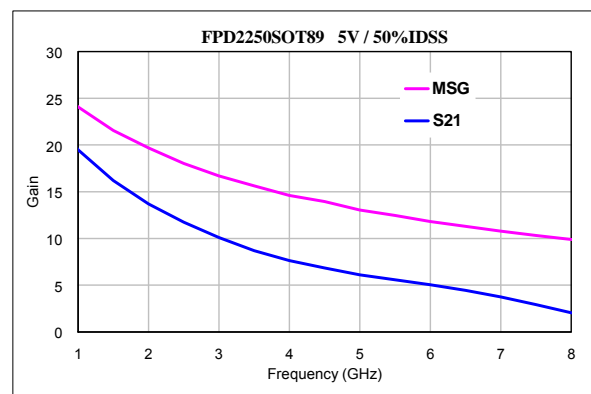
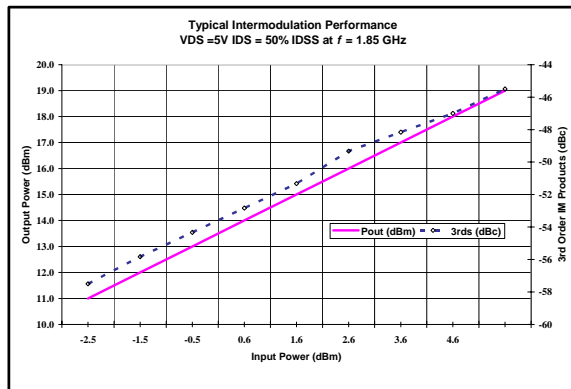
Example: For a 65°C carrier temperature: $P_{TOT} = 2.5W - (0.02 \times (65 - 22)) = 1.64W$

BIASING GUIDELINES:

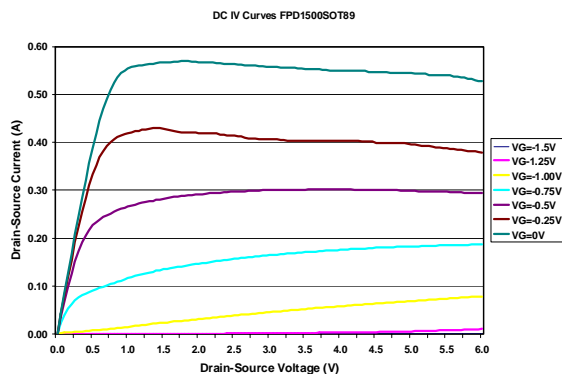
- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B bias of 25-33% of IDSS to achieve better OIP3 and Noise Figure performance is suggested.

TYPICAL TUNED RF PERFORMANCE:


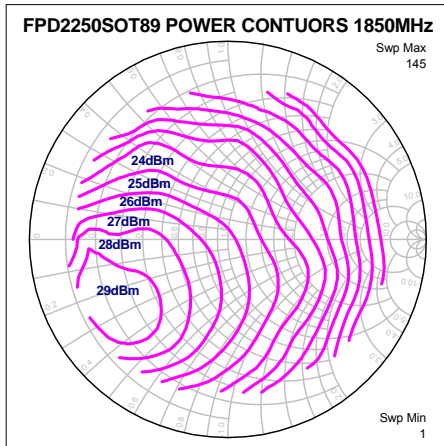
NOTE: Typical power and efficiency is shown above. The devices were biased nominally at $V_{DS} = 5V$, $I_{DS} = 50\%$ of I_{DSS} , at a test frequency of 1.85 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.



Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about $P_{1dB} + 14dBm$. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.

TYPICAL I-V CHARACTERISTICS:


Note: The recommended method for measuring I_{DSS} , or any particular I_{DS} , is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the $V_{DS} > 1.3V$ will generally cause errors in the current measurements, even in stabilized circuits.

TYPICAL OUTPUT PLANE POWER CONTOURS: (VDS = 5v, IDS = 50%IDSS)

1850 MHz

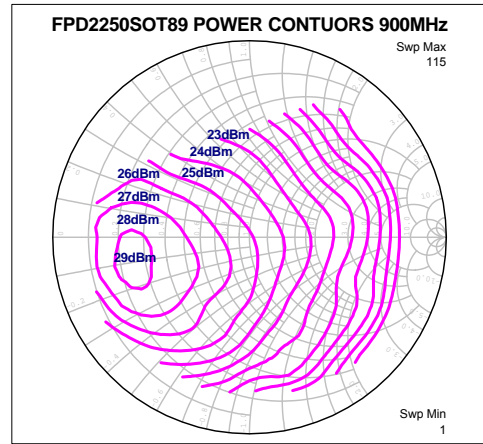
 Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

 Input (Source plane) Γ_s :

$$0.59 \angle -177.5^\circ$$

$$0.25 - j0.02 \text{ (normalized)}$$

$$12.5 - j1.0 \Omega$$

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

900 MHz

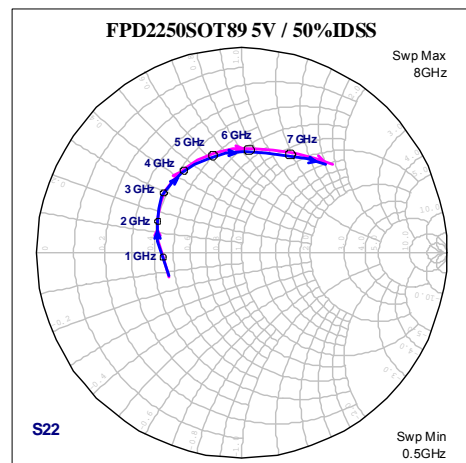
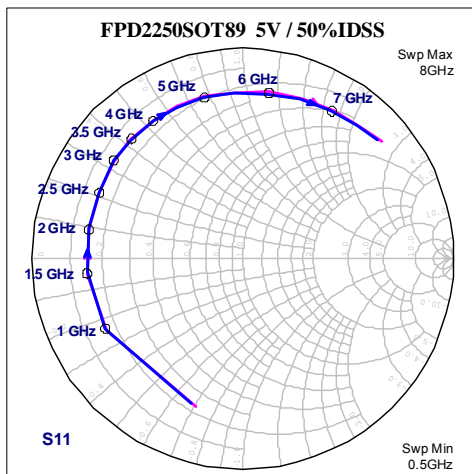
 Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

 Input (Source plane) Γ_s :

$$0.67 \angle 103.6^\circ$$

$$0.30 + j0.74 \text{ (normalized)}$$

$$15 + j37.0 \Omega$$

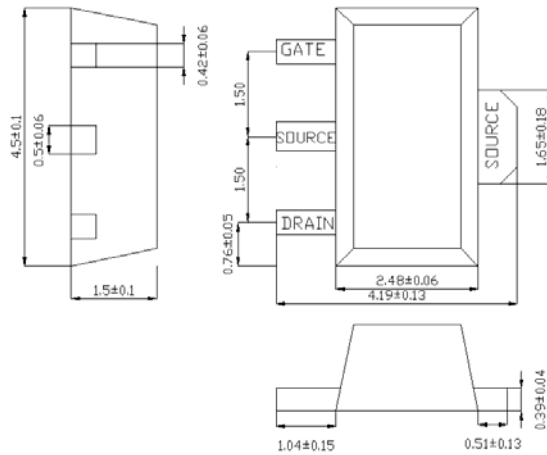
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.
TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM):


S-PARAMETERS: BIASED @ 5V, 50%IDSS

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.500	0.823	-119.1	16.103	109.2	0.027	46.5	0.459	-159.0
0.750	0.772	-142.8	11.584	97.3	0.033	44.3	0.450	-167.9
1.000	0.758	-157.5	9.092	87.6	0.038	42.7	0.455	-176.0
1.250	0.753	-168.0	7.526	79.7	0.044	41.6	0.445	178.5
1.500	0.752	-178.1	6.335	72.9	0.049	40.2	0.445	172.0
1.750	0.745	174.3	5.505	65.7	0.054	37.8	0.447	167.4
2.000	0.746	166.8	4.905	59.1	0.060	35.6	0.439	162.5
2.250	0.740	159.4	4.410	52.7	0.066	32.8	0.439	157.4
2.500	0.743	152.6	4.030	46.3	0.072	29.4	0.433	152.2
2.750	0.744	145.5	3.702	40.4	0.078	26.8	0.436	146.2
3.000	0.740	138.4	3.409	33.7	0.083	22.5	0.436	140.8
3.250	0.751	132.4	3.173	27.4	0.089	18.7	0.436	134.3
3.500	0.750	125.7	2.953	21.2	0.095	14.7	0.450	128.5
3.750	0.755	119.7	2.753	15.0	0.100	10.7	0.459	122.9
4.000	0.762	113.4	2.573	9.1	0.104	6.4	0.473	117.7
4.250	0.762	107.4	2.408	2.9	0.108	2.1	0.487	112.8
4.500	0.781	102.3	2.260	-2.7	0.112	-1.8	0.497	108.0
4.750	0.788	97.0	2.119	-8.2	0.115	-5.8	0.512	103.2
5.000	0.803	92.1	2.000	-13.6	0.118	-9.6	0.521	98.7
5.250	0.809	86.7	1.896	-18.9	0.122	-13.3	0.532	94.6
5.500	0.810	82.3	1.801	-24.3	0.125	-17.2	0.537	90.5
5.750	0.828	78.1	1.718	-29.3	0.129	-20.8	0.548	86.8
6.000	0.880	71.8	1.701	-35.9	0.137	-26.3	0.589	82.7
6.250	0.862	67.8	1.610	-40.7	0.138	-29.6	0.583	79.0
6.500	0.878	62.1	1.540	-47.5	0.142	-35.4	0.599	72.5
6.750	0.853	58.8	1.452	-51.7	0.142	-38.2	0.589	67.5
7.000	0.854	55.3	1.385	-56.3	0.144	-41.7	0.584	61.7
7.250	0.851	51.5	1.337	-60.9	0.147	-45.3	0.578	56.7
7.500	0.847	47.7	1.283	-65.9	0.148	-49.2	0.580	51.6
7.750	0.856	43.8	1.247	-71.0	0.153	-53.4	0.591	46.6
8.000	0.869	39.4	1.203	-76.8	0.155	-58.3	0.602	41.0
8.250	0.873	33.4	1.145	-82.4	0.155	-62.8	0.620	36.4
8.500	0.868	28.1	1.094	-87.5	0.155	-67.5	0.634	31.8
8.750	0.878	23.1	1.043	-92.9	0.155	-72.2	0.655	28.2
9.000	0.885	17.4	0.995	-97.9	0.155	-76.6	0.671	24.5
9.250	0.886	12.5	0.949	-102.8	0.154	-81.1	0.687	22.0
9.500	0.894	7.8	0.897	-107.9	0.153	-85.9	0.702	19.5
9.750	0.897	3.5	0.851	-112.4	0.151	-90.3	0.715	17.2
10.000	0.899	0.0	0.812	-116.8	0.149	-95.2	0.724	14.2
10.250	0.902	-3.1	0.771	-121.0	0.146	-100.3	0.731	11.1
10.500	0.905	-6.0	0.743	-125.0	0.142	-104.9	0.733	8.5
10.750	0.906	-8.5	0.711	-129.0	0.137	-109.0	0.743	5.9
11.000	0.907	-10.9	0.684	-132.7	0.135	-112.4	0.746	3.1
11.250	0.912	-13.0	0.662	-136.8	0.133	-115.3	0.749	0.1
11.500	0.916	-15.8	0.644	-140.1	0.133	-118.3	0.739	-3.4
11.750	0.915	-18.3	0.632	-144.0	0.133	-121.2	0.734	-6.9
12.000	0.912	-21.2	0.620	-147.9	0.136	-124.8	0.723	-11.4

PACKAGE OUTLINE:

(dimensions in millimeters – mm)


HANDLING PRECAUTIONS:

To avoid damage to the devices care should be exercised during handling.



Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

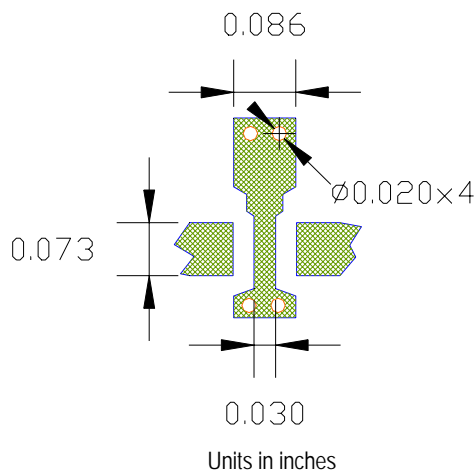
Application Notes and design data including S-parameters are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FPD2250SOT89	Packaged pHEMT
FPD2250SOT89E	RoHS Compliant Packaged pHEMT
FPD2250SOT89CE	RoHS Compliant Packaged pHEMT with enhanced passivation (Recommended for New Designs)

PCB Foot Print

PREFERRED ASSEMBLY INSTRUCTIONS:

Available on request.