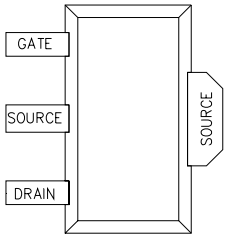
- PERFORMANCE (1850 MHz)
  - ♦ 27.5 dBm Output Power (P_{1dB})
  - ♦ 17 dB Small-Signal Gain (SSG)
  - ♦ 1.2 dB Noise Figure
  - ♦ 42 dBm Output IP3
  - ♦ 50% Power-Added Efficiency
  - ♦ Evaluation Boards Available
  - ♦ Available in Lead Free Finish: FPD1500SOT89E



- DESCRIPTION AND APPLICATIONS

The FPD1500SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 x 1500 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels. The FPD1500 is available in die form and in other packages. Typical applications include drivers or output stages in PCS/Cellular base station high-intercept-point LNAs, WLL and WLAN systems, and other types of wireless infrastructure systems.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT *f* = 1850 MHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 5.0V; I_{DS} = 50% I_{DSS}	26.0	27.5		dBm
Small-Signal Gain	SSG	V_{DS} = 5.0V; I_{DS} = 50% I_{DSS}	15.5	17		dB
Power-Added Efficiency P_{OUT} = P_{1dB}	PAE	V_{DS} = 5.0V; I_{DS} = 50% I_{DSS}		50		%
Noise Figure	NF	V_{DS} = 5.0V; I_{DS} = 50% I_{DSS}		1.2	1.5	dB
Output Third-Order Intercept Point (from 15 to 5 dB below P_{1dB})	IP3	V_{DS} = 5.0V; I_{DS} = 50% I_{DSS} Matched for best P_{1dB}	38	40		dBm
		Matched for best IP3 at 50% I_{DSS}		42		
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	375	465	550	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		750		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		400		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		1	15	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 1.5 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 1.5 mA	12	16		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 1.5 mA	12	16		V

• ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		15	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		350	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		2.3	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:
  $P_{TOT} = 2.3W - (0.015W/°C) \times T_{PACK}$
  where T_{PACK} = *source tab lead temperature above 22°C*
  (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 65°C source lead temperature: $P_{TOT} = 2.3W - (0.015 \times (65 - 22)) = 1.66W$

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

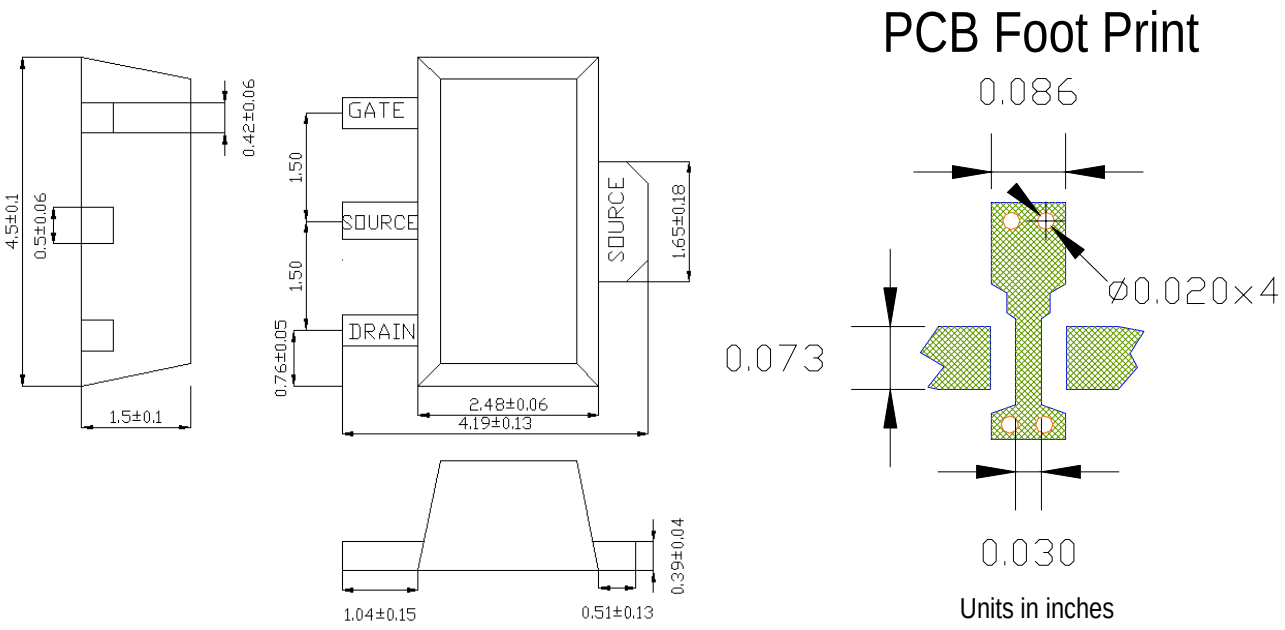
• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD1500SOT89.
  - Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 2.6 Ω for a 50% of I_{DSS} operating point.
  - For standard Class A operation, a 50% of I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are "quasi- E/D mode" devices, exhibit Class AB traits when operated at 50% of I_{DSS}. To achieve a larger separation between P_{1dB} and IP3, an operating point in the 25% to 33% of I_{DSS} range is suggested. Such Class AB operation will not degrade the IP3 performance.

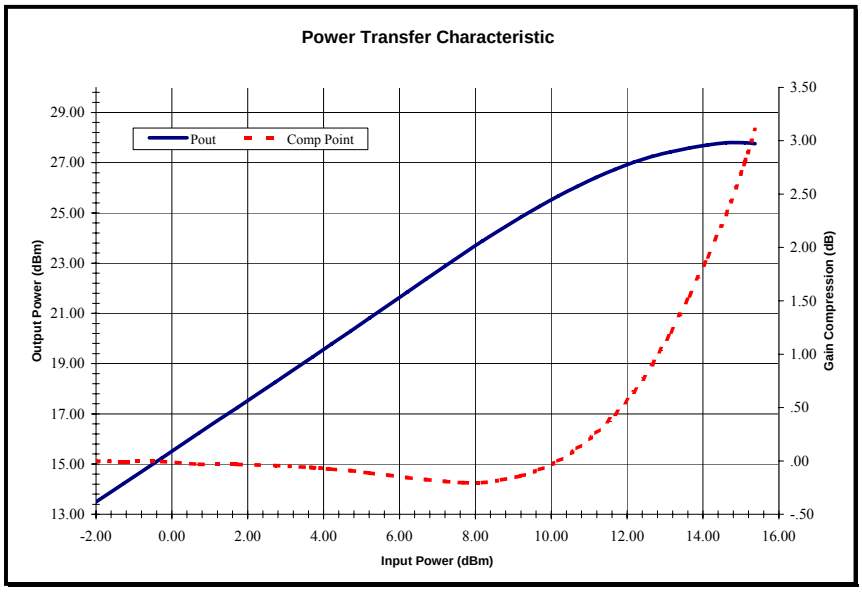
- PACKAGE OUTLINE

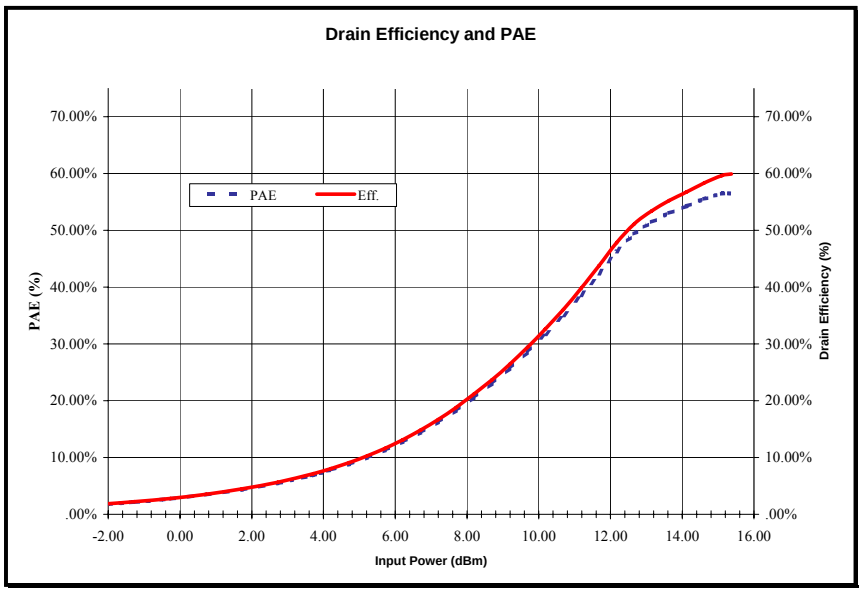
(dimensions in mm)



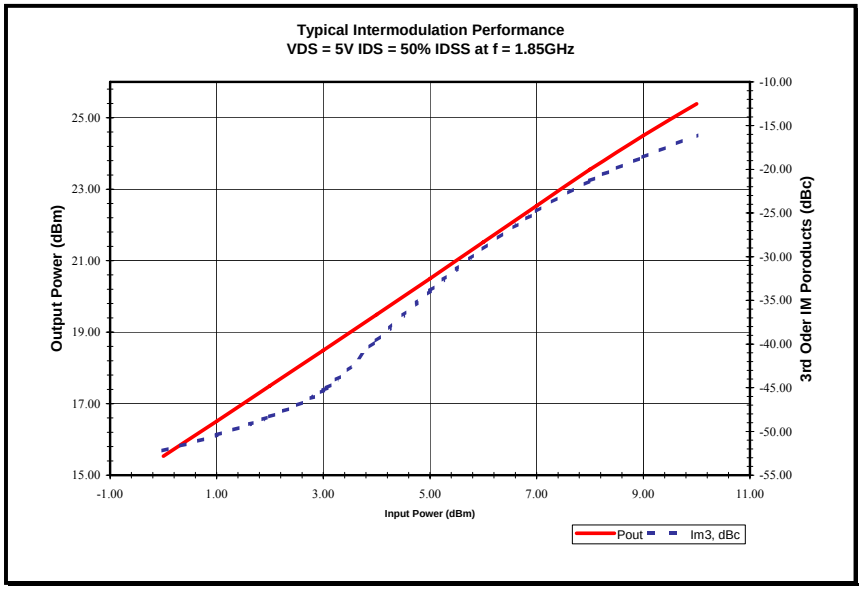
All information and specifications subject to change without notice.

- TYPICAL TUNED RF PERFORMANCE



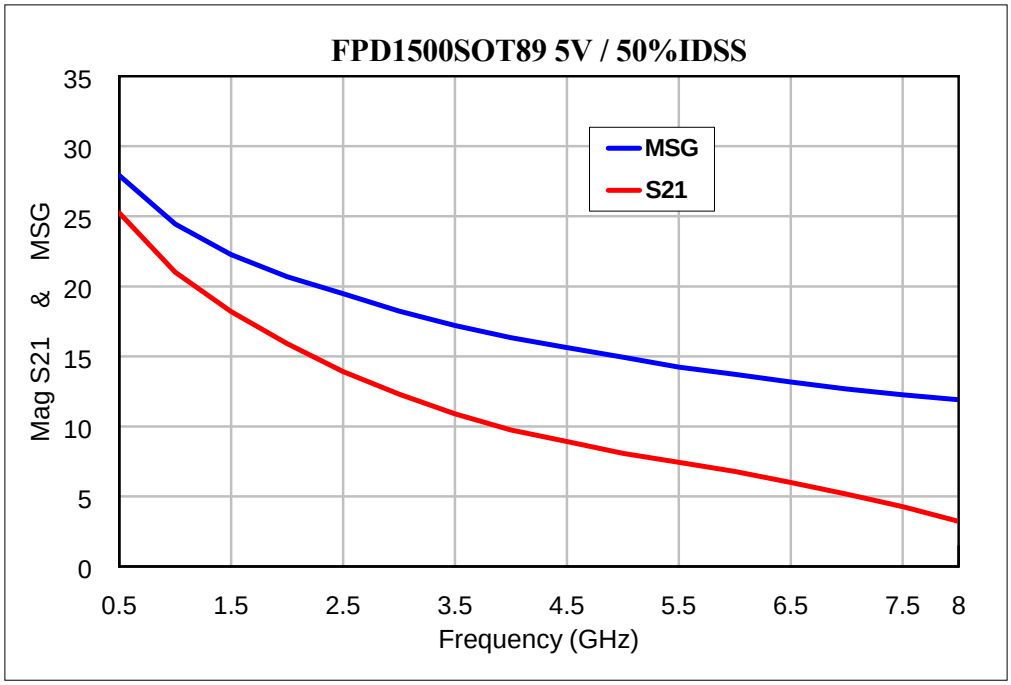


Typical power, efficiency, and intermodulation performance is shown above. The devices were biased nominally at V_{DS} = 5V, I_{DS} = 50% of I_{DSS}, at a test frequency of 2 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.

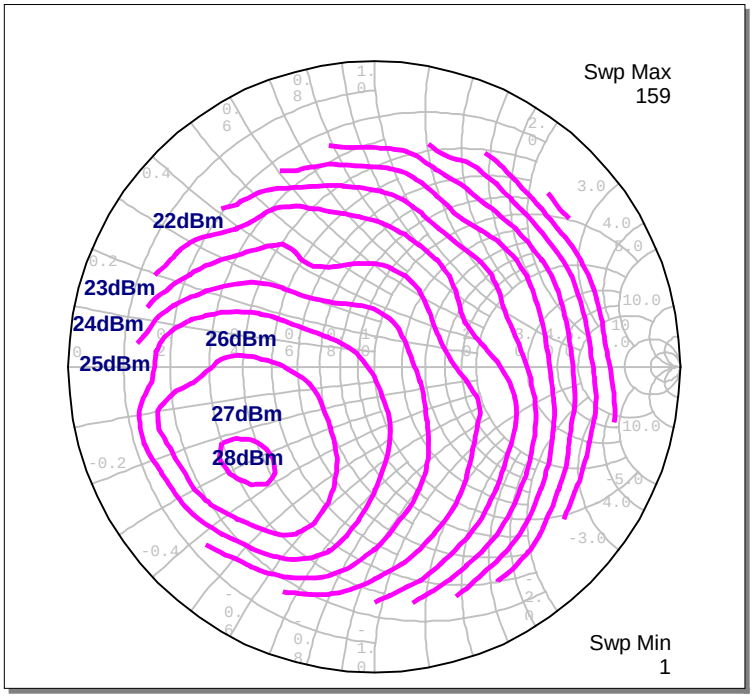


Note: pHEMT devices exhibit non-classical intermodulation performance, with equivalent IPvalues exceeding 14 dB above P_{1dB}. This IMD enhancement is affected by the quiescent bias current, the Drain-Source voltage, and the tuning or matching applied to the device.

Maximum Stable Gain & S_{21}



- TYPICAL OUTPUT PLANE POWER CONTOURS (VDS = 5V, IDS = 50% IDSS)



1850 MHz

Contours swept with a constant input power, set so that nominal P_{1dB} is achieved at the point of optimum output match.

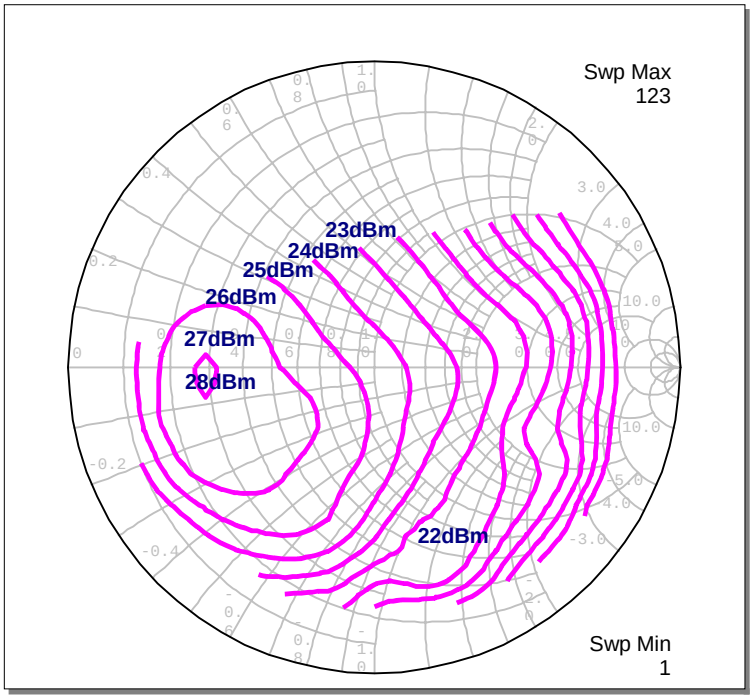
Input (Source plane) Γ_s:

0.74 ∠ 168.2º

0.15 + j0.1 (normalized)

7.5 + j5.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.



900 MHz

Contours swept with a constant input power, set so that nominal P_{1dB} is achieved at the point of optimum output match.

Input (Source plane) Γ_s:

0.67 ∠ 103.6º

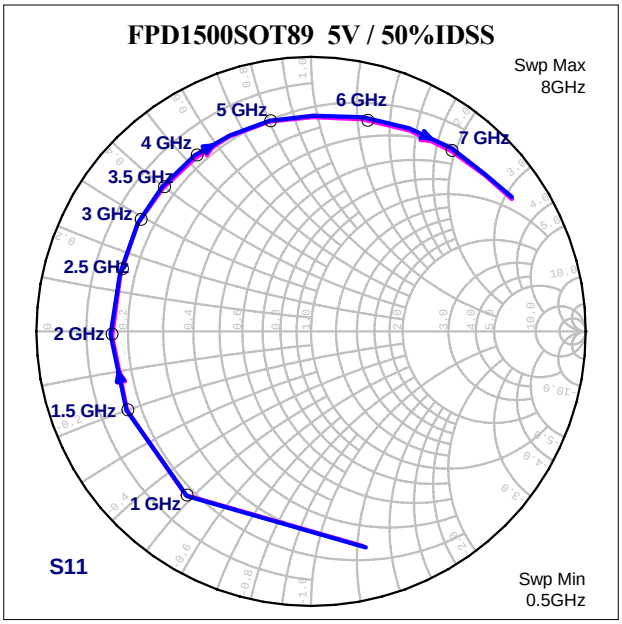
0.30 + j0.74 (normalized)

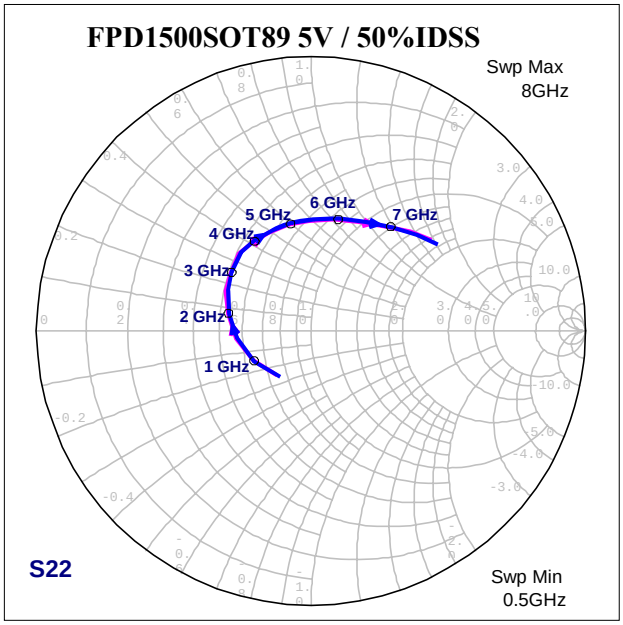
15 + j37.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

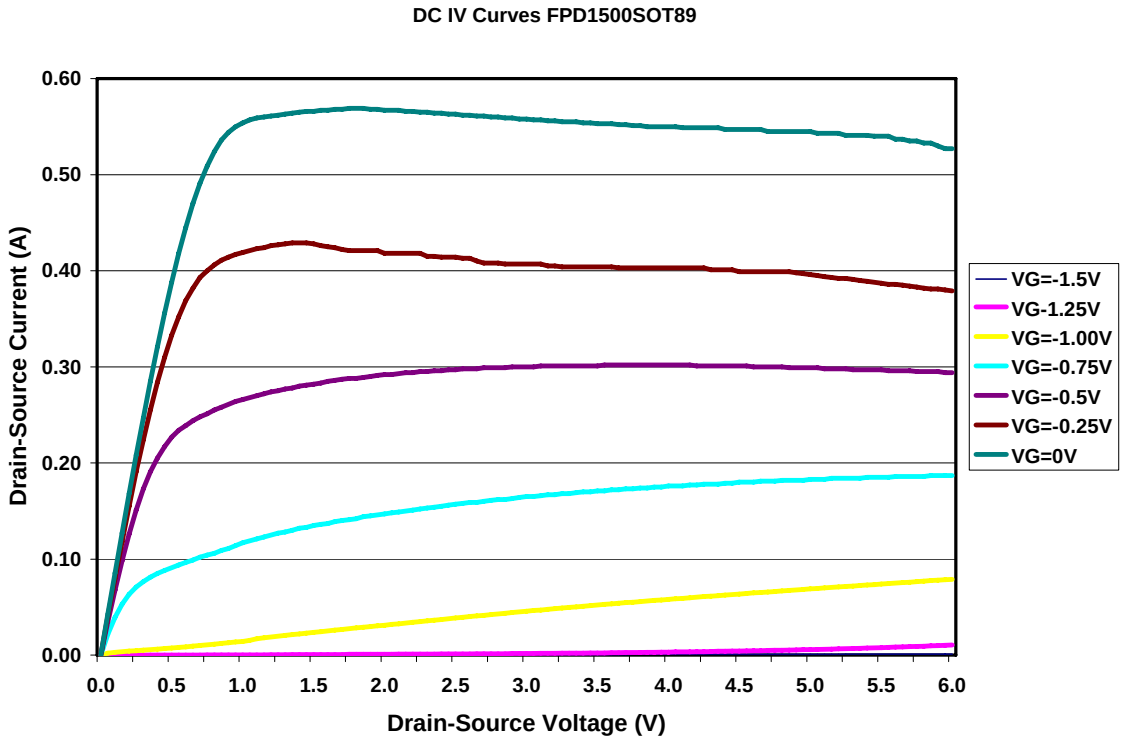
- TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM)

See Website "More Info" for S-parameter design files.





- TYPICAL I-V CHARACTERISTICS



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

Recommendation: Traditionally a device's I_{DSS} rating (I_{DS} at V_{GS} = 0V) was used as a predictor of RF power, and for MESFETs there is a correlation between I_{DSS} and P_{1dB} (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between I_{DSS} and P_{1dB}; specifically a linear regression analysis shows $r^2 < 0.7$, and the regression fails the F-statistic test. I_{DSS} is sometimes useful as a guide to circuit tuning, since the S_{22} does vary with the quiescent operating point I_{DS}.

- **REFERENCE DESIGNS (0.9 & 1.85GHZ)**

Frequency	GHz	0.9	1.85
Gain	dB	20	16
P1dB	dBm	27	27
IP3	dBm	38	40
S11	dB	-5	-9
S22	dB	-15	-14
Vd	V	5	5
Vg	V	-0.4 to -0.6	-0.4 to -0.6
Id	mA	200	200

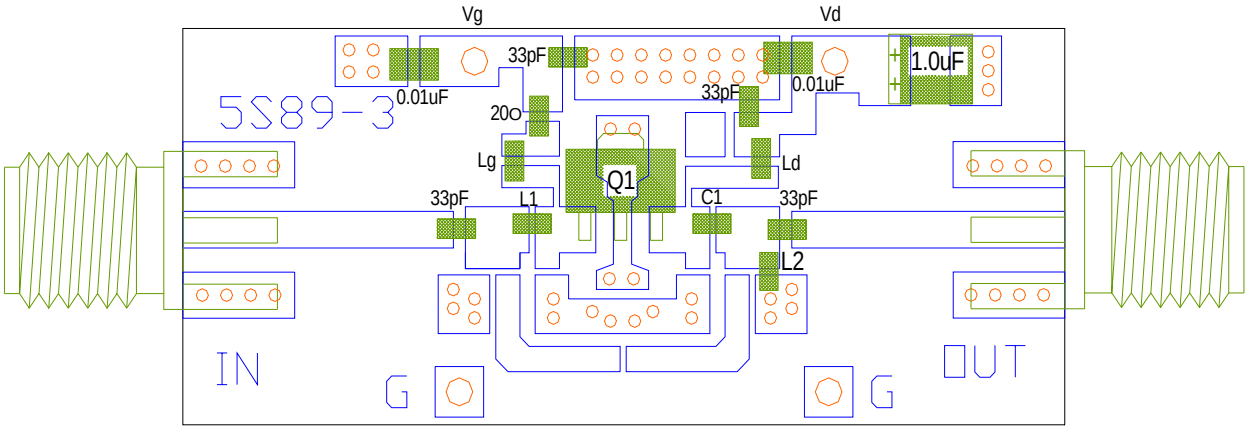
Component Values

Component	0.9GHz	1.85GHz
Lg	47nH	27nH
Ld	47nH	27nH
L1	12nH	1.5nH
L2	4.7nH	4.7nH
C1	5.6pF	2.2pF

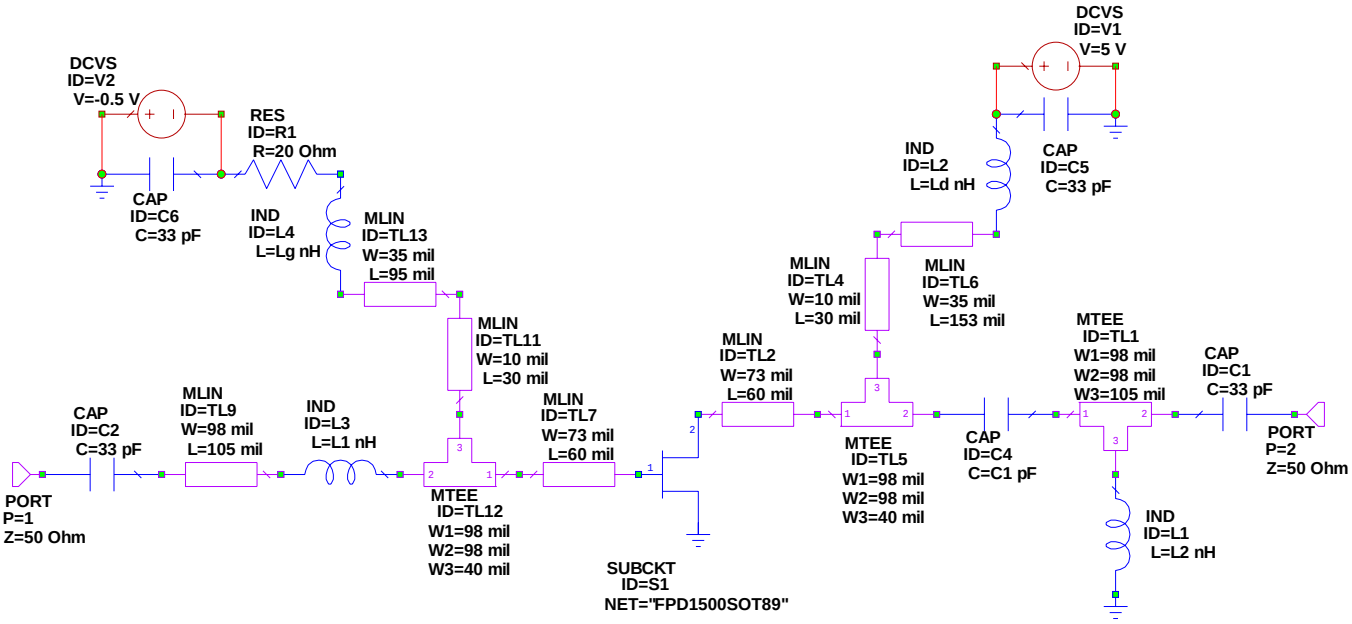
Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

- **Negative gate voltage required to be established before drain bias**
- **Use test clips at the bias vias at the top and bottom of the board for biasing**

Eval Board Layout



Eval board Schematic



- **REFERENCE DESIGNS (2.4 & 2.6GHZ)**

Frequency	GHz	2.4	2.6
Gain	dB	12	11.5
P1dB	dBm	28	27.5
IP3	dBm	41	40
S11	dB	-6	-16
S22	dB	-5	-5
Vd	V	5	5
Vg	V	-0.4 to -0.6	-0.4 to -0.6
Id	mA	200	200

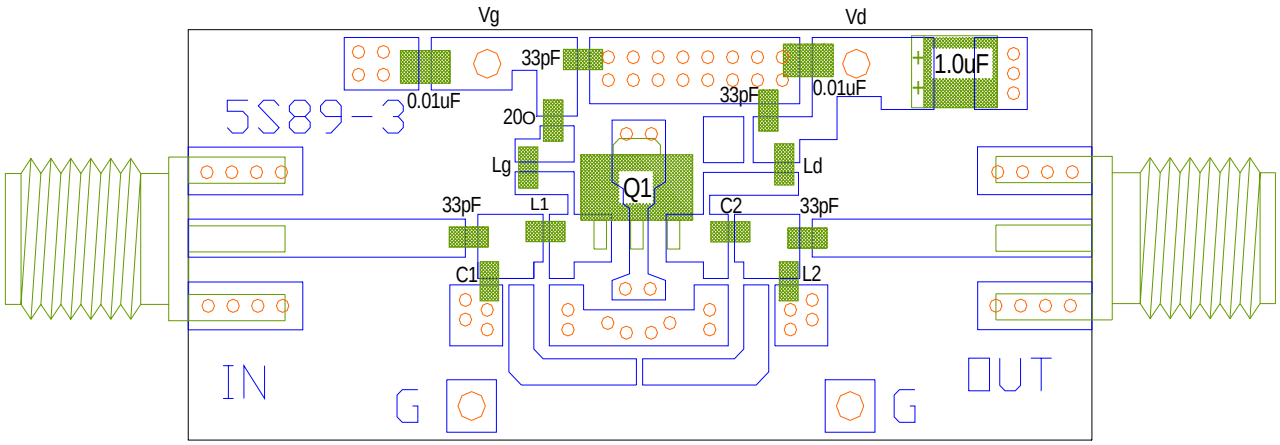
Component Values

Component	2.4GHz	2.6GHz
Lg	22nH	18nH
Ld	22nH	18nH
L1	1.0nH	Tab
L2	3.3nH	3.9nH
C1	1.8pF	1.0pF
C2	1.0pF	1.0pF

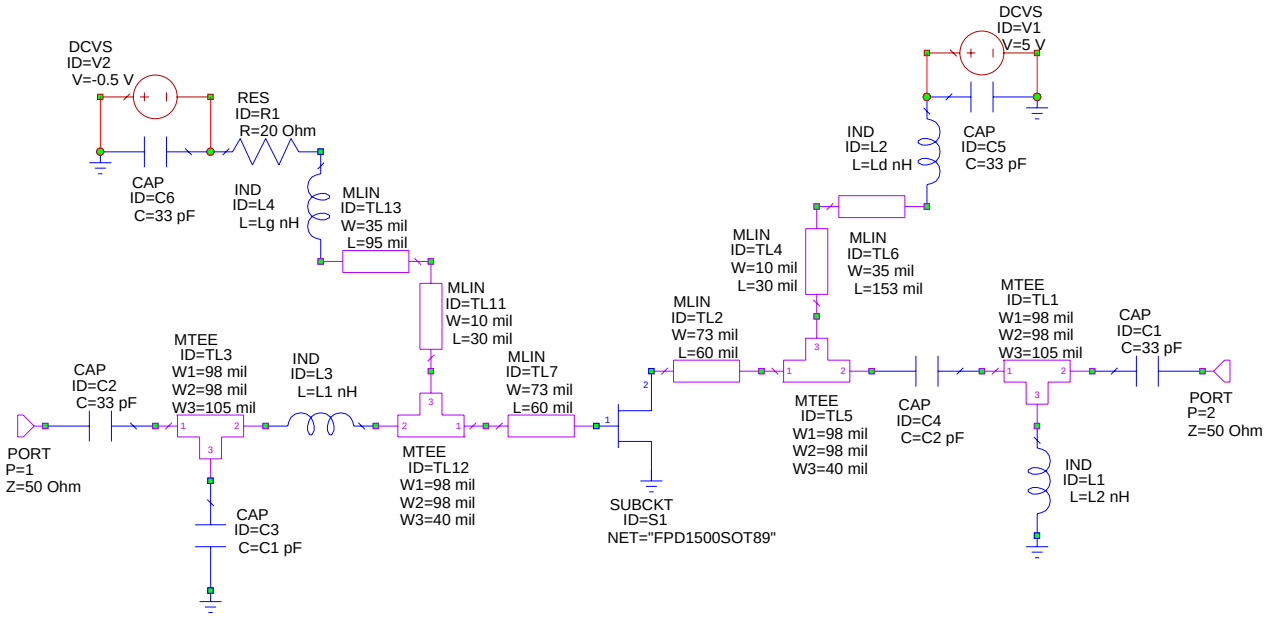
Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

- **Negative gate voltage required to be established before drain bias**
- **Use test clips at the bias vias at the top and bottom of the board for biasing**

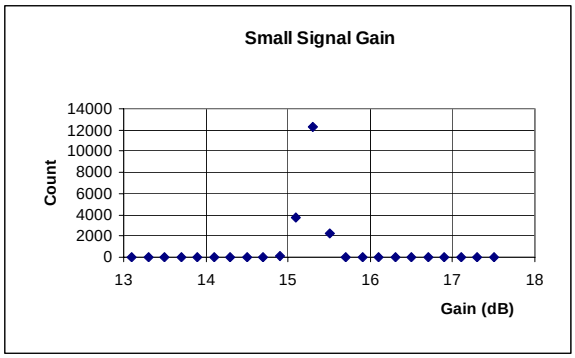
Eval Board Layout

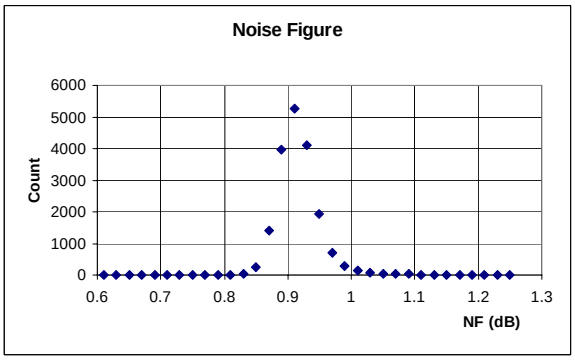


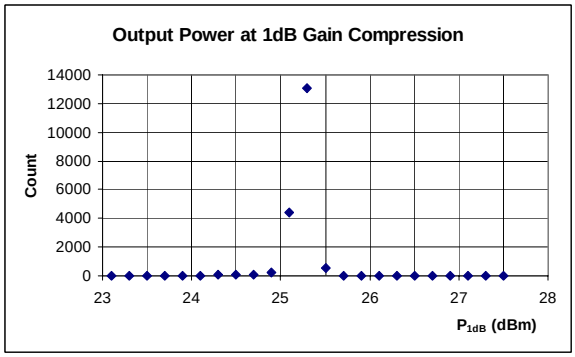
Eval board Schematic

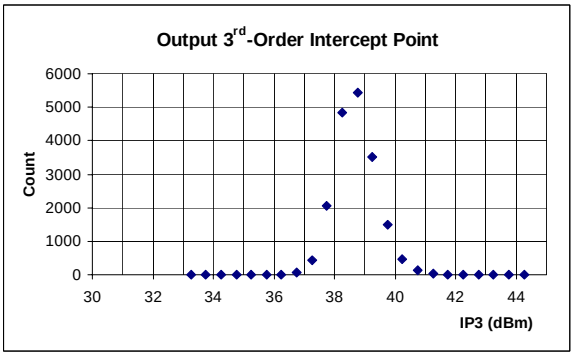


- STATISTICAL SAMPLE OF RF PERFORMANCE









The histograms above represent a sample of over 20,000 representative devices. The devices were tested by a high-speed automatic test system, in a matched circuit based on the EB1500SOT89AA Evaluation Board design (see the Website for a schematic). This circuit is a dual-bias single-pole lowpass topology, and the devices were biased at V_{DS} = 4.5V, I_{DS} = 120mA. The performance data is summarized below:

Parameter	Median	Standard Deviation	Test Limit	C_{PK}
Small-Signal Gain	15.5	0.20	14.5	1.7
Noise Figure	0.91	0.03	1.20	3.2
Output Power (P1dB)	25.2	0.25	24.5	0.93
3rd-Order Intercept	38.7	1.1	36.5	0.67