

March 2003 Revised March 2003

FSAV332

Low On Resistance Quad Video Switch with Individual Enables (Preliminary)

General Description

The Fairchild Switch FSAV332 provides four high-speed CMOS TTL-compatible video switches. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The <u>device</u> is organize<u>d</u> as four 1-bit switches with separate \overline{OE} inputs. When \overline{OE} is LOW, the <u>switch</u> is ON and Port A is connected to Port B. When \overline{OE} is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

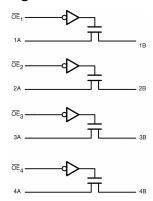
- \blacksquare 3 Ω switch connection between two ports
- Wide bandwidth 250 MHz
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level

Ordering Code:

Order Number	Package Number	Package Description			
FSAV332M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
FSAV332QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide			
FSAV332MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

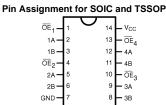
Logic Diagram



Pin Descriptions

Pin Name	Description		
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4$	Bus Switch Enables		
1A, 2A, 3A, 4A	Bus A		
1B, 2B, 3B, 4B	Bus B		
NC	Not Connected		

Connection Diagrams



Pin Assignment for QSOP



Truth Table

Inputs	Inputs/Outputs
ŌĒ	A,B
L	A = B
Н	Z

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions (Note 3)

 $\begin{array}{lll} \mbox{Power Supply Operating (V_{CC})} & 4.75\mbox{V to } 5.25\mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0\mbox{V to } 5.25\mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0\mbox{V to } 5.25\mbox{V} \\ \mbox{Ov to } 5.25\mbox{V} \\ \mbox{O$

Input Rise and Fall Time (t_r, t_f)

Switch Control Input 0 ns/V to 5 ns/V Switch I/O 0 ns/V to DC Free Air Operating Temperature (T_A) -40° C to $+85^{\circ}$ C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

			T _A = -40 °C to +85 °C				
Symbol	Parameter	V _{CC}	Min	Тур	Max	Units	Conditions
		(V)		(Note 4)			
	Analog Signal Range	4.75 - 5.25	0		2.0	V	
V _{IK}	Clamp Diode Voltage	4.75			-1.2	V	$I_{IN} = -18 \text{ mA}$
V _{IH}	High Level Input Voltage	4.75 - 5.25	2.0			V	
V _{IL}	Low Level Input Voltage	4.75 - 5.25			0.8	V	
I	Input Leakage Current	5.25			±1.0	μΑ	$0 \le V_{IN} \le 5.5V$
I _{OZ}	OFF-STATE Leakage Current	5.25			±1.0	μΑ	0 ≤ A, B ≤ V _{CC}
R _{ON}	Switch On Resistance	4.75		3	7	Ω	$V_{IN} = 0V$, $I_{IN} = 13 \text{ mA}$
	(Note 5)	4.75		7	10	32	V _{IN} = 2.4V, I _{IN} = 26 mA
I _{CC}	Quiescent Supply Current	5.25			3	μΑ	$V_{IN} = V_{CC}$ or GND,
							I _{OUT} = 0
ΔI_{CC}	Increase in I _{CC} per Input	5.25			2.5	mA	One Input at 3.4V.
(Note 6)							Other Inputs at V _{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 6: Per TTL driven inputs, control pins only.

AC Electrical Characteristics

Symbol	Parameter		C to +85°C, RU = RD = 75 Ω	Units	Conditions	Figure
Symbol	r al allietei	V _{CC} = 4.	75V-5.25V	Offics	Conditions	Number
		Min	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 7)		0.1	ns	V _I = OPEN	Figures 1, 2
t _{PZH} , t _{PZL}	Output Enable Time	1.0	5.0	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figures 1, 2
t _{PHZ} , t _{PLZ}	Output Disable Time	1.0	5.0	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figures 1, 2
B _W ⁽⁸⁾	-3 dB Bandwidth (Note 8)	250		MHz	$R_L = 150\Omega$, $T_A = 25^{\circ}C$	
X _{TALK}	Crosstalk		-58	dB	$R_{IN} = 10\Omega$ $R_{L} = 150\Omega$, 10 MHz	
D _G	Differential Gain		0.64	%	$R_L = 150\Omega,$ $f = 3.58 \text{ MHz}$	
D _P	Differential Phase		0.27	Degree	$R_L = 150\Omega$, f = 3.58 MHz	
O _{IRR}	Off Insolation		-38	dB	$R_L = 150\Omega$, 10 MHz	

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

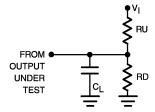
Note 8: This parameter is characterized but not tested in production.

Capacitance (Note 9)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	3		pF	V _{CC} = 5.0V
C _{OFF}	Switch-Off Capacitance	5		pF	V_{CC} , $\overline{OE} = 5.0V$
C _{ON}	Switch-On Capacitance	TBD		pF	$V_{CC} = \overline{OE} = 5.0V$

Note 9: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω Note: C_L includes load and stray capacitance Note: Input PRR = 1.0 MHz, t_W = 500ns

FIGURE 1. AC Test Circuit

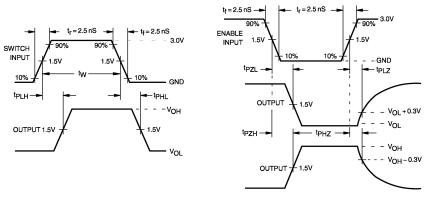
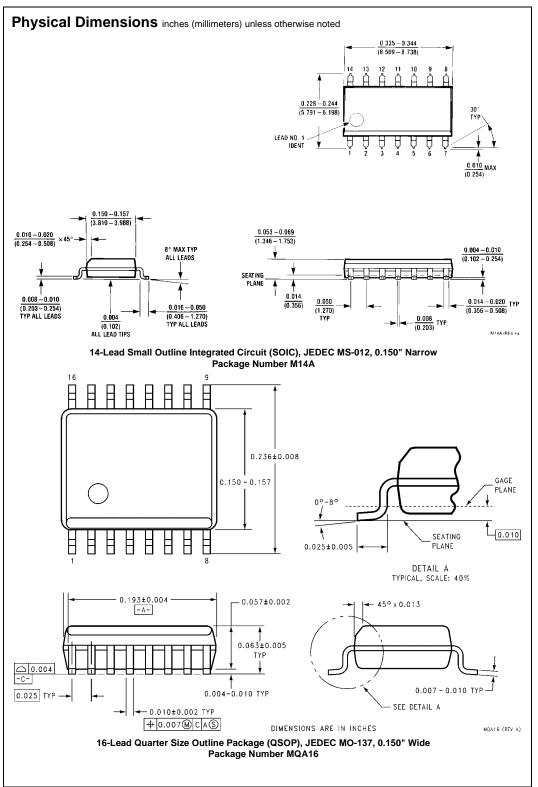


FIGURE 2. AC Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.43 TYF 6.4 -B-3.2 0.2 C B A ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT SEE DETAIL A 1.2 MAX 0.90+0.15 0.1 C 0.09-0.20 -C-0.10+0.05 0.65 12.00° TOP & BOTTOM B0.09 MIN GAGE PLANE 0.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. R0.09 MIN MTC14RevC3 DETAIL A

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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