



81 X 128 SINGLE CHIP LCD CONTROLLER / DRIVER

- 104 x 128 bits Display Data RAM
- Programmable MUX rate
- Programmable Frame Rate
- X,Y Programmable Carriage Return
- Dual Partial Display Mode
- Row by Row Scrolling
- Automatic data RAM Blanking procedure
- Selectable Input Interface:
 - I²C Bus Fast and Hs-mode (read and write)
 - Parallel Interface (read and write)
 - Serial Interface (read and write)
- Fully Integrated Oscillator requires no external components
- CMOS Compatible Inputs
- Fully Integrated Configurable LCD bias voltage generator with:
 - Selectable multiplication factor (up to 6X)
 - Effective sensing for High Precision Output
 - Eight selectable temperature compensation coefficients
- Designed for chip-on-glass (COG) applications

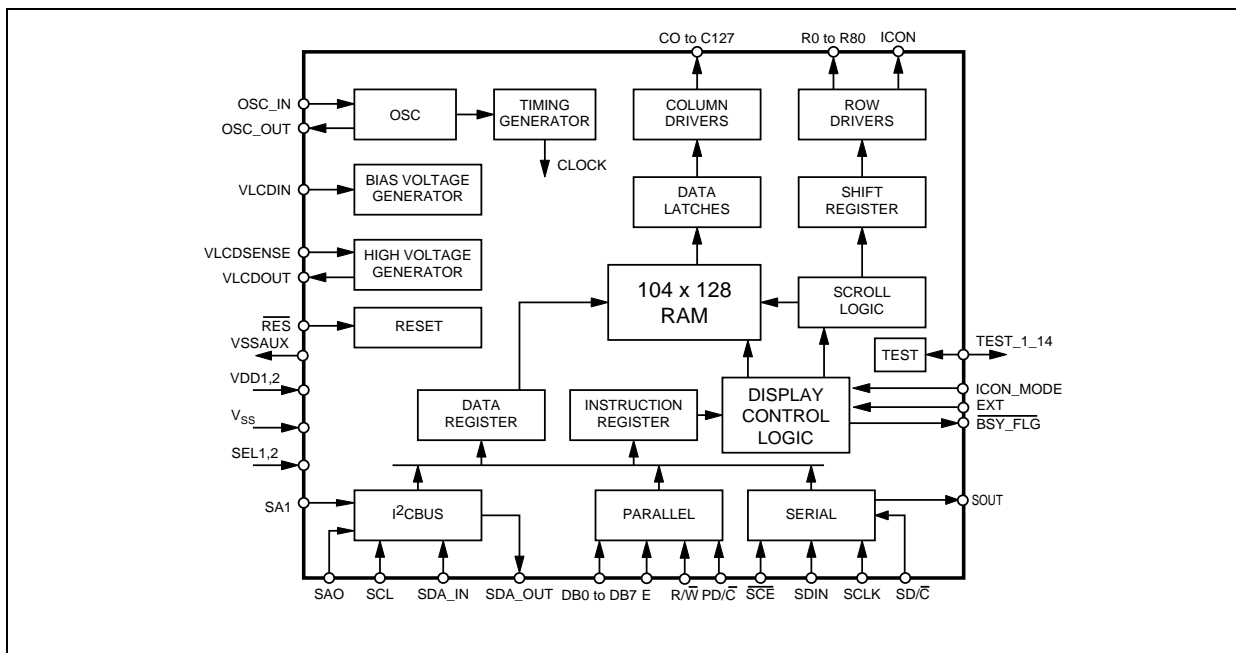
- Low Power Consumption, suitable for battery operated systems
- Logic Supply Voltage range from 1.7 to 3.6V
- High Voltage Generator Supply Voltage range from 1.75 to 4.2V
- Display Supply Voltage range from 4.5 to 11V
- Backward Compatibility with STE2001

DESCRIPTION

The STE2002 is a low power CMOS LCD controller driver. Designed to drive a 81 rows by 128 columns graphic display, provides all necessary functions in a single chip, including on-chip LCD supply and bias voltages generators, resulting in a minimum of external components and in a very low power consumption. The STE2002 features three standard interfaces (Serial, Parallel & I²C) for ease of interfacing with the host mcontroller.

| Type | Ordering Number |
|----------------------------|-----------------|
| Bumped Wafers | STE2002DIE1 |
| Bumped Dice on Waffle Pack | STE2002DIE2 |

Figure 1. Block Diagram



PIN DESCRIPTION

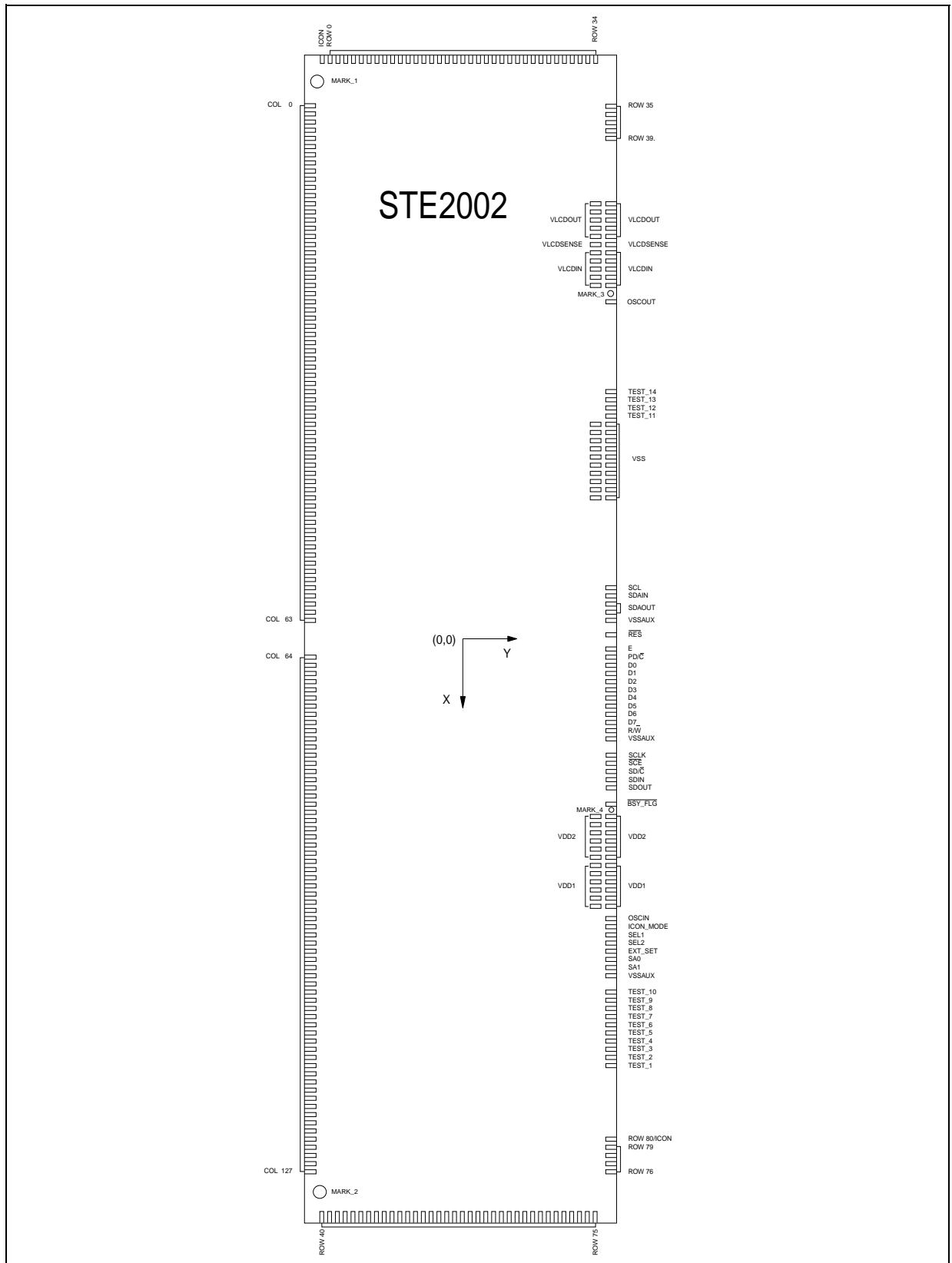
| N° | Pad | Type | Function | | | | | | |
|--------------------------|--------------------------|--------|--|----------------------|--------------------------|---------------|----------|------|----------|
| R0 to R80 | 129-169 282-322 | O | LCD Row Driver Output | | | | | | |
| ICON | 323 | O | ICON Row Driver | | | | | | |
| C0 to C127 | 1-128 | O | LCD Column Driver Output | | | | | | |
| VSS | 236-255 | GND | Ground pads. | | | | | | |
| VDD1 | 188-199 | Supply | IC Positive Power Supply | | | | | | |
| VDD2 | 200-211 | Supply | Internal Generator Supply Voltages. | | | | | | |
| VLCDIN | 261-270 | Supply | LCD Supply Voltages for the Column and Row Output Drivers. | | | | | | |
| VLCDOUT | 273-282 | Supply | Voltage Multiplier Output | | | | | | |
| VLCDSENSE | 271-272 | Supply | Voltage Multiplier Regulation Input. VLCDOUT Sensing for Output Voltage Fine Tuning | | | | | | |
| VSSAUX | 180, 231, 218 | O | Ground Reference for Selection Pins Configuration | | | | | | |
| SEL1,2 | 184,185 | I | Interface Mode Selection | | | | | | |
| EXT | 183 | I | Extended Instruction Set Selection <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">EXT PAD CONFIG</th> <th style="width: 50%;">INSTRUCTION SET SELECTED</th> </tr> </thead> <tbody> <tr> <td>VSS or VSSAUX</td> <td>BASIC</td> </tr> <tr> <td>VDD1</td> <td>EXTENDED</td> </tr> </tbody> </table> | EXT PAD CONFIG | INSTRUCTION SET SELECTED | VSS or VSSAUX | BASIC | VDD1 | EXTENDED |
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| VSS or VSSAUX | BASIC | | | | | | | | |
| VDD1 | EXTENDED | | | | | | | | |
| ICON_MODE | 186 | I | ICON ROW Management <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">ICON MODE PAD CONFIG</th> <th style="width: 50%;">ICON MODE STATUS</th> </tr> </thead> <tbody> <tr> <td>VSS or VSSAUX</td> <td>DISABLED</td> </tr> <tr> <td>VDD1</td> <td>ENABLED</td> </tr> </tbody> </table> | ICON MODE PAD CONFIG | ICON MODE STATUS | VSS or VSSAUX | DISABLED | VDD1 | ENABLED |
| ICON MODE PAD CONFIG | ICON MODE STATUS | | | | | | | | |
| VSS or VSSAUX | DISABLED | | | | | | | | |
| VDD1 | ENABLED | | | | | | | | |
| SDA_IN | 234 | I | I ² C Bus Data In | | | | | | |
| SDA_OUT | 232 | O | I ² C Bus Data Out | | | | | | |
| SCL | 235 | I | I ² C bus Clock | | | | | | |
| SA0 | 182 | I | I ² C Slave Address BIT 0 | | | | | | |
| SA1 | 181 | I | I ² C Slave Address BIT 1 | | | | | | |
| OSCIN | 187 | I | External Oscillator Input | | | | | | |
| OSCOU | 260 | O | Internal/External Oscillator Out | | | | | | |
| $\overline{\text{RES}}$ | 230 | I | Reset Input. Active Low. | | | | | | |
| DB0 to DB7 | 220-227 | I/O | Parallel Interface 8 Bit Data Bus | | | | | | |
| $\overline{\text{R/W}}$ | 219 | I | Parallel Interface Read & Write Control Line | | | | | | |
| E | 229 | I | Parallel Interface Data Latch Signal. | | | | | | |
| $\overline{\text{PD/C}}$ | 228 | I | Parallel Interface Data/Command Selector | | | | | | |
| SDIN | 214 | I | Serial Interface Data Input | | | | | | |



PIN DESCRIPTION (continued)

| N° | Pad | Type | Function | | | | | | | | |
|---|---------------------|------|---|-----------|-------------------|--------------------------------------|------|---|--------------|--|--------------|
| SCLK | 217 | I | Serial Interface Clock | | | | | | | | |
| $\overline{\text{SCE}}$ | 216 | I | Serial Interface ENABLE. When Low the Incoming Data are Clocked In. | | | | | | | | |
| $\overline{\text{SD/C}}$ | 215 | I | Serial Interface Data/Command Selector | | | | | | | | |
| SOUT | 213 | O | Serial Out | | | | | | | | |
| $\overline{\text{BSYFLG}}$ | 212 | O | Active Procedure Flag. Notice if There is an ongoing Internal Operation or an active reset. Active Low. | | | | | | | | |
| T1 to T14 | 170-179, 256-259 | I/O | <p>Test Pads. - A 50kohm pull-down resistor is added on input pins.</p> <table border="1"> <thead> <tr> <th>Test Num.</th> <th>Pin Configuration</th> </tr> </thead> <tbody> <tr> <td>TEST_1 TEST_2 TEST_3 TEST_4</td> <td>OPEN</td> </tr> <tr> <td>TEST_5 TEST_6 TEST_7 TEST_8 TEST_9 TEST_10</td> <td>VSS / VSSAUX</td> </tr> <tr> <td>TEST_11 TEST_12 TEST_13 TEST_14</td> <td>VSS / VSSAUX</td> </tr> </tbody> </table> | Test Num. | Pin Configuration | TEST_1 TEST_2 TEST_3 TEST_4 | OPEN | TEST_5 TEST_6 TEST_7 TEST_8 TEST_9 TEST_10 | VSS / VSSAUX | TEST_11 TEST_12 TEST_13 TEST_14 | VSS / VSSAUX |
| Test Num. | Pin Configuration | | | | | | | | | | |
| TEST_1 TEST_2 TEST_3 TEST_4 | OPEN | | | | | | | | | | |
| TEST_5 TEST_6 TEST_7 TEST_8 TEST_9 TEST_10 | VSS / VSSAUX | | | | | | | | | | |
| TEST_11 TEST_12 TEST_13 TEST_14 | VSS / VSSAUX | | | | | | | | | | |

Figure 2. Chip Mechanical Drawing



CIRCUIT DESCRIPTION

Supplies Voltages and Grounds

V_{DD2} is supply voltages to the internal voltage generator (see below). If the internal voltage generator is not used, this should be connected to V_{DD1} pad. V_{DD1} supplies the rest of the IC. V_{DD1} supply voltage could be different form V_{DD2}.

Internal Supply Voltage Generator

The IC has a fully integrated (no external capacitors required) charge pump for the Liquid Crystal Display supply voltage generation. The multiplying factor can be programmed to be: Auto, X6, X5, X4, X3, X2, using the 'set CP Multiplication' Command. If Auto is set, the multiplying factor is automatically selected to have the lowest current consumption in every condition. This make possible to have an input voltage that changes over time and a constant V_{LCD} voltage. The output voltage (V_{LCDOUT}) is tightly controlled through the V_{LCDSENSE} pad. For this voltage, eight different temperature coefficients (TC, rate of change with temperature) can be programmed using the bits TC1 and TC0 and T2,T1 & T0. This will ensure no contrast degradation over the LCD operating range. Using the internal charge pump, the V_{LCDIN} and V_{LCDOUT} pads must be connected together. An external supply could be connected to V_{LCDIN} to supply the LCD without using the internal generator. In such event the V_{LCDOUT} and V_{LCDSENSE} must be connected to GND and the internal voltage generator must be programmed to zero (PRS = [0;0], Vop = 0 - Reset condition).

Oscillator

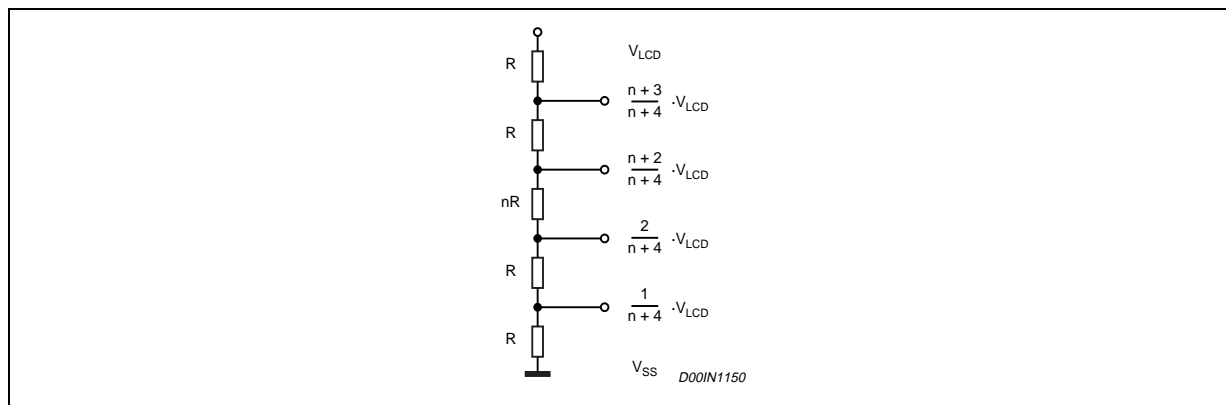
A fully integrated oscillator (requires no external components) is present to provide the clock for the Display System. When used the OSC pad must be connected to V_{DD1} pad. An external oscillator could be used and fed into the OSC pin. An oscillator out is provided on the OSCOUT Pad to cascade two or more drivers

Bias Levels

To properly drive the LCD, six (Including VLCD and VSS) different voltage (Bias) levels are generated. The ratios among these levels and VLCD, should be selected according to the MUX ratio (m). They are established to be (Fig. 4):

$$V_{LCD}, \frac{n+3}{n+4} V_{LCD}, \frac{n+2}{n+4} V_{LCD}, \frac{2}{n+4} V_{LCD}, \frac{1}{n+4} V_{LCD}, V_{SS}$$

Figure 4. Bias level Generator



thus providing an 1/(n+4) ratio, with n calculated from:

$$n = \sqrt{m} - 3$$

For m = 81, n = 6 and an 1/10 ratio is set.

For m = 65, n =5 and an 1/9 ratio is set.

The STE2002 provides three bits (BS0, BS1, BS2) for programming the desired Bias Ratio as shown below:

| BS2 | BS1 | BS0 | n |
|-----|-----|-----|---|
| 0 | 0 | 0 | 7 |
| 0 | 0 | 1 | 6 |
| 0 | 1 | 0 | 5 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 3 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The following table Bias Level for m = 65 and m = 81 are provided:

| Symbol | m = 65 (1/9) | m = 81 (1/10) |
|--------|----------------------|-----------------------|
| V1 | V _{LCD} | V _{LCD} |
| V2 | 8/9*V _{LCD} | 9/10*V _{LCD} |
| V3 | 7/9*V _{LCD} | 8/10*V _{LCD} |
| V4 | 2/9*V _{LCD} | 2/10*V _{LCD} |
| V5 | 1/9*V _{LCD} | 1/10*V _{LCD} |
| V6 | V _{SS} | V _{SS} |

LCD Voltage Generation

The LCD Voltage at reference temperature (T₀ = 27°C) can be set using the VOP register content according to the following formula:

$$V_{LCD}(T=T_0) = V_{LCD0} = (A_i + V_{OP} \cdot B) \quad (i=0,1,2)$$

with the following values:

| Symbol | Value | Unit | Note |
|----------------|--------|------|-------------|
| A ₀ | 2.95 | V | PRS = [0;0] |
| A ₁ | 6.83 | V | PRS = [0;1] |
| A ₂ | 10.71 | V | PRS = [1;0] |
| B | 0.0303 | V | |
| T ₀ | 27 | °C | |

Note that the three PRS values produce three adjacent ranges for VLCD. If the V_{OP} register and PRS bits are set to zero the internal voltage generator is switched off.

The proper value for the VLCD is a function of the Liquid Crystal Threshold Voltage (V_{th}) and of the Multiplexing Rate. A general expression for this is:

$$V_{LCD} = \frac{1 + \sqrt{m}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{m}}\right)}} \cdot V_{th}$$

For MUX Rate m = 65 the ideal V_{LCD} is:

$$V_{LCD(to)} = 6.85 \cdot V_{th}$$

than:

$$V_{op} = \frac{(6.85 \cdot V_{th} - A_i)}{0.03}$$

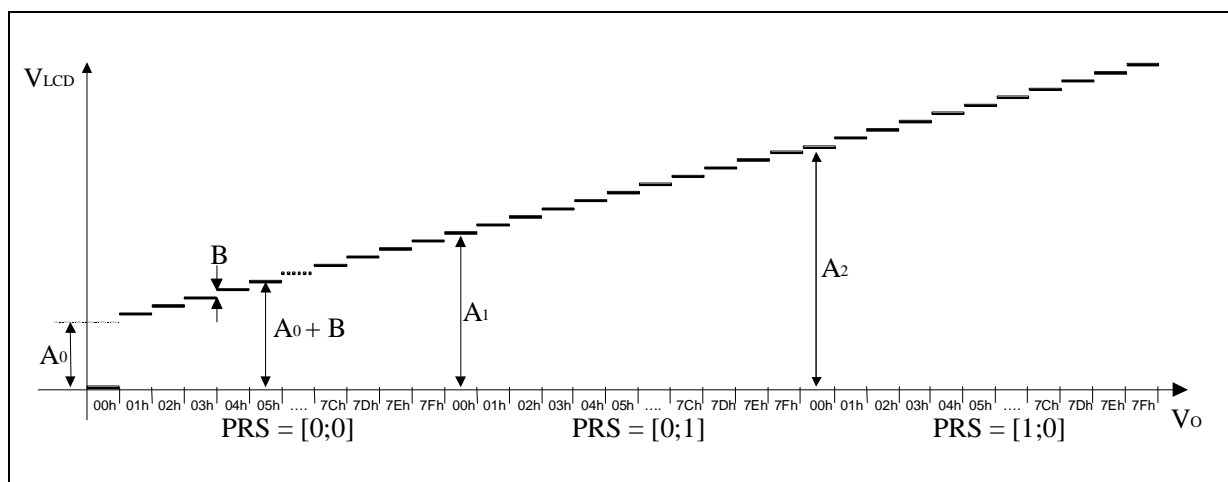
Temperature Coefficient

As the viscosity, and therefore the contrast, of the LCD are subject to change with temperature, there's the need to vary the LCD Voltage with temperature. The STE2002 provides the possibility to change the VLCD in a linear fashion against temperature with eight different Temperature Coefficient selectable through the T2, T1 and T0 bits. Only four of them are available with basic instruction set (TC1 & TC0 Bits).

| NAME | TC1 | TC0 | Value | Unit |
|------|-----|-----|-----------------------|------|
| TC0 | 0 | 0 | $-0.0 \cdot 10^{-3}$ | 1/°C |
| TC2 | 0 | 1 | $-0.7 \cdot 10^{-3}$ | 1/°C |
| TC3 | 1 | 0 | $-1.05 \cdot 10^{-3}$ | 1/°C |
| TC6 | 1 | 1 | $-2.1 \cdot 10^{-3}$ | 1/°C |

| NAME | TC2 | TC1 | TC0 | Value | Unit |
|------|-----|-----|-----|-----------------------|------|
| TC0 | 0 | 0 | 0 | $-0.0 \cdot 10^{-3}$ | 1/°C |
| TC1 | 0 | 1 | 1 | $-0.35 \cdot 10^{-3}$ | 1/°C |
| TC2 | 1 | 0 | 0 | $-0.7 \cdot 10^{-3}$ | 1/°C |
| TC3 | 1 | 1 | 1 | $-1.05 \cdot 10^{-3}$ | 1/°C |
| TC4 | 1 | 1 | 1 | $-1.4 \cdot 10^{-3}$ | 1/°C |
| TC5 | 1 | 1 | 1 | $-1.75 \cdot 10^{-3}$ | 1/°C |
| TC6 | 1 | 1 | 1 | $-2.1 \cdot 10^{-3}$ | 1/°C |
| TC7 | 1 | 1 | 1 | $-2.3 \cdot 10^{-3}$ | 1/°C |

Figure 5.



Finally, the VLCD voltage at a given (T) temperature can be calculated as:

$$V_{LCD}(T) = V_{LCD0} \cdot [1 + (T-T_0) \cdot TC]$$

Display Data RAM

The STE2002, provides an 104X128 bits Static RAM to store Display data. This is organized into 13 (Bank0 to Bank12) banks with 128 Bytes. One of these banks (128 bits wide) can be used for Icons. RAM access is accomplished in either one of the Bus Interfaces provided (see below). Allowed addresses are X0 to X127 (Horizontal) and Y0 to Y12 (Vertical).

When writing to RAM, four addressing mode are provided:

- Normal Horizontal (MX=0 and V=0), having the column with address X= 0 located on the left of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the following bank and X restarts from X=0. (Fig. 6)
- Normal Vertical (MX=0 and V=1), having the column with address X= 0 located on the left of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), X address pointer is set to jump to next column and Y restarts from Y=0 (Fig. 7).
- Mirrored Horizontal (MX=1 and V=0), having the column with address X= 0 located on the right of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the next bank and X restarts from X=0 (fig. 8).
- Mirrored Vertical (MX=1 and V=1), having the column with address X= 0 located on the right of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), the X pointer is set to jump to next column and Y restarts from Y=0 (fig. 9).

After the last allowed address (X;Y)=(X-Carriage; Y-Carriage), the address pointers always jump to the cell with address (X;Y) = (0;0) (Fi. 10, 11, 12 & 13).

Data bytes in the memory could have the MSB either on top (D0 = 0, Fig.14) or on the bottom (D0=1, Fig. 15).

The STE2002 provides also means to alter the normal output addressing. A mirroring of the Display along the X axis is enabled setting to a logic one MY bit. This function doesn't affect the content of the memory RAM. It is only related to the visualization process.

When ICON MODE=1 the Icon Row is not mirrored with MY and is not scrolled. When ICON Mode=0 the Icon Row is like the other graphic lines and is mirrored and scrolled.

Four are the multiplex ratio available when the partial display mode is disabled (MUX 33, MUX 49, MUX 65 and MUX 81).

Only a subset of writable rows are output on Row drivers.

When **Y-Carriage<MUX/8**, if Mux 65 is selected only the first 65 memory rows are visualized, if Mux 49 is selected only the first 49 memory rows are visualized, if Mux 33 is selected only the first 33 memory rows are visualized. All unused Row and Column drivers must be left floating.

When **Y-Carriage<MUX/8**, the icon Bank is located to BANK 10 in MUX 81 Mode, to BANK8 in MUX 65 Mode, to BANK 6 in MUX 49 Mode and to BANK 4 in MUX 33 Mode.

When **Y-Carriage>MUX/8** lines only 33, 49, 65 or 81 lines are visualized but it is possible to select which lines of DDRAM are connected on the output drivers. The DDRAM rows to visualized can be selected in the 0-Y-Carriage*8 range using the scrolling function.

When **Y-Carriage>MUX lines**, the icon row is moved in DDRAM to the first row of the Y-CARRIAGE Return BANK even if it is always connected on the same output Driver.

When **MY=0**, the icon Row is output on R80 in mux 81 mode, on R72 in MUX 65, on R64 in MUX49 and on R56 in MUX 33.

When **MY=1**, and **ICON MODE=1**, the icon Row is output on R80 in mux 81 mode, on R72 in MUX 65, on R64 in MUX49 and on R56 in MUX 33.

When **MY=1**, and **ICON MODE=0**, the icon Row is output on R0 whatever is the MUX Rate.

When **ICON MODE =1**, the Memory ICON Row content is output on ICON Pad.

If Not Used ICON Pad must be left floating.

Figure 6. Automatic data RAM writing sequence with V=0 and Data RAM Normal Format (MX=0)¹

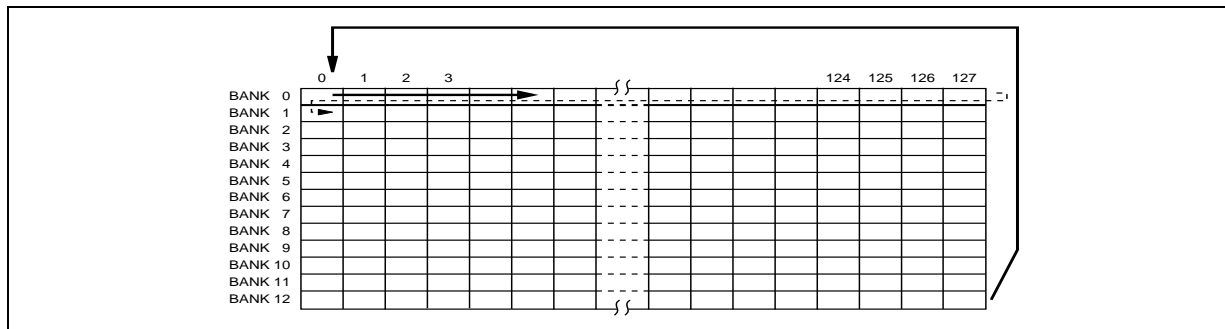


Figure 7. Automatic data RAM writing sequence with V=1 and Data RAM Normal Format (MX=0)¹

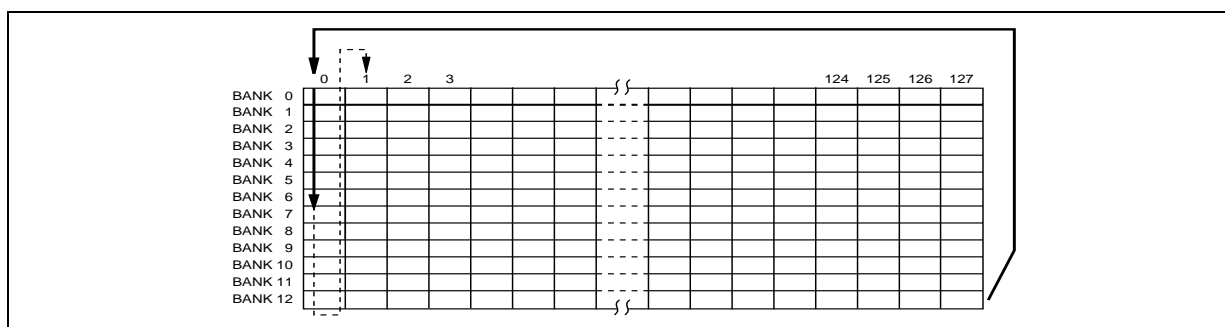


Figure 8. Automatic data RAM writing sequence with V=0 and Data RAM Mirrored Format (MX=1)¹

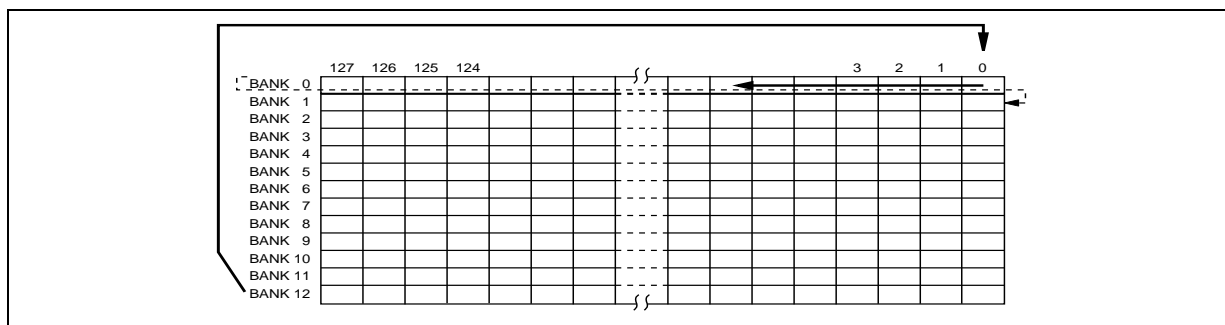
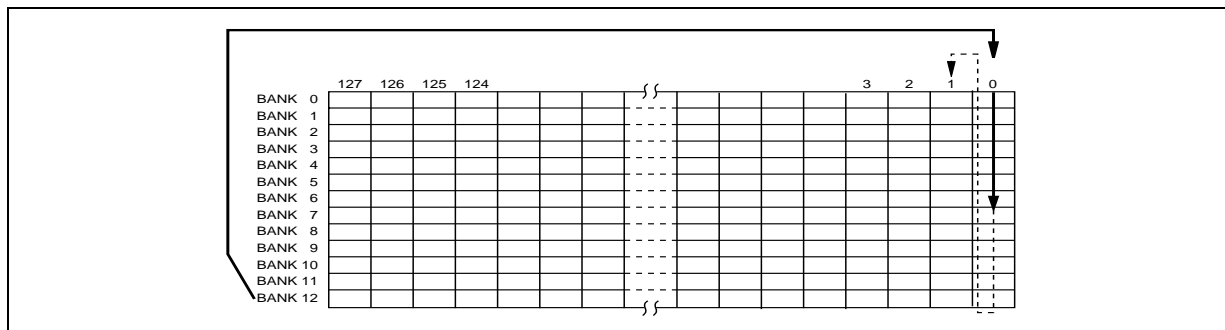


Figure 9. Automatic data RAM writing sequence with V=1 and Data RAM Mirrored Format (MX=1)¹



1. X Carriage=127; Y-Carriage = 12

Figure 14. Data RAM Byte organization with D0 = 0

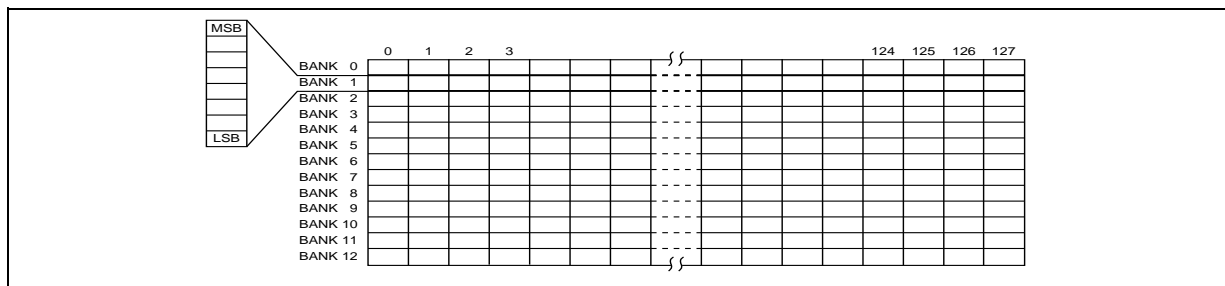


Figure 15. Data RAM Byte organization with D0 = 1

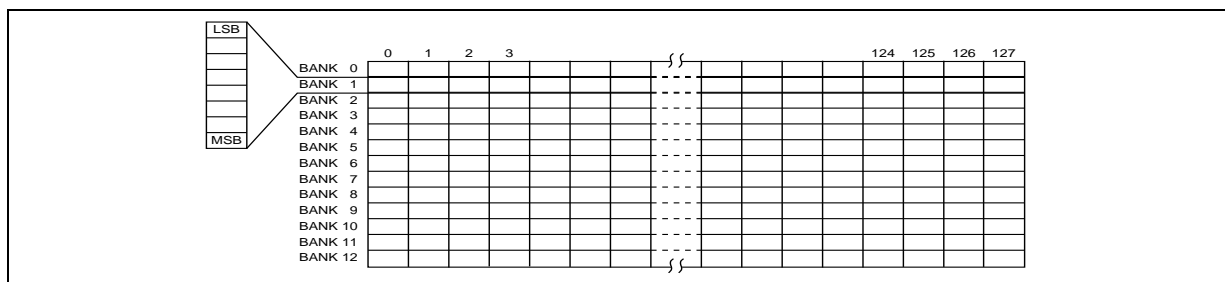


Figure 16. Memory Rows vs. Row drivers mapping with MY=0, MUX81, ICON MODE=0,1

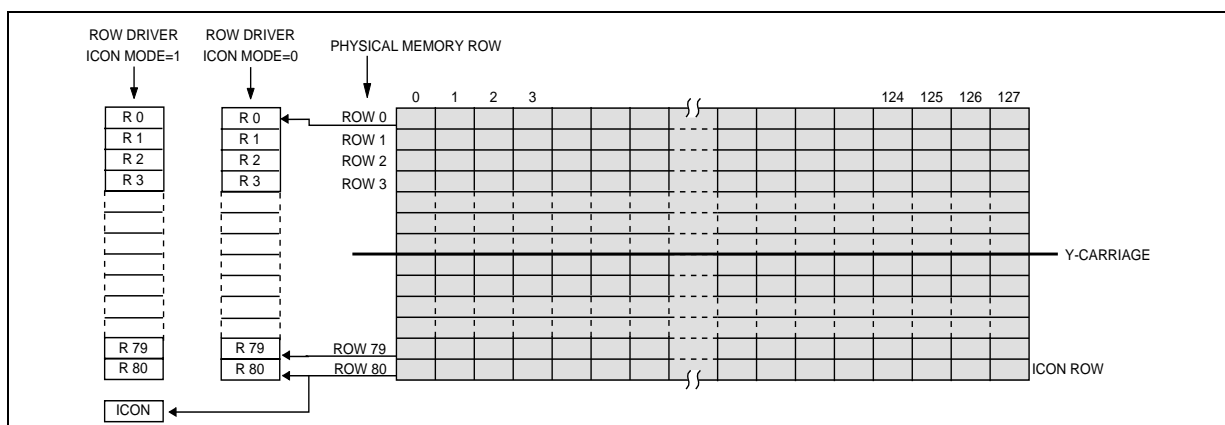


Figure 17. Memory Rows vs. Row drivers mapping with MY=0, MUX 81, SCROLL POINTER = +3, ICON MODE=1

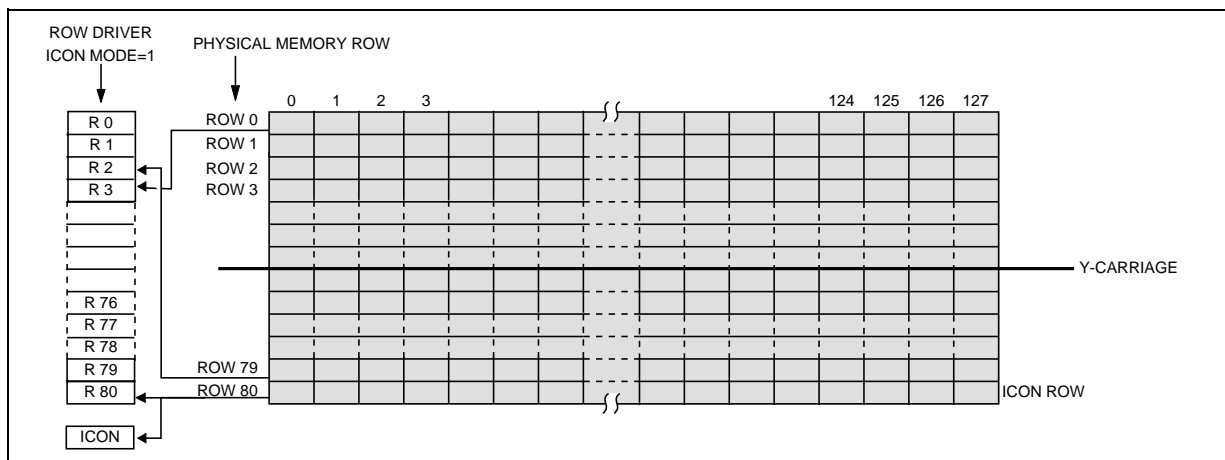


Figure 18. Memory Rows vs. Row drivers mapping with MY=0, MUX 81, SCROLL POINTER=+3, ICON MODE=0

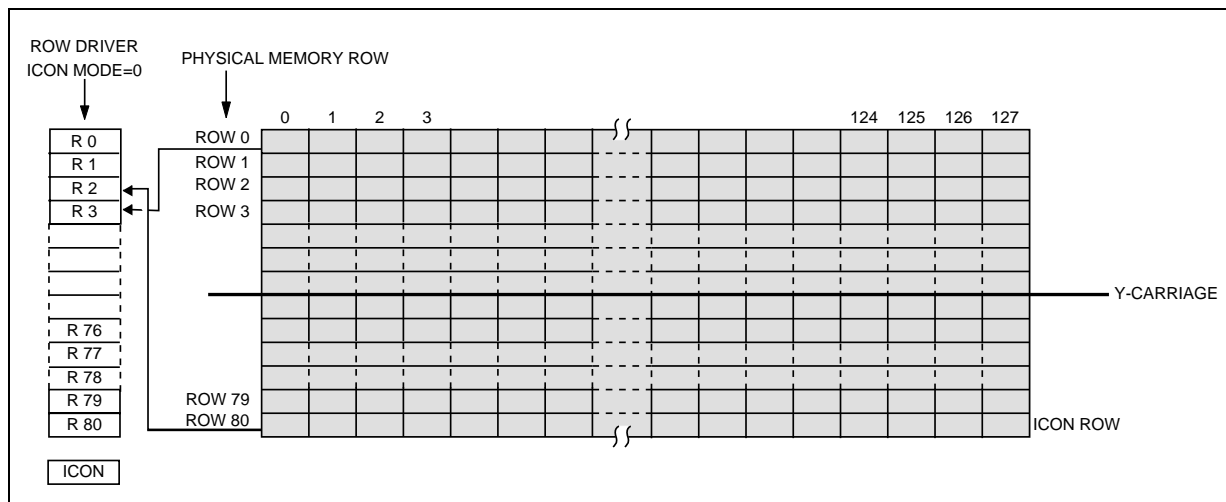


Figure 19. Memory Rows vs. Row drivers mapping with MUX 65 Y-CARRIAGE<=8 SCROLL POINTER=0, ICON MODE=1

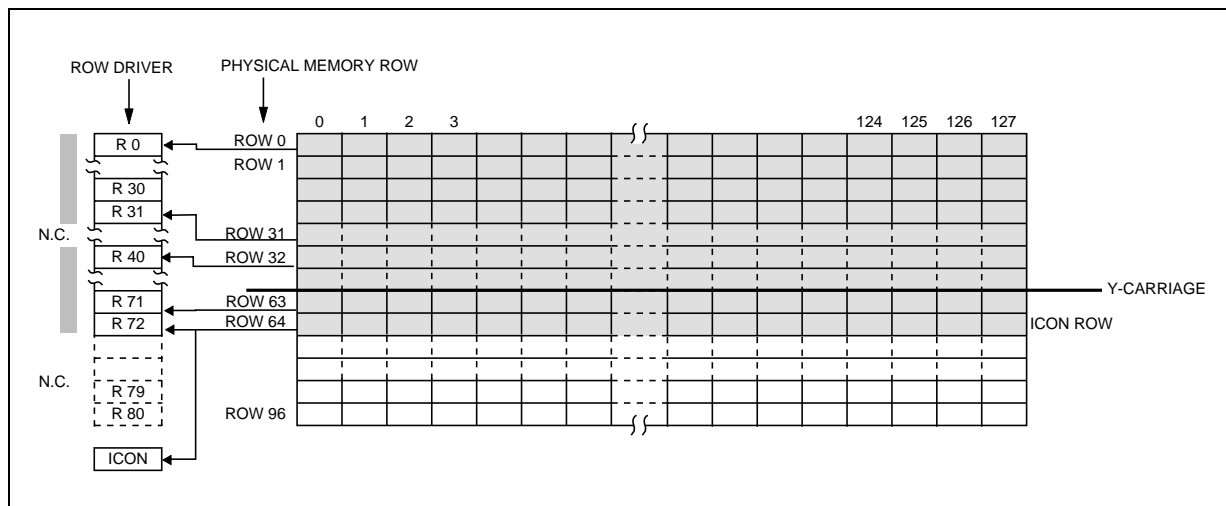


Figure 20. Memory Rows vs. Row drivers mapping with MUX65, Y-CARRIAGE>8, SCROLL POINTER=0, ICON MODE=1

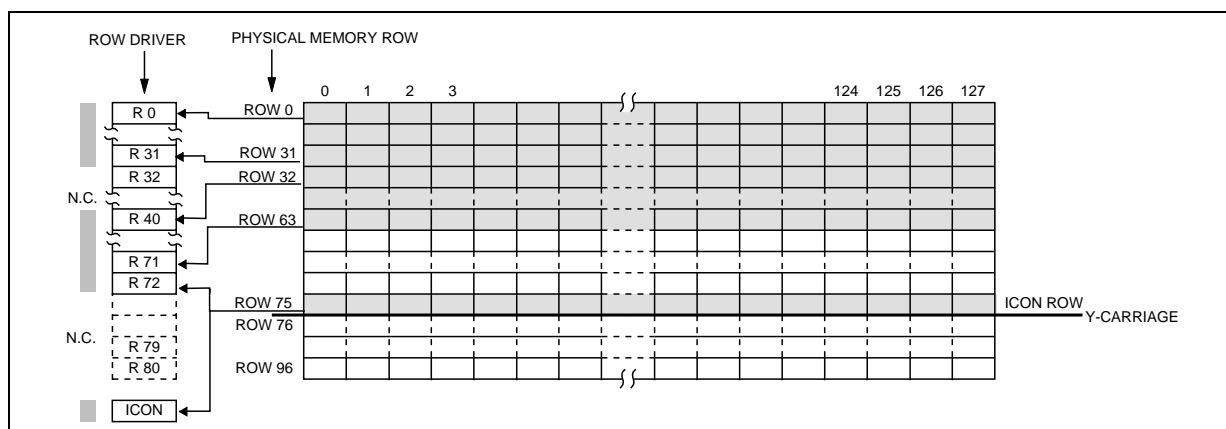


Figure 21. Memory Rows vs. Row drivers mapping with MUX65, Y-CARRIAGE>8, SCROLL POINTER=3, ICON MODE=1,

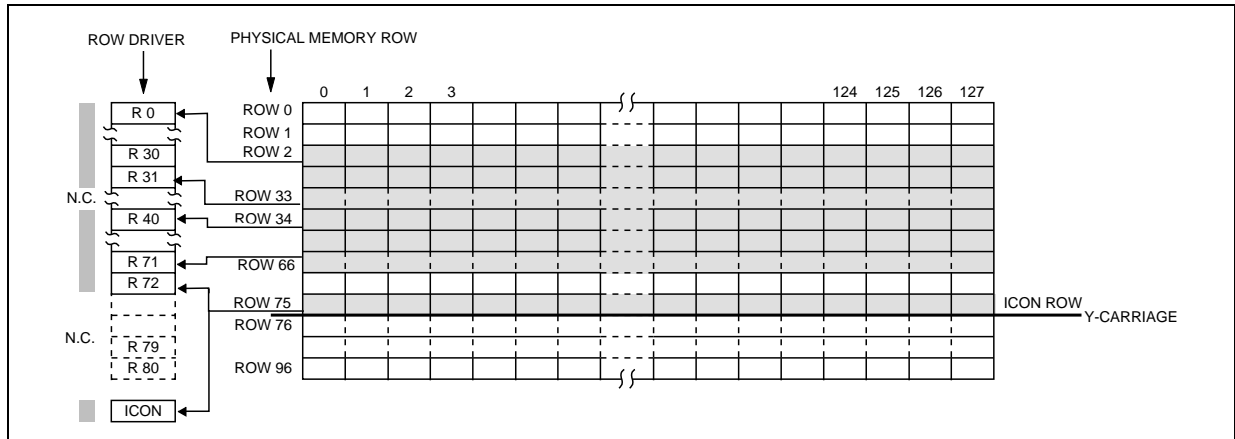


Figure 22. Memory Rows vs. Row drivers mapping with MY=1, MUX81, ICON MODE 0,1 SCROLL POINTER=0

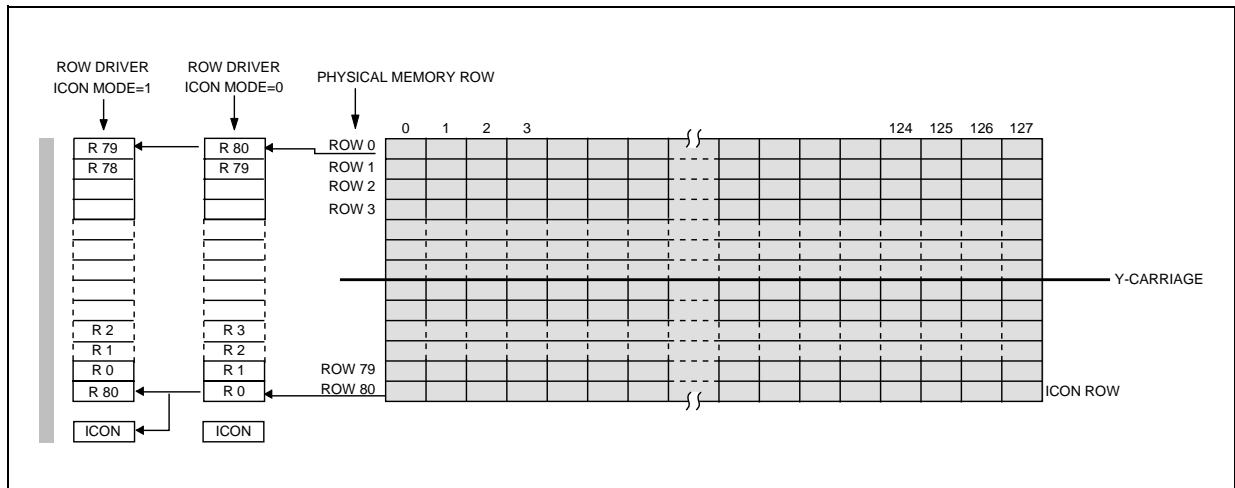


Figure 23. Memory Rows vs. Row drivers mapping with MY=1, MUX81, SCROLL OFFSET= +3, ICON MODE =0

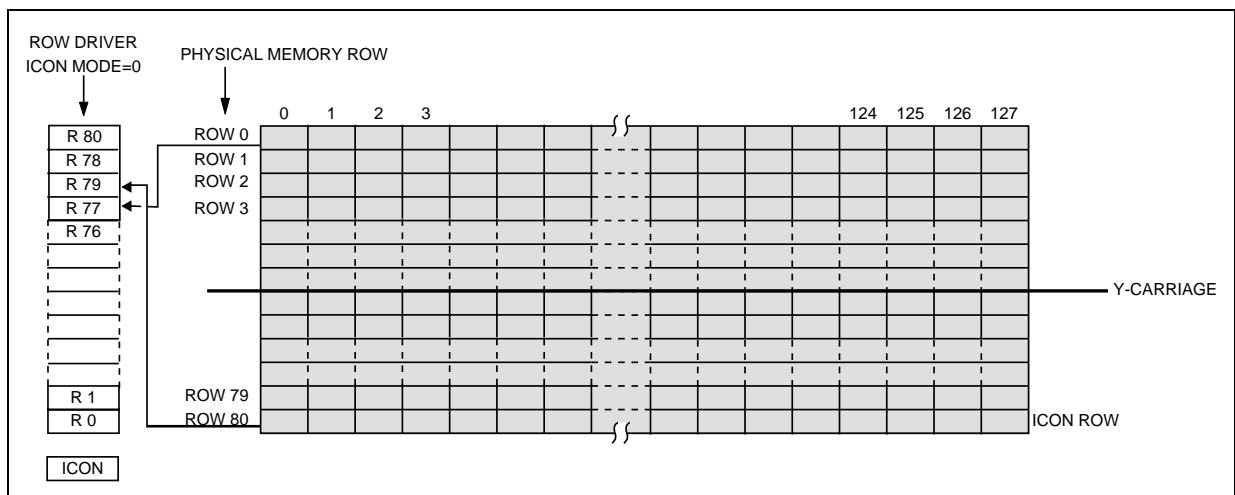


Figure 24. Memory Rows vs. Row drivers mapping with MY=1, MUX81, SCROLL OFFSET= +3, ICON MODE =1

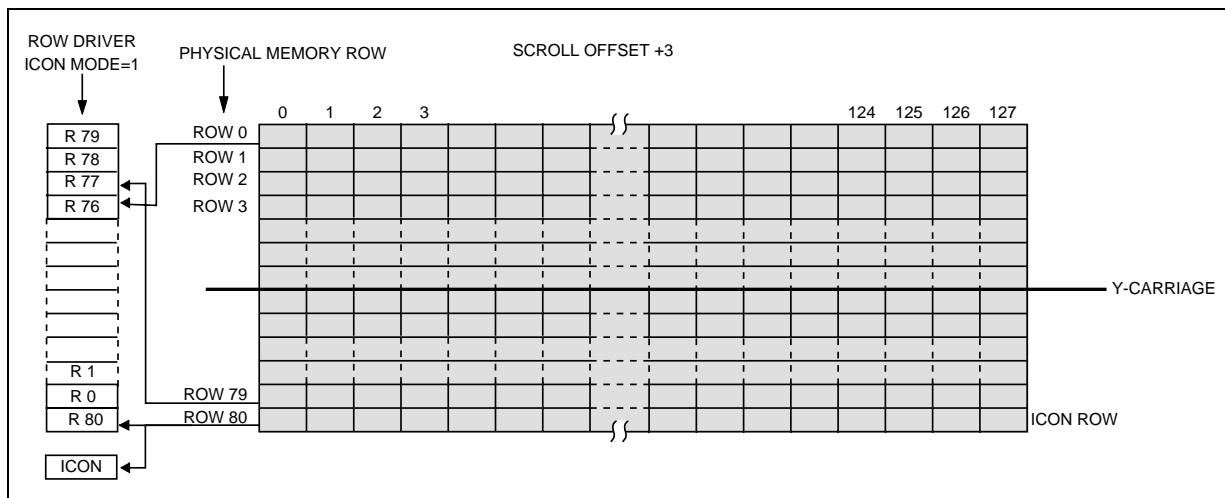


Figure 25. Row Drivers vs. LCD Panel Interconnection in MUX81 Mode

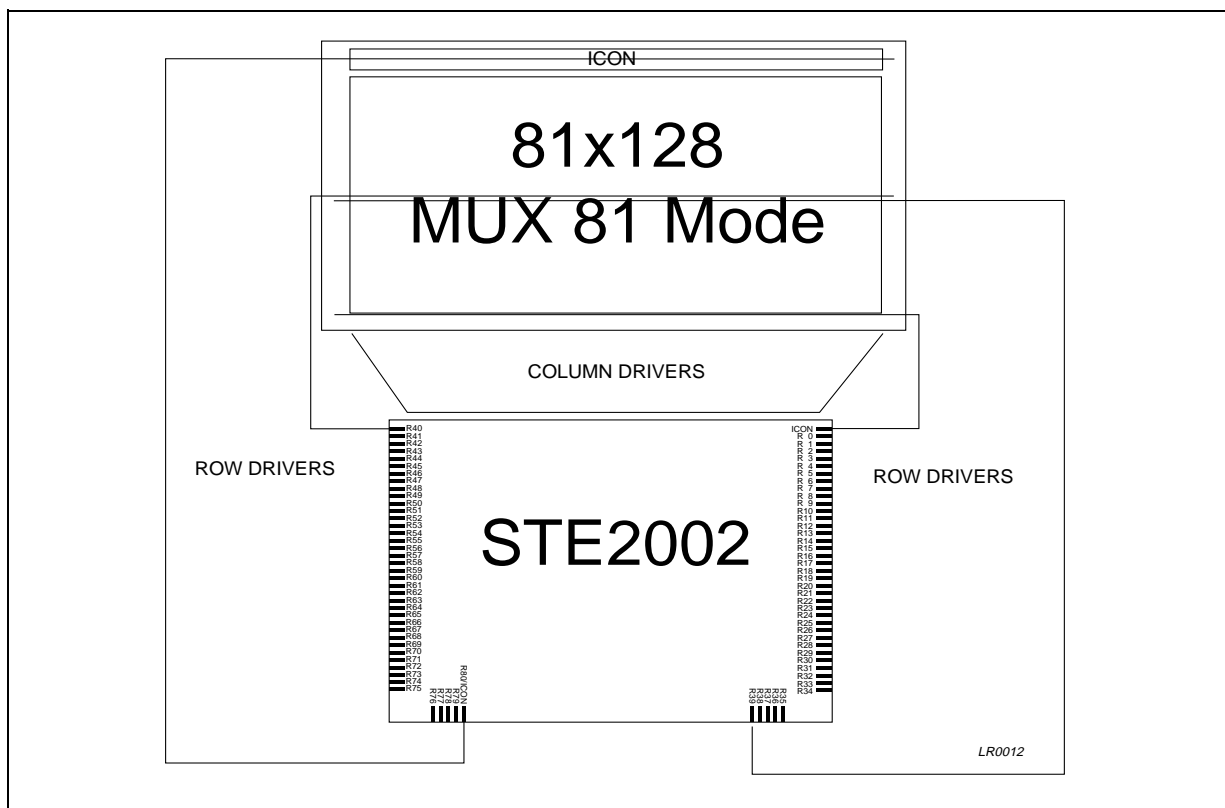


Figure 26. Row Drivers vs. LCD Panel Interconnection in MUX65 Mode

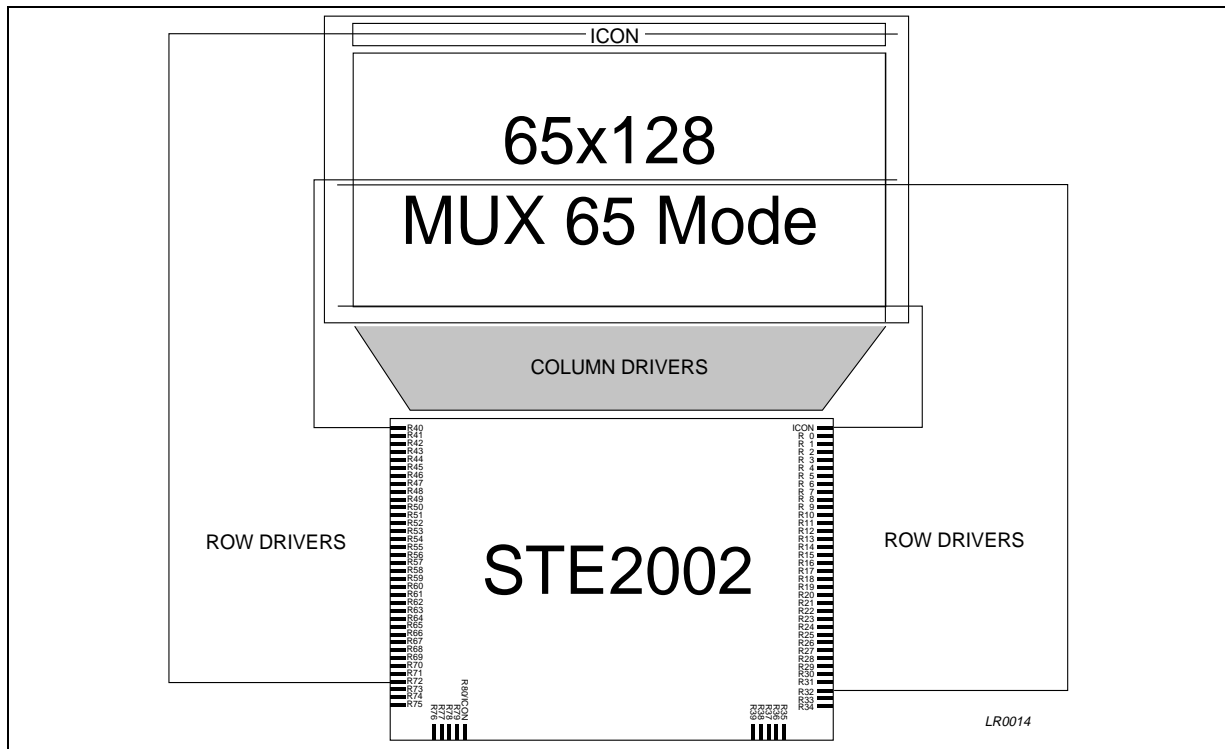


Figure 27. Row Drivers vs. LCD Panel Interconnection in MUX49 Mode

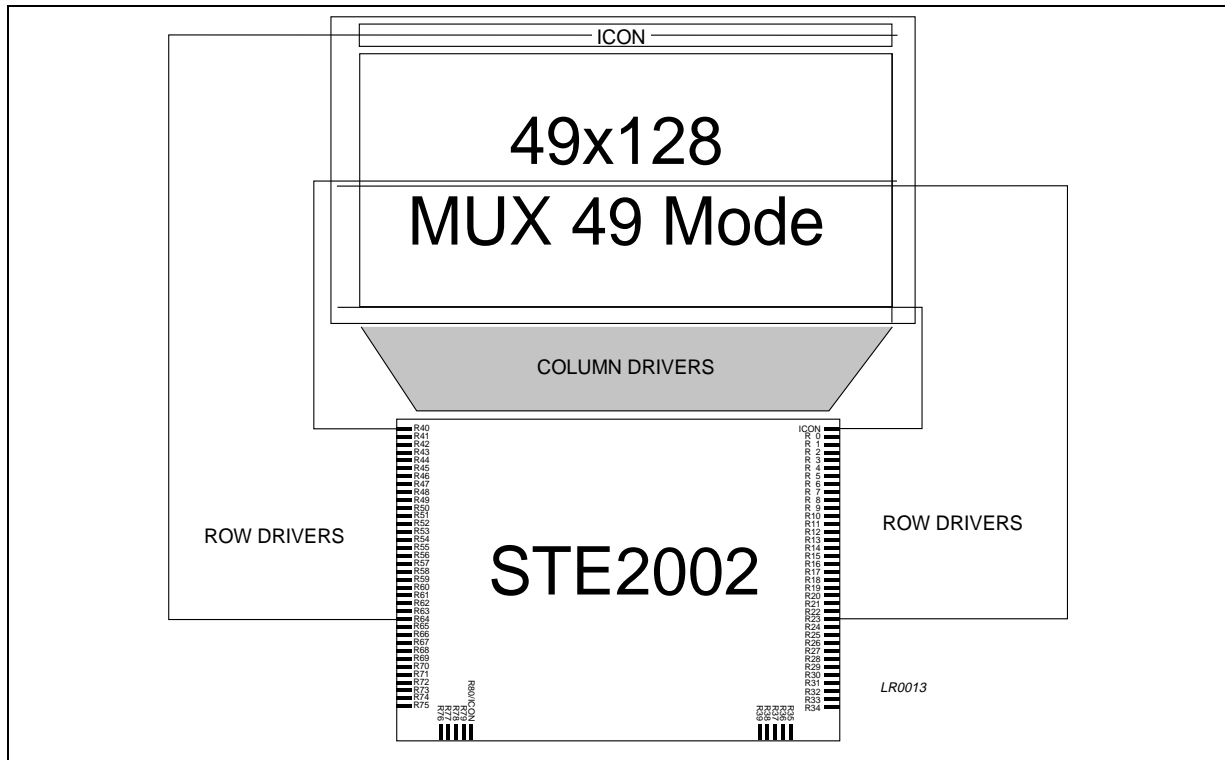
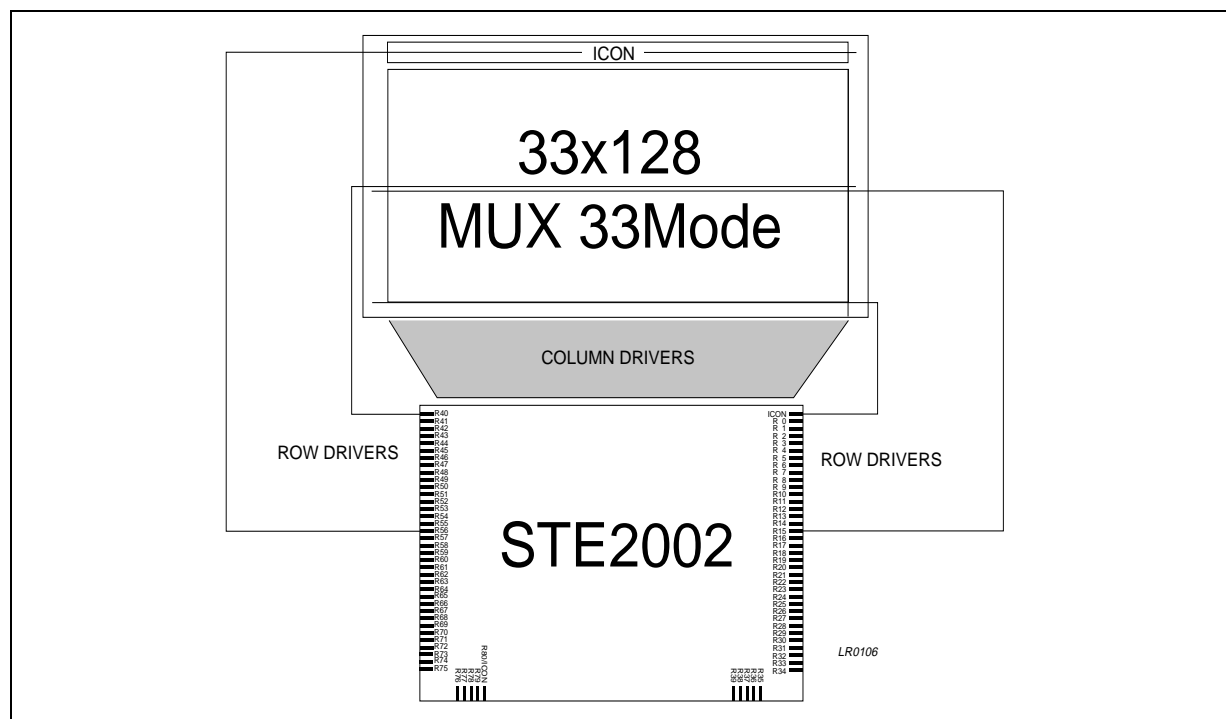


Figure 28. Row Drivers vs. LCD Panel Interconnection in MUX33 Mode



Instruction Set

Two different instructions formats are provided:

- With D/C set to LOW commands are sent to the Control circuitry.
- With D/C set to HIGH the Data RAM is addressed.

Two different instruction set are embedded: the STE2001-like instruction set and the extended instruction set. To select the STE2001-like instruction set the EXT pad has to be connected to a logic LOW (connect to VSS). To select the extended instruction the EXT pad has to be connected to a logic HIGH (connect to VDD1).

The instructions have the syntax summarized in Table 1 (basic-set) and Table 2 (extended set)

Reset (RES)

At power-on, all internal registers are configured with the default value. The RAM content is not defined. A Reset pulse on RES pad (active low) re-initialize the internal registers content (see Tables 3,4,5,&6). Applying a reset pulse, every on-going communication with the host controller is interrupted. After the power-on, the Software Reset instruction can be used to re-load the reset configuration into the internal registers

The Default configurations is: .

- | | |
|---|--|
| - Horizontal addressing (V = 0) | - Bias system (BS[2: 0] = 0) |
| - Normal instruction set (H[1:0] = 0) | - Multiplexing Ratio (M[1:0]=0) |
| - Normal display (MX = MY = 0) | - Frame Rate (FR[1:0]="75Hz") |
| - Display blank (E = D = 0) | - Power Down (PD = 1) |
| - Address counter X[6: 0] = 0 and Y[4: 0] = 0 | - Dual Partial Display Disabled (PE=0) |
| - Temperature coefficient (TC[1: 0] = 0) | - V _{OP} =0 |

A MEMORY BLANK instruction can be executed to clear the RAM content.

Power Down (PD = 1)

When at Power Down, all LCD outputs are kept at V_{SS} (display off). Bias generator and V_{LCD} generator are OFF (V_{LCDOUT} output is discharged to V_{SS} , and then is possible to disconnect V_{LCDOUT}). The internal Oscillator is in off state. An external clock can be provided. The RAM contents is not cleared.

Memory Blanking Procedure

This instruction allows to fill the memory with "blank" patterns, in order to delete patterns randomly generated in memory when starting up the device. This instruction substitutes (128X13) single "write" instructions. It is possible to program "Memory Blanking Procedure" only under the following conditions:

- PD bit = 0

The end of the procedure will be notified on the $\overline{BSY_FLG}$ pad going HIGH (while LOW the procedure is running). Any instruction programmed with $\overline{BSY_FLG}$ LOW will be ignored that is, no instruction can be programmed for a period equivalent to 128X13 internal write cycles (128X13X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I²C interface).

Checker Board Procedure

This instruction allows to fill the memory with "checker-board" pattern. It is mainly intended to developers, who can now simply obtain complex module test configuration by means of a single instruction. It is possible to program "Checker Board Procedure" only under the following conditions:

- PD bit = 0

The end of the procedure will be notified on the $\overline{BSY_FLG}$ pad going HIGH, while LOW the procedure is running. Any instruction programmed with $\overline{BSY_FLG}$ LOW will be ignored, that is, no instruction can be programmed for a period equivalent to 128X13 internal write cycles (128X13X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I²C interface).

Scrolling function

The STE2002 can scroll the graphics display in units of raster-rows. The scrolling function is achieved changing the correspondence between the rows of the logical memory map and the output row drivers. The scroll function doesn't affect the data ram content. It is only related to the visualization process. The information output on the drivers is related to the row reading sequence (the 1st row read is output on R0, the 2nd on R1 and so on). Scrolling means reading the matrix starting from a row that is sequentially increased or decreased. After every scrolling command the offset between the memory address and the memory scanning pointer is increased or decreased by one. The offset range changes in accordance with MUX Rate. After 80th/81th scrolling commands in MUX 81 mode, or after the 64th/65th scrolling commands in mux 65 mode, or after 48nd/49rd scrolling command in MUX 49 mode, or after 32nd/33rd scrolling command in MUX 33 mode, the offset between the memory address and the memory scanning pointer is again zero (Cyclic Scrolling).

A Reset Scrolling Pointer instruction can be executed to force to zero the offset between the memory address and the memory scanning pointer

The Icon Row is not scrolled if ICON MODE =1. If ICON MODE=0 the last row is like a general purpose row and it is scrolled as other rows.

If the DIR Bit is set to a logic zero the offset register is increased by one and the raster is scrolled from top down. If the DIR Bit is set to a logic one the offset register is decreased by one and the raster is scrolled from bottom-up.

| MUX RATE | ICON MODE | OFFSET RANGE | DESCRIPTION | ICON Row Driver with MY=0 |
|----------|-----------|--------------|------------------------|---------------------------|
| MUX 33 | 1 | 0-31 | ICON ROW NOT SCROOLED | R56 |
| MUX 33 | 0 | 0-32 | 33 LINE GRAPHIC MATRIX | R56 |
| MUX 49 | 1 | 0-47 | ICON ROW NOT SCROOLED | R64 |
| MUX 49 | 0 | 0-48 | 49 LINE GRAPHIC MATRIX | R64 |
| MUX 65 | 1 | 0-63 | ICON ROW NOT SCROOLED | R72 |
| MUX 65 | 0 | 0-64 | 65 LINE GRAPHIC MATRIX | R72 |
| MUX 81 | 1 | 0-79 | ICON ROW NOT SCROOLED | R80 |
| MUX 81 | 0 | 0-80 | 81 LINE GRAPHIC MATRIX | R80 |

Dual Partial Display

If the PE Bit is set to a logic one the dual partial display mode is enabled.

Eight partial display modes are available. The offset of the two partial display zones is row by row programmable. The Icon row is accessed last in each partial display frame.

Two sets of register for the HV-generator parameters are provided (PRS[1:0], Vop[6:0], BS[2:0], CP[2:0]). This allows switching from normal mode to partial display mode applying one instruction. The HV generator is automatically re configured using the parameters related to the enabled mode. The parameters of the two sets of registers with the same function are located in the same position of the instruction set. The registers related to the normal mode are accessible when normal mode (PE=0) is selected, the others are accessible when the partial display mode is enabled (PE=1). To Setup PRS[1:0], Vop[6:0], BS[2:0], CP[2:0] values the instruction flow proposed in Fig.46 must be followed. To setup Partial Display Sectors Start Address and Partial Display Mode no particular instruction flow has to be followed.

| PD2 | PD1 | PD0 | SECTION 1 | SECTION2 | RESET STATE |
|-----|-----|-----|-----------|---------------|-------------|
| 0 | 0 | 0 | 0 | 8 + Icon Row | 000 |
| 0 | 0 | 1 | 8 | 0 + Icon Row | |
| 0 | 1 | 0 | 8 | 8 + Icon Row | |
| 0 | 1 | 1 | 0 | 16 + Icon Row | |
| 1 | 0 | 0 | 16 | 0 + Icon Row | |
| 1 | 0 | 1 | 8 | 16 + Icon Row | |
| 1 | 1 | 0 | 16 | 8 + Icon Row | |
| 1 | 1 | 1 | 16 | 16 + Icon Row | |

Bus Interfaces

To provide the widest flexibility and ease of use the STE2002 features three different methods for interfacing the host Controller. To select the desired interface the SEL1 and SEL2 pads need to be connected to a logic LOW (connect to GND) or a logic HIGH (connect to VDD). All the I/O pins of the unused interfaces must be connected to GND.

All interfaces are working while the STE2002 is in Power Down

| SEL2 | SEL1 | Interface | Note |
|------|------|------------------|--|
| 0 | 0 | I ² C | Read and Write; Fast and High Speed Mode |
| 0 | 1 | Serial | Read and Write |
| 1 | 0 | Parallel | Read and Write |
| 1 | 1 | | Not Used |

I²C Interface

The I²C interface is a fully complying I²C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different Ics. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP

condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2002 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAOUT pad to the system SDA line to guarantee a valid LOW level.

To be compliant with the I²C-bus Hs-mode specification the STE2002 is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 29. Bit transfer and START,STOP conditions definition

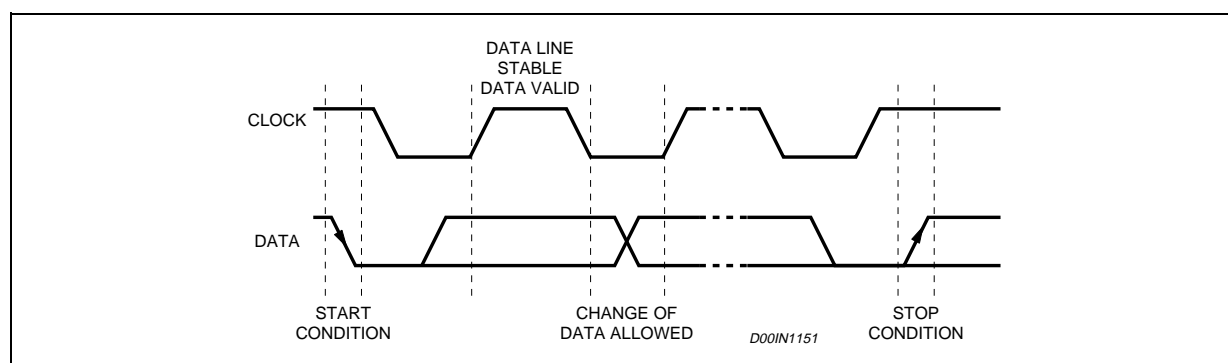
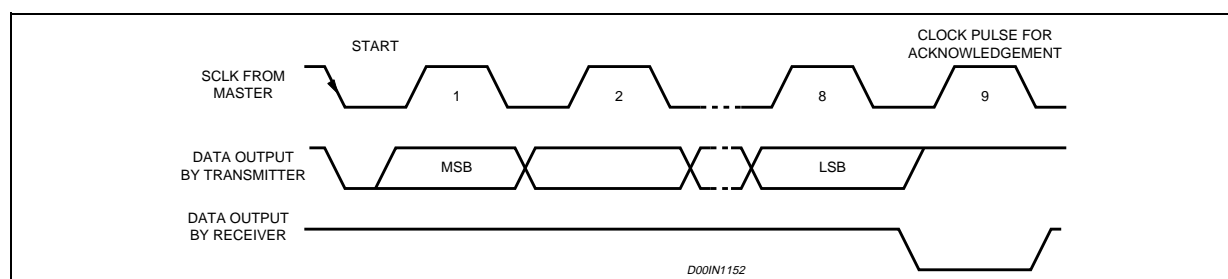


Figure 30. Acknowledgment on the I²C-bus



Communication Protocol

The STE2002 is an I²C slave. The access to the device is bi-directional since data write and status read are allowed. Four are the device addresses available for the device. All have in common the first 5 bits (01111). The two least significant bit of the slave address are set by connecting the SA0 and SA1 inputs to a logic 0 or to a logic 1.

To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, shown in Fig. 30, on the SDA bus line (Most significant bit first). This consists of the 7-bit Device select Code, and the 1-bit Read/Write Designator (R/W).

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

Writing Mode.

If the R/W bit is set to logic 0 the STE2002 is set to be a receiver. After the slaves acknowledge one or more command word follows to define the status of the device.

A command word is composed by two bytes. The first is a control byte which defines the Co and D/C values,

the second is a data byte (fig 31). The Co bit is the command MSB and defines if after this command will follow one data byte and an other command word or if will follow a stream of data (Co = 1 Command word, Co = 0 Stream of data). The D/C bit defines whether the data byte is a command or RAM data (D/C = 1 RAM Data, D/C = 0 Command).

If Co = 1 and D/C = 0 the incoming data byte is decoded as a command, and if Co = 1 and D/C = 1, the following data byte will be stored in the data RAM at the location specified by the data pointer.

Every byte of a command word must be acknowledged by all addressed units.

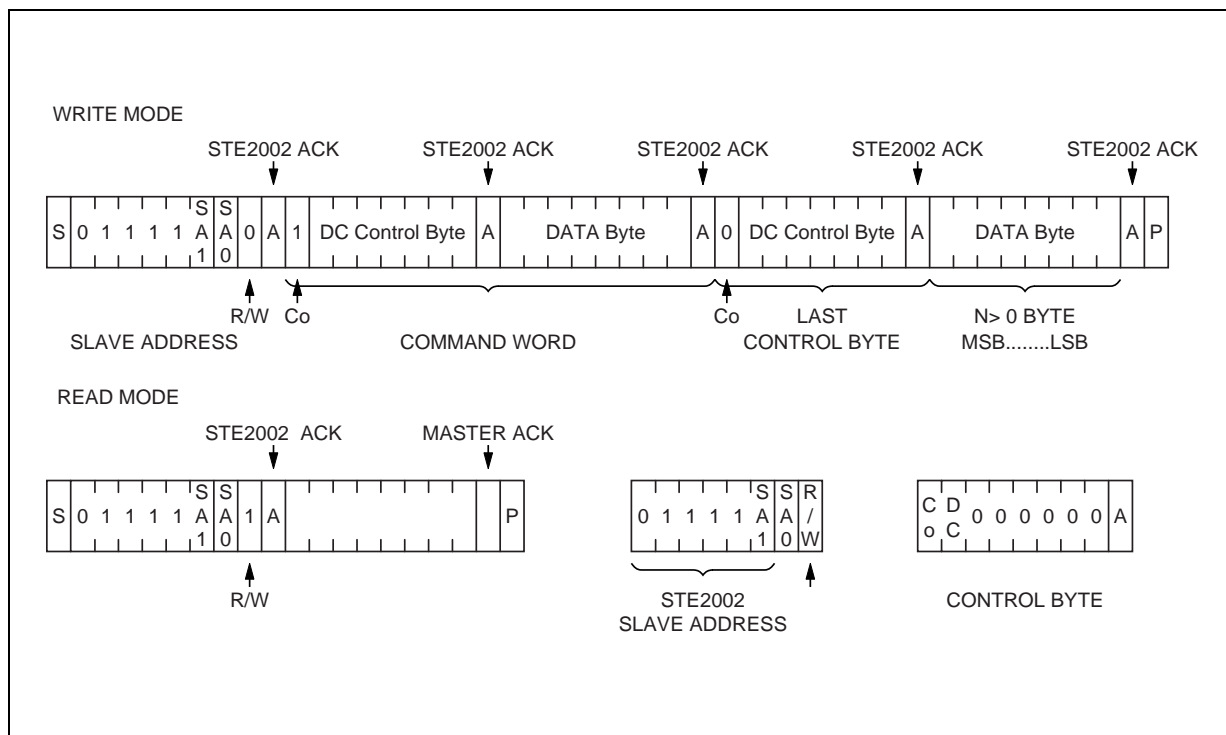
After the last control byte, if D/C is set to a logic 1 the incoming data bytes are stored inside the STE2002 Display RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.

Every byte must be acknowledged by all addressed units.

Reading Mode.

If the R/W bit is set to logic 1 the chip will output data immediately after the slave address. If the D/C bit sent during the last write access, is set to a logic 0, the byte read is the status byte.

Figure 31. Communication Protocol



SERIAL INTERFACE

The STE2002 serial Interface is a bidirectional link between the display driver and the application supervisor.

It consists of five lines: two for data signals (SDIN, SOUT), one for clock signals (SCLK), one for the peripheral enable (SCE) and one for mode selection (SD/C).

The serial interface is active only if the SCE line is set to a logic 0. When SCE line is high the serial peripheral power consumption is zero. While SCE pin is high the serial interface is kept in reset.

The STE2002 is always a slave on the bus and receive the communication clock on the SCLK pin from the master.

Information are exchanged byte-wide. During data transfer, the data line is sampled on the positive SCLK edge.

SD/C line status indicates whether the byte is a command (SD/C = 0) or RAM data (SD/C = 1); it is read on the eighth SCLK clock pulse during every byte transfer.



If \overline{SCE} stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next byte at the next SCLK positive edge.

A reset pulse on \overline{RES} pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.

If \overline{SCE} is low after the positive edge of \overline{RES} , the serial interface is ready to receive data.

Throughout SOUT can be read only the driver I²C slave address. The Command sequence that allows to read I²C slave address is reported in Fig. 34 & 35. SOUT is in High impedance in steady state and during data write. It is possible to short circuit DOUT and SDIN and read I²C address without any additional lines.

Figure 32. Serial bus protocol - one byte transmission

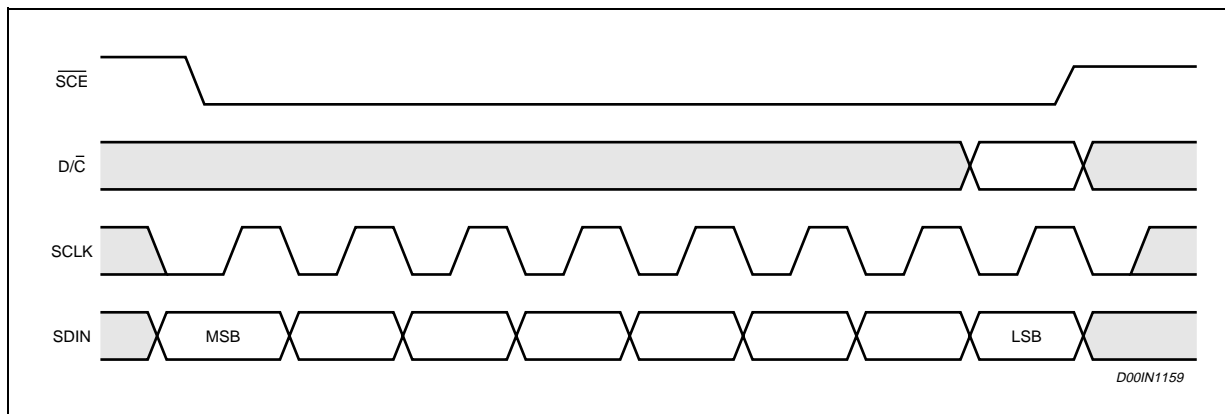


Figure 33. Serial bus protocol - several byte transmission

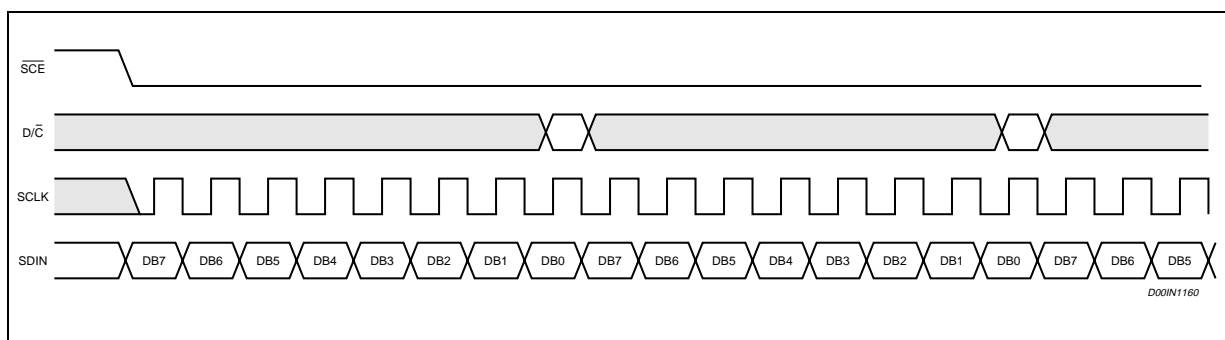


Figure 34. Serial bus protocol - several byte transmission

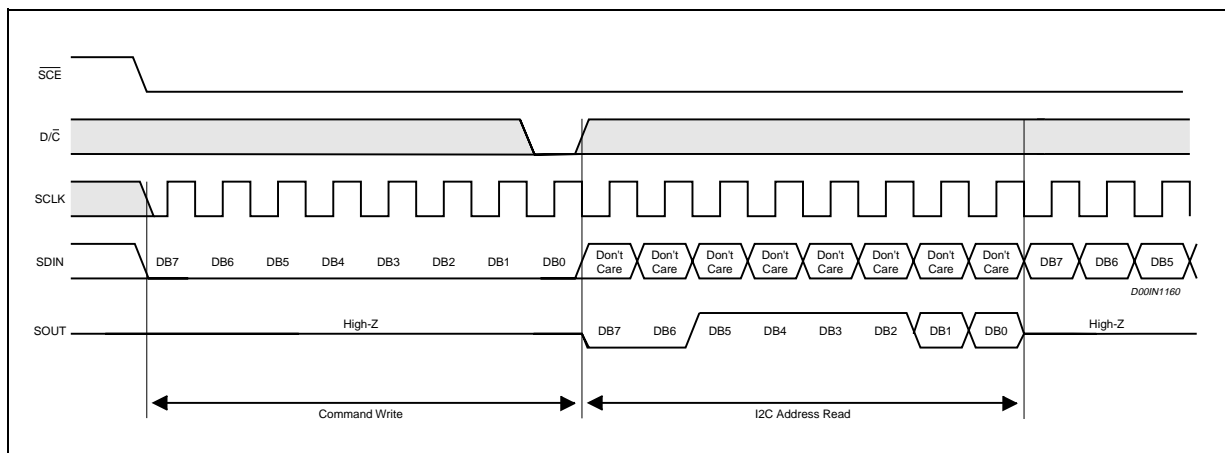
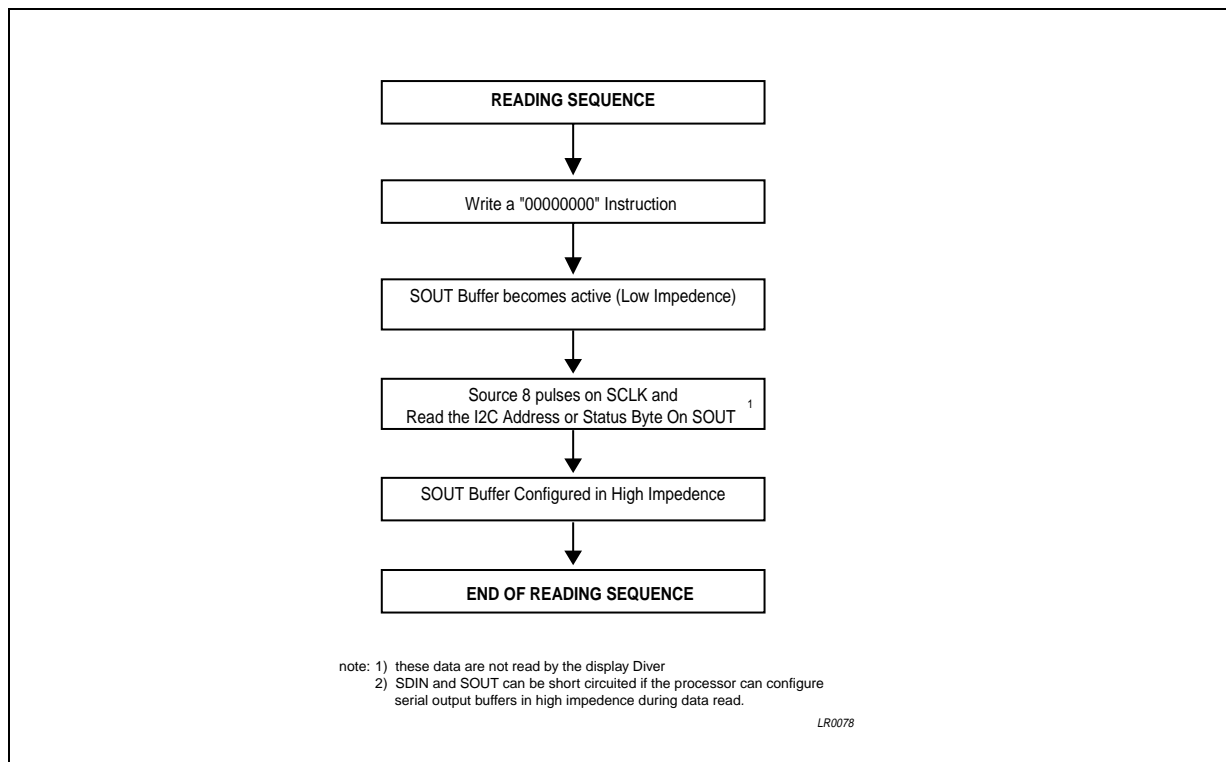


Figure 35. Reading Sequence



Parallel Interface

The STE2002 parallel Interface is a bidirectional link between the display driver and the application supervisor. It consists of eleven lines: eight data lines (from DB7 to DB0) and three control lines. The control lines are: enable (E) for data latch, PD/C for mode selection and R/W for reading or writing.

The data lines and the control line values are internally latched on E rising edge (fig. 50).

When the parallel interface is selected, if R/W line is set to "one", D0-D7 lines are configured as output drivers (low impedance) and it is possible to read the driver I²C address (Fig. 51)

Table 1. STE2001-like instruction Set

| Instruction | D/C | R/W | | | | | | | | | Description | |
|--------------------------------|-----|-----|----|-----|-----|-----|-----|-----|-----|------|-------------|---|
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| H=0 or H=1 | | | | | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Read I ² C Address (with Serial Interface only) |
| Function Set | 0 | 0 | 0 | 0 | 1 | MX | MY | PD | V | H[0] | | Power Down Management; Entry Mode; |
| Read Status Byte | 0 | 1 | PD | A1 | A2 | D | E | MX | MY | DO | | (I ² C interface only) |
| Write Data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Writes data to RAM |
| H=0 | | | | | | | | | | | | |
| Memory Blank | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Memory Blank Procedure |
| Scroll | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DIR | Scrolls by one Row UP or DOWN |
| V _{LCD} Range Setting | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | PRS [0] | V _{LDC} programming range selection |
| Display Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | 0 | E | Select Display Configuration |
| Set CP Factor | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S2 | S1 | S0 | | Charge Pump Multiplication factor |
| Set RAM Y | 0 | 0 | 0 | 1 | 0 | 0 | Y3 | Y2 | Y1 | Y0 | | Set Horizontal (Y) RAM Address |
| Set RAM X | 0 | 0 | 1 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | | Set Vertical (X) RAM Address |
| H=1 | | | | | | | | | | | | |
| Checker Board | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Checker Board Procedure |
| Multiplex Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | MUX | Selects MUX factor |
| TC Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | TC1 | TC0 | Set Temperature Coefficient for V _{LDC} |
| Output Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DO | A1 | A2 | No function |
| Bias Ratios | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BS2 | BS1 | BS0 | | Set desired Bias Ratios |
| Reserved | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | Not to be used |
| Set V _{OP} | 0 | 0 | 1 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | | V _{OP} register Write instruction |

Table 2. Extended Instruction Set

| Instruction | D/C | R/W | | | | | | | | | Description | |
|-----------------------------------|-----|-----|----|-------|-------|-------|-------|-------|-------|---------|---|--|
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| H Independent Instructions | | | | | | | | | | | | |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Read I ² C Address (with Serial Interface only) | |
| Function Set | 0 | 0 | 0 | 0 | 1 | MX | MY | PD | H[1] | H[0] | Power Down Management; Entry Mode; Extended Instruction Set | |
| Read Status Byte | 0 | 1 | PD | 0 | 0 | D | E | MX | MY | DO | (I ² C interface only) | |
| Write Data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Writes data to RAM | |
| H=[0;0] RAM Commands | | | | | | | | | | | | |
| Memory Blank | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Memory Blank Procedure | |
| Scroll | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DIR | Scrolls by one Row UP or DOWN |
| V _{LCD} Range Setting | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | PRS [1] | PRS [0] | V _{LDC} programming range selection |
| Display Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | 0 | E | Select Display Configuration | |
| Set CP Factor | 0 | 0 | 0 | 0 | 0 | 1 | 0 | S2 | S1 | S0 | Charge Pump Multiplication factor | |
| Set RAM Y | 0 | 0 | 0 | 1 | 0 | 0 | Y3 | Y2 | Y1 | Y0 | Set Horizontal (Y) RAM Address | |
| Set RAM X | 0 | 0 | 1 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Set Vertical (X) RAM Address | |
| H=[0;1] | | | | | | | | | | | | |
| Checker Board | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Checker Board Procedure |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | V | Vertical Addressing Mode |
| TC Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | TC1 | TC0 | Set Temperature Coefficient for V _{LDC} |
| Data Format | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DO | 0 | 0 | MSB Position |
| Bias Ratios | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BS2 | BS1 | BS0 | Set desired Bias Ratios | |
| | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | Reserved |
| Set V _{OP} | 0 | 0 | 1 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | V _{OP} register Write instruction | |
| H=[1;0] | | | | | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software RESET |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | PE | Partial Enable |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | FR1 | FR0 | Frame rate Control |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | M[1] | M[0] | Mux Ratio |
| Partial Mode | 0 | 0 | 0 | 0 | 0 | 1 | 0 | PD2 | PD1 | PD0 | Partial Display Config | |
| | 0 | 0 | 0 | 1 | PD Y5 | PD Y4 | PD Y3 | PD Y2 | PD Y1 | PDY 0 | 1 st Sector Start Address | |
| | 0 | 0 | 1 | PD Y6 | PD Y5 | PD Y4 | PD Y3 | PD Y2 | PD Y1 | PD Y0 | 2 nd Sector Start Address | |
| H=[1;1] | | | | | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Scrolling Pointer Reset |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Not Used |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | Not Used |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | T2 | T1 | T0 | Set Temperature Coefficient for V _{LDC} |
| | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | Not Used |
| | 0 | 0 | 0 | 1 | 0 | 0 | YC-3 | YC-2 | YC-1 | YC-0 | Y-CARRIAGE RETURN | |
| | 0 | 0 | 1 | XC-6 | XC-5 | XC-4 | XC-3 | XC-2 | XC-1 | XC-0 | X CARRIAGE RETURN | |

Table 3. Explanations of Table 2 symbols

| BIT | 0 | 1 | RESET STATE |
|------|--|--|-------------|
| DIR | Scroll by one down | Scroll by one up | |
| PD | Device fully working | Device in power down | 1 |
| V | Horizontal addressing | Vertical addressing | 0 |
| MX | Normal X axis addressing | X axis address is mirrored. | 0 |
| MY | Image is displayed not vertically mirrored | Image is displayed vertically mirrored | 0 |
| DO | MSB on TOP | MSB on BOTTOM | 0 |
| PE | Partial Display disabled | Partial Display enabled | 0 |
| H[0] | Select page 0 | Select page 1 | 0 |
| MUX | MUX 65 | MUX 33 | 0 |

Table 4. PAGE NUMBER

| H[1] | H[0] | DESCRIPTION | RESET STATE |
|------|------|-------------|-------------|
| 0 | 0 | Page 0 | Page 0 |
| 0 | 1 | Page 1 | |
| 1 | 0 | Page 2 | |
| 1 | 1 | Page 3 | |

Table 5. DISPLAY MODE

| D | E | DESCRIPTION | RESET STATE |
|---|---|-------------------------|-------------|
| 0 | 0 | display blank | D=0 E=0 |
| 0 | 1 | all display segments on | |
| 1 | 0 | normal mode | |
| 1 | 1 | inverse video mode | |

Table 6. FRAME RATE CONTROL

| FR[1] | FR[0] | DESCRIPTION | RESET STATE |
|-------|-------|-------------|-------------|
| 0 | 0 | 65Hz | 75Hz |
| 0 | 1 | 70Hz | |
| 1 | 0 | 75Hz | |
| 1 | 1 | 80Hz | |

Table 7. VLCD RANGE SELECTION

| PRS[1] | PRS[0] | DESCRIPTION | RESET STATE |
|--------|--------|-------------|-------------|
| 0 | 0 | 2.94 | |
| 0 | 1 | 6.78 | |
| 1 | 0 | 10.62 | |
| 1 | 1 | Not Used | |

Table 8. MULTIPLEXING RATIO

| M[1] | M[0] | DESCRIPTION | RESET STATE |
|------|------|-------------|-------------|
| 0 | 0 | 49 | 01 |
| 0 | 1 | 65 | |
| 1 | 0 | 81 | |
| 1 | 1 | Not Used | |

Table 9. TEMPERATURE COEFFICIENT

| T2 | T1 | T0 | DESCRIPTION | RESET STATE |
|----|----|----|--------------------------------|-------------|
| 0 | 0 | 0 | VLCD temperature Coefficient 0 | 000 |
| 0 | 0 | 1 | VLCD temperature Coefficient 1 | |
| 0 | 1 | 0 | VLCD temperature Coefficient 2 | |
| 0 | 1 | 1 | VLCD temperature Coefficient 3 | |
| 1 | 0 | 0 | VLCD temperature Coefficient 4 | |
| 1 | 0 | 1 | VLCD temperature Coefficient 5 | |
| 1 | 1 | 0 | VLCD temperature Coefficient 6 | |
| 1 | 1 | 1 | VLCD temperature Coefficient 7 | |

Table 10.

| TC1 | TC0 | DESCRIPTION | RESET STATE |
|-----|-----|--------------------------------|-------------|
| 0 | 0 | VLCD temperature Coefficient 0 | 00 |
| 0 | 1 | VLCD temperature Coefficient 2 | |
| 1 | 0 | VLCD temperature Coefficient 3 | |
| 1 | 1 | VLCD temperature Coefficient 6 | |

Table 11. CHARGE PUMP MULTIPLICATION FACTOR

| CP2 | CP1 | CP0 | DESCRIPTION | RESET STATE |
|-----|-----|-----|--------------------------|-------------|
| 0 | 0 | 0 | Multiplication Factor X2 | 000 |
| 0 | 0 | 1 | Multiplication Factor X3 | |
| 0 | 1 | 0 | Multiplication Factor X4 | |
| 0 | 1 | 1 | Multiplication Factor X5 | |
| 1 | 0 | 0 | Multiplication Factor X6 | |
| 1 | 0 | 1 | NOT USED | |
| 1 | 1 | 0 | NOT USED | |
| 1 | 1 | 1 | AUTOMATIC | |

Table 12. BIAS RATIO

| BS2 | BS1 | BS0 | DESCRIPTION | RESET STATE |
|-----|-----|-----|-----------------------|-------------|
| 0 | 0 | 0 | Bias Ratio equal to 7 | 000 |
| 0 | 0 | 1 | Bias Ratio equal to 6 | |
| 0 | 1 | 0 | Bias Ratio equal to 5 | |
| 0 | 1 | 1 | Bias Ratio equal to 4 | |
| 1 | 0 | 0 | Bias Ratio equal to 3 | |
| 1 | 0 | 1 | Bias Ratio equal to 2 | |
| 1 | 1 | 0 | Bias Ratio equal to 1 | |
| 1 | 1 | 1 | Bias Ratio equal to 0 | |

Table 13. Y CARRIAGE RETURN REGISTER

| Y-C[3] | Y-C[2] | Y-C[1] | Y-C[0] | DESCRIPTION | RESET STATE |
|--------|--------|--------|--------|----------------|-------------|
| 0 | 0 | 0 | 0 | | 1000 |
| 0 | 0 | 0 | 1 | Y-CARRIAGE =1 | |
| 0 | 0 | 1 | 0 | Y-CARRIAGE =2 | |
| 0 | 0 | 1 | 1 | Y-CARRIAGE =3 | |
| 0 | 1 | 0 | 0 | Y-CARRIAGE =4 | |
| 0 | 1 | 0 | 1 | Y-CARRIAGE =5 | |
| . | . | . | . | | |
| 1 | 0 | 1 | 0 | Y-CARRIAGE =10 | |
| 1 | 0 | 1 | 1 | Y-CARRIAGE =11 | |
| 1 | 1 | 0 | 0 | Y-CARRIAGE =12 | |

Table 14. PARTIAL DISPLAY CONFIGURATION

| PD2 | PD1 | PD0 | SECTION 1 | SECTION2 | RESET STATE |
|-----|-----|-----|-----------|---------------|-------------|
| 0 | 0 | 0 | 0 | 8 + Icon Row | 000 |
| 0 | 0 | 1 | 8 | 0 + Icon Row | |
| 0 | 1 | 0 | 8 | 8 + Icon Row | |
| 0 | 1 | 1 | 0 | 16 + Icon Row | |
| 1 | 0 | 0 | 16 | 0 + Icon Row | |
| 1 | 0 | 1 | 8 | 16 + Icon Row | |
| 1 | 1 | 0 | 16 | 8 + Icon Row | |
| 1 | 1 | 1 | 16 | 16 + Icon Row | |

Figure 36. Host Processor Interconnection with I2C Interface

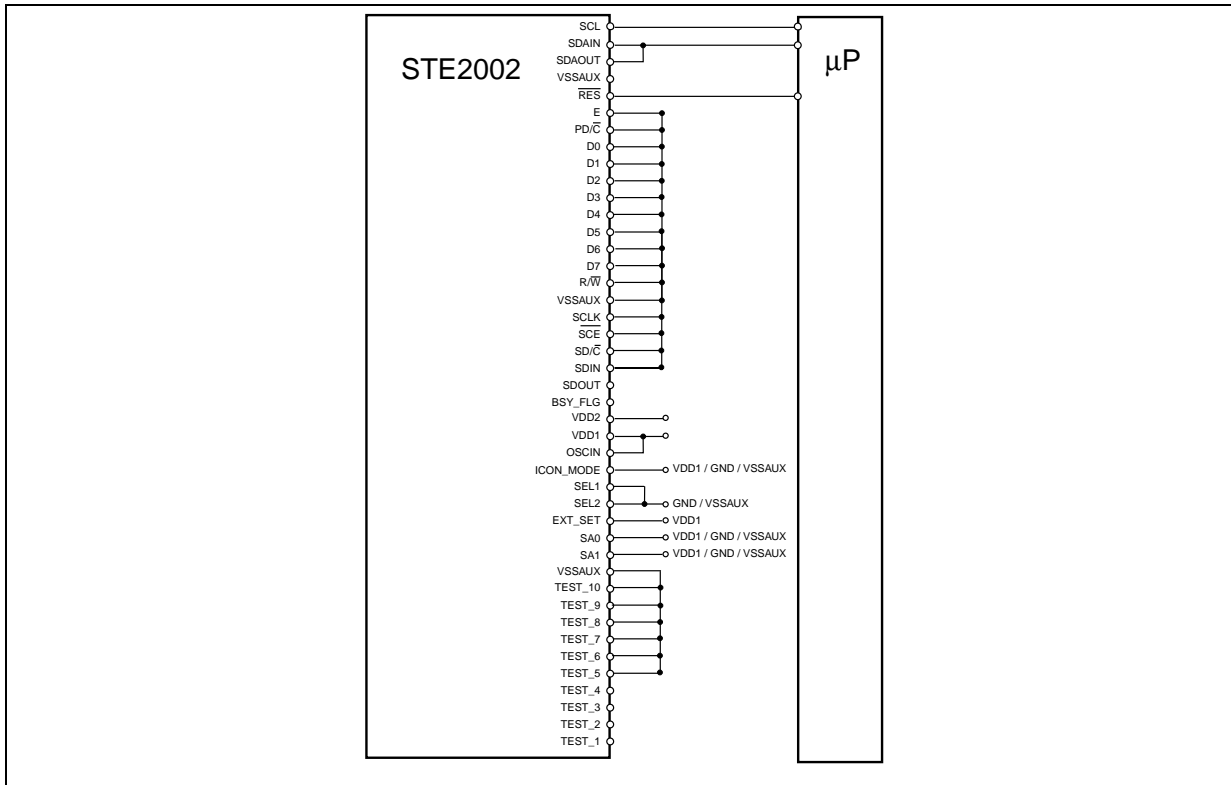


Figure 37. Host Processor Interconnection with Serial Interface

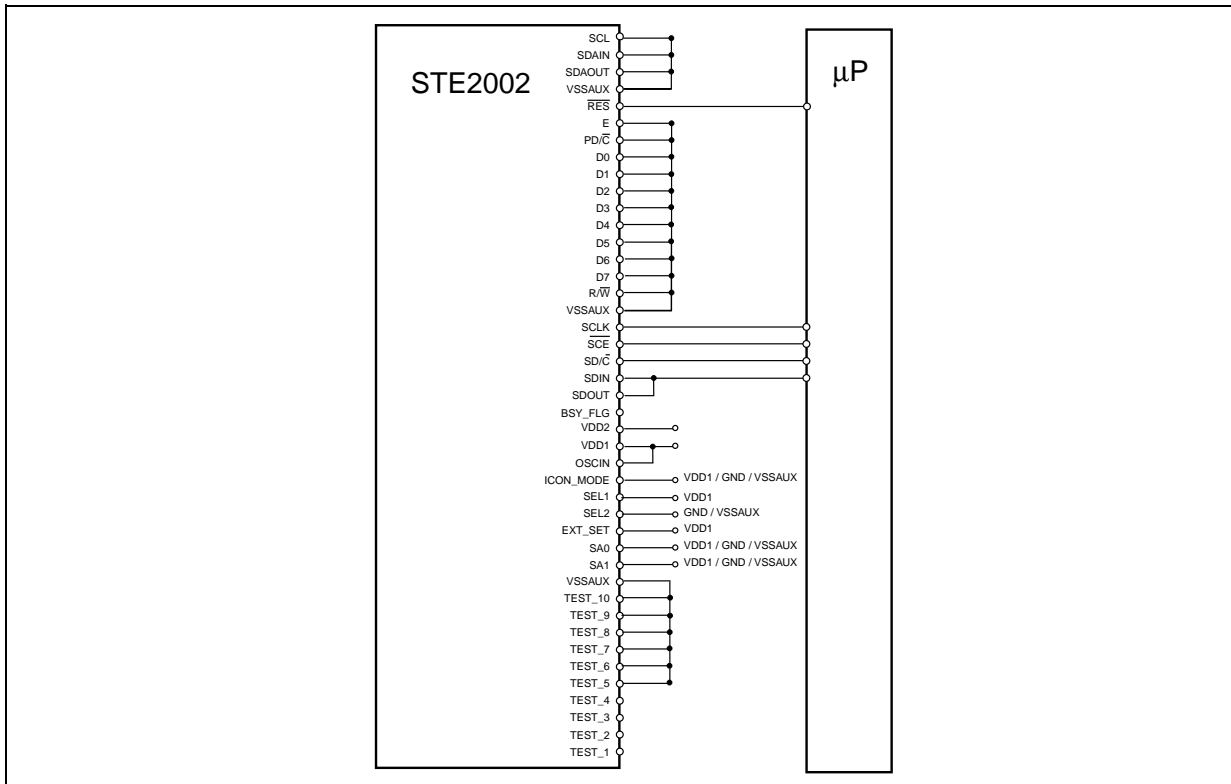


Figure 38. Host Processor Interconnection with Parallel Interface

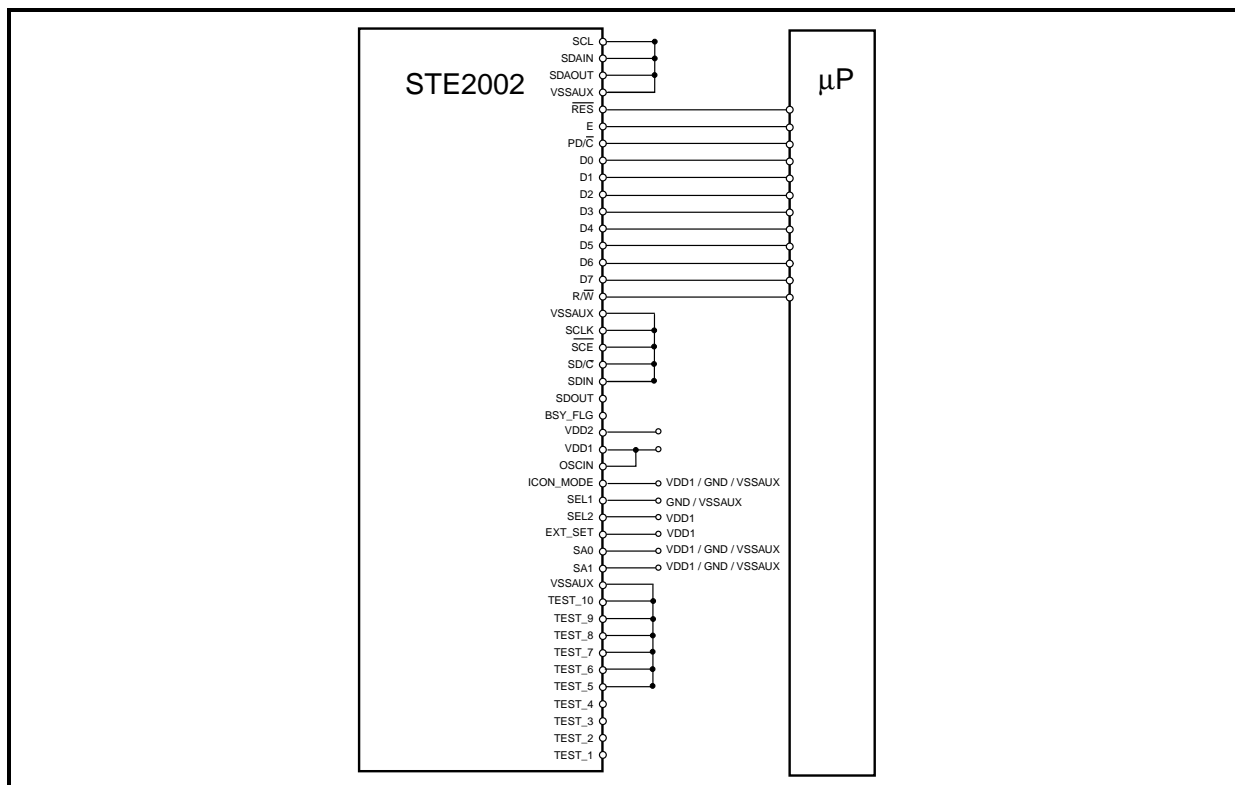


Figure 39. Application Schematic Using an External LCD Voltage Generator

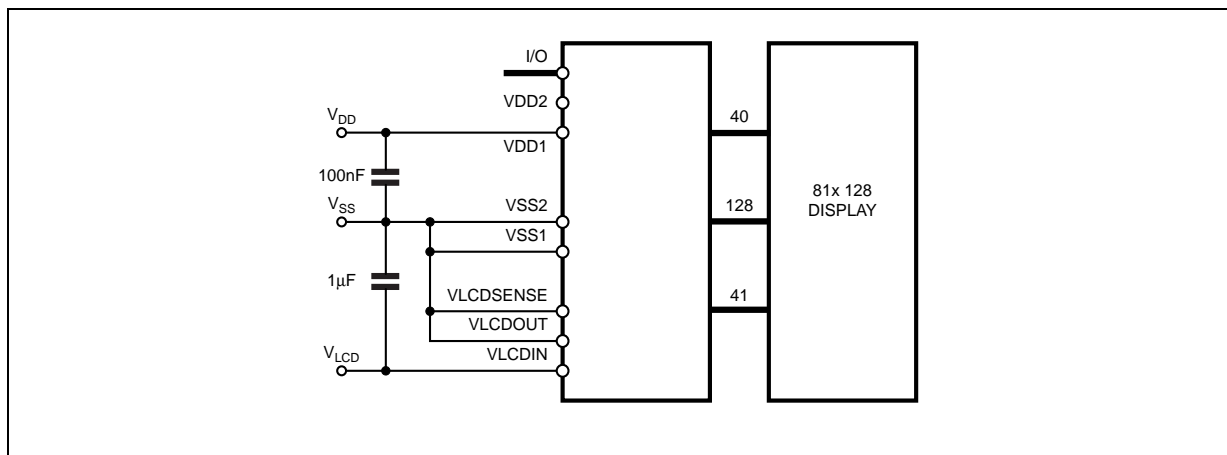


Figure 40. Application Schematic using the Internal LCD Voltage Generator and two separate supplies

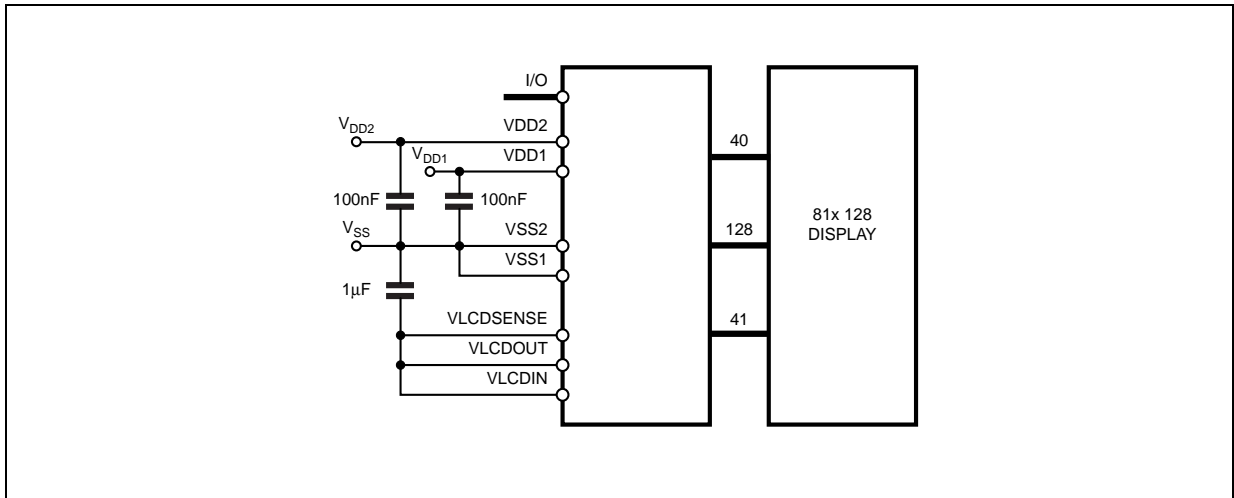


Figure 41. Application Schematic using the Internal LCD Voltage Generator and a single supply

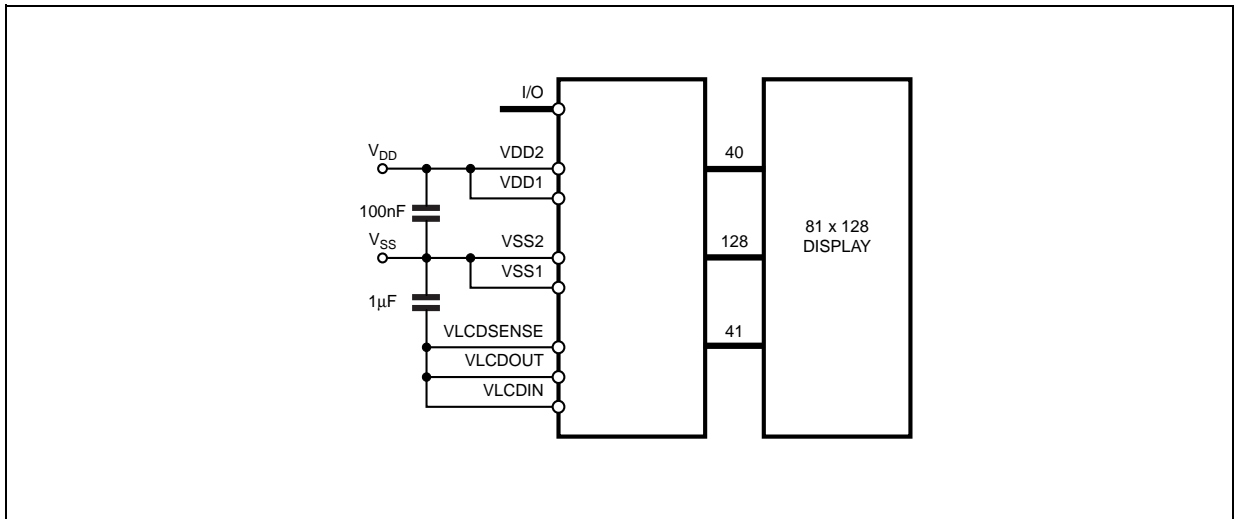


Figure 42. Power-Up sequence

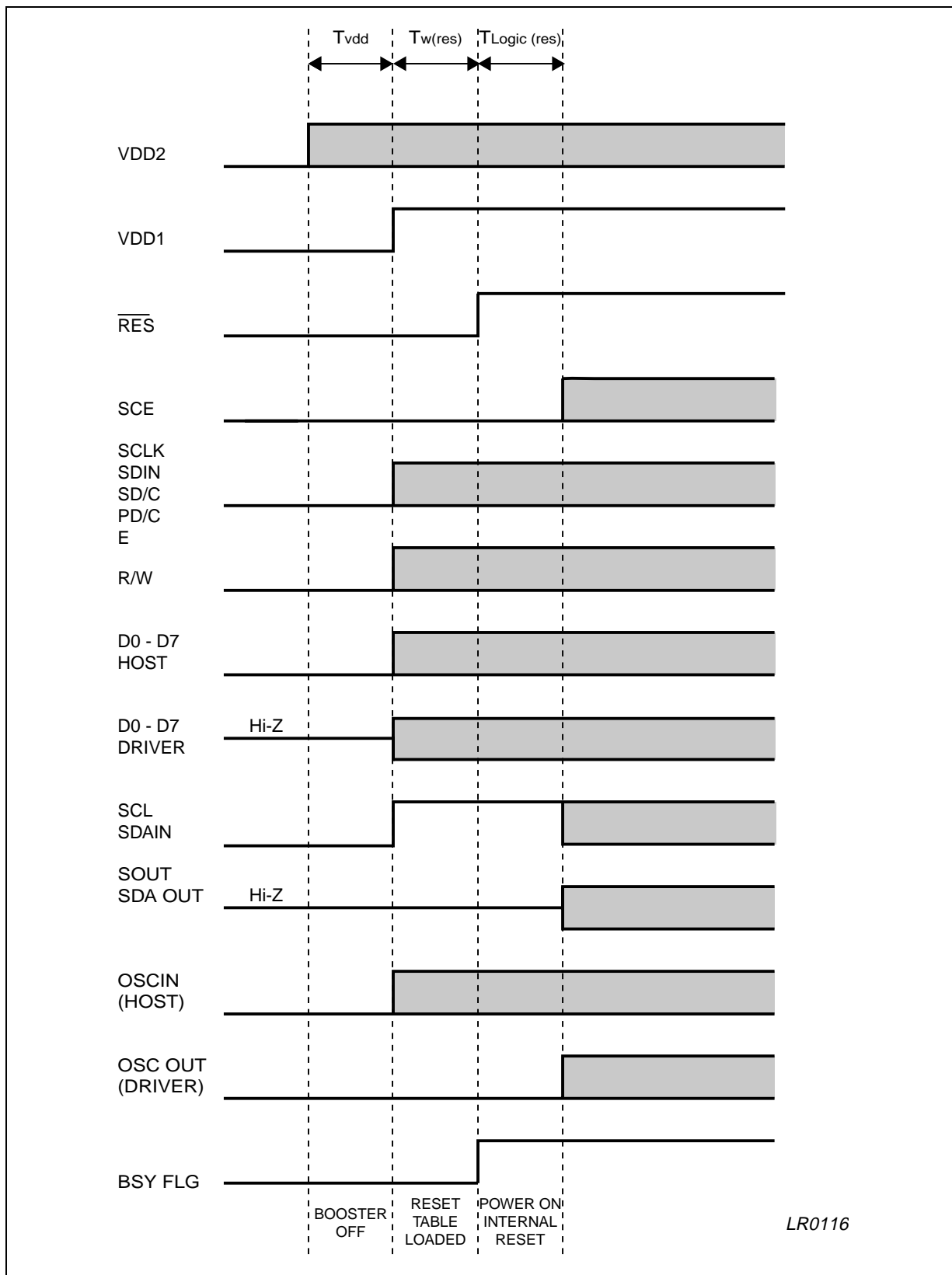
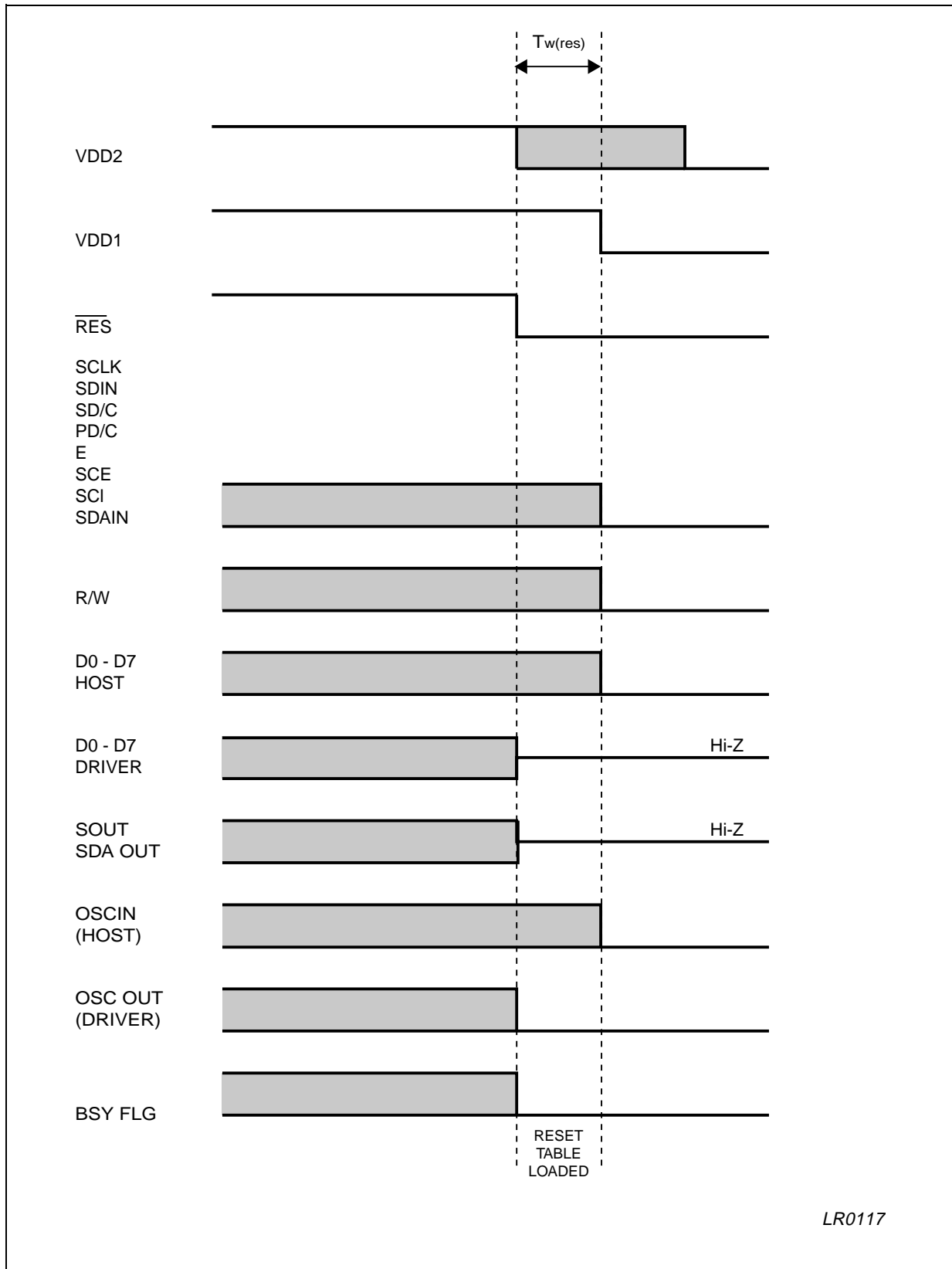


Figure 43. Power-OFF Sequence



LR0117

Figure 44. Initialization with built-in Booster

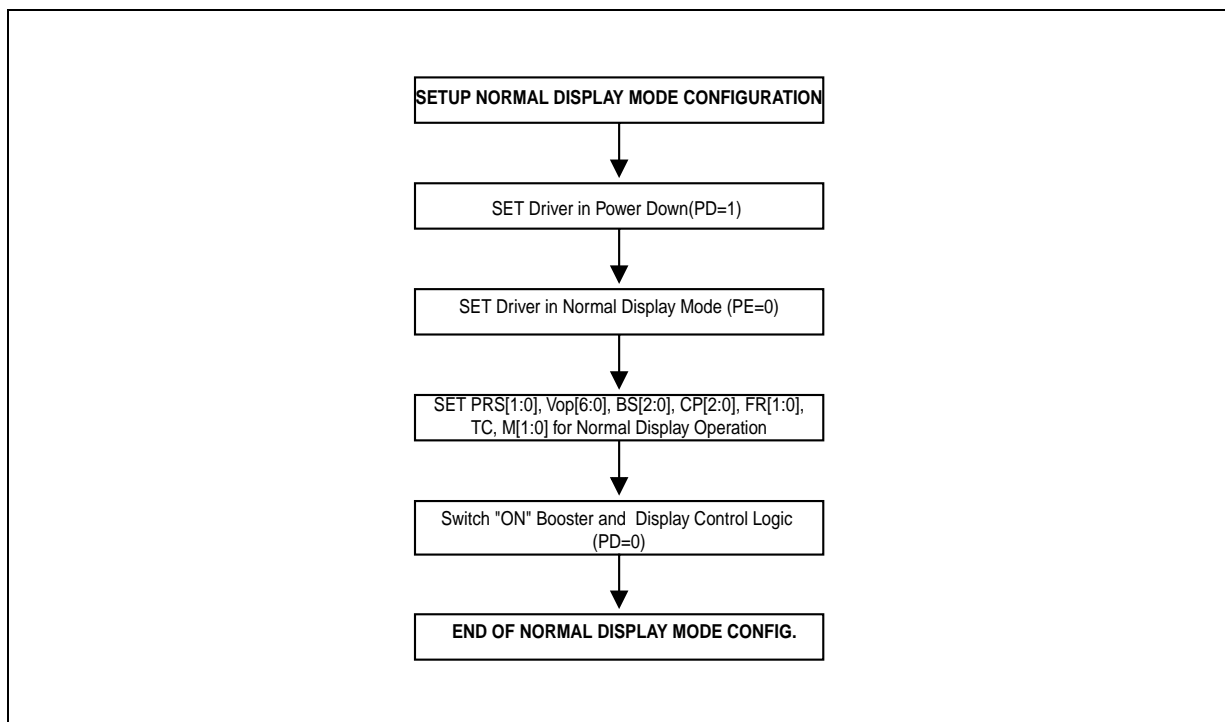


Figure 45. Dual Partial Display Enabling Instruction Flow

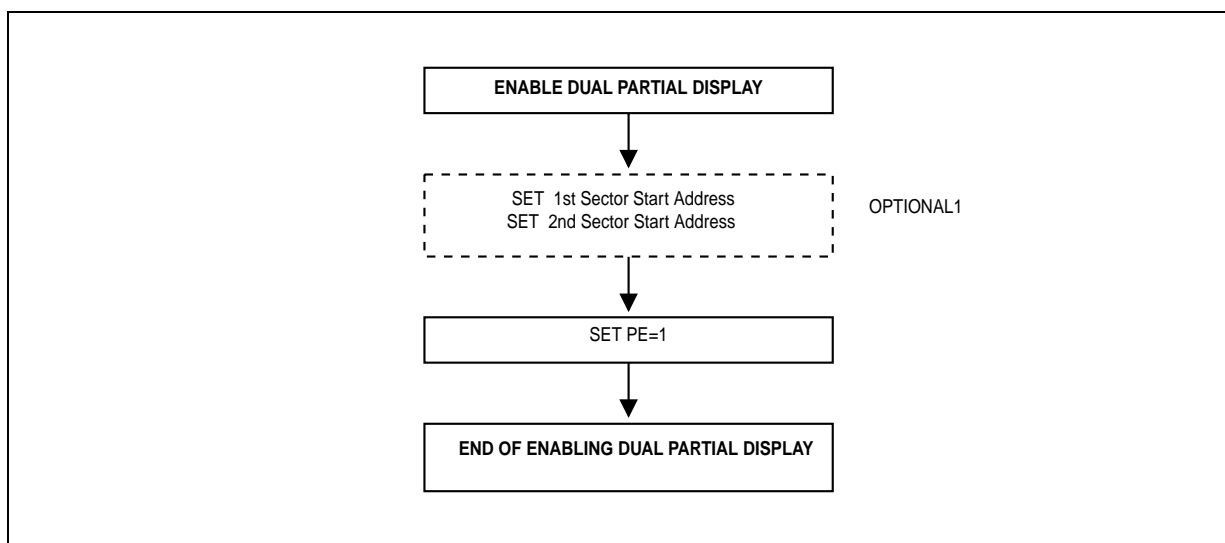


Figure 46. Dual Partial Display Mode configuration or Duty Change

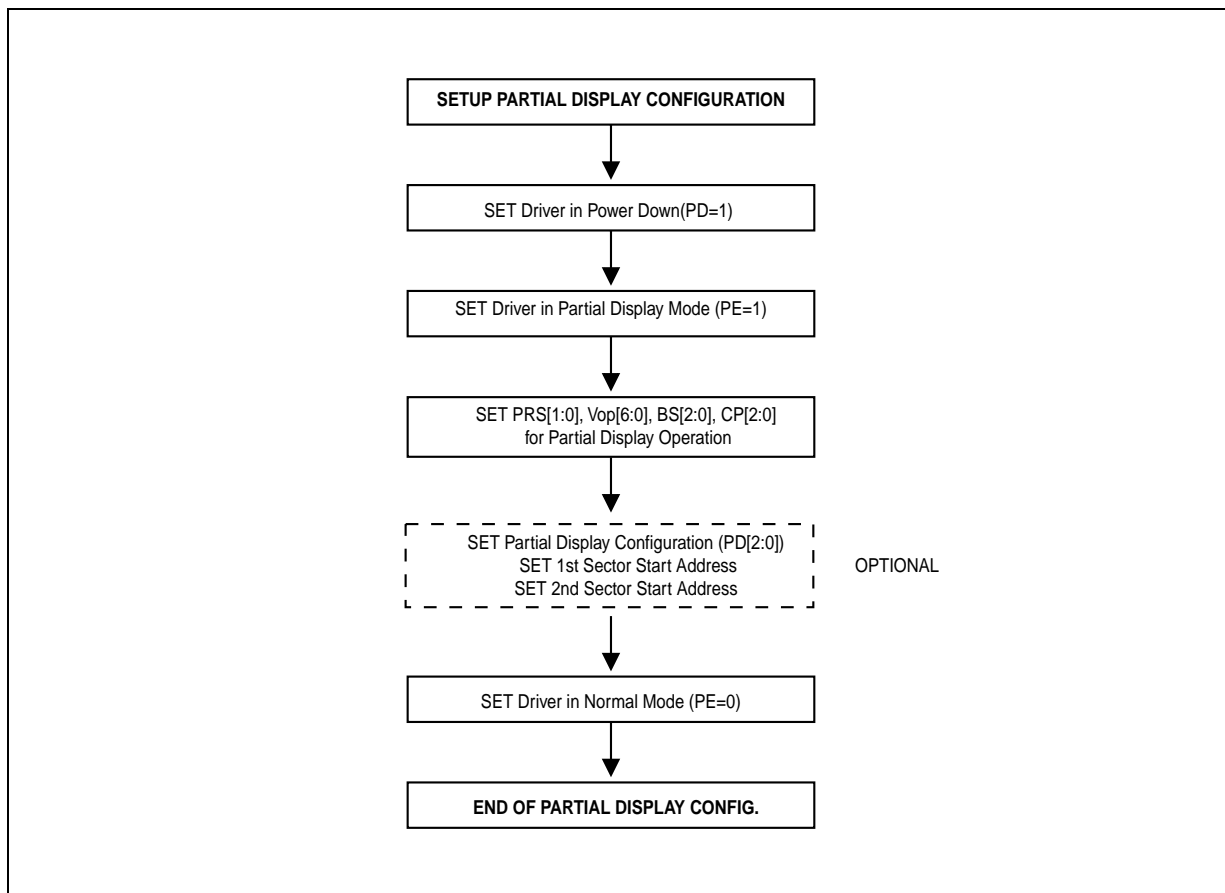


Figure 47. DATA RAM to display Mapping

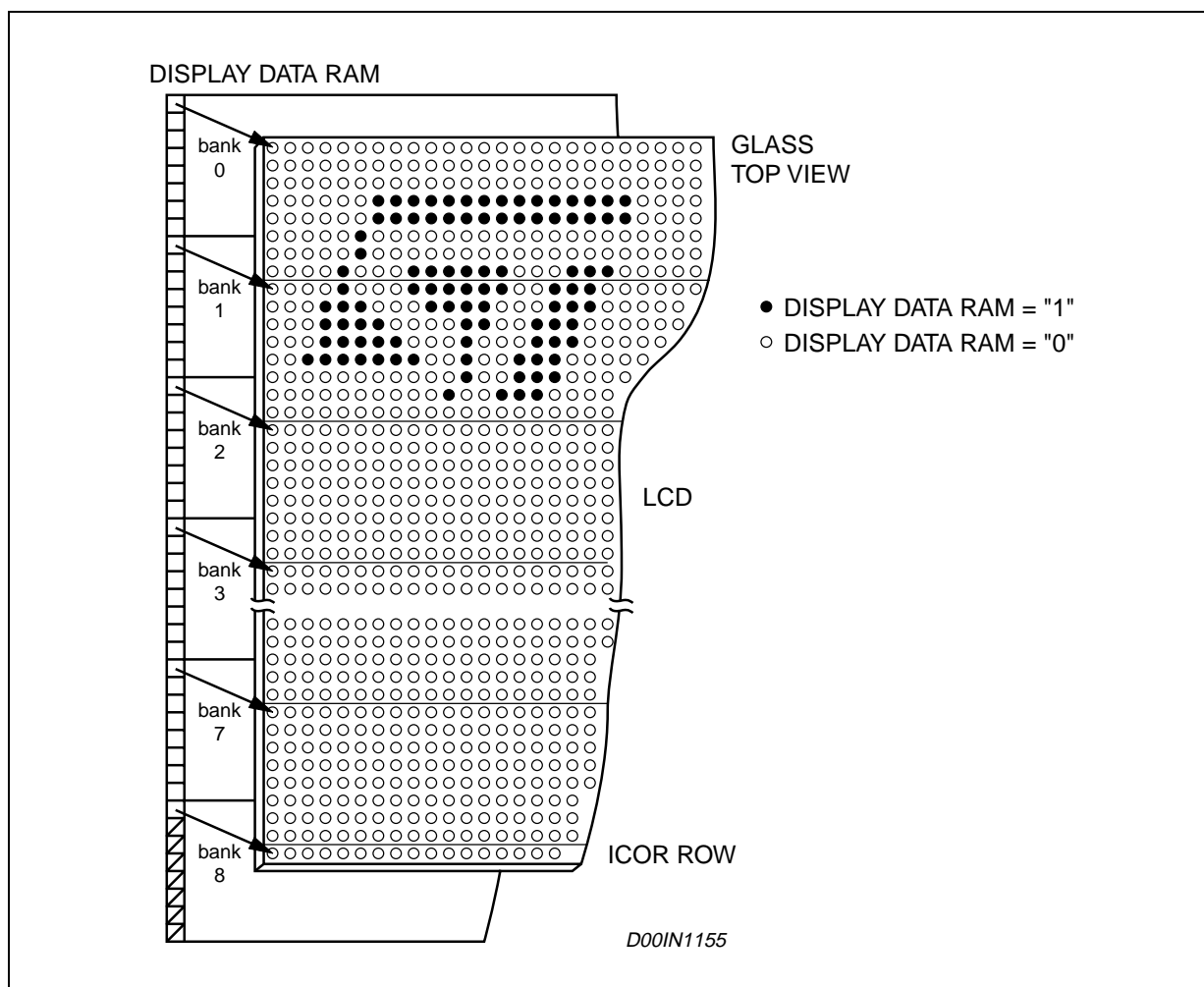


Table 15. Test Pin Configuration

| Test Numb. | Pin Configuration |
|---|-------------------|
| TEST_1 TEST_2 TEST_3 TEST_4 | OPEN |
| TEST_5 TEST_6 TEST_7 TEST_8 TEST_9 TEST_10 | GND |
| TEST_11 TEST_12 TEST_13 TEST_14 | GND |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---|--------------------------------|------|
| V _{DD1} | Supply Voltage Range | - 0.5 to + 5 | V |
| V _{DD2} | Supply Voltage Range | - 0.5 to + 7 | V |
| V _{LCD} | LCD Supply Voltage Range | - 0.5 to + 12 | V |
| I _{SS} | Supply Current | - 50 to +50 | mA |
| V _i | Input Voltage (all input pads) | -0.5 to V _{DD2} + 0.5 | V |
| I _{in} | DC Input Current | - 10 to + 10 | mA |
| I _{out} | DC Output Current | - 10 to + 10 | mA |
| P _{tot} | Total Power Dissipation (T _j = 85°C) | 300 | mW |
| P _o | Power Dissipation per Output | 30 | mW |
| T _j | Operating Junction Temperature | -40 to + 85 | °C |
| T _{stg} | Storage Temperature | - 65 to 150 | °C |

ELECTRICAL CHARACTERISTICS

DC OPERATION

(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 1.75 to 4.2V; V_{SS1,2} = 0V; V_{LCD} = 4.5 to 11 V; T_{amb} = -40 to 85°C; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------|-------------------------------------|--|---------------------|------|---------------------|------|
| Supply Voltages | | | | | | |
| V _{DD1} | Supply Voltage | note 9 | 1.7 | | 3.6 | V |
| V _{DD2} | Supply Voltage | LCD Voltage Internally generated | 1.75 | | 4.2 | V |
| V _{LCDIN} | LCD Supply Voltage | LCD Voltage Supplied externally | 4.5 | | 11 | V |
| V _{LCDOUT} | LCD Supply Voltage | Internally generated; note 1 | 4.5 | | 11 | V |
| I(V _{DD1}) | Supply Current | V _{DD1} = 2.8V; V _{LCD} = 7.6V; f _{sclk} = 0; T _{amb} = 25°C; note 3. | 15 | 20 | 30 | μA |
| | | V _{DD1} = 2.8V; V _{LCD} = 7.6V; f _{sclk} = 1Mhz; T _{amb} = 25°C; note 3, 8. OSC_IN=GND; parallel port | | 120 | 150 | μA |
| I(V _{DD2}) | Voltage Generator Supply Current | with V _{OP} = 0 and PRS = [0:0] with external V _{LCD} | | | 1 | μA |
| | | V _{DD2} = 2.8V; V _{LCD} = 7.6V; f _{sclk} = 0; T _{amb} = 25°C; no display load; 4x charge pump; note 2,3,6, | 10 | | 35 | μA |
| I(V _{DD1,2}) | Total Supply Current | V _{DD1} , V _{DD2} = 2.8V; V _{LCD} = 7.6V; 4x charge pump; f _{sclk} = 0; T _{amb} = 25°C; no display load; note 2,3,6 | 25 | | 65 | μA |
| | | Power down Mode with internal or External VLCD. Note 4 | | 3 | 5 | μA |
| I(V _{LDCIN}) | External LCD Supply Voltage Current | V _{DD} = 2.8V; V _{LCD} = 7.6V; no display load; f _{sclk} = 0; T _{amb} = 25°C; note 3. | 5 | 10 | 15 | μA |
| Logic Outputs | | | | | | |
| V _{OH} | High logic Level Output Voltage | I _{OH} = -500μA | 0.8V _{DD1} | | V _{DD1} | V |
| V _{OL} | Low logic Level Output Voltage | I _{OL} = 500μA | V _{SS} | | 0.2V _{DD1} | V |

ELECTRICAL CHARACTERISTICS (continued)**DC OPERATION**(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 1.75 to 4.2V; V_{SS1,2} = 0V; V_{LCD} = 4.5 to 11 V; T_{amb} = -40 to 85°C; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------------|--|---|---------------------|------------------------|---------------------------|------|
| Logic Inputs | | | | | | |
| V _{IL} | Logic LOW voltage level | | V _{SS} | | 0.3V _{DD1} | V |
| V _{IH} | Logic HIGH Voltage Level | | 0.7V _{DD1} | | V _{DD2} | V |
| I _{in} | Input Current | V _{in} = V _{SS1} or V _{DD1} | -1 | | 1 | μA |
| Logic Inputs/Outputs | | | | | | |
| V _{IL} | Logic LOW voltage level | | V _{SS} | | 0.3V _{DD1} | V |
| V _{IH} | Logic HIGH Voltage Level | | 0.7V _{DD1} | | V _{DD1} +0.5V | V |
| Column and Row Driver | | | | | | |
| R _{row} | ROW Output Resistance | V _{LCD} = 10V; | | 3K | 5K | kohm |
| R _{col} | Column Output resistance | V _{LCD} = 10V; | | 5K | 10K | kohm |
| V _{col} | Column Bias voltage accuracy | No load | -50 | | +50 | mV |
| V _{row} | Row Bias voltage accuracy | | -50 | | +50 | mV |
| LCD Supply Voltage | | | | | | |
| V _{LCD} | LCD Supply Voltage accuracy; Internally generated | V _{DD} = 2.8V; V _{LCD} = 10V; f _{sclk} =0; T _{amb} =25°C; no display load; note 2, 3, 6 & 7; VOP = 61h, PRS = 2hex | -1.5 | | 1.5 | % |
| TC0 | Temperature coefficient | | | -0.0·10 ⁻³ | | 1/°C |
| TC1 | | | | -0.35·10 ⁻³ | | 1/°C |
| TC2 | | | | -0.7·10 ⁻³ | | 1/°C |
| TC3 | | | | -1.05·10 ⁻³ | | 1/°C |
| TC4 | | | | -1.4·10 ⁻³ | | 1/°C |
| TC5 | | | | -1.75·10 ⁻³ | | 1/°C |
| TC6 | | | | -2.1·10 ⁻³ | | 1/°C |
| TC7 | | | | -2.3·10 ⁻³ | | 1/°C |

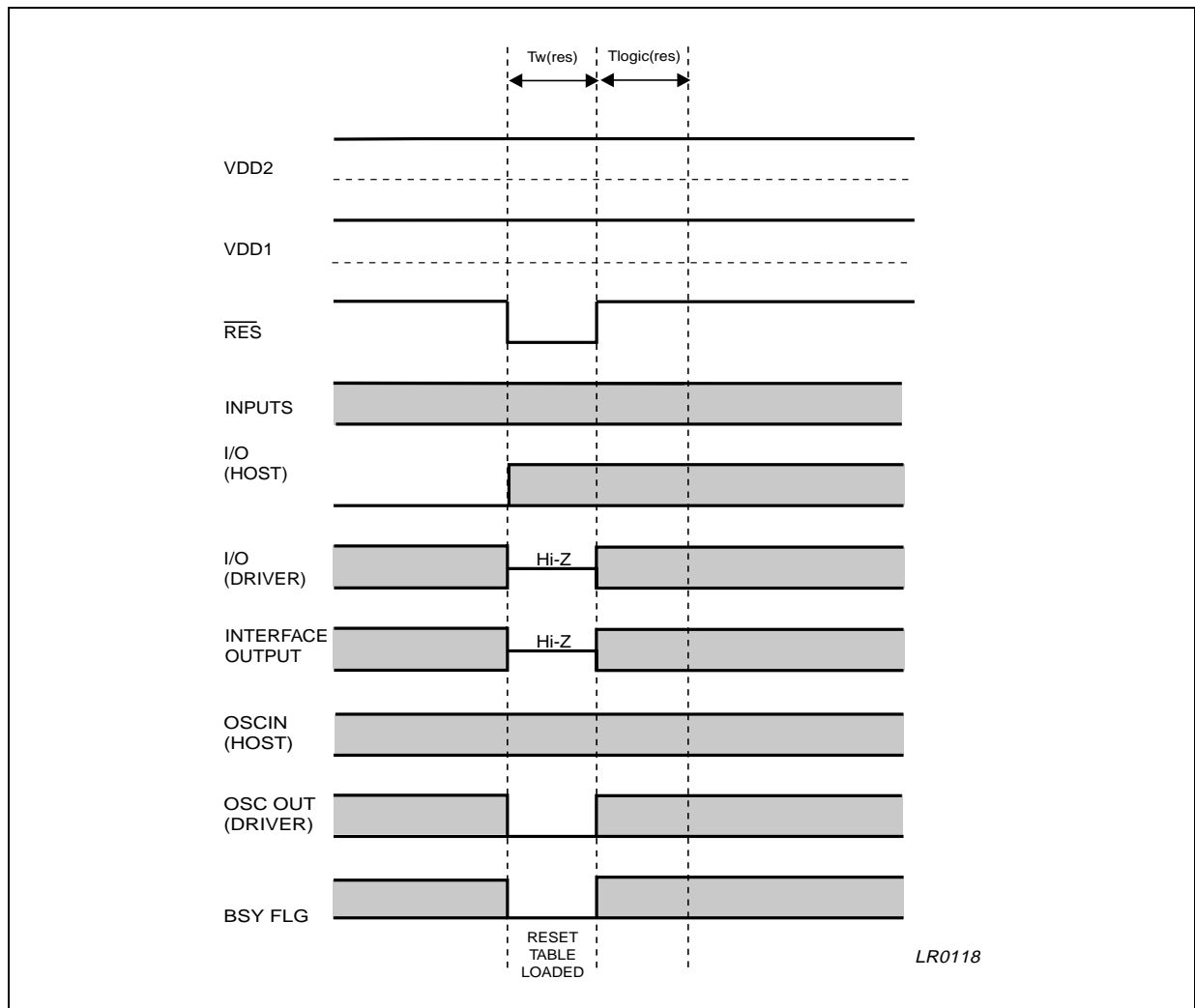
- Notes: 1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. When f_{sclk} = 0 there is no interface clock.
4. Power-down mode. During power-down all static currents are switched-off.
5. f external V_{LCD}, the display load current is not transmitted to I_{DD}
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27°C), maximum tolerance values are measured at the temperature range limit.
7. For TC0 to TC7
8. Data Byte Writing Mode
9. V_{DD1} ≤ V_{DD2}

ELECTRICAL CHARACTERISTICS
AC OPERATION

($V_{DD1} = 1.7$ to $3.6V$; $V_{DD2} = 1.75$ to $4.2V$; $V_{SS1,2} = 0V$; $V_{LCD} = 4.5$ to $11V$; $T_{amb} = -40$ to $85^{\circ}C$; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|----------------------------|---|---|------|------|------|------|
| INTERNAL OSCILLATOR | | | | | | |
| F _{OSC} | Internal Oscillator frequency | V _{DD} = 2.8V; T _{amb} = -20 to +70 °C | 64 | 72 | 80 | kHz |
| F _{EXT} | External Oscillator frequency | | 20 | | 100 | kHz |
| F _{FRAME} | Frame frequency | fosc or fext = 72 kHz; note 1 | | 75 | | Hz |
| T _{w(RES)} | RES LOW pulse width | | 5 | | | μs |
| | Reset Pulse Rejection | | | | 1 | μs |
| T _{LOGIC (RES)} | Internal Logic Reset Time | | | | 5 | μs |
| T _{VDD} | V _{DD1} vs. V _{DD2} Delay | | 0 | | | μs |

Figure 48. RESET timing diagram



ELECTRICAL CHARACTERISTICS (continued)

AC OPERATION

($V_{DD1} = 1.7$ to $3.6V$; $V_{DD2} = 1.75$ to $4.2V$; $V_{SS1,2} = 0V$; $V_{LCD} = 4.5$ to $11V$; $T_{amb} = -40$ to $85^{\circ}C$; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---------------------------|-------------------------------|-------------------------------------|------|------|------|------|
| PARALLEL INTERFACE | | | | | | |
| $T_{CY(EN)}$ | Enable Cycle Time | $V_{DD1} = 1.7V$; Write; note 2, 6 | 150 | | | ns |
| $T_{W(EN)}$ | Enable Pulse width | | 60 | | | ns |
| $T_{SU(A)}$ | Address Set-up Time | | 30 | | | ns |
| $T_{H(A)}$ | Address Hold Time | | 40 | | | ns |
| $T_{SU(D)}$ | Data Set-Up Time | | 30 | | | ns |
| $T_{H(D)}$ | Data Hold Time | | 30 | | | ns |
| $T_{SU(D)}$ | Data Set-Up Time in read Mode | | | | 100 | ns |
| $T_{HU(D)}$ | Data Hold Time In Read mode | | 100 | | | ns |

Figure 50. Parallel interface Write timing

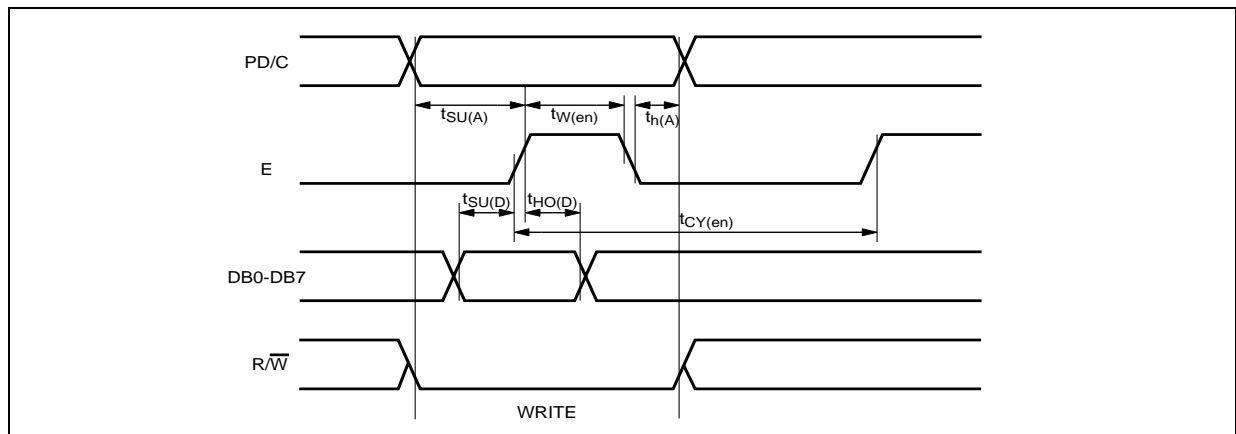
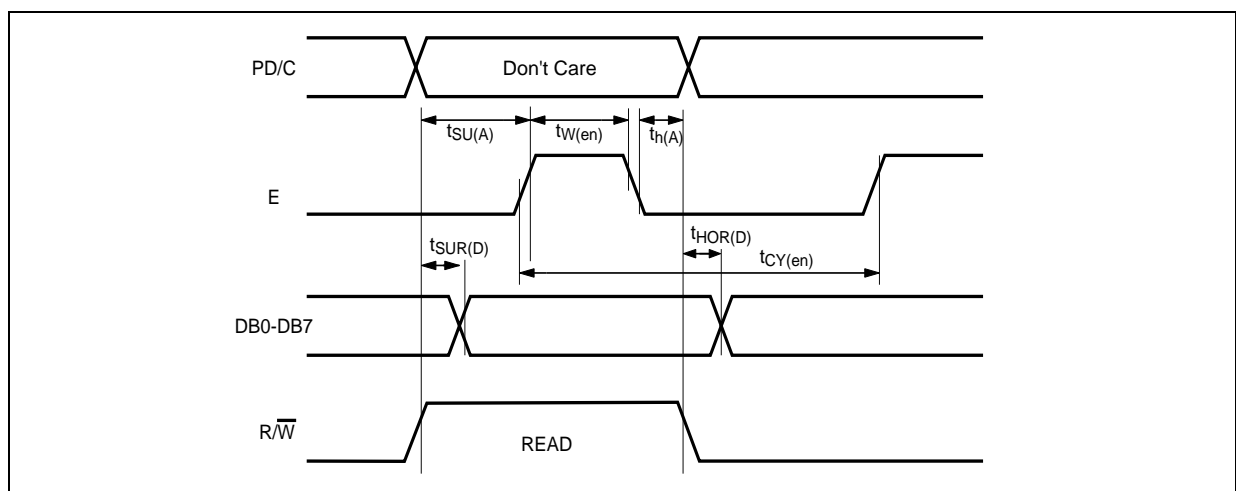


Figure 51. Parallel interface Read timing



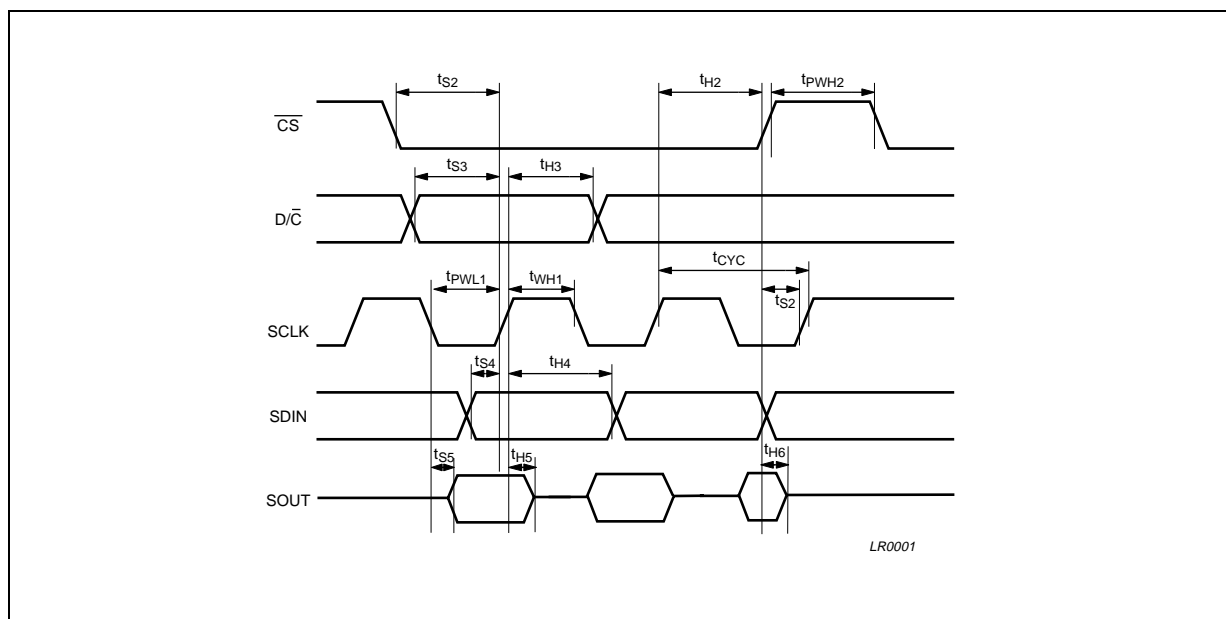
ELECTRICAL CHARACTERISTICS (continued)

AC OPERATION

(V_{DD1} = 1.7 to 3.6V; V_{DD2} = 1.75 to 4.2V; V_{SS1,2} = 0V; V_{LCD} = 4.5 to 11V; T_{amb} = -40 to 85°C; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | |
|-------------------------|----------------------------|---|------|------|------|------|----|
| SERIAL INTERFACE | | | | | | | |
| T _{CYC} | Clock Cycle SCLK | V _{DD1} = 1.7V; Write; note 2, 6 | 150 | | | ns | |
| T _{PWH1} | SCLK pulse width HIGH | | 60 | | | ns | |
| T _{PWL1} | SCLK Pulse width LOW | | 60 | | | ns | |
| T _{S2} | SCE setup time | | 30 | | | ns | |
| T _{H2} | SCE hold time | | 50 | | | ns | |
| T _{PWH2} | SCE minimum high time | | 50 | | | ns | |
| T _{S3} | SD/C setup time | | 30 | | | ns | |
| T _{H3} | SD/C hold time | | 40 | | | ns | |
| T _{S4} | SDIN setup time | | 30 | | | ns | |
| T _{H4} | SDIN hold time | | 40 | | | ns | |
| T _{S5} | SOUT Access Time | | | | | 100 | ns |
| T _{H5} | SOUT Disable Time vs. SCLK | | | | | 100 | ns |
| T _{H6} | SOUT Disable Time vs. SCE | | | | | 100 | ns |

Figure 52. Serial interface Timing



Notes: 1. $F_{frame} = \frac{f_{osc}}{960}$

- All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}
- C_b is the capacitive load for each bus line.
- For bus line loads C_b between 100 and 400pF the timing parameters must be linearly interpolated
- C_{VLCD} is the filtering Capacitor on VLCDOUT
- T_{rise} and T_{fall} (30%-70%) = 10 ns

Table 16. Pad Coordinates

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|---------|
| C0 | 1 | -3275.0 | -946.5 |
| C1 | 2 | -3225.0 | -946.11 |
| C2 | 3 | -3175.0 | -946.5 |
| C3 | 4 | -3125.0 | -946.5 |
| C4 | 5 | -3075.0 | -946.5 |
| C5 | 6 | -3025.0 | -946.5 |
| C6 | 7 | -2975.0 | -946.5 |
| C7 | 8 | -2925.0 | -946.5 |
| C8 | 9 | -2875.0 | -946.5 |
| C9 | 10 | -2825.0 | -946.5 |
| C10 | 11 | -2775.0 | -946.5 |
| C11 | 12 | -2725.0 | -946.5 |
| C12 | 13 | -2675.0 | -946.5 |
| C13 | 14 | -2625.0 | -946.5 |
| C14 | 15 | -2575.0 | -946.5 |
| C15 | 16 | -2525.0 | -946.5 |
| C16 | 17 | -2475.0 | -946.5 |
| C17 | 18 | -2425.0 | -946.5 |
| C18 | 19 | -2375.0 | -946.5 |
| C19 | 20 | -2325.0 | -946.5 |
| C20 | 21 | -2275.0 | -946.5 |
| C21 | 22 | -2225.0 | -946.5 |
| C22 | 23 | -2175.0 | -946.5 |
| C23 | 24 | -2125.0 | -946.5 |
| C24 | 25 | -2075.0 | -946.5 |
| C25 | 26 | -2025.0 | -946.5 |
| C26 | 27 | -1975.0 | -946.5 |
| C27 | 28 | -1925.0 | -946.5 |
| C28 | 29 | -1875.0 | -946.5 |
| C29 | 30 | -1825.0 | -946.5 |
| C30 | 31 | -1775.0 | -946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|--------|
| C31 | 32 | -1725.0 | -946.5 |
| C32 | 33 | -1675.0 | -946.5 |
| C33 | 34 | -1625.0 | -946.5 |
| C34 | 35 | -1575.0 | -946.5 |
| C35 | 36 | -1525.0 | -946.5 |
| C36 | 37 | -1475.0 | -946.5 |
| C37 | 38 | -1425.0 | -946.5 |
| C38 | 39 | -1375.0 | -946.5 |
| C39 | 40 | -1325.0 | -946.5 |
| C40 | 41 | -1275.0 | -946.5 |
| C41 | 42 | -1225.0 | -946.5 |
| C42 | 43 | -1175.0 | -946.5 |
| C43 | 44 | -1125.0 | -946.5 |
| C44 | 45 | -1075.0 | -946.5 |
| C45 | 46 | -1025.0 | -946.5 |
| C46 | 47 | -975.0 | -946.5 |
| C47 | 48 | -925.0 | -946.5 |
| C48 | 49 | -875.0 | -946.5 |
| C49 | 50 | -825.0 | -946.5 |
| C50 | 51 | -775.0 | -946.5 |
| C51 | 52 | -725.0 | -946.5 |
| C52 | 53 | -675.0 | -946.5 |
| C53 | 54 | -625.0 | -946.5 |
| C54 | 55 | -575.0 | -946.5 |
| C55 | 56 | -525.0 | -946.5 |
| C56 | 57 | -475.0 | -946.5 |
| C57 | 58 | -425.0 | -946.5 |
| C58 | 59 | -375.0 | -946.5 |
| C59 | 60 | -325.0 | -946.5 |
| C60 | 61 | -275.0 | -946.5 |
| C61 | 62 | -225.0 | -946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|--------|
| C62 | 63 | -175.0 | -946.5 |
| C63 | 64 | -125.0 | -946.5 |
| C64 | 65 | +125.0 | -946.5 |
| C65 | 66 | +175.0 | -946.5 |
| C66 | 67 | +225.0 | -946.5 |
| C67 | 68 | +275.0 | -946.5 |
| C68 | 69 | +325.0 | -946.5 |
| C69 | 70 | +375.0 | -946.5 |
| C70 | 71 | +425.0 | -946.5 |
| C71 | 72 | +475.0 | -946.5 |
| C72 | 73 | +525.0 | -946.5 |
| C73 | 74 | +575.0 | -946.5 |
| C74 | 75 | +625.0 | -946.5 |
| C75 | 76 | +675.0 | -946.5 |
| C76 | 77 | +725.0 | -946.5 |
| C77 | 78 | +775.0 | -946.5 |
| C78 | 79 | +825.0 | -946.5 |
| C79 | 80 | +875.0 | -946.5 |
| C80 | 81 | +925.0 | -946.5 |
| C81 | 82 | +975.0 | -946.5 |
| C82 | 83 | +1025.0 | -946.5 |
| C83 | 84 | +1075.0 | -946.5 |
| C84 | 85 | +1125.0 | -946.5 |
| C85 | 86 | +1175.0 | -946.5 |
| C86 | 87 | +1225.0 | -946.5 |
| C87 | 88 | +1275.0 | -946.5 |
| C88 | 89 | +1325.0 | -946.5 |
| C89 | 90 | +1375.0 | -946.5 |
| C90 | 91 | +1425.0 | -946.5 |
| C91 | 92 | +1475.0 | -946.5 |
| C92 | 93 | +1525.0 | -946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|--------|
| C93 | 94 | +1575.0 | -946.5 |
| C94 | 95 | +1625.0 | -946.5 |
| C95 | 96 | +1675.0 | -946.5 |
| C96 | 97 | +1725.0 | -946.5 |
| C97 | 98 | +1775.0 | -946.5 |
| C98 | 99 | +1825.0 | -946.5 |
| C99 | 100 | +1875.0 | -946.5 |
| C100 | 101 | +1925.0 | -946.5 |
| C101 | 102 | +1975.0 | -946.5 |
| C102 | 103 | +2025.0 | -946.5 |
| C103 | 104 | +2075.0 | -946.5 |
| C104 | 105 | +2125.0 | -946.5 |
| C105 | 106 | +2175.0 | -946.5 |
| C106 | 107 | +2225.0 | -946.5 |
| C107 | 108 | +2275.0 | -946.5 |
| C108 | 109 | +2325.0 | -946.5 |
| C109 | 110 | +2375.0 | -946.5 |
| C110 | 111 | +2425.0 | -946.5 |
| C111 | 112 | +2475.0 | -946.5 |
| C112 | 113 | +2525.0 | -946.5 |
| C113 | 114 | +2575.0 | -946.5 |
| C114 | 115 | +2625.0 | -946.5 |
| C115 | 116 | +2675.0 | -946.5 |
| C116 | 117 | +2725.0 | -946.5 |
| C117 | 118 | +2775.0 | -946.5 |
| C118 | 119 | +2825.0 | -946.5 |
| C119 | 120 | +2875.0 | -946.5 |
| C120 | 121 | +2925.0 | -946.5 |
| C121 | 122 | +2975.0 | -946.5 |
| C122 | 123 | +3025.0 | -946.5 |
| C123 | 124 | +3075.0 | -946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|--------|
| C124 | 125 | +3125.0 | -946.5 |
| C125 | 126 | +3175.0 | -946.5 |
| C126 | 127 | +3225.0 | -946.5 |
| C127 | 128 | +3275.0 | -946.5 |
| R40 | 129 | +3571.5 | -875.0 |
| R41 | 130 | +3571.5 | -825.0 |
| R42 | 131 | +3571.5 | -775.0 |
| R43 | 132 | +3571.5 | -725.0 |
| R44 | 133 | +3571.5 | -675.0 |
| R45 | 134 | +3571.5 | -625.0 |
| R46 | 135 | +3571.5 | -575.0 |
| R47 | 136 | +3571.5 | -525.0 |
| R48 | 137 | +3571.5 | -475.0 |
| R49 | 138 | +3571.5 | -425.0 |
| R50 | 139 | +3571.5 | -375.0 |
| R51 | 140 | +3571.5 | -325.0 |
| R52 | 141 | +3571.5 | -275.0 |
| R53 | 142 | +3571.5 | -225.0 |
| R54 | 143 | +3571.5 | -175.0 |
| R55 | 144 | +3571.5 | -125.0 |
| R56 | 145 | +3571.5 | -75.0 |
| R57 | 146 | +3571.5 | -25.0 |
| R58 | 147 | +3571.5 | +25.0 |
| R59 | 148 | +3571.5 | +75.0 |
| R60 | 149 | +3571.5 | +125.0 |
| R61 | 150 | +3571.5 | +175.0 |
| R62 | 151 | +3571.5 | +225.0 |
| R63 | 152 | +3571.5 | +275.0 |
| R64 | 153 | +3571.5 | +325.0 |
| R65 | 154 | +3571.5 | +375.0 |
| R66 | 155 | +3571.5 | +425.0 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|-----------|-----|---------|--------|
| R67 | 156 | +3571.5 | +475.0 |
| R68 | 157 | +3571.5 | +525.0 |
| R69 | 158 | +3571.5 | +575.0 |
| R70 | 159 | +3571.5 | +625.0 |
| R71 | 160 | +3571.5 | +675.0 |
| R72 | 161 | +3571.5 | +725.0 |
| R73 | 162 | +3571.5 | +775.0 |
| R74 | 163 | +3571.5 | +825.0 |
| R75 | 164 | +3571.5 | +875.0 |
| R76 | 165 | +3275.0 | +946.5 |
| R77 | 166 | +3225.0 | +946.5 |
| R78 | 167 | +3175.0 | +946.5 |
| R79 | 168 | +3125.0 | +946.5 |
| R80/ICON | 169 | +3075.0 | +946.5 |
| TEST_1 | 170 | +2825.0 | +946.5 |
| TEST_2 | 171 | +2775.0 | +946.5 |
| TEST_3 | 172 | +2725.0 | +946.5 |
| TEST_4 | 173 | +2675.0 | +946.5 |
| TEST_5 | 174 | +2625.0 | +946.5 |
| TEST_6 | 175 | +2575.0 | +946.5 |
| TEST_7 | 176 | +2525.0 | +946.5 |
| TEST_8 | 177 | +2475.0 | +946.5 |
| TEST_9 | 178 | +2425.0 | +946.5 |
| TEST_10 | 179 | +2375.0 | +946.5 |
| VSSAUX | 180 | +2225.0 | +946.5 |
| SA1 | 181 | +2175.0 | +946.5 |
| SA0 | 182 | +2125.0 | +946.5 |
| EXT | 183 | +2075.0 | +946.5 |
| SEL2 | 184 | +2025.0 | +946.5 |
| SEL1 | 185 | +1975.0 | +946.5 |
| ICON_MODE | 186 | +1925.0 | +946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y (μm) |
|------------------|-----|---------|--------|
| OSC_IN | 187 | +1875.0 | +946.5 |
| VDD1_1 | 188 | +1825.0 | +946.5 |
| VDD1_2 | 189 | +1825.0 | +839.5 |
| VDD1_3 | 190 | +1775.0 | +946.5 |
| VDD1_4 | 191 | +1775.0 | +839.5 |
| VDD1_5 | 192 | +1725.0 | +946.5 |
| VDD1_6 | 193 | +1725.0 | +839.5 |
| VDD1_7 | 194 | +1675.0 | +946.5 |
| VDD1_8 | 195 | +1675.0 | +839.5 |
| VDD1_9 | 196 | +1625.0 | +946.5 |
| VDD1_10 | 197 | +1625.0 | +839.5 |
| VDD1_11 | 198 | +1575.0 | +946.5 |
| VDD1_12 | 199 | +1575.0 | +839.5 |
| VDD2_1 | 200 | +1525.0 | +946.5 |
| VDD2_2 | 201 | +1525.0 | +839.5 |
| VDD2_3 | 202 | +1475.0 | +946.5 |
| VDD2_4 | 203 | +1475.0 | +839.5 |
| VDD2_5 | 204 | +1425.0 | +946.5 |
| VDD2_6 | 205 | +1425.0 | +839.5 |
| VDD2_7 | 206 | +1375.0 | +946.5 |
| VDD2_8 | 207 | +1375.0 | +839.5 |
| VDD2_9 | 208 | +1325.0 | +946.5 |
| VDD2_10 | 209 | +1325.0 | +839.5 |
| VDD2_11 | 210 | +1275.0 | +946.5 |
| VDD2_12 | 211 | +1275.0 | +839.5 |
| BUSY_FLAG | 212 | +1125.0 | +946.5 |
| SDOUT | 213 | +975.0 | +946.5 |
| SDIN | 214 | +925.0 | +946.5 |
| SD/C | 215 | +875.0 | +946.5 |
| SCE | 216 | +825.0 | +946.5 |
| SCLK | 217 | +775.0 | +946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y (μm) |
|---------|-----|---------|--------|
| VSSAUX | 218 | +625.0 | +946.5 |
| R/W | 219 | +575.0 | +946.5 |
| D7 | 220 | +525.0 | +946.5 |
| D6 | 221 | +475.0 | +946.5 |
| D5 | 222 | +425.0 | +946.5 |
| D4 | 223 | +375.0 | +946.5 |
| D3 | 224 | +325.0 | +946.5 |
| D2 | 225 | +275.0 | +946.5 |
| D1 | 226 | +225.0 | +946.5 |
| D0 | 227 | +175.0 | +946.5 |
| PD/C | 228 | +125.0 | +946.5 |
| E | 229 | +75.0 | +946.5 |
| RES | 230 | -75.0 | +946.5 |
| VSSAUX | 231 | -225.0 | +946.5 |
| SDA_OUT | 232 | -275.0 | +946.5 |
| SDA_OUT | 233 | -325.0 | +946.5 |
| SDA_IN | 234 | -375.0 | +946.5 |
| SCL | 235 | -425.0 | +946.5 |
| VSS_1 | 236 | -975.0 | +946.5 |
| VSS_2 | 237 | -975.0 | +839.5 |
| VSS_3 | 238 | -1025.0 | +946.5 |
| VSS_4 | 239 | -1025.0 | +839.5 |
| VSS_5 | 240 | -1075.0 | +946.5 |
| VSS_6 | 241 | -1075.0 | +839.5 |
| VSS_7 | 242 | -1125.0 | +946.5 |
| VSS_8 | 243 | -1125.0 | +839.5 |
| VSS_9 | 244 | -1175.0 | +946.5 |
| VSS_10 | 245 | -1175.0 | +839.5 |
| VSS_11 | 246 | -1225.0 | +946.5 |
| VSS_12 | 247 | -1225.0 | +839.5 |
| VSS_13 | 248 | -1275.0 | +946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|-------------|-----|---------|--------|
| VSS_14 | 249 | -1275.0 | +839.5 |
| VSS_15 | 250 | -1325.0 | +946.5 |
| VSS_16 | 251 | -1325.0 | +839.5 |
| VSS_17 | 252 | -1375.0 | +946.5 |
| VSS_18 | 253 | -1375.0 | +839.5 |
| VSS_19 | 254 | -1425.0 | +946.5 |
| VSS_20 | 255 | -1425.0 | +839.5 |
| TEST_11 | 256 | -1475.0 | +946.5 |
| TEST_12 | 257 | -1525.0 | +946.5 |
| TEST_13 | 258 | -1575.0 | +946.5 |
| TEST_14 | 259 | -1625.0 | +946.5 |
| OSC_OUT | 260 | -2175.0 | +946.5 |
| VLCDIN_1 | 261 | -2325.0 | +946.5 |
| VLCDIN_2 | 262 | -2325.0 | +839.5 |
| VLCDIN_3 | 263 | -2375.0 | +946.5 |
| VLCDIN_4 | 264 | -2375.0 | +839.5 |
| VLCDIN_5 | 265 | -2425.0 | +946.5 |
| VLCDIN_6 | 266 | -2425.0 | +839.5 |
| VLCDIN_7 | 267 | -2475.0 | +946.5 |
| VLCDIN_8 | 268 | -2475.0 | +839.5 |
| VLCDIN_9 | 269 | -2525.0 | +946.5 |
| VLCDIN_10 | 270 | -2525.0 | +839.5 |
| VLCDSENSE_1 | 271 | -2575.0 | +946.5 |
| VLCDSENSE_2 | 272 | -2575.0 | +839.5 |
| VLCDOUT_1 | 273 | -2625.0 | +946.5 |
| VLCDOUT_2 | 274 | -2625.0 | +839.5 |
| VLCDOUT_3 | 275 | -2675.0 | +946.5 |
| VLCDOUT_4 | 276 | -2675.0 | +839.5 |
| VLCDOUT_5 | 277 | -2725.0 | +946.5 |
| VLCDOUT_6 | 278 | -2725.0 | +839.5 |
| VLCDOUT_7 | 279 | -2775.0 | +946.5 |

Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------------|-----|---------|--------|
| VLCDOUT_8 | 280 | -2775.0 | +839.5 |
| VLCDOUT_9 | 281 | -2825.0 | +946.5 |
| VLCDOUT_10 | 282 | -2825.0 | +839.5 |
| R39 | 283 | -3075.0 | +946.5 |
| R38 | 284 | -3125.0 | +946.5 |
| R37 | 285 | -3175.0 | +946.5 |
| R36 | 286 | -3225.0 | +946.5 |
| R35 | 287 | -3275.0 | +946.5 |
| R34 | 288 | -3571.5 | +875.0 |
| R33 | 289 | -3571.5 | +825.0 |
| R32 | 290 | -3571.5 | +775.0 |
| R31 | 291 | -3571.5 | +725.0 |
| R30 | 292 | -3571.5 | +675.0 |
| R29 | 293 | -3571.5 | +625.0 |
| R28 | 294 | -3571.5 | +575.0 |
| R27 | 295 | -3571.5 | +525.0 |
| R26 | 296 | -3571.5 | +475.0 |
| R25 | 297 | -3571.5 | +425.0 |
| R24 | 298 | -3571.5 | +375.0 |
| R23 | 299 | -3571.5 | +325.0 |
| R22 | 300 | -3571.5 | +275.0 |
| R21 | 301 | -3571.5 | +225.0 |
| R20 | 302 | -3571.5 | +175.0 |
| R19 | 303 | -3571.5 | +125.0 |
| R18 | 304 | -3571.5 | +75.0 |
| R17 | 305 | -3571.5 | +25.0 |
| R16 | 306 | -3571.5 | -25.0 |
| R15 | 307 | -3571.5 | -75.0 |
| R14 | 308 | -3571.5 | -125.0 |
| R13 | 309 | -3571.5 | -175.0 |
| R12 | 310 | -3571.5 | -225.0 |



Table 16. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------|--------|
| R11 | 311 | -3571.5 | -275.0 |
| R10 | 312 | -3571.5 | -325.0 |
| R9 | 313 | -3571.5 | -375.0 |
| R8 | 314 | -3571.5 | -425.0 |
| R7 | 315 | -3571.5 | -475.0 |
| R6 | 316 | -3571.5 | -525.0 |
| R5 | 317 | -3571.5 | -575.0 |
| R4 | 318 | -3571.5 | -625.0 |
| R3 | 319 | -3571.5 | -675.0 |
| R2 | 320 | -3571.5 | -725.0 |
| R1 | 321 | -3571.5 | -775.0 |
| R0 | 322 | -3571.5 | -825.0 |
| ICON | 323 | -3571.5 | -875.0 |

Figure 53. Alignment marks coordinates

| X | Y | MARKS |
|---------|--------|-------|
| -3574.5 | -949.5 | mark1 |
| +3574.5 | -949.5 | mark2 |
| -2250 | +949.5 | mark3 |
| +1200 | +949.5 | mark4 |

Figure 54. Alignment marks dimensions

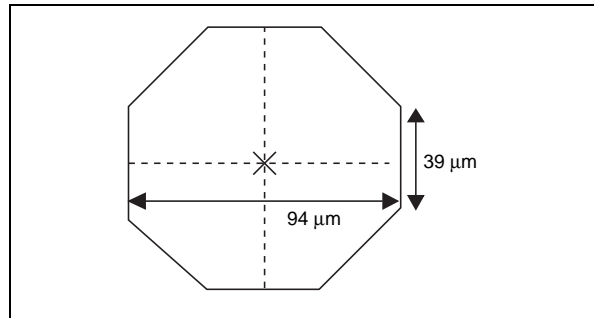


Table 17. Bumps

| | Bump Number | Dimensions |
|---------------------------------|--|---------------------|
| Bumps on Single Row Size | 1-187 212-235 256-260 283-323 | 30μm X 98 μm X 17.5 |
| Bumps on Two Rows Size | 188-211 236-255 261-282 | 30μm X 87 μm X 17.5 |
| Pad Size | 1-323 | 43μm X 107μm |
| Pad Pitch | 1-323 | 50μm |
| Spacing between Bumps | 1-323 | 20μm |

Table 18. Die Mechanical Dimensions

| | |
|-------------------------|-----------------|
| Die Size | 2.07mm x 7.32mm |
| Wafers Thickness | 500μm |

Figure 55. DIE ORIENTATION IN TRAY

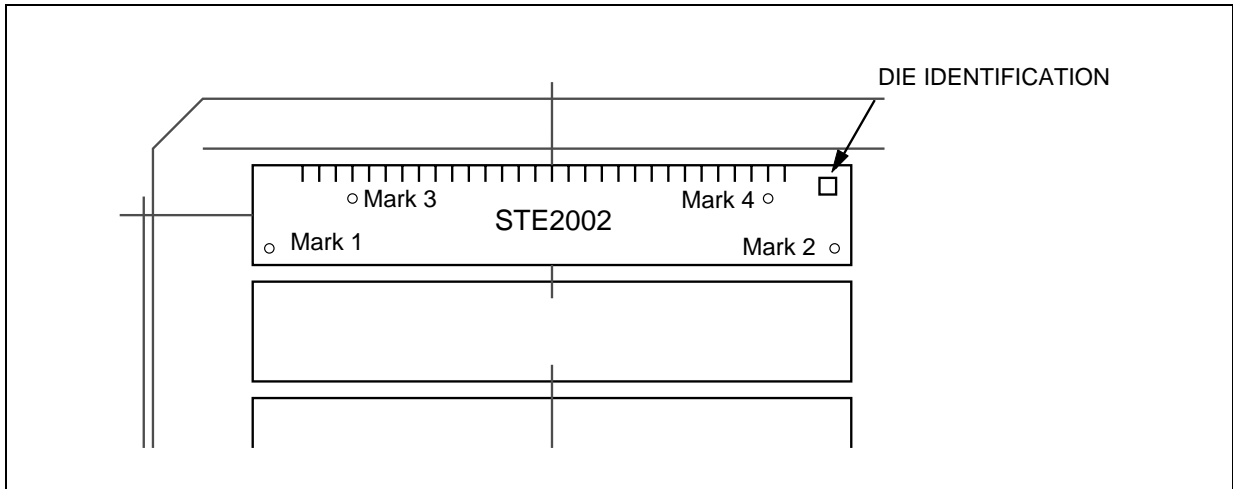
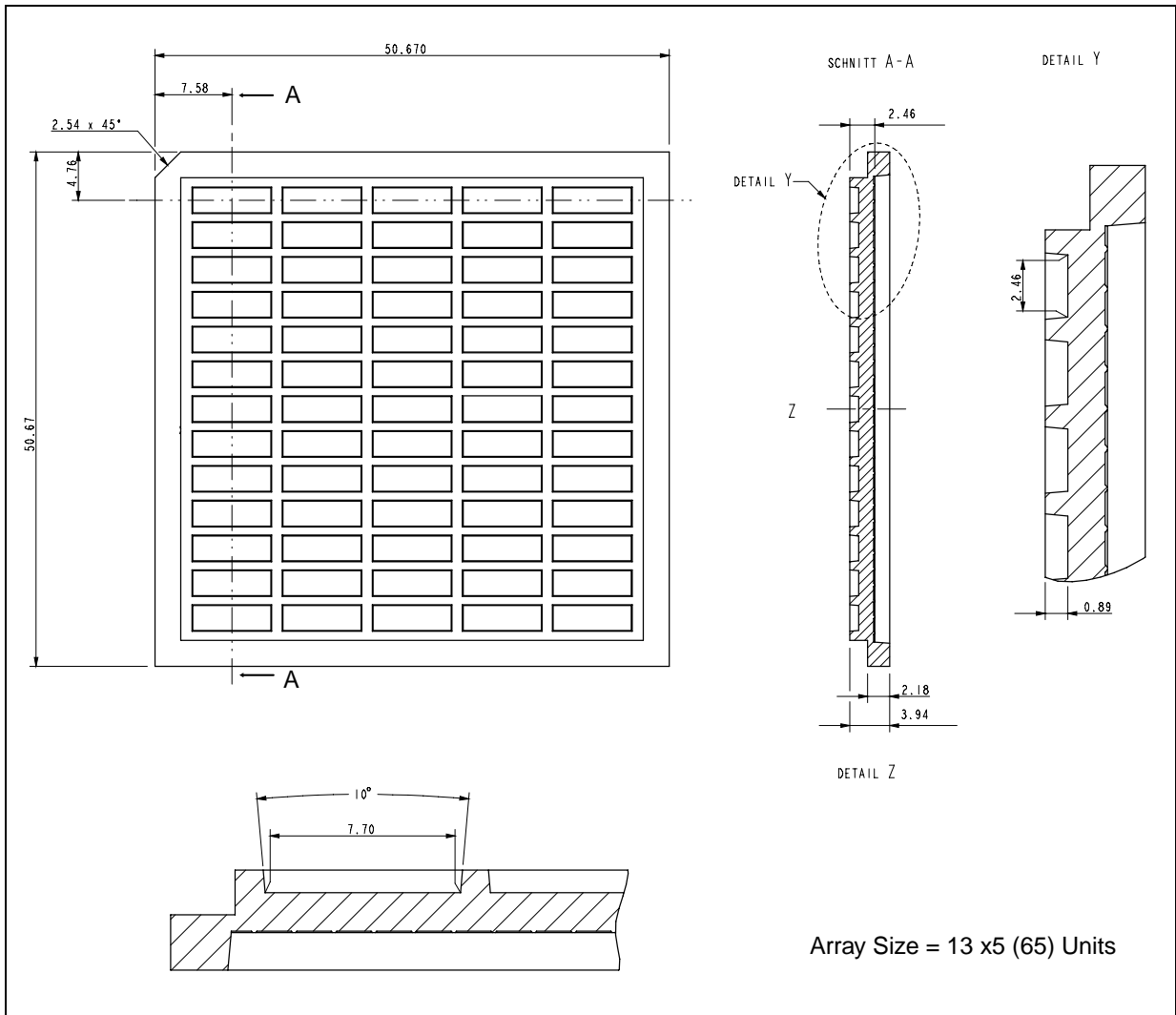


Figure 56. TRAY INFORMATION



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