



虹冠電子工業股份有限公司  
Champion Microelectronic Corporation

*Specialized in Integrated High Efficient Switching Power Management Solutions*  
高整合高效率交換型電源管理方案之專業 I C 設計



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## GENERAL DESCRIPTION

The CM6900 is a controller for power factor corrected, switched mode power suppliers. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with IEC-1000-3-2 specifications. Intended as a BiCMOS version of the industry-standard ML4824, CM6900 includes circuits for the implementation of leading edge, average current, "boost" type power factor correction and a trailing edge, pulse width modulator (PWM). The CM6900 has additional features besides all the features of CM6800. Additional features are Inrush Current Control, Separated PFC OVP pin, Separated Power VCCA pin and Analog VCCA pin, and Separated Power Ground pin and Analog Ground pin. Gate-driver with 1A capabilities minimizes the need for external driver circuits. Low power requirements improve efficiency and reduce component costs.

An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current or voltage mode, at up to 250kHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

## FEATURES

- ◆ Patent Filed #5,565,761, #5,747,977, #5,742,151, #5,804,950, #5,798,635
- ◆ Inrush Current Control
- ◆ Separated PFC OVP pin
- ◆ Separated Power VCCA and Analog VCCA
- ◆ Separated Power Ground and Analog Ground
- ◆ Additional folded-back current limit for PWM section.
- ◆ 23V Bi-CMOS process
- ◆ VIN OK guaranteed turn on PWM at 2.5V instead of 1.5V
- ◆ Internally synchronized leading edge PFC and trailing edge PWM in one IC
- ◆ Slew rate enhanced transconductance error amplifier for ultra-fast PFC response
- ◆ Low start-up current (100µA typ.)
- ◆ Low operating current (3.0mA type.)
- ◆ Low total harmonic distortion, high PF
- ◆ Reduces ripple current in the storage capacitor between the PFC and PWM sections
- ◆ Average current, continuous or discontinuous boost leading edge PFC
- ◆ VCCA OVP Comparator
- ◆ Low Power Detect Comparator
- ◆ PWM configurable for current mode or voltage mode operation
- ◆ Current fed gain modulator for improved noise immunity
- ◆ Brown-out control, over-voltage protection, UVLO, and soft start, and Reference OK

### **24 Hours Technical Support---WebSIM**

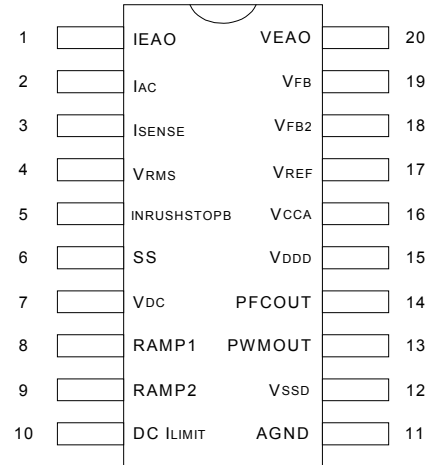
Champion provides customers an online circuit simulation tool called WebSIM. You could simply logon our website at [www.champion-micro.com](http://www.champion-micro.com) for details.

## APPLICATIONS

- ◆ Desktop PC Power Supply
- ◆ Internet Server Power Supply
- ◆ IPC Power Supply
- ◆ UPS
- ◆ Battery Charger
- ◆ DC Motor Power Supply
- ◆ Monitor Power Supply
- ◆ Telecom System Power Supply
- ◆ Distributed Power

## PIN CONFIGURATION

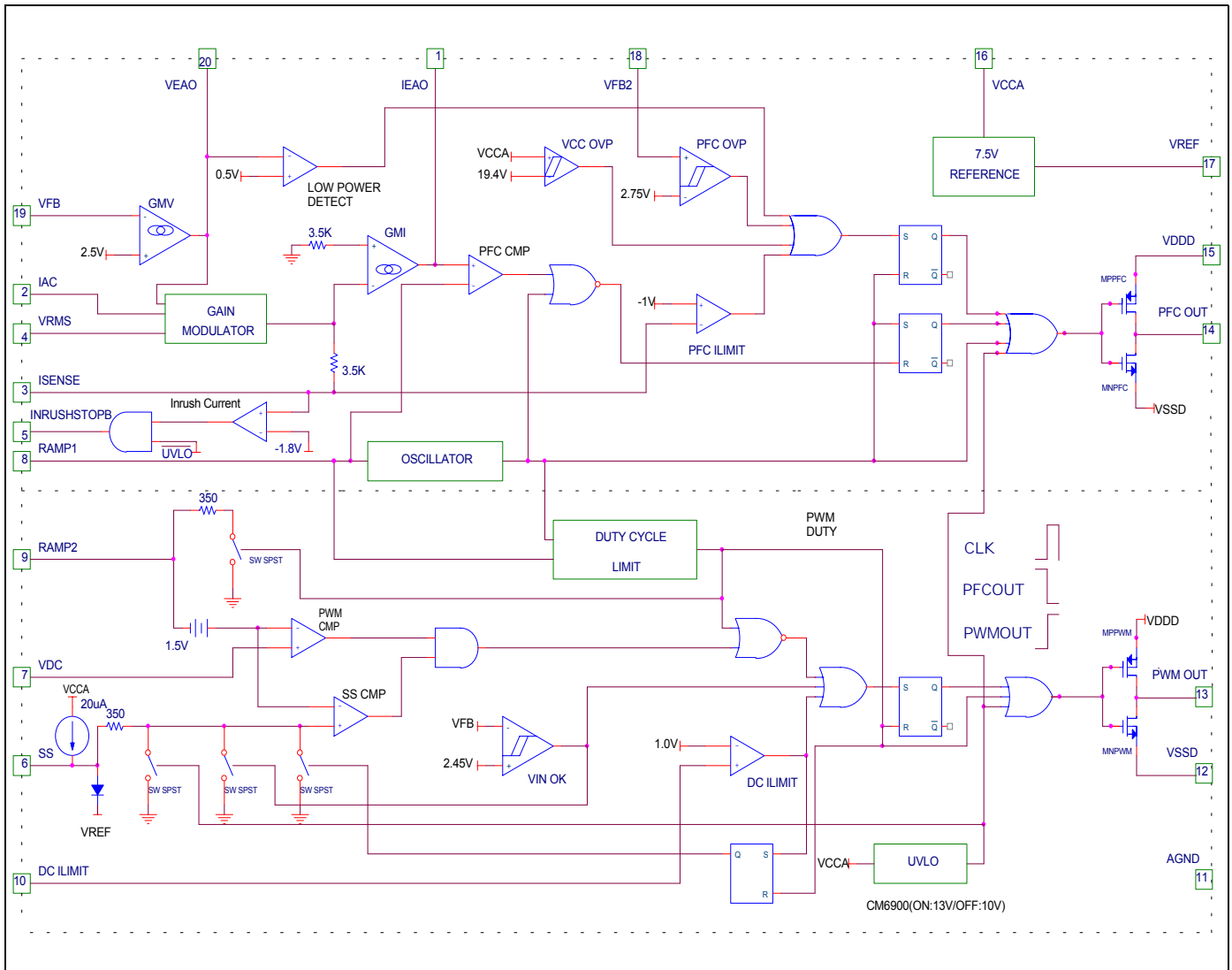
SOP-20 (S20) / PDIP-20 (P20)  
Top View



## PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	IEAO	PFC transconductance current error amplifier output	0		4.25	V
2	I <sub>AC</sub>	PFC gain control reference input	0		1	mA
3	I <sub>SENSE</sub>	Current sense input to the PFC current limit comparator	-5		0.7	V
4	V <sub>RMS</sub>	Input for PFC RMS line voltage compensation	0		6	V
5	INRUSHSTO PB	Inrush Current Control pin, It is low when Inrush current is high or during the start-up condition and it is VCCA when Inrush condition has been removed.	0		VCCA	V
6	SS	Connection point for the PWM soft start capacitor	0		VREF+0.7	V
7	V <sub>DC</sub>	PWM voltage feedback input	0		VREF+0.7	V
8	RAMP 1 (RTCT)	Oscillator timing node; timing set by RT CT	1.2		3.9	V
9	RAMP 2 (PWM RAMP)	When in current mode, this pin functions as the current sense input; when in voltage mode, it is the PWM input from PFC output (feed forward ramp).	0		VREF+0.7	V
10	DC I <sub>LIMIT</sub>	PWM current limit comparator input	0		1	V
11	AGND	Analog Ground				
12	V <sub>SSD</sub>	Digital Ground				
13	PWM OUT	PWM driver output	0		VDDD	V
14	PFC OUT	PFC driver output	0		VDDD	V

15	V <sub>DDD</sub>	Digital Power	VCCA- 0.3	VCCA	VCCA+0. 3	
16	V <sub>CCA</sub>	Analog Power	10	15	20	V
17	V <sub>REF</sub>	Buffered output for the internal 7.5V reference		7.5		V
18	V <sub>FB2</sub>	PFC transconductance voltage error amplifier input	0	2.5	3	V
19	V <sub>FB</sub>	PFC transconductance voltage error amplifier input	0	2.5	3	V
20	VEAO	PFC transconductance voltage error amplifier output	0		6	V

**SIMPLIFIED BLOCK DIAGRAM**


**ORDERING INFORMATION**

Part Number	Temperature Range	Package
CM6900IP	-40°C to 125°C	20-Pin PDIP (P20)
CM6900IS	-40°C to 125°C	20-Pin Wide SOP (S20)

**ABSOLUTE MAXIMUM RATINGS**

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V <sub>CCA</sub> and P <sub>VDD</sub>		23	V
IEAO	0	4.5	V
I <sub>SENSE</sub> Voltage	-5	0.7	V
PFC OUT	GND – 0.3	V <sub>CCA</sub> + 0.3	V
PWMOUT	GND – 0.3	V <sub>CCA</sub> + 0.3	V
INRUSHSTOPB	GND – 0.3	V <sub>CCA</sub> + 0.3	V
Voltage on Any Other Pin	GND – 0.3	V <sub>REF</sub> + 0.3	V
I <sub>REF</sub>		10	mA
I <sub>AC</sub> Input Current		1	mA
Peak PFC OUT Current, Source or Sink		1	A
Peak PWM OUT Current, Source or Sink		1	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Operating Temperature Range	-40	125	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ <sub>JA</sub> )			
Plastic DIP		80	°C/W
Plastic SOIC		105	°C/W

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply V<sub>CCA</sub>=+15V, R<sub>T</sub> = 52.3kΩ, C<sub>T</sub> = 470pF, T<sub>A</sub>=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6900			Unit
			Min.	Typ.	Max.	
<b>Voltage Error Amplifier (g<sub>mv</sub>)</b>						
	Input Voltage Range		0		5	V
	Transconductance	V <sub>NONINV</sub> = V <sub>INV</sub> , VEAO = 3.75V	30	65	90	μmho
	Feedback Reference Voltage		2.45	2.5	2.55	V
	Input Bias Current	Note 2	-1.0	-0.5		μA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V <sub>FB</sub> = 3V, VEAO = 6V		-35	-20	μA
	Source Current	V <sub>FB</sub> = 1.5V, VEAO = 1.5V	30	40		μA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	11V < V <sub>CCA</sub> < 16.5V	50	60		dB

**ELECTRICAL CHARACTERISTICS** (Conti.) Unless otherwise stated, these specifications apply  
 $V_{CCA}=+15V$ ,  $R_T = 52.3k\Omega$ ,  $C_T = 470pF$ ,  $T_A=$ Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6900			Unit
			Min.	Typ.	Max.	
<b>Current Error Amplifier (<math>g_{mi}</math>)</b>						
	Input Voltage Range		-1.5		0.7	V
	Transconductance	$V_{NONINV} = V_{INV}$ , $VEAO = 3.75V$	50	100	150	$\mu mho$
	Input Offset Voltage		-12		12	mV
	Input Bias Current		-1.0	-0.5		$\mu A$
	Output High Voltage		4.0	4.25		V
	Output Low Voltage			0.65	1.0	V
	Sink Current	$I_{SENSE} = +0.5V$ , $IEAO = 4.0V$		-65	-35	$\mu A$
	Source Current	$I_{SENSE} = -0.5V$ , $IEAO = 1.5V$	35	75		$\mu A$
	Open Loop Gain		60	70		dB
	Power Supply Rejection Ratio	$11V < V_{CCA} < 16.5V$	60	75		dB
<b>PFC OVP Comparator</b>						
	Threshold Voltage		2.70	2.77	2.85	V
	Hysteresis		230		290	mV
<b>Low Power Detect Comparator</b>						
	Threshold Voltage		0.4	0.5	0.6	V
<b>VCCA OVP Comparator</b>						
	Threshold Voltage		19	19.4	20	V
	Hysteresis		1.40	1.5	1.65	V
<b>PFC <math>I_{LIMIT}</math> Comparator</b>						
	Threshold Voltage		-1.10	-1.00	-0.90	V
	(PFC $I_{LIMIT} V_{TH}$ – Gain Modulator Output)		80	200		mV
	Delay to Output (Note 4)	Overdrive Voltage = -100mV		250		ns
<b>DC <math>I_{LIMIT}</math> Comparator</b>						
	Threshold Voltage		0.95	1.0	1.05	V
	Delay to Output (Note 4)	Overdrive Voltage = 100mV		250		ns
<b><math>V_{IN}</math> OK Comparator</b>						
	Threshold Voltage		2.35	2.45	2.55	V
	Hysteresis		0.8	1.0	1.2	V
<b>GAIN Modulator</b>						
	Gain (Note 3)	$I_{AC} = 100\mu A$ , $V_{RMS} = V_{FB} = 1V$	0.59		0.81	
		$I_{AC} = 100\mu A$ , $V_{RMS} = 1.1V$ , $V_{FB} = 1V$	1.47		2.03	
		$I_{AC} = 150\mu A$ , $V_{RMS} = 1.8V$ , $V_{FB} = 1V$	0.66		0.92	
		$I_{AC} = 300\mu A$ , $V_{RMS} = 3.3V$ , $V_{FB} = 1V$	0.21		0.29	
	Bandwidth	$I_{AC} = 100\mu A$		10		MHz
	Output Voltage = $3.5K \cdot (I_{SENSE} - I_{OFFSET})$	$I_{AC} = 250\mu A$ , $V_{RMS} = 1.1V$ , $V_{FB} = 1V$	0.70	0.80	0.90	V
<b>Oscillator</b>						
	Initial Accuracy	$T_A = 25^\circ C$	66		75.5	kHz
	Voltage Stability	$11V < V_{CCA} < 16.5V$		1		%
	Temperature Stability			2		%

**ELECTRICAL CHARACTERISTICS (Conti.)** Unless otherwise stated, these specifications apply  
 $V_{CCA}=+15V$ ,  $R_T = 52.3k\Omega$ ,  $C_T = 470pF$ ,  $T_A$ =Operating Temperature Range (Note 1)

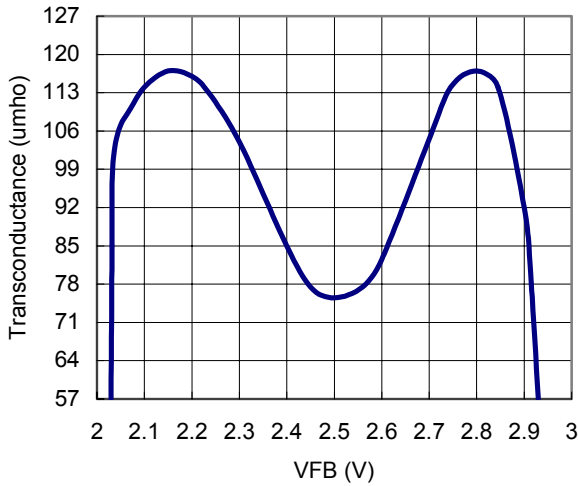
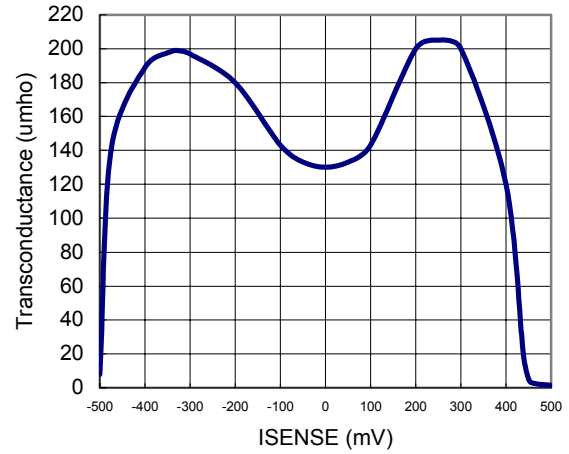
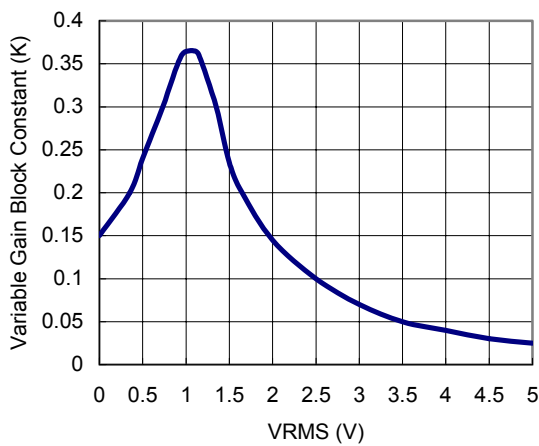
Symbol	Parameter	Test Conditions	CM6900			Unit
			Min.	Typ.	Max.	
	Total Variation	Line, Temp	68		84	kHz
	Ramp Valley to Peak Voltage			2.5		V
	PFC Dead Time (Note 4)		500		700	ns
	CT Discharge Current	$V_{RAMP2} = 0V, V_{RAMP1} = 2.5V$	6.5		10.5	mA
<b>Reference</b>						
	Output Voltage	$T_A = 25^\circ C, I(V_{REF}) = 1mA$	7.4	7.5	7.6	V
	Line Regulation	$11V < V_{CCA} < 16.5V$		10	25	mV
	Load Regulation	$0mA < I(V_{REF}) < 7mA; T_A = 0^\circ C \sim 70^\circ C$		10	20	mV
		$0mA < I(V_{REF}) < 5mA; T_A = -40^\circ C \sim 85^\circ C$		10	20	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	$T_J = 125^\circ C, 1000HRs$	5		25	mV
<b>PFC</b>						
	Minimum Duty Cycle	$V_{IEAO} > 4.0V$			0	%
	Maximum Duty Cycle	$V_{IEAO} < 1.2V$	90	95		%
	Output Low Rdson	$I_{OUT} = -20mA$ at room temp			15	ohm
		$I_{OUT} = -100mA$ at room temp			15	ohm
		$I_{OUT} = 10mA, V_{CCA} = 9V$ at room temp		0.4	0.8	V
	Output High Rdson	$I_{OUT} = 20mA$ at room temp		15	20	ohm
		$I_{OUT} = 100mA$ at room temp		15	20	ohm
	Rise/Fall Time (Note 4)	$C_L = 1000pF$		50		ns
<b>PWM</b>						
	Duty Cycle Range		0-45	0-47	0-49.3	%
	Output Low Rdson	$I_{OUT} = -20mA$ at room temp			15	ohm
		$I_{OUT} = -100mA$ at room temp			15	ohm
		$I_{OUT} = 10mA, V_{CCA} = 9V$		0.4	0.8	V
	Output High Rdson	$I_{OUT} = 20mA$ at room temp		15	20	ohm
		$I_{OUT} = 100mA$ at room temp		15	20	ohm
	Rise/Fall Time (Note 4)	$C_L = 1000pF$		50		ns
<b>Supply</b>						
	Start-Up Current	$V_{CCA} = 12V, C_L = 0$		100	150	$\mu A$
	Operating Current	$14V, C_L = 0$		3.0	7.0	mA
	Undervoltage Lockout Threshold	CM6900	12.74	13	13.26	V
	Undervoltage Lockout Hysteresis	CM6900	2.85	3.0	3.15	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

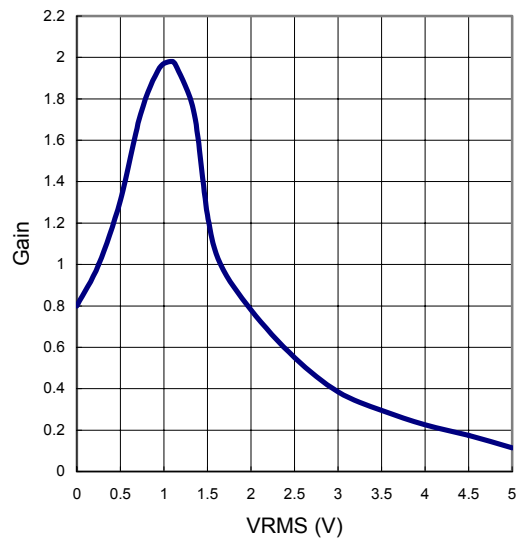
Note 2: Includes all bias currents to other circuits connected to the  $V_{FB}$  pin.

Note 3: Gain =  $K \times 5.375V$ ;  $K = (I_{SENSE} - I_{OFFSET}) \times [I_{AC} (VEAO - 0.625)]^{-1}$ ;  $VEAO_{MAX} = 6V$

Note 4: Guaranteed by design, not 100% production test.

**TYPICAL PERFORMANCE CHARACTERISTIC**

**Voltage Error Amplifier ( $g_{mv}$ ) Transconductance**

**Current Error Amplifier ( $g_{mi}$ ) Transconductance**

**Gain Modulator Transfer Characteristic (K)**

$$K = \frac{I_{\text{GAINMOD}} - I_{\text{OFFSET}}}{I_{\text{AC}} \times (6 - 0.625)} \text{mV}^{-1}$$


**Gain**

$$\text{Gain} = \frac{I_{\text{SENSE}} - I_{\text{OFFSET}}}{I_{\text{AC}}}$$



## Functional Description

The CM6900 consists of an average current controlled, continuous boost Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feedforward from the PFC output buss can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing edge duty cycle modulation, while the PFC uses leading edge modulation. This patented leading/trailing edge modulation technique results in a higher usable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the CM6900 runs at the same frequency as the PFC.

In addition to power factor correction, a number of protection features have been built into the CM6900. These include soft-start, PFC overvoltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

## Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6900 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input

line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of 270VAC<sub>rms</sub>. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to  $1/V_{IN2}$ , which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CM6900 PFC is of the current-averaging type, no slope compensation is required.

## PFC Section

### Inrush Current Control

This section is an additional function besides CM6800 functions. The INRUSHSTOPB pin is low during inrush current condition. It happens during start-up and high input current when ISENSE is less than  $-1.8V$ .

### Gain Modulator

Figure 1 shows a block diagram of the PFC section of the CM6900. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at  $I_{AC}$ . Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at  $V_{RMS}$ . The gain modulator's output is inversely proportional to  $V_{RMS}^2$  (except at unusually low values of  $V_{RMS}$  where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between  $V_{RMS}$  and gain is called  $K$ , and is illustrated in the Typical Performance Characteristics.
3. The output of the voltage error amplifier, VEOA. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form of the output of the gain modulator is:

$$I_{\text{GAINMOD}} = \frac{I_{\text{AC}} \times \text{VEAO}}{V_{\text{RMS}}^2} \times 1\text{V} \quad (1)$$

More exactly, the output current of the gain modulator is given by:

$$I_{\text{GAINMOD}} = K \times (\text{VEAO} - 0.625\text{V}) \times I_{\text{AC}}$$

Where K is in units of  $\text{V}^{-1}$

Note that the output current of the gain modulator is limited around  $228.47\mu\text{A}$  and the maximum output voltage of the gain modulator is limited to  $228.47\mu\text{A} \times 3.5\text{K} = 0.8\text{V}$ . This 0.8V also will determine the maximum input power.

However,  $I_{\text{GAINMOD}}$  cannot be measured directly from  $I_{\text{SENSE}}$ .  $I_{\text{SENSE}} = I_{\text{GAINMOD}} - I_{\text{OFFSET}}$  and  $I_{\text{OFFSET}}$  can only be measured when VEAO is less than 0.5V and  $I_{\text{GAINMOD}}$  is 0A. Typical  $I_{\text{OFFSET}}$  is around  $60\mu\text{A}$ .

#### Selecting $R_{\text{AC}}$ for IAC pin

IAC pin is the input of the gain modulator. IAC also is a current mirror input and it requires current input. By selecting a proper resistor  $R_{\text{AC}}$ , it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

$R_{\text{AC}} = V_{\text{in peak}} \times 7.9\text{K}$ . For example, if the minimum line voltage is 80VAC, the  $R_{\text{AC}} = 80 \times 1.414 \times 7.9\text{K} = 894\text{Kohm}$ .

#### Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the  $I_{\text{SENSE}}$  pin. The negative voltage on  $I_{\text{SENSE}}$  represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on  $I_{\text{SENSE}}$  is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the  $I_{\text{SENSE}}$  pin.

#### Cycle-By-Cycle Current Limiter and Selecting $R_{\text{S}}$

The  $I_{\text{SENSE}}$  pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than  $-1\text{V}$ , the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

$R_{\text{S}}$  is the sensing resistor of the PFC boost converter. During the steady state, line input current  $\times R_{\text{S}} = I_{\text{GAINMOD}} \times 3.5\text{K}$ . Since the maximum output voltage of the gain modulator is  $I_{\text{GAINMOD max}} \times 3.5\text{K} = 0.8\text{V}$  during the steady state,  $R_{\text{S}} \times$  line input current will be limited below 0.8V as well. Therefore, to choose  $R_{\text{S}}$ , we use the following equation:

$$R_{\text{S}} = 0.7\text{V} \times V_{\text{in peak}} / (2 \times \text{Line Input power})$$

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 200Watt,  $R_{\text{S}} = (0.7\text{V} \times 80\text{V} \times 1.414) / (2 \times 200) = 0.197\text{ohm}$ .

#### Separated PFC Overvoltage Protection

In the CM6900, PFC OVP is using VFB2, which is separated from VFB to sense OVP condition. The PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB2 exceeds 2.75V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below 2.50V. The VFB power components and the CM6900 are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop. Also, VCCA OVP can be served as a redundant PFCOVP protection. VCCA OVP threshold is 19.4V with 1.5V hysteresis.

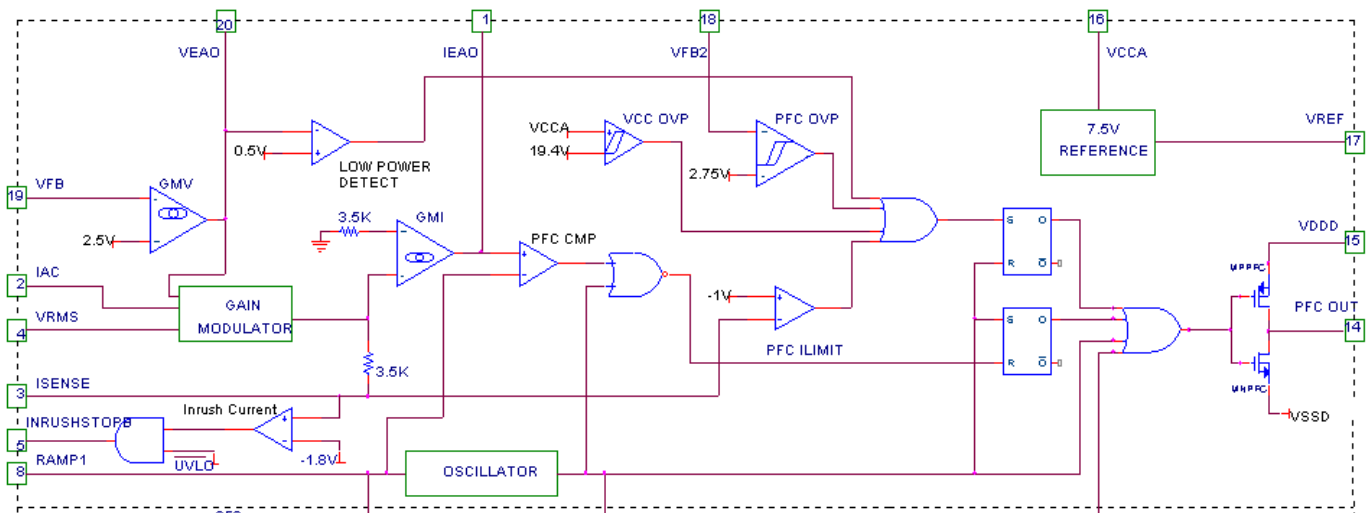


Figure 1. PFC Section Block Diagram

#### Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to  $V_{REF}$  to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on  $I_{EAO}$  which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

#### PFC Voltage Loop:

There are two major concerns when compensating the voltage loop error amplifier,  $V_{EAO}$ ; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the CM6900's voltage error amplifier,  $V_{EAO}$  has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier ( $V_{FB}$ ) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

#### The Voltage Loop Gain (S)

$$\begin{aligned} &= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}} \\ &\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV} \end{aligned}$$

$Z_{CV}$ : Compensation Net Work for the Voltage Loop

$GM_V$ : Transconductance of  $V_{EAO}$

$P_{IN}$ : Average PFC Input Power

$V_{OUTDC}$ : PFC Boost Output Voltage; typical designed value is 380V.

$C_{DC}$ : PFC Boost Output Capacitor

#### PFC Current Loop:

The current amplifier,  $I_{EAO}$  compensation is similar to that of the voltage error amplifier,  $V_{EAO}$  with exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

#### The Current Loop Gain (S)

$$\begin{aligned} &= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}} \\ &\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI} \end{aligned}$$

$Z_{CI}$ : Compensation Net Work for the Current Loop  
 $GM_I$ : Transconductance of IEAO  
 $V_{OUTDC}$ : PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the  $Z_{CI}$   
 $R_S$ : The Sensing Resistor of the Boost Converter  
 2.5V: The Amplitude of the PFC Leading Modulation Ramp  
 L: The Boost Inductor

There is a modest degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations. However, the boost inductor will usually be the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier. This is illustrated in the Typical Performance Characteristics.

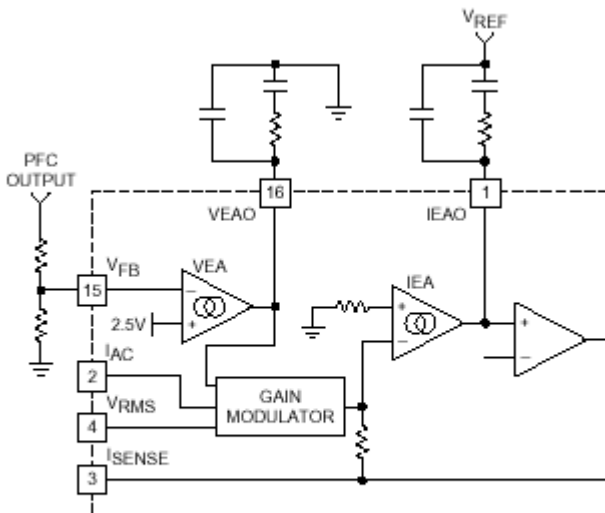


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

$I_{SENSE}$  Filter, the RC filter between  $R_S$  and  $I_{SENSE}$  :

There are 2 purposes to add a filter at  $I_{SENSE}$  pin:

- 1.) Protection: During start up or inrush current conditions, it will have a large voltage cross  $R_S$  which is the sensing resistor of the PFC boost converter. It requires the  $I_{SENSE}$  Filter to attenuate the energy.
- 2.) To reduce L, the Boost Inductor: The  $I_{SENSE}$  Filter also can reduce the Boost Inductor value since the  $I_{SENSE}$  Filter behaves like an integrator before going  $I_{SENSE}$  which is the input of the current error amplifier, IEAO.

The  $I_{SENSE}$  Filter is a RC filter. The resistor value of the  $I_{SENSE}$  Filter is between 100 ohm and 50 ohm because  $I_{OFFSET} \times$  the resistor can generate an offset voltage of IEAO. By selecting  $R_{FILTER}$  equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of  $I_{SENSE}$  Filter at  $f_{pfc}/6$ , one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the  $I_{SENSE}$  Filter,  $C_{FILTER}$ , will be around 283nF.

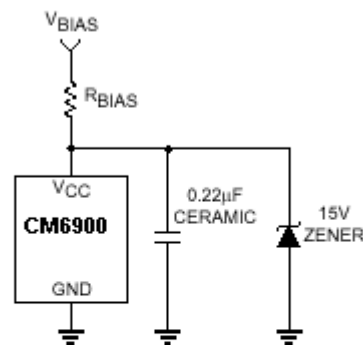


Figure 3. External Component Connections to  $V_{CC}$

### Oscillator (RAMP1)

The oscillator frequency is determined by the values of  $R_T$  and  $C_T$ , which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75}$$

at  $V_{REF} = 7.5V$ :

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{5.5mA} \times C_T = 450 \times C_T$$

The dead time is so small ( $t_{RAMP} \gg t_{DEADTIME}$ ) that the operating frequency can typically be approximately by:

$$f_{OSC} = \frac{1}{t_{RAMP}}$$

EXAMPLE:

For the application circuit shown in the datasheet, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}}$$

Solving for  $C_T \times R_T$  yields  $1.96 \times 10^{-5}$ . Selecting standard components values,  $C_T = 390pF$ , and  $R_T = 51.1k\Omega$

The dead time of the oscillator adds to the Maximum PWM Duty Cycle (it is an input to the Duty Cycle Limiter). With zero oscillator dead time, the Maximum PWM Duty Cycle is typically 45%. In many applications, care should be taken that  $C_T$  not be made so large as to extend the Maximum Duty Cycle beyond 50%. This can be accomplished by using a stable 390pF capacitor for  $C_T$ .

### PWM Section

Pulse Width Modulator

The PWM section of the CM6900 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative

of the current flowing in the converter's output stage.

$DC_{LIMIT}$ , which provides cycle-by-cycle current limiting, is typically connected to RAMP2 in such applications. For voltage-mode, operation or certain specialized applications, RAMP2 can be connected to a separate RC timing network to generate a voltage ramp against which  $V_{DC}$  will be compared. Under these conditions, the use of voltage feedforward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the  $DC_{LIMIT}$  input is used for output stage overcurrent protection.

No voltage error amplifier is included in the PWM stage of the CM6900, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP2 input which allows  $V_{DC}$  to command a zero percent duty cycle for input voltages below 1.25V.

#### PWM Current Limit

The  $DC_{LIMIT}$  pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. Beside, the cycle-by-cycle current, when the  $DC_{LIMIT}$  triggered the cycle-by-cycle current, it also softly discharge the voltage of soft start capacitor. It will limit PWM duty cycle mode. Therefore, the power dissipation will be reduced during the dead short condition.

#### $V_{IN}$ OK Comparator

The  $V_{IN}$  OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on  $V_{FB}$  is less than its nominal 2.45V. Once this voltage reaches 2.45V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

#### PWM Control (RAMP2)

When the PWM section is used in current mode, RAMP2 is generally used as the sampling point for a voltage representing the current un the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components ( $R_{RAMP2}$ ,  $C_{RAMP2}$ ), that will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feedforward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

#### Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of  $20\mu A$  supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{20\mu A}{1.25V}$$

where  $C_{SS}$  is the required soft start capacitance, and the  $t_{DEALY}$  is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of  $C_{SS}$ :

$$C_{SS} = 5ms \times \frac{20\mu A}{1.25V} = 80nF$$

Caution should be exercised when using this minimum soft start capacitance value because premature charging of the SS capacitor and activation of the PWM section can result if  $V_{FB}$  is in the hysteresis band of the  $V_{IN}$  OK comparator at start-up. The magnitude of  $V_{FB}$  at start-up is related both to line voltage and nominal PFC output voltage. Typically, a  $1.0\mu F$  soft start capacitor will allow time for  $V_{FB}$  and PFC out to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

#### Generating $V_{CCA}$

After turning on CM6900 at 13V, the operating voltage can vary from 10V to 19.4V. The threshold voltage of  $V_{CCA}$  OVP comparator is 19.4V. The hysteresis of  $V_{CCA}$  OVP is 1.5V. When  $V_{CCA}$  see 19.4V, PFCOUT will be low, and PWM section will not be disturbed. That's the two ways to generate  $V_{CCA}$ . One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias CM6900 system. The bootstrap winding can be either taped from PFC boost choke or from the transformer of the DC to DC stage.

The ratio of winding transformer for the bootstrap should be set between 18V and 15V. A filter network is recommended between  $V_{CCA}$  (pin 16) and bootstrap winding. The resistor of the filter can be set as following.

$$R_{FILTER} \times I_{V_{CCA}} \sim 2V, I_{V_{CCA}} = I_{OP} + (Q_{PFCFET} + Q_{PWMFET}) \times f_{sw}$$

$$I_{OP} = 3mA \text{ (typ.)}$$

If anything goes wrong, and  $V_{CCA}$  goes beyond 19.4V, the PFC gate (pin 14) drive goes low and the PWM gate drive (pin 13) remains function. The resistor's value must be chosen to meet the operating current requirement of the CM6900 itself (5mA, max.) plus the current required by the two gate driver outputs.

#### EXAMPLE:

With a wanting voltage called,  $V_{BIAS}$ , of 18V, a  $V_{CCA}$  of 15V and the CM6900 driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA$$

$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_g}$$

$$R_{BIAS} = \frac{18V - 15V}{5mA + 9mA}$$

Choose  $R_{BIAS} = 214\Omega$

The CM6900 should be locally bypassed with a  $1.0\mu F$  ceramic capacitor. In most applications, an electrolytic capacitor of between  $47\mu F$  and  $220\mu F$  is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

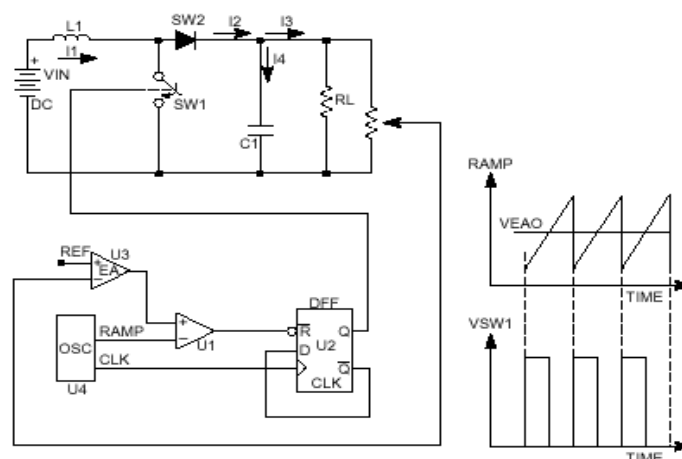


Figure 4. Typical Trailing Edge Control Scheme

### Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch. Figure 5 shows a leading edge control scheme.

One of the advantages of this control technique is that it required only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

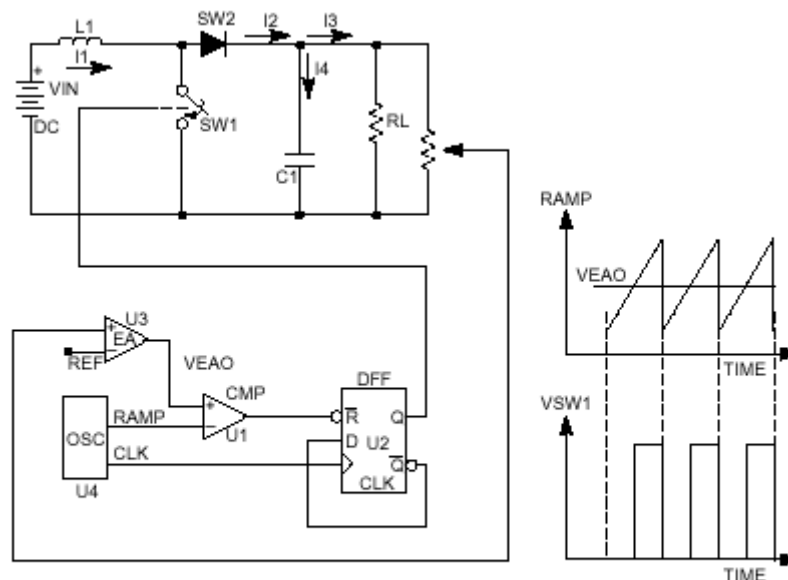
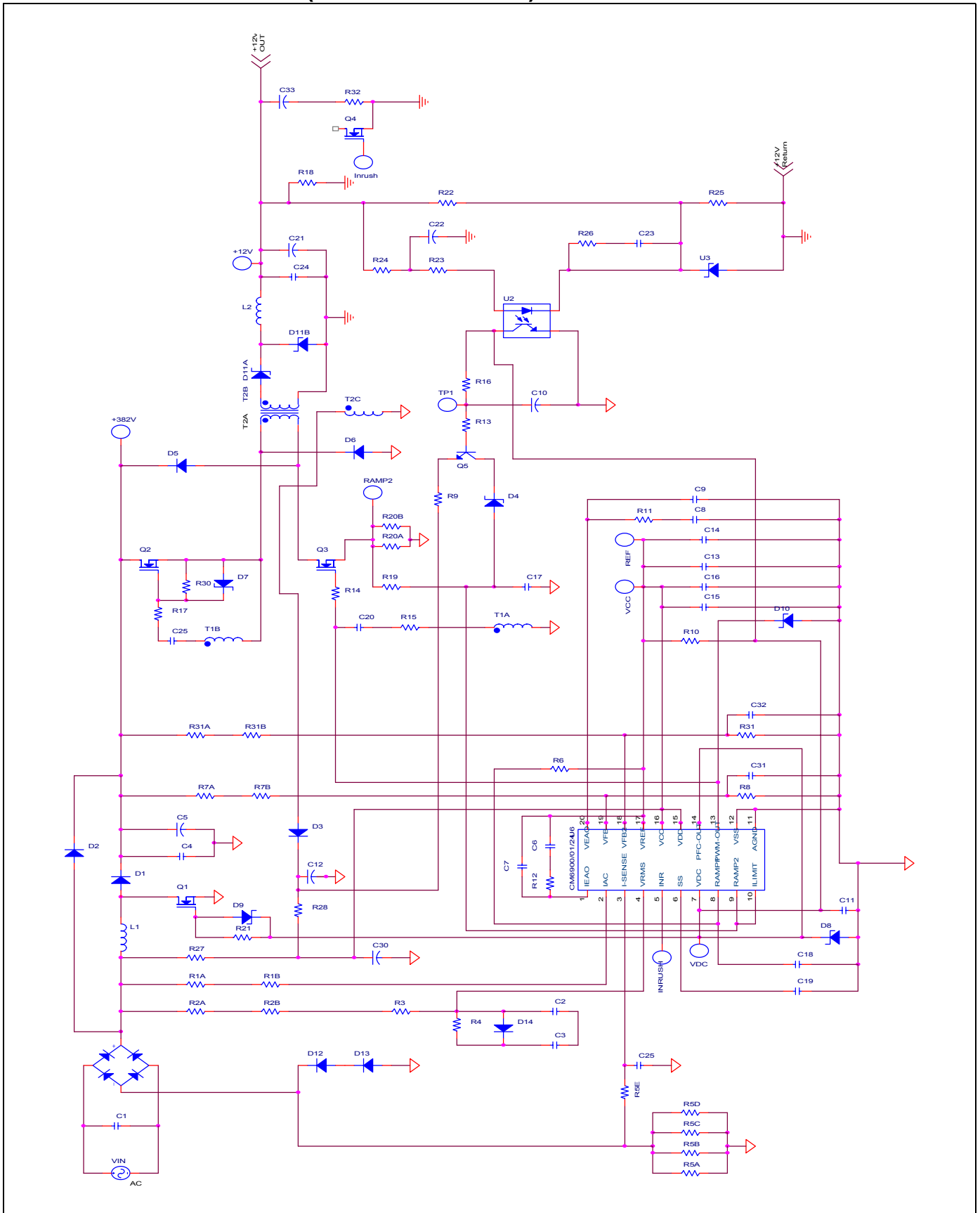
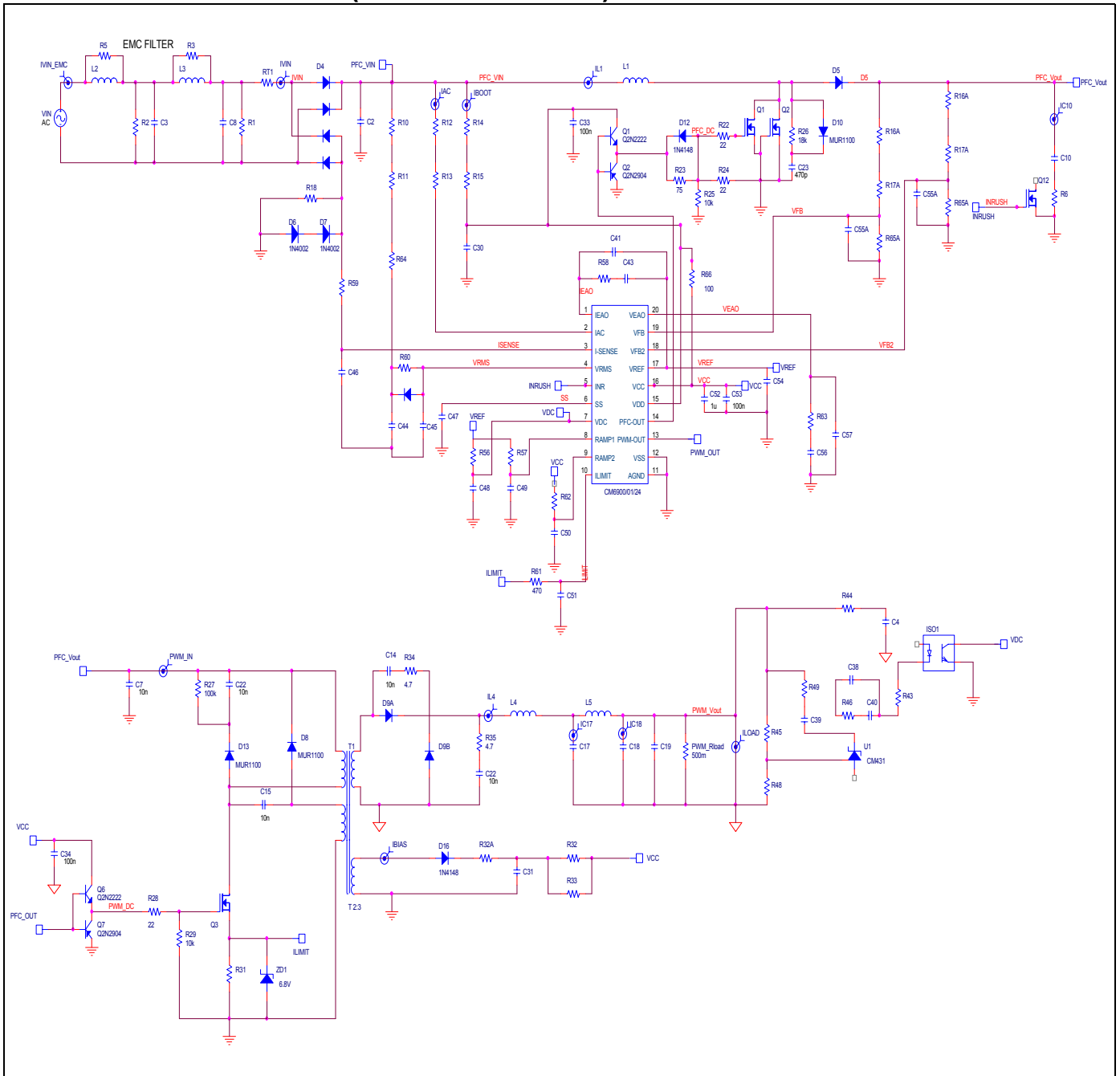


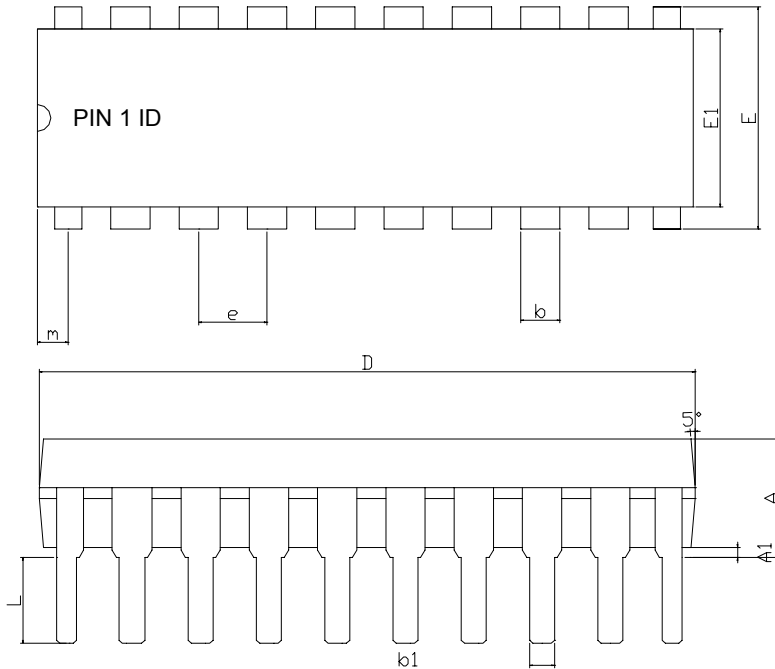
Figure 5. Typical Leading Edge Control Scheme

**APPLICATION CIRCUIT (CURRENT MODE)**


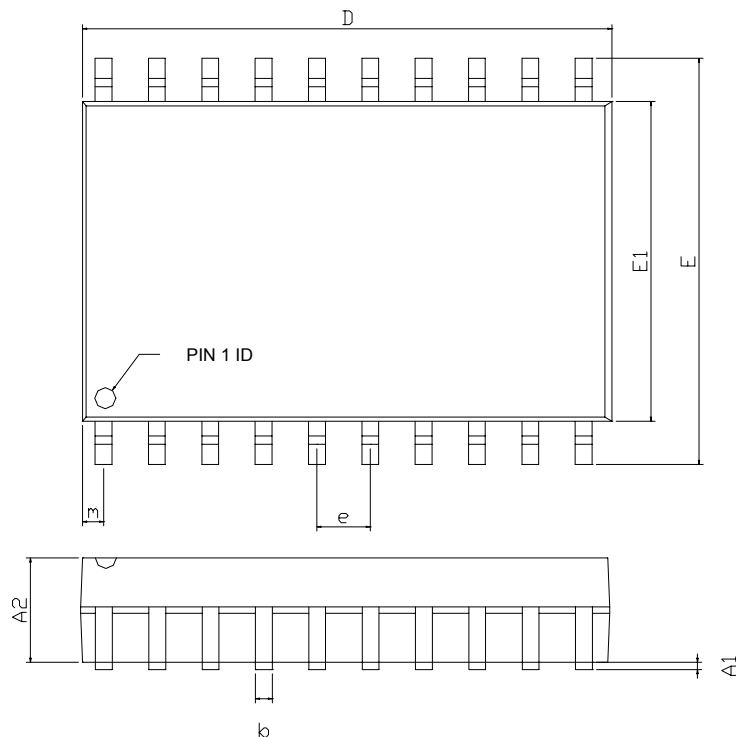


### APPLICATION CIRCUIT (VOLTAGE MODE)



**PACKAGE DIMENSION**
**20-PIN PDIP (P20)**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.32	---	---	0.170
A1	0.38	---	---	0.015	---	---
b	1.40	---	1.65	0.055	---	0.065
b1	0.40	---	0.56	0.016	---	0.022
C	0.20	---	0.31	0.008	---	0.012
D	25.65	---	26.29	1.010	---	1.035
E	7.49	---	8.26	0.295	---	0.325
E1	6.09	---	6.61	0.240	---	0.260
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
m	0.50	---	---	0.02	---	---
theta	0°	---	15°	0°	---	15°

**20-PIN SOP (P20), 0.300" Wide**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.35	0.089	---	0.093
b	0.35	---	0.51	0.014	---	0.020
C	0.23	---	0.32	0.0091	---	0.013
D	12.60	---	13.00	0.496	---	0.512
E	10.00	---	10.65	0.394	---	0.419
E1	7.40	---	7.60	0.291	---	0.299
e	---	1.27	---	---	0.050	---
L	0.40	---	1.27	0.016	---	0.050
m	0.43	---	0.69	0.017	---	0.027
theta	0°	---	8°	0°	---	8°

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