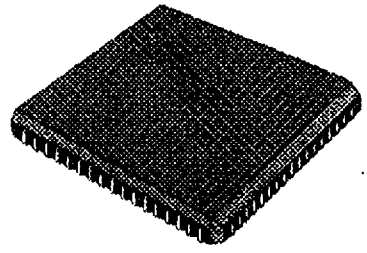
SGS-THOMSON MICROELECTRONICS

STG 1703

DUAL CLOCK SYNTHESIS PALETTE-DAC WITH 16-BIT PIXEL PORT

- Fully integrated dual clock synthesizer and 16-bit pixel port true color Palette-DAC
- Two phase-locked loop synthesizers provide independently controlled video and memory clock outputs
- On-chip PLL clock reference requires single external crystal
- 16-bit pixel port supports VGA high color and true color standards up to 135MHz
- Programmable power-down features
- On-chip checksum test



PLCC 68

DESCRIPTION

The STG 1703 is a super VGA compatible Palette-DAC with integrated clock synthesizers that can provide the memory and subsystem clock signals for the PC graphics subsystem. The video clock can be one of 2 VGA base frequencies or 14 VESA standard frequencies which can also be reprogrammed through the standard micro port interface.

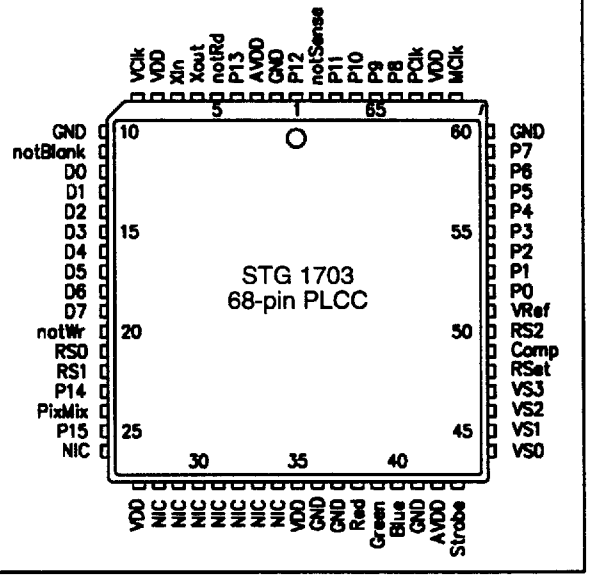
The memory clock output is also user programmable, at frequencies of up to 80MHz.

Pixel modes supported by the STG 1703 include:

- Serializing 16-bit pixel port providing 135MHz 8-bit and 56MHz 24-bit packed pixel modes using an internal PLL
- 16-bit pixel port giving faster high color/true color operation up to 110MHz sampling rate
- 8-bit pixel port giving standard SVGA and high/true color modes up to 110MHz sampling rate

The 68 PLCC pinout is designed to permit easy upgrade from the STG1700/1702 44 pin PLCC.

PIN CONNECTIONS



EXAMPLE MODES AND FREQUENCIES (ALL NON-INTERLACED)

Pixel port mode	Screen resolution	Simultaneous colors	Refresh rate (Hz)	PClk and data frequency (MHz)	Video frequency (MHz)
8-bit pixel port	1280ψ1024	256	60	110	110
	800ψ600	65K	80	110	55
	640ψ480	16.7M	80	102	34
16-bit pixel port	1024ψ768	65K	80	90	90
	800ψ600	16.7M	80	110	55
Serializing 16-bit pixel port	1280ψ1024	256	75	67.5	135
	1024ψ768	16.7M	55	85	56

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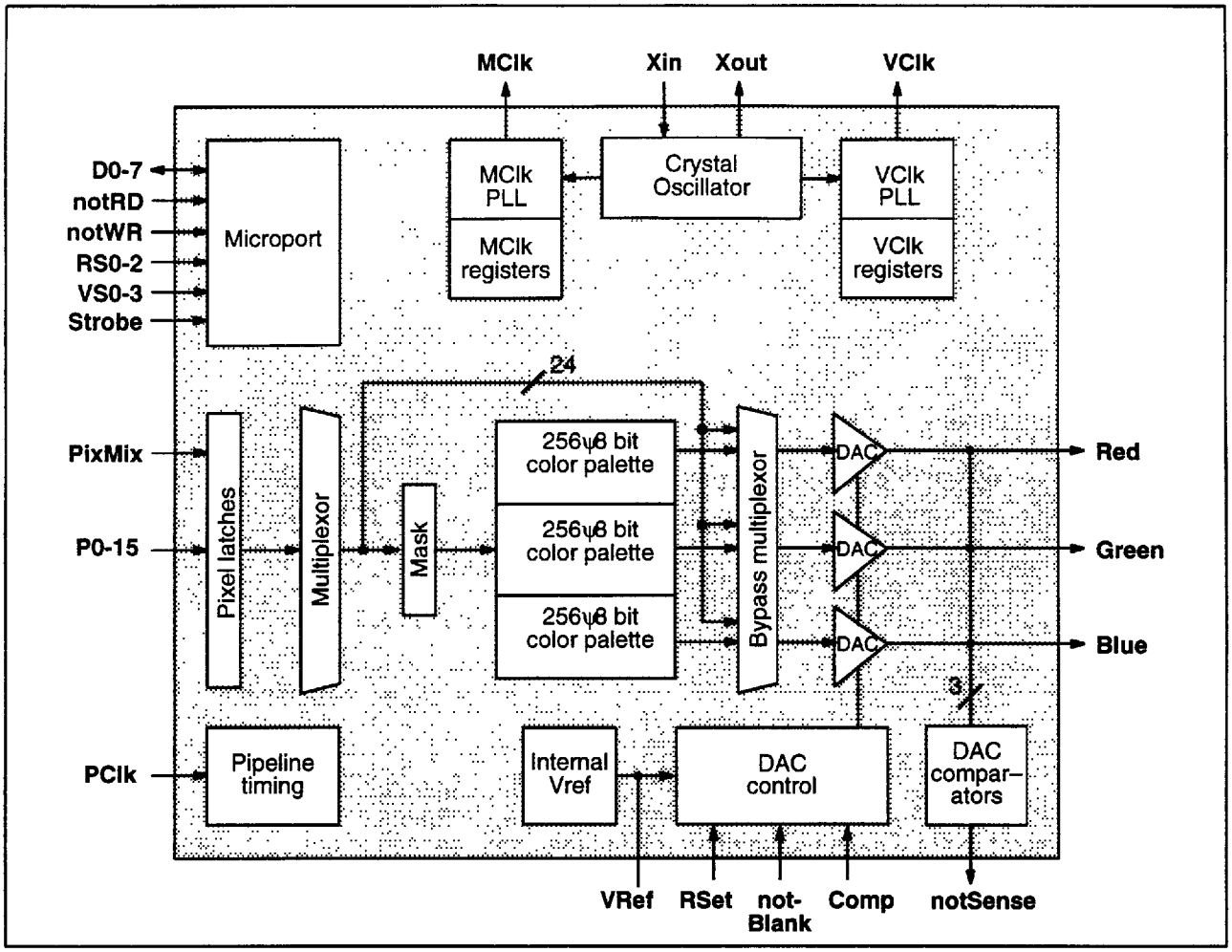
1 BLOCK DIAGRAM



2 PIN DESCRIPTIONS

2.1 MICRO PORT

Signal	Description
notRD, notWR	The Read Enable and Write Enable signals, **notRD** and **notWR**, control the timing of read and write operations on the micro port. Most of the operations on the micro port can take place asynchronously to the pixel stream being processed by the color palette. Various minimum periods between operations are specified (in terms of pixel clocks) to allow this asynchronous behavior. **notRD** and **notWR** should not be low at the same time.
RS0-2	The values on **RS0-2** specify which internal register is to be accessed. The **RS0-2** inputs are sampled on the falling edge of the active enable signal (**notRD** or **notWR**). Information on register access and contents is given in Section 3. The additional **RS2** signal allows access to the extended features without the need for performing a 'magic access' sequence.
D0-7	Data is transferred between the 8-bit wide program data bus and the registers within the STG 1703 under control of the active enable signal (**notRD** or **notWR**). In a write cycle the rising edge of **notWR** validates the data on the program data bus and causes it to be written to the register selected. The rising edge of **notRD** signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

Signal	Description
VS0-3	These inputs select the frequency (default or user programmed) of the video clock PLL. These pins are ignored if the video clock frequency is selected by register control.
Strobe	The falling edge of **Strobe** latches **VS0-3**.

2.2 PIXEL PORT

Signal	Description
PClk	The rising edge on PClk controls the sampling of data on **P0-15**, **notBlank** and **PixMix** in all modes.
P0-15	The pixel data word. The selected pixel mode determines how this pixel data is interpreted.
PixMix	Controls the switching between primary and secondary pixel modes when the extended pixel modes are selected. (**PixMix** = 0 selects primary mode.)
notBlank	A low value sampled on this pin will, after the pipeline delay, turn the DAC outputs off.

2.3 DAC INTERFACE

Signal	Description
Red, Green, Blue	The DAC video outputs. These are designed to drive a doubly terminated 75 ohm load.
VRef	External 1.235V Vref input. When used in internal Vref mode this pin should be left floating, with or without the optional external Vref bypass capacitor.
RSet	A precision resistor placed between this pin and GND sets the full-scale DAC current. The required resistor value can be calculated from: Rset (Ω) = (2.1ψVref)/Iout where Vref is the external or internal reference voltage and Iout is the required DAC full scale output current. Rset is typically 147Ω for VGA (see Section 6).
Comp	External compensation capacitor for DACs.
notSense	This pin is a logical 0 if one or more of the DAC outputs exceeds the internal DAC comparator trip voltage (which is mid-way between the DAC full scale and GND potentials).

2.4 FREQUENCY SYNTHESIZER INTERFACE

Signal	Description
Xout	A series resonant crystal must be connected between these two pins to provide the reference clock for the PLLs.
Xin	
VClk	Video clock PLL output
MClk	Memory clock PLL output

2.5 POWER SUPPLY

Signal	Description
VDD	Digital power supply
AVDD	Analog power supply for the DACs and PLL.
GND	Common GND rail for all circuitry.
NIC	No internal connection. For future upgrade to a 24-bit pixel port the controller outputs P16–23 can be routed to pins 26, 28–34 respectively.

3 MICRO PORT

The STG 1703 micro port (see Table 1) is an extension of the standard VGA micro port and will power up with a register configuration compatible with standard and high color VGA.

There are two methods for accessing the register set of STG 1703; direct RS access and "magic access".

3.1 DIRECT RS ACCESS

This new feature supports direct RS mapping to eight address locations that access the VGA color palette, Pixel Command Register and an indexed register.

Table 1. Direct RS micro port accesses

RS[2:0]	VGA Register
000	Address Register (palette write)
001	Palette Color Value
010	Pixel Mask/Magic Access
011	Address Register (palette read)
100	Index LO byte
101	Indexed register
110	Pixel Command Register
111	Index HI byte

The index LO/HI registers increment after every access to the indexed register.

3.2 MAGIC ACCESS

The indexed register space can also be accessed by a special mechanism of successive reads ("magic access") to the mask register location 2h, as shown in Table 2. Reads from RS location 2h cause a state counter to be advanced by 1. Hence, five successive reads of RS location 2h will return the mask register contents four times followed by the Pixel Command Register value.

If the indexed register space is not enabled the next access is directed to the pixel mask (state 1 in Table 2). States 3 to 4 require three reads from the Pixel Mask Register and when the Pixel Command Register is written to enable the indexed register space, the next access is again directed to the mask register (the next state after state 5 is state 1).

The magic access sequence can now enter states 6 and 7 to access the lower and higher byte of the index register respectively. Subsequent reads or writes to location 2h access the register space pointed to by the index register. After each indexed register access, the index register will increment automatically. In this way the entire indexed register space may be "block moved" without the need to keep writing to the index register.

At any point in the above sequence a read or write to any location other than 2h will reset the state counter to state 1.

On power up the magic access sequence is truncated through the default setting of Pixel Command Register bit [4], so that the STG 1703 is identified by existing video BIOS code as a fast ATT20C490.

Table 2. Magic access sequence

Current state[1]		Next state			
	Register mapped at RS=2h	Read from RS=2h *and* index space enabled	Read from RS=2h and index space disabled (default)	Write to RS=2h	Read/ write to other RS location
1	Pixel Mask	2	2	1	1
2	Pixel Mask	3	3	1	1
3	Pixel Mask	4	4	1	1
4	Pixel Mask	5	5	1	1
5	Pixel Command	6	1	1	1
6	Index LO byte	7		7	1
7	Index HI byte	8		8	1
8	Indexed register	8*		8*	1

NOTES

1 Power-up state is state 1

* increment index register after access

3.3 INDEXED REGISTER SPACE

Table 3.

Index	Index register contents[1]	Notes[2]
00 00h	Company ID=44h	
00 01h	Device ID=03h	
00 02h	Reserved	3
00 03h	Primary Pixel Mode Select	
00 04h	Secondary Pixel Mode Select	
00 05h	Pipeline Timing Control	
00 06h	Soft Reset	
00 07h	Power Management A	
00 08h	Power Management B	
00 09h–00 1Fh	Reserved	3
00 20h	**VClk** V0 parameters LO (3Dh)	25.175
00 21h	**VClk** V0 parameters HI (47h)	
00 22h	**VClk** V1 parameters LO (55h)	28.332
00 23h	**VClk** V1 parameters HI (49h)	
00 24h	**VClk** V2 parameters LO (41h)	40.0
00 25h	**VClk** V2 parameters HI (2Ah)	
00 26h	**VClk** V3 parameters LO (26h)	72.0
00 27h	**VClk** V3 parameters HI (06h)	
00 28h	**VClk** V4 parameters LO (36h)	50.0
00 29h	**VClk** V4 parameters HI (26h)	
00 2Ah	**VClk** V5 parameters LO (29h)	77.0
00 2Bh	**VClk** V5 parameters HI (06h)	
00 2Ch	**VClk** V6 parameters LO (26h)	36.0
00 2Dh	**VClk** V6 parameters HI (26h)	
00 2Eh	**VClk** V7 parameters LO (43h)	44.90
00 2Fh	**VClk** V7 parameters HI (29h)	
00 30h	**VClk** V8 parameters LO (59h)	Re-served
00 31h	**VClk** V8 parameters HI (08h)	
00 32h	**VClk** V9 parameters LO (41h)	Re-served
00 33h	**VClk** V9 parameters HI (06h)	
00 34h	**VClk** V10 parameters LO (41h)	80.0
00 35h	**VClk** V10 parameters HI (0Ah)	
00 36h	**VClk** V11 parameters LO (56h)	31.50
00 37h	**VClk** V11 parameters HI (48h)	
00 38h	**VClk** V12 parameters LO (43h)	110.0
00 39h	**VClk** V12 parameters HI (07h)	
00 3Ah	**VClk** V13 parameters LO (59h)	65.0
00 3Bh	**VClk** V13 parameters HI (28h)	
00 3Ch	**VClk** V14 parameters LO (28h)	75.0
00 3Dh	**VClk** V14 parameters HI (06h)	
00 3Eh	**VClk** V15 parameters LO (40h)	94.50
00 3Fh	**VClk** V15 parameters HI (08h)	
00 40h	**MClk** M0 parameters LO (3Dh)	45.0
00 41h	**MClk** M0 parameters HI (28h)	
00 42h	**MClk** M1 parameters LO (51h)	66.0
00 43h	**MClk** M1 parameters HI (27h)	
00 44h	**MClk** M2 parameters LO (2Ah)	70.0
00 45h	**MClk** M2 parameters HI (07h)	
00 46h	**MClk** M3 parameters LO (36h)	80.0
00 47h	**MClk** M3 parameters HI (08h)	
00 48h	Clock Synthesizer Control (00h)	
00 49h–FF D5h	Reserved	3
FF D6h	Checksum Control register	
FF D7h	Checksum Value byte [2]	
FF D8h	Checksum Value byte [1]	
FF D9h	Checksum Value byte [0]	
FF DAh–FF FFh	Reserved	3

NOTES

1 Register power-up values for given synthesizer frequencies shown in brackets.

2 Synthesizer frequencies given for f_{Xin} = 14.31818MHz

3 Do not write to reserved locations

3.4 REGISTER CONTENT DESCRIPTIONS

A write to any register containing reserved bits should always write 0 to the reserved bits (the exception being bit [7] of Power Management Register A). On reads all reserved bits should be masked out.

Bits within registers which are reset on power-up are marked in the column headed "Reset value".

Table 4. Pixel Command Register

Bit	Value	Function	Reset value
7:5	000	8-bit indexed color	000
	001	Reserved	
	010	Reserved	
	011	Reserved	
	100	Reserved	
	101	15-bit direct color	
	110	16-bit direct color	
	111	24-bit direct color	
4		'1' = Enable extended register space	0
3		'1' = Enable extended pixel modes	0
2		'1' = Add 7.5 IRE blanking pedestal	0
1		'1'= Micro port interface to RAM is 8-bit not 6-bit	0
0		'1' = Sleep mode (micro port and palette RAM still enabled, see Section 3.6)	0

Table 5. Index LO and Index HI Registers

Bit	Function	Reset value
7:0	LO/HI byte of 16-bit Index	0

Indexed Register Space

Index 0000h Company ID Register

Bit	Function	Reset value
7:0	44h (= SGS-THOMSON)	read only

Index 0001h Device ID Register

Bit	Function	Reset value
7:0	03h (=STG 1703)	read only

Indexes 0003, 0004h Pixel Mode Select Registers (Primary and Secondary)

Bit	Value	Function	Max PClk (MHz)	Max Video rate (MHz)	Reset value
7:0	00h	8-bit indexed color	110	110	not reset
	01h	15-bit direct color or 8-bit indexed color	110	110	
	02h	15-bit direct color	110	110	
	03h	16-bit 5:6:5 direct color	110	110	
	04h	24-bit direct color	110	55	
	05h	Double 8-bit indexed color	67.5	135	
	06h	16-bit 5:6:5 direct color (2ψ8-bit input)	110	55	
	07h	8-bit indexed color (2ψ4-bit input)	110	55	
	08h	15-bit direct color (2ψ8-bit input)	110	55	
	09h	Double 24-bit direct color	85	56.6	
	0Ah–FFh	Reserved			

Index 0005h Pipeline Timing Control Register (double 8-bit and double 24-bit modes only)

Bit	Value	PClk input frequency (MHz)	Resulting DAC clock frequency (MHz)		Reset value
			Double 8-bit	Double 24-bit	
7:2		Reserved			0
1:0	00	8–16	16–32	5.3–10.7	
	01	16–32	32–64	10.7–21.3	
	10	32–67.5	64–135	21.3 –45.0	10
	11	64–85	Not available	42.7–56.6	

Index 0006h Soft Reset Register

Bit	Function	Reset value
7:1	Reserved	0
0	1 = Reset all registers to power-on default state	0