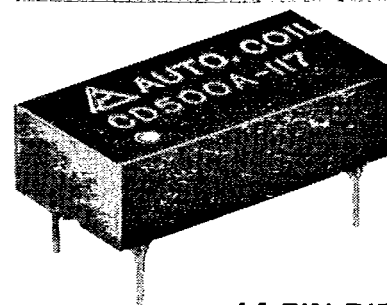


CD500 Series TTL Digital Delay Module, Single Delay

T-47-131

- TTL input and output
- Precise and stable delay
- Reliable hybrid construction
- No external components required
- Fan out 10TTL loads
- Operating temperature 0° to 70°C
- Storage temperature -55° to +125°C



14 PIN DIP

Electrical Characteristics:

V _{IH} (High level input voltage)	2.0 to 5.0V
I _{IH} (High level input current)	50 μA Max.
V _{IL} (Low level input voltage)	0.8 V Max.
I _{IL} (Low level input current)	-2 ma Max.
V _{OH} (High level output voltage)	2.5 V Min.
V _{OL} (Low level output voltage)	0.5 V Max.
V _{CC} (Supply voltage)	5.0 V ± 0.25 V DC
I _{CC} (Supply current)	75 ma Max.

Mechanical Specifications:

Case: Epoxy filled D.A.P.

Leads: Alloy 42 or equiv.
solder coated

Marking: White epoxy ink

Also Available:

Intermediate delays

Tighter delay tolerances

Falling edge delay specifications

Tapped modules

Lower profiles

Military versions

AS, LS & advanced low

power Schottky versions

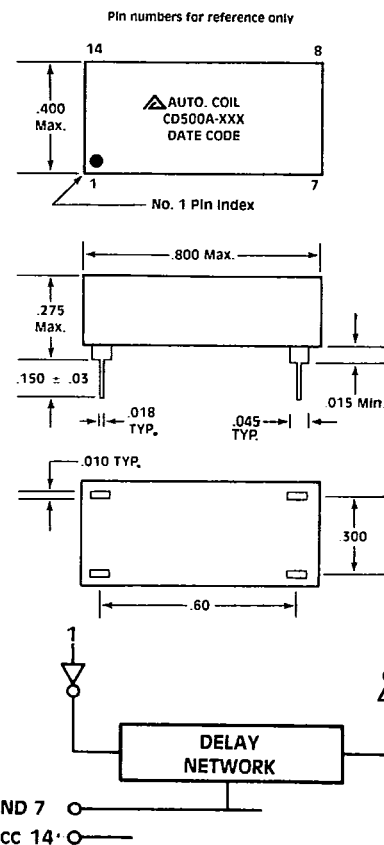
Input & test conditions are not limiting parameters. All digital delay modules can be operated at conditions other than specified. Since accuracies may be slightly affected, we suggest that the module be evaluated under specific operating conditions.

Specifications subject to change without notice.

Nominal Delays (In NS) ±2 NS or 5% Whichever Is Greater

Automatic Coil Part Number	PIN 1 to 8	Automatic Coil Part Number	PIN 1 to 8
CD500A-101	6	CD500A-118	60
CD500A-102	8	CD500A-119	70
CD500A-103	10	CD500A-120	80
CD500A-104	12	CD500A-121	90
CD500A-105	14	CD500A-122	100
CD500A-106	16	CD500A-123	110
CD500A-107	18	CD500A-124	120
CD500A-108	20	CD500A-125	130
CD500A-109	22	CD500A-126	140
CD500A-110	24	CD500A-127	150
CD500A-111	26	CD500A-128	200
CD500A-112	28	CD500A-129	250
CD500A-113	30	CD500A-130	300
CD500A-114	35	CD500A-131	350
CD500A-115	40	CD500A-132	400
CD500A-116	45	CD500A-133	450
CD500A-117	50	CD500A-134	500

Output rise time (TPLH) 4.0 NS max. (0.75 to 2.4 V level).



Test Conditions:

- 1) All measurements are made @ 25°C
- 2) V_{CC} is maintained @ 5.0 VDC
- 3) All measurements are made with no loads on output
- 4) Delay measured @ 1.5V level
- 5) Delay & tolerance for leading edges only (TPLH) - falling edges (TPHL) closely matched to TPLH

Input Conditions:

- 1) Pulse amplitude: 3.20V
- 2) Input rise time 3.0 NS (10 to 90%)
- 3) Pulse width 2 × total delay
- 4) Duty cycle < 25%